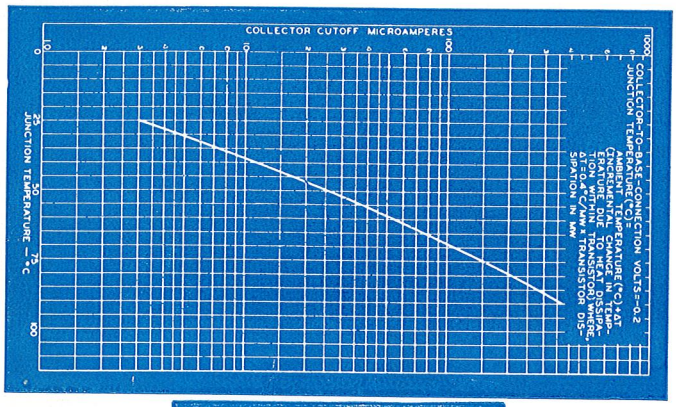
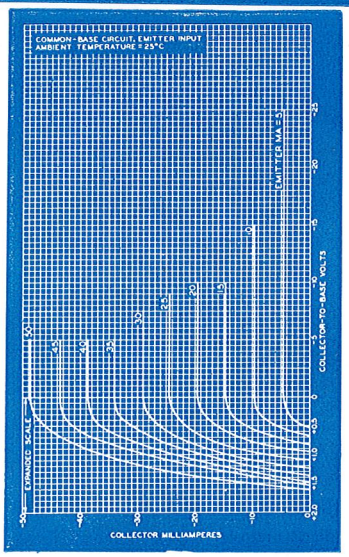
# RADIOTRONICS

Registered at the General Post Office, Sydney, for transmission by post as a periodical. Single Copy, One Shilling.

VOL. 22 NOVEMBER 1957 NO. 11

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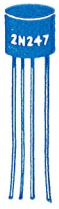



AMALGAMATED WIRELESS VALVE COMPANY PTY. LTD.

# The Application of Transistors to Audio Frequency Amplifiers

by

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## SUMMARY

**Simple methods of approach to the design of transistor audio amplifier low level and power output stages are treated. The need for, and a method of, bias stabilization and class A and class B amplifier design are discussed. A method of evaluating transistors for power amplifier applications is detailed.**



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Radiotronics is published twelve times a year by The Wireless Press for Amalgamated Wireless Valve Company Pty. Ltd. The annual subscription rate in Australasia is 10/-; in U.S.A. and dollar countries $1.50, and in all other countries 12/6. Price of a single copy is 1/-.

Subscribers should promptly notify Amalgamated Wireless Valve Company Pty. Ltd., 47 York Street, Sydney, and also the local Post Office of any change in address, allowing one month for the change to become effective.

# Introduction

Since the first transistors appeared on the commercial market, a tremendous volume of literature has been written covering the manufacture and use of this interesting little device. It is the intention of this article to deal briefly with some of the things that an experimenter will come across while becoming acquainted with his new toy. There is nothing new presented, but a down to earth approach is adhered to in audio power amplifier design. One can read through many pages of technical literature to find equations suitable for use in the required design, when all one need do is extend a little further the knowledge that has been gained in the use of valves, and draw suitable load lines on the collector characteristics of the transistor.

Before starting let us observe a few elementary precautions. The transistor can be ruined by excessive heat. It is advisable to use some form of heat sink (usually long nosed pliers) when soldering a transistor lead into a circuit. By applying the heat sink between the soldered joint and the actual transistor itself, most of the heat is prevented from reaching the transistor.

Another important precaution is the prevention of sudden overloads. A transistor can be permanently damaged by high transient currents. The manufacturer's ratings must be observed at all times. Connections should not be made to a transistor circuit with the power supply switched on because accidental short circuiting of a bias resistor or some other freak condition could cause a damaging high transient current. A wise precaution when first switching on is to insert a resistor in the collector supply lead to limit the short circuit current from the power supply to a safe value. A series variable resistance in the input lead can also be used to enable the desired operating point to be approached gradually. This applies particularly in transformer coupled power amplifiers where the supply voltage is applied directly to the collector through the winding resistance of the transformer, and also in common emitter circuits where there is a large current gain between the input and output circuits.

The peak collector voltage of a transistor is limited by what is known as the "Zener Effect". When the magnitude of the collector voltage exceeds "the critical field potential" the collector current begins to rise rapidly and excessive distortion occurs. If this condition is prolonged the collector current may commence to "run away" due to temperature rise within the transistor and eventually a point can be reached where the transistor becomes permanently damaged. This rating will govern the maximum supply voltage that can be used in transformer coupled amplifiers where the collector can swing to a voltage of twice the supply voltage.

# Bias stabilization for R.C. amplifiers

Stabilization of the operating point becomes very important in transistor R.C. amplifiers because of the very large drift in collector current with variations of temperature. Temperature compensation can be achieved at the expense of some battery power, and hence efficiency but in low level stages the power lost is quite negligible. Quite a number of different circuit arrangements may be used[1] but only one will be considered here. This circuit[2] is applicable where a single battery power supply is used and is shown in Fig. 1.

The stability factor S is given by

$$S = \frac{\triangle I_C}{\triangle I_{CO}}$$

$$= \frac{1 + \frac{R_1}{R_2} + \frac{R_1}{R_3}}{1 - \alpha + \frac{R_1}{R_2} + \frac{R_1}{R_3}}$$

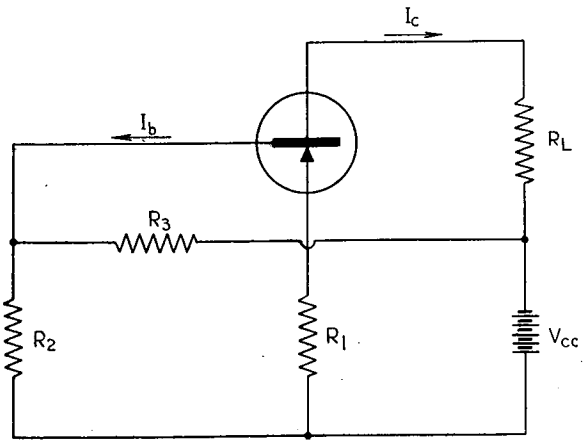



Fig. I Single Battery Bias Circuit

$\alpha$ ( $= h_{fb}$) is the small signal current amplification factor for common base connection. $I_{CO}$ is the collector current which flows in common-base connection when the emitter current is zero and is normally specified at a particular collector voltage and temperature. It varies appreciably with changing temperature and hence $I_C$ varies at a much greater rate depending on the stability factor of the circuit. The need for temperature compensation is best illustrated by considering an uncompensated stage. Referring to Fig. 2 we find that if $R_1 = 0$

$$R_2 = \infty$$

$$\alpha\ (=h_{fb}) = 0.973$$

$$\text{Then } S = \frac{1}{1-\alpha}$$

$$= 37$$

For a rise in temperature of from 25°C to 45°C (77°F to 113°F), $I_{CO}$ can change from 4 to 25 microamperes at a collector voltage of –4.5 volts in a typical transistor. Hence under normal operating conditions a change in $I_{CO}$ of 100 percent can be envisaged causing a change of 3700 percent in $I_C$ if no other factor limited the change. Thus the necessity for temperature compensation is clearly illustrated. The value of $I_{CO}$ used in calculating S is that for common-base connection. The formula given is for a common emitter circuit but uses the value $I_{CO}$ and not $I'_{CO}$ which is the corresponding current for grounded emitter connection and which is much larger.

To illustrate the effect of bias stabilizing circuits a suitable network will be calculated for the above conditions. An approach shown in Reference 2 is to decide suitable values for $V_{CC}$, $I_C$, $R_L$, S and $V_C$ and find $R_1$, $R_2$ and $R_3$ by substituting in the equations:—

$$R_1 = \frac{\alpha\ (V_{CC} - I_C R_L - V_C)}{I_C - I_{CO}}$$

$$R_3 = \frac{V_{CC}\ (S - 1)}{I_C - S\ .\ I_{CO}}$$

$$R_2 = \frac{R_1\ .\ R_3\ .\ (S - 1)}{R_3\ .\ S\ .\ \alpha - (S - 1)\ (R_1 + R_3)}$$

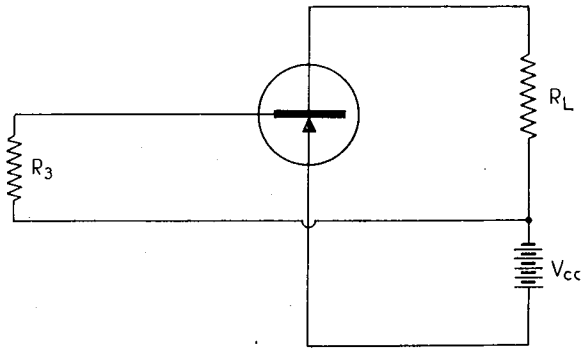



Fig. 2 Uncompensated Stage

Two factors must be considered here:—

1. Bias stabilization is gained at the expense of battery power and hence a compromise must be reached between the degree of stabilization required and the battery power that can be spared.
2. The resistance $R_2$ shunts the input resistance to the stage and hence must be made much larger than this resistance.

Let us consider the stage operating from a 9V battery with $R_L$ 3,300 ohms and $I_C$ 1mA. Before proceeding any further it is required to know the input resistance of the stage. This can be calculated from the following formula:—

A.C. Input Resistance

$$= R_i$$

$$= r_b + r_e \cdot \frac{r_c + R_L'}{r_c - r_m + r_e + R_L'}$$

$R_L'$ is the parallel combination of $R_L$, the load resistance, and the input resistance of the following stage. This latter resistance is in turn dependent on a similar combination in the following output circuit. Hence to accurately calculate the input resistance at first seems quite

a difficult task. However, examination of the equation for $R_i$ will show that provided $R_L'$ is quite small compared to $(r_c - r_m)$ it does not have much of an effect on the value of $R_i$.

If the value of $R_L$ can be approximated from previous experience, the approximation can then be used. It was found that an error in $R_L'$ of two times in this particular case altered $R_i$ by only 2%. If no idea of the value of $R_L$ can be formed, a two stage approach will make the problem quite simple. For example if the following stage is the same as the stage being considered:—

1. Take $R_L' = R_L$
   Calculate $R_i$ from formula.
2. Recalculate $R_i$ using the parallel combination of $R_i$ and $R_L$ for $R_L'$.

Using this method the input resistance to the stage being considered is then found as follows:—

For the transistor being considered, the T network parameters are:—

$r_e = 30$ ohms
$r_b = 500$ ohms
$r_c = 1.5 \times 10^6$ ohms
$r_m = \alpha r_c$
$= 1.45 \times 10^6$ ohms

A preliminary calculation assuming a similar following stage suggested a value for $R_L'$ of 1000 ohms.

Then

$$R_i = 500 + 30 \times \frac{1.5 \times 10^6 + 1000}{0.05 \times 10^6 + 30 + 1000}$$

$$= 1383 \text{ ohms.}$$

Note that $R_i \parallel R_L \approx 1000$ ohms, justifying the previous assumption.

For grounded base operation

$$R_i = r_e + r_b \cdot \frac{r_c (1 - \alpha) + R_L'}{r_e + R_L'}$$

For grounded collector operation

$$R_i = r_b + r_c \cdot \frac{r_e + R_L'}{r_c - r_m + r_e + R_L'}$$

The value of $R_3$ is fixed by the stability factor, battery voltage, $I_C$ and $I_{CO}$. Hence $R_1$ can be chosen to give a suitably high value for $R_2$. We can now choose a suitable value for $R_1$ which will not upset the operating conditions. The effect of $R_1$ if properly bypassed is to shift the d.c. loadline along the $V_{CE}$ axis towards the origin. With $R_1 = 0$, $V_{CE} = V_{CC} - I_C R_L$
$= 9 - 3.3 = 5.7$ volts.
We can reduce this voltage further by at least 3 volts without upsetting the operation of this stage, Let us take a value for $R_1$ of 2,200 ohms which reduces $V_{CE}$ to a value as shown below:—

$V_{CE} = 9 - I_C R_L - I_E R_1$
If we make the approximation
$I_E \approx I_C$
$V_{CE} = 9 - 10^{-3} \times (3300 + 2200)$
$= 9 - 5.5$
$= 3.5$ volts.

Now if we design for a value $S = 4$ we have

$$R_3 \approx \frac{V_{CC} (S - 1)}{I_C}$$

($S I_{CO}$ is very small compared to $I_C$ in our case)

$$= \frac{9 \times 3}{10^{-3}}$$

$$= 27000 \text{ ohms}$$

$$\text{and } R_2 = \frac{2200 \times 27000 \times 3}{27000 \times 4 \times 0.973 - 3 \times 29200}$$

$$= 9{,}700 \text{ ohms}$$

$$\approx 10{,}000 \text{ ohms}$$

This is several times higher than the input impedance of the stage. The bias stabilized stage with a stability factor $S = 4$ is shown in Fig. 3.

As a check on the calculations, the values for $R_1$, $R_2$ and $R_3$ can be substituted in the formula for S.

$$S = \frac{1 + \frac{2200}{10000} + \frac{2200}{27000}}{1 - 0.973 + \frac{2200}{10000} + \frac{2200}{27000}}$$

$$= \frac{1.3015}{0.329}$$

$$= 3.96$$

$$\approx 4$$

Hence a change in $I_{CO}$ of 100% now causes a change in $I_C$ of 400% which is a vast improvement over the change in an uncompensated stage and is quite enough for normal low level stages. It now remains to be seen how much extra battery power we are using to achieve this compensation. For the uncompensated stage the battery power input is approximately 9 mW (the small base current required can be neglected). For the compensated stage

$$P_{DC} = V_{CC}\left[\frac{I_C}{a}\left(1+\frac{R_1}{R_2}\right) + I_{CO}\left(\frac{R_1}{aR_3} - \frac{S}{S-1}\right)\right]$$

$$\approx V_{CC}\left[\frac{I_C}{a}\left(1 + \frac{R_1}{R_2}\right)\right]$$

$$\approx \frac{9 \times 10^{-3} \times 1.22}{0.973}$$

$$\approx 11.2 \text{ mW}$$

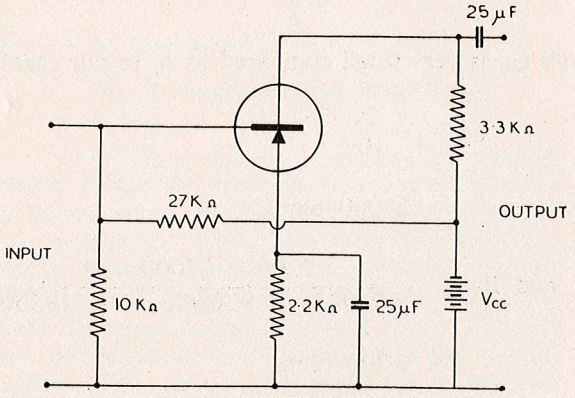



Fig. 3 Bias Stabilized Stage.

Hence the additional battery power used is 2.2 mW which is extremely small.

There is another very important reason for using bias stabilisation[3]. Consider the stage shown in Fig. 2 when $R_L$ is 3,300 ohms and the collector current $I_C$ is – 1 mA.

$$I_C = h_{FE}\, I_B$$

where $h_{FE}$ is the grounded emitter static current transfer ratio. (Note that $h_{FE} \approx h_{fe}$ which is the small signal current transfer ratio).

For the transistor being considered $h_{fe}$ can vary from 20 to 50, the bogie value being 35.

$$\text{For } h_{FE} = 35$$
$$I_B = \frac{-10^{-3}}{35}$$
$$= -28.6\ \mu A$$

This current will be fixed by choice of the resistor $R_3$. Now if we change the transistor in the circuit to one with a transfer ratio of 49 the collector current will be

$$I_C = -28.6 \times 49 \times 10^{-6}$$
$$= -1.4 \text{ mA}$$
$$\text{and } V_{CE} = -(9 - 1.4 \times 3.3)$$
$$= -(9 - 4.6)$$
$$= -4.4 \text{ volts}$$
$$\text{For } h_{FE} = 21$$
$$I_C = -28.6 \times 21 \times 10^{-6}$$
$$= -0.6 \text{ mA}$$
$$\text{and } V_{CE} = -(9 - 0.6 \times 3.3)$$
$$= -(9 - 1.7)$$
$$= -7.3 \text{ volts}$$

Hence the operating point could vary from
$V_{CE} = 4.4$ volts $I_C = 1.4$ mA
to $V_{CE} = 7.3$ volts $I_C = 0.6$ mA

by just changing transistors at a constant temperature (the effect will be slightly worse than shown because as the operating current falls, $h_{FE}$ will also fall resulting in a slightly lower end point and vice-versa). The change shown above may not seem very large but if the optimum operating point was chosen at a lower collector to emitter voltage, the additional drop for transistors with high limit values of $h_{FE}$ could carry this voltage down to a point where the transistor becomes inoperative as a class A amplifier.

When bias stabilization is used, the d.c. feedback will hold the operating point relatively constant for quite a wide variety of transistors.

# CLASS A POWER AMPLIFIERS

The choice of operating point in a class A transformer coupled transistor amplifier being designed for maximum output power is affected by three things:—

1. The power dissipation in the collector circuit when there is no input signal must not exceed the collector dissipation rating.
2. The mean and peak collector current ratings must not be exceeded.
3. The mean and peak collector voltage ratings must not be exceeded.

The last point can be fixed by correct choice of the supply voltage, $V_{CC}$, which must not be

greater than the mean collector voltage rating and not be greater than half of the peak collector voltage rating. Some manufacturers do not give the two separate ratings and the value given has to be taken as an absolute maximum.

The best procedure when the supply voltage is fixed is to design to keep within the collector dissipation rating and check to see whether the collector current ratings are being exceeded. The peak collector current rating $I_{CM}$, of a transistor is not set by any damaging effect on the transistor but by the rapid fall off of the current amplification factor which occurs if the collector current is allowed to rise too high. If the supply voltage can be chosen to suit the optimum requirements the transistor stage can be designed to have a dissipation equal to the maximum collector dissipation rating for zero input signal and a peak collector current equal to the peak collector current rating or twice the mean current rating depending on which is the smallest. The optimum battery voltage is then

$$V_{CC} = \frac{2\ P_{CM}}{I_{CM}} \text{ or } \frac{P_{CM}}{I_{CAV}}$$

where $P_C$ is the collector dissipation rating.
$I_{CM}$ is the peak collector current rating.
$I_{CAV}$ is the average collector current rating.

In most cases the supply voltage will be fixed by available batteries and once an idea of the optimum voltage is obtained a battery must be chosen which is as near as possible to this value. Having decided on the supply voltage the next step is to calculate the optimum load impedance. Resistive loads are assumed here to simplify the calculations.

## Calculation of optimum load impedance

Theoretical Considerations:—

It is assumed that the collector characteristics are ideal, having "knee" voltages of zero.

Average collector current

$= I_{CQ}$ (the symbol Q denotes the average value when a signal is applied)

$$= \frac{P_{CM}}{V_{CC}}$$

The collector current for maximum output power, will swing down to zero on one half cycle and up to a value of $2\ I_{CQ}$ on the other half cycle. Hence Peak Collector Current

$$= I_{cm}$$

$$= 2 \times \frac{P_{CM}}{V_{CC}}$$

Hence, we can see from Fig. 4 that

$$R_L = \frac{V_{CC}}{I_{CQ}}$$

$$= \frac{V_{C}{}^2}{P_{CM}}$$

Power Input $= V_{CC} \cdot I_{CQ}$

Max. Power Output $= \frac{V_{CC} \cdot I_{CQ}}{2}$

Max. Efficiency $= 50\%$

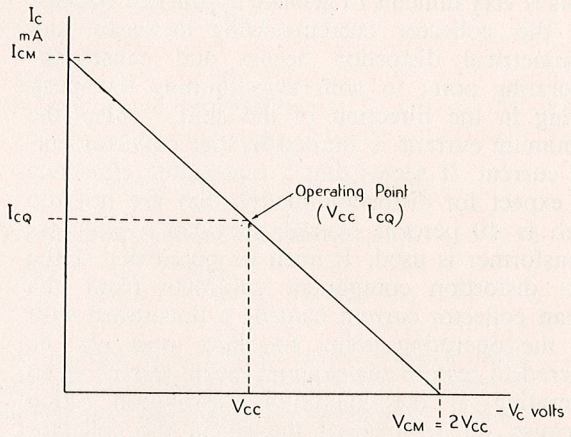



Fig. 4 Ideal Load Line.

## Practical considerations

The theoretical considerations assume that the collector voltage swings right down to zero volts during one half of the cycle. In practice of course, this voltage swing is limited by the knee of the collector characteristics. The knee voltage of most transistors is well below 1 volt and hence it is usually quite reasonable to assume that the peak voltage swing can be equal to 0.9 $V_{CC}$.

$$\text{Hence } R_L = \frac{0.9\ V_{CC}}{I_{CQ}}$$

$$\text{Max. Power Out} = \frac{0.9\ V_{CC} \cdot I_{CQ}}{2}$$

$$\text{Power In} = V_{CC} \cdot I_{CQ}$$

$$\text{Max. Efficiency} = 45\%$$

This is the collector efficiency and does not include losses in the output transformer. A collector current swing from zero to 2 $I_{CQ}$ is assumed in gaining an efficiency of 45 percent. This is very difficult to achieve in practice because as the collector current swing increases, unsymmetrical distortion occurs and causes the operating point to shift thus limiting the peak swing in the direction of the shift. Also the minimum current is limited by the collector cut-off current. It seems that a reasonable efficiency to expect for distortion figures that are not too high is 40 percent overall provided a low loss transformer is used. It must be noted that if the d.c. distortion component subtracts from the mean collector current causing a downward shift in the operating point, the bias must not be altered to restore the original mean current when operating at the maximum dissipation rating because on removal of the signal the collector dissipation will be higher.

Let us now determine suitable operating conditions for the 2N109 where maximum power output is required.

The relevant maximum ratings are

$P_{CM} = 50$ mW
$I_{CM} = -70$ mA
$I_{CAV} = -35$ mA
$V_{CM} = -25$ V

$$I_{CQ} = \frac{P_{CM}}{V_{CC}}$$

$$= \frac{-50 \times 10^{-3}}{9} \text{ for a 9 volt supply.}$$

$$= -5.5 \text{ mA}$$

Hence $I_{cm} = -11$ mA which is well below the rating of 70 mA.

$$R_L = \frac{0.9\ V_{CC}}{I_{CQ}}$$

$$= \frac{0.9 \times 9}{5.5 \times 10^{-3}}$$

$$= 1470 \text{ ohms.}$$

$$\approx 1500 \text{ ohms.}$$

For a smaller battery voltage $R_L$ will be smaller and vice-versa. If a smaller battery voltage is used, $I_{cm}$ will be greater for the same power output and hence a limit will be set by the maximum permissible value, $I_{CM}$.

$$\text{Minimum } V_{CC} = \frac{2\ P_{CM}}{I_{CM}} = \frac{-2 \times 50 \times 10^{-3}}{70 \times 10^{-3}}$$

$= -1.43$ volts for maximum power output from this transistor.

## CLASS B POWER AMPLIFIERS

When designing a class B audio amplifier the first requirement is to find a suitable pair of transistors to give the desired power output. The maximum power output from a pair of transistors can be expressed directly in terms of 2 $P_{CM}$ the combined collector dissipation rating for the two

transistors.

Consider one cycle of operation of a class B pushpull stage:—

Referring to Fig. 5 we find that the average current per transistor over one full cycle

$$= \frac{1}{2\pi} \int_0^{2\pi} I_{CM} \sin\theta \, d\theta \quad (\theta \text{ in radians})$$

$$= \frac{I_{cm}}{\pi}$$

Hence the average current for two transistors over one full cycle $= 2 \frac{I_{CM}}{\pi}$

$$\text{Power input to stage} = V_{CC} \cdot \frac{2}{\pi} \cdot I_{cm}$$

$$\text{Power output} = \frac{V_{cm} I_{cm}}{2}$$

where $V_{cm}$ is the peak collector voltage swing

$$\text{Hence dissipation} = V_{CC} \cdot I_{cm} \cdot \frac{2}{\pi} - \frac{V_{cm} \cdot I_{cm}}{2}$$

$$= \frac{2 I_{cm}}{\pi} \left[ V_{CC} - V_{cm} \cdot \frac{\pi}{4} \right]$$

The maximum theoretical output power is obtained when the peak voltage swing is equal to the collector supply voltage.

i.e. $V_{cm} = V_{CC}$

Then, the maximum theoretical efficiency is given by

$$= \frac{V_{CC} \cdot I_{cm}}{2} \times \frac{\pi}{2 V_{CC} \cdot I_{cm}} \times \frac{100}{1}$$

$$= \frac{\pi}{4} \cdot \frac{100}{1}$$

$$= 78.6\%$$

The maximum theoretical output power can be calculated from the following relationship:—

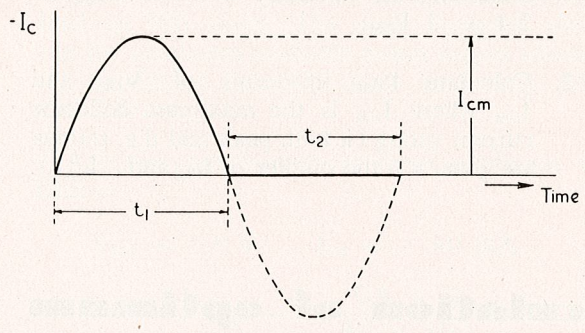
$$\frac{\text{Maximum Power Output}}{\text{Maximum Allowable Dissipation}} = \frac{V_{CC} I_{cm}}{2} \cdot \frac{\pi}{2 I_{cm} \cdot V_{CC} (1 - \frac{\pi}{4})}$$

$$= \frac{\pi}{4 - \pi}$$

i.e. $\frac{P_{OM}}{2 P_{CM}} = 3.86$

Hence for a pair of 2N109's at 55°C.

$P_{OM} = 386$ mW




Fig, 5 Collector Current for one transistor,

t1 = time during which transistor 1 conducts.
t2 = time during which transistor 2 conducts

Certain practical limitations must now be applied to these considerations. As in the case of the class A amplifier, let us take a typical case where $V_{CM} = 0.9\ V_{CC}$.

$$\text{Then dissipation} = \frac{2}{\pi} \cdot I_{cm} V_{cm} (1.11 - 0.786)$$

$$= \frac{2}{\pi} \cdot I_{cm} V_{cm} \cdot 0.324$$

$$= 0.206\ I_{cm} \cdot V_{cm}$$

$$P_{OM} = 2 \frac{P_{CM}}{2 \times 0.206}$$

$$= 2.42 \times 2\ P_{CM}$$

$$\approx 240 \text{ mW for the 2N109's.}$$

This corresponds to an efficiency of

$$\frac{0.9}{2} \cdot \frac{\pi}{2} \cdot \frac{100}{1} = 70.6\%$$

The maximum available power output from a pair of transistors as calculated above is dependent on the collector dissipation alone. However, for a given supply voltage it may not be possible to achieve this power without exceeding the collector current rating. For any transistor type there will be a minimum supply voltage (the approximation is made that the supply voltage is equal to the collector to emitter voltage) below which the calculated power output can only be achieved by exceeding the collector current rating. For lower supply voltages the collector current rating will limit the output power. For higher supply voltages the dissipation will limit the output power as calculated above. To quickly establish the available

output power from a pair of transistors operating from a supply voltage $V_{c'c}$, the procedure is as follows:—

1. Calculate $P_{OM}$ in terms of dissipation. Assuming an efficiency of 70% $P_{OM} = 2.4 \times 2\ P_{CM}$.

2. Calculate $P_{OM}$ in terms of $V_{c'c}$ and $I_{CM}$ where $I_{CM}$ is the maximum collector current rating (if both peak and d.c. ratings are given use the smaller of $I_{CM}$ and $\pi\ I_{CAV}$).

$$P_{OM} = \frac{0.9 \cdot V_{CC} \cdot I_{CM}}{2}$$

3. The lower of these is the maximum available output power for the supply voltage $V_{CC}$.
It may be required to know the minimum supply voltage for which $2.4 \times 2\ P_{CM}$ can be obtained.

$$V_{CC}\ \text{min.} = \frac{4.8 \times 2P_{CM}}{I_{CM}}$$

## Calculation of optimum load impedance

When designing a class B stage the following points have to be considered:—

1. The supply voltage $V_{c'c}$ must be chosen so that the collector voltage rating is not exceeded at any time. During the half cycle when one transistor is conducting, transformer action causes the voltage across the other transistor to rise in magnitude to a value of $V_{CC} + V_{cm}$. ($V_{cm}$ is the peak collector voltage swing). Ideally, the maximum value of $V_{cm}$ is equal to $V_{c'c}$. Hence $V_{c'c}$ must be equal to or less than half of the collector voltage rating. If both peak and d.c. ratings are given $V_{CC}$ must be equal to or less than both the d.c. rating and half of the peak rating.

2. Having decided on a supply voltage the load impedance must be chosen so that when the stage is driven to full output the dissipation and current ratings will not be exceeded.

Let us consider a stage using two 2N109's.

As calculated from the dissipation, taking

$\eta = 70\%$,

$P_{OM} = 240$ mW

In terms of $V_{c'c}$ and $I_{CM}$, taking $V_{c'c} = 9$ volts.

$$P_{OM} = \frac{0.9\ V_{CC}\ I_{CM}}{2}$$

$$= \frac{0.9 \times 9 \times 70}{2}\ \text{mW}$$

$$= 284\ \text{mW}$$

Hence the dissipation is the limiting factor.
(We also note that the minimum supply voltage at which the $P_O$ max. can be obtained is

$$V_{CC} = -\frac{4.8 \times 2\ P_{CM}}{I_{CM}}$$

$$= -\frac{4.8 \times 100}{70}$$

$$= -6.9\ \text{volts.})$$

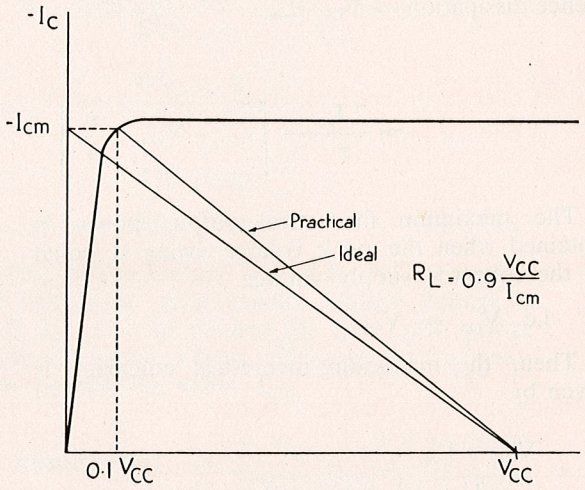



Fig. 6 Load-line for one transistor.

The next step it to find the peak collector current which will be reached and then the load impedance can be calculated.

$$2\ P_{CM} = \frac{2}{\pi} V_{CC}\ I_{cm}\ \left(1 - \frac{\eta}{100}\right)$$

$$\text{hence } I_{cm} = \frac{\pi\ P_{CM}}{V_{CC}\left(1 - \frac{\eta}{100}\right)}$$

$$= \frac{\pi P_{CM}}{0.3 V_{CC}}$$

Now $R_L = \frac{0.9 V_{CC}}{I_{cm}}$ (from Fig. 6)

$$= \frac{0.9 V_{CC} 0.3 V_{CC}}{\pi P_{cm}}$$ (Substituting for $I_{cm}$)

$$= \frac{0.27 \times V_{CC}^2}{\pi P_{CM}}$$ ohms per transistor

Collector to collector impedance = 4 $R_L$. Substituting the values for the 2N109.

$$I_{cm} = -\frac{\pi P_{CM}}{0.3 V_{CC}}$$

$$= -\frac{\pi \times 50 \times 10^{-3}}{0.3 \times 9}$$

$$= -58 \text{ mA}$$

$$R_L = \frac{0.9 V_{CC}}{I_{cm}}$$

$$= \frac{0.9 \times 9}{58 \times 10^{-3}}$$

$$= 140 \text{ ohms}$$

Collector to collector load = 560 ohms. (When $I_{CM}$ is the limiting factor

$$R_L = \frac{0.9 V_{CC}}{I_{CM}})$$

The conditions quoted for the 2N109 in class B with a 9 volt supply in Radiotronics, September, 1957, show the collector to collector load as 800 ohms. The stage designed above was for maximum available power output whereas the conditions for 800 ohms load only yield 160 mW output.

Applying our formula to these conditions we find:—

$V_{CC} = -9$ V $\quad I_{cm} = -40$ mA

$$R_L = \frac{0.9 \times 9}{40 \times 10^{-3}}$$

$$= 200 \text{ ohms}$$

$$P_O = -\frac{0.9 \times 9 \times 40}{2} \text{ mW}$$

$$= 162 \text{ mW}$$

These agree with the load and power output quoted. It will be noted that the average current for full output is – 26 mA.

$$\text{In our case } I_Q = -\frac{2}{\pi} \times 58$$

$$= -37 \text{ mA}$$

## Cross-over distortion

Having selected a suitable load impedance we must now fix the zero signal collector current. Ideally we would apply no bias and operate with a zero signal collector current equal to $I'_{CO}$ at the supply voltage used. However due to the non-linearity of the input voltage versus collector current characteristic (shown for the 2N109 in Fig. 7) in the small signal region, distortion occurs when the input signal passes through zero. This is termed cross-over distortion because it occurs during the change-over from one transistor to the other. Cross-over distortion can be kept quite small by applying a forward bias to the input circuit. This bias produces a zero signal standing collector current which of course must not be large enough to cause the collector dissipation to exceed the maximum rating. The bias required can be determined from the $I_C$ versus $V_{BE}$ characteristic. The characteristic is normally plotted for a low collector to emitter voltage to keep the dissipation down. The full line in Fig. 7 is the curve given in the data on the 2N109. The dotted line has been plotted from the collector characteristics for $V_{CE} = -9$ volts. A bias point sometimes quoted is the projected cut-off voltage which is shown as point X in Fig. 7. It is found by projecting the main part of the curve down in a straight line until it cuts the axis and then projecting vertically upwards to find the appropriate point on the curve[4]. However, in practice a much smaller bias can be used without introducing very much distortion. It is hard to eliminate cross-over distortion completely and the best method of determining the optimum compromise seems to be to adjust the bias for a pre-determined distortion level at a fairly low output level (say 50 mW for the stage being described). The bias which will be used in this stage (and which has been determined experimentally) is point Y in Fig. 7 and

corresponds to a base to emitter voltage of – 150 mV.

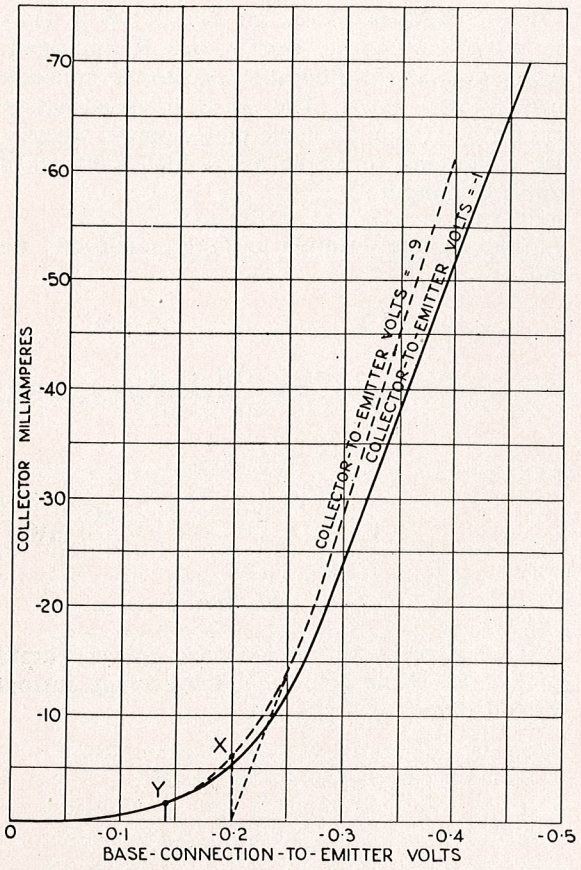



**Fig. 7** Collector current versus Input Voltage

There is another point of interest which should be included in this discussion of cross-over distortion. The $I_C$ versus $V_{BE}$ curve which really applies to our case would follow the $V_{CE} = -9$ volt curve for low collector currents but deviate towards, or even past the $V_{CE} = -1$ volt curve as the operating point approaches the "knee" of the collector characteristics. This curve can be viewed in the manner shown in Fig. 8 on the face of a c.r.o. The input is adjusted up until $I_{cm} = -58$ mA. It can be seen that the conditions simulate the operating conditions of one transistor in our stage except for the omission of the forward bias. The curve that will be observed using this method will be found to show a hysteresis type of loop as in Fig. 9. This is because the transistor is undergoing a thermal cycle which is caused by the varying instantaneous dissipation within the transistor.

This illustrates the need for experimental determination of the forward bias because the curves available do not and cannot simulate the conditions required. However a more interesting

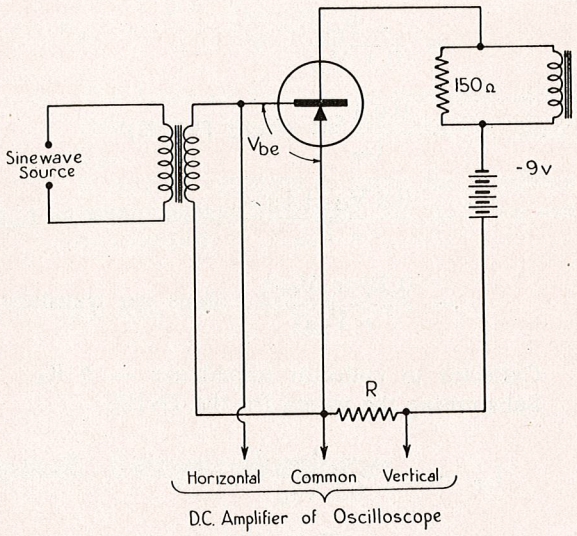



Fig. 8 Method of illustrating transfer characteristic R ≈ 5 ohms is used to measure the emitter current which approximately equals the collector current.

point is the effect of this thermal cycle on the stage output waveform. The irregularity in this waveform which has been termed "crossover distortion" is not symmetrical about the zero axis due to the hysteresis loop shown in Fig. 9, as shown in Fig. 10.

The reason for this is best explained by reference to Figs. 9 and 10. The path traced out by the collector current of the first transistor follows the curve from A to B and then returns along BC. During the early portion of the following half cycle, this transistor becomes completely cut-off. The collector current of the

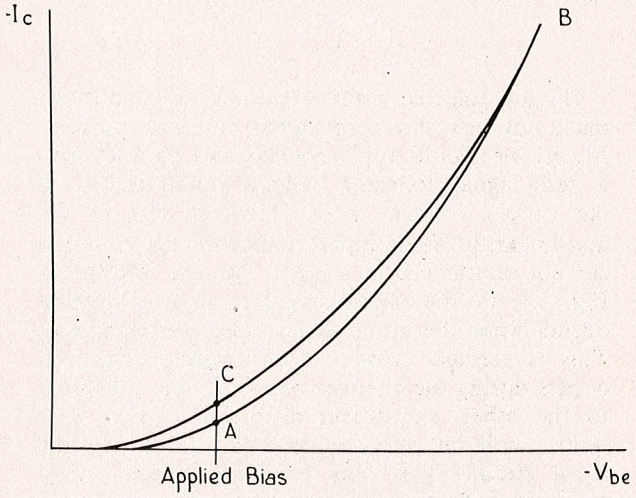



Fig. 9 Effect of thermal cycle on transfer characteristic

second transistor begins to rise just before the end of the first half cycle and is at point A as

the second half cycle commences. Let us consider the resultant current at this instant.

If the points C and A coincided, the currents in each half of the transformer primary winding would be equal but opposite in direction and hence cancel. Because the current corresponding to point C is larger than that for point A the currents flowing in the two halves of the primary winding do not cancel. The effective current in the primary at this instant is that of the first transistor (point C) minus that of the second transistor (point A). Hence the current transformed to the load is not zero at this instant as it should be. A short time later, the first transistor becomes cut-off and the current waveform suffers a slight change in direction as it becomes dependent on the second transistor alone. At this instant, the current can be quite large, depending on the difference between the two paths on the transfer characteristic. Fig. 10 shows the resultant output current waveform derived from the input characteristics for a perfectly matched pair of transistors. It is easy to see that the effect described will vary if the transistors used are not properly matched and that the resultant distortion percentage will be

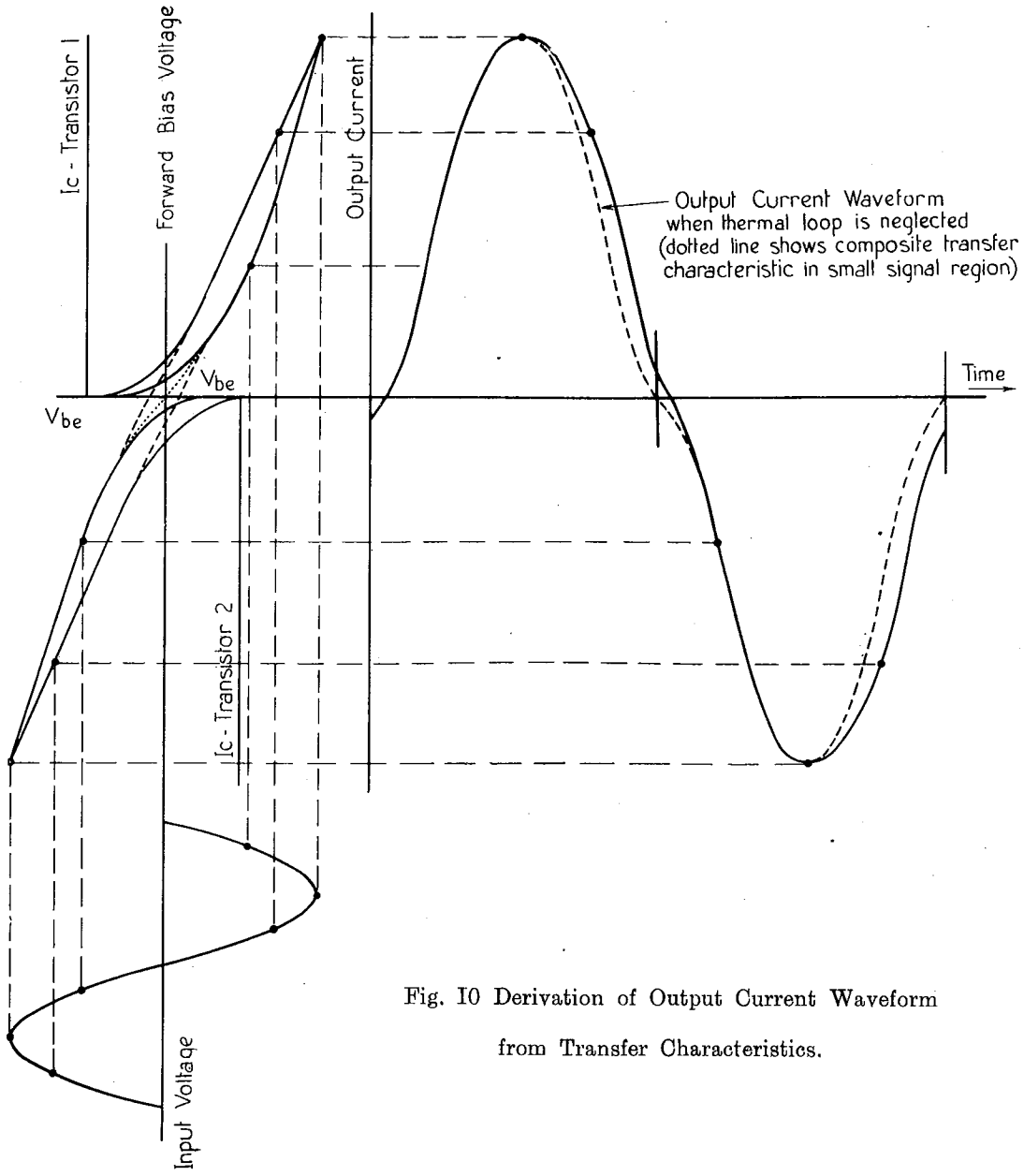



Fig. I0 Derivation of Output Current Waveform from Transfer Characteristics.

higher. It will also be observed that the output current waveform has suffered some phase shift due to the thermal cycle within the transistor. The loop in the transfer characteristics will vary with frequency and so there will be some phase distortion introduced by this stage.

The bias is applied to the centre tap of secondary of the driver transformer and must be developed in a very low impedance source because this source will be in series with the input signal. Furthermore, the bias impedance cannot be bypassed by a capacitor because rectification of the input signal would cause the capacitor to become charged and thus present an additional bias.

The bias developing circuit is shown in Fig. 11. Here we know that $I_{BIAS} \cdot R_2 = 150$ mV. If $I_{BIAS}$ is small, $R_2$ must be made large and will attenuate the input signal appreciably. However, if $R_2$ is made extremely small the bias current will have to be extremely large. For example if $R_1$ is 15 ohms, $I_{BIAS}$ is 10 mA for 9 volts $V_{CC}$. This is, of course, much too large. The best approach seems to be to choose the maximum current which is considered permissible and then calculate $R_2$.

Taking $I_{BIAS} = 1.3$ mA

$$R_2 = \frac{0.150}{1.3}$$

$$= 115 \text{ ohms}$$

$$\approx 120 \text{ ohms}$$

$$R_1 = \frac{9}{1.3} \times 10^3$$

$$= 6.8 \text{ K}\Omega$$

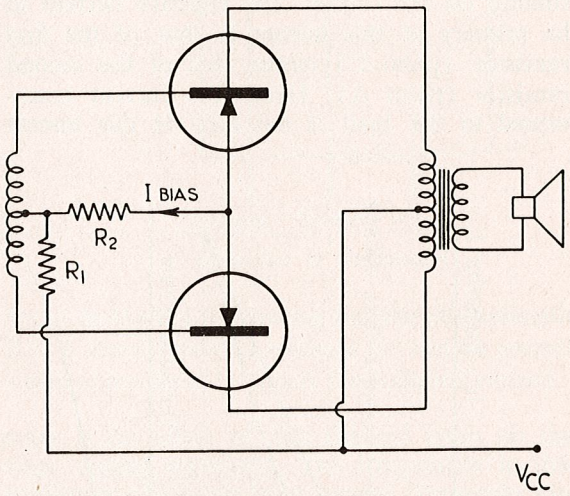



Fig. 11 Biasing developing circuit.

To stabilize this stage against drift due to temperature variations, the resistance $R_2$ is normally made up of a thermistor with a shunt and series resistance network to achieve the correct degree of compensation [5].

## Power input for maximum power output

It is now possible to determine approximately the power input required to drive this stage for maximum output. Referring to Fig. 7 we find that for a peak collector current of 58 mA the required peak input voltage is 420 mV. From the $I_B$ versus $V_{BE}$ curve shown in Fig. 12 (this curve is the same for $V_{CE} = -1$ to $-9$ volts) it will be noted that for an input voltage of 420 mV the base current is 0.89 mA. The peak input voltage from the driver transformer can be calculated from the formula shown in Fig. 13.

$$v_M = v_{BE} + v_{AC} - V_{BIAS}$$

$$= 420 + 107 - 150$$

$$= 377 \text{ mV.}$$

Hence, due to the forward bias voltage on the transistor, the peak transformer voltage is less than the required peak input voltage by an amount equal to the bias voltage minus the a.c. voltage drop across the bias resistor.

The input power required from the transformer is then, $P_{in}$ per transistor

$$\approx \frac{420 \times 10^{-3} \times 0.89 \times 10^{-3}}{2}$$

$$\approx 0.187 \text{ mW for one half cycle.}$$

During the other half cycle the power input to the other transistor is the same.

$$\therefore P_{in} \approx 0.187 \text{ mW}$$

Although some approximations have been made in calculating this input power, it can now be used to determine, approximately, the stage gain.

$$\text{Power Output} = \frac{0.9\, I_{cm} \times V_{CC}}{2} = 240 \text{ mW}$$

$$\text{Power Input} \approx 0.187 \text{ mW}$$

$$\therefore \text{ Power Gain} \approx \frac{240 \times 10^{-3}}{0.187 \times 10^{-3}}$$

$$\approx 1280$$

$$\approx 31 \text{ db}$$

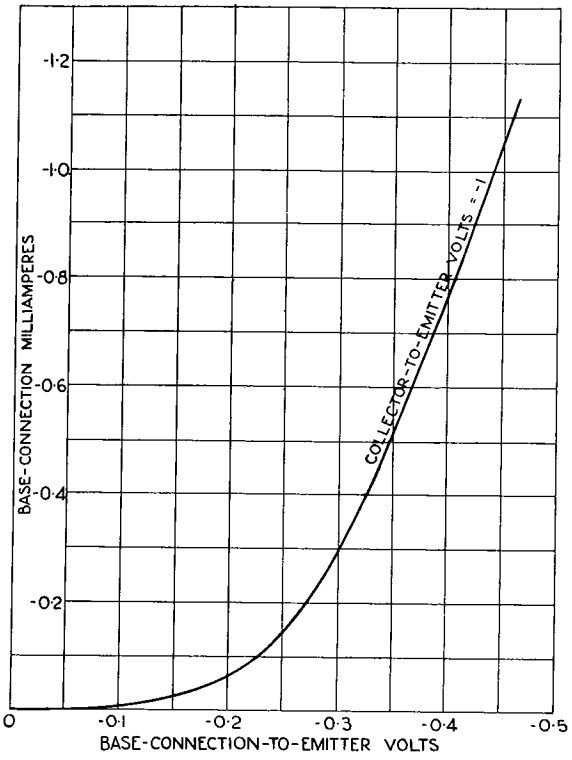



Fig. 12 Base current versus Input Voltage

The input impedance to each transistor during its conducting period varies as can be seen from the varying slope of the input characteristic of Fig. 12. Here, once again, an approximation can be made by determining the slope of the curve at a mid-point in the operating region (the major part of the variation has been eliminated by the forward bias). The impedance measured in this way is approximately 180 ohms. However, the impedance seen by the transformer is much greater than this due to the effect of the biasing circuit. At the instant of peak current flow.

$$R_{in} = \frac{420 \times 10^{-3}}{0.89 \times 10^{-3}}$$

$$= 470 \text{ ohms}$$

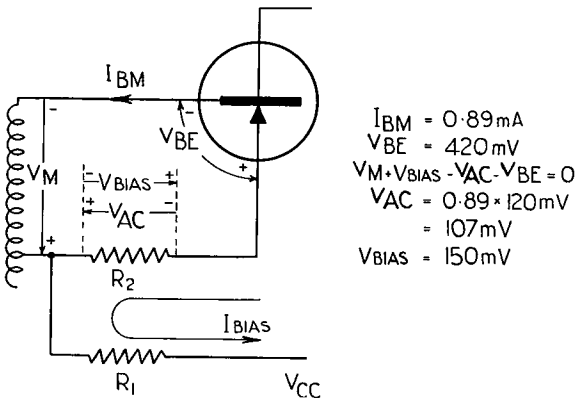



Fig. 13 Voltage relationships at instant of peak input voltage

Hence the peak to peak impedance is approximately 940 ohms. To obtain good linearity it is necessary to make the source impedance at least ten times the input impedance to simulate a constant current source. This increased linearity (or reduced distortion) is obtained at the expense of power gain because of the mismatch in the input. Assuming a factor of ten times, and a transformer efficiency of 70 percent the power required to drive this stage is

$$0.187 \times 10^{-3} \times 11 \times \frac{10}{7} \text{ watts}$$

$$\approx 3 \text{ mW}$$

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