ELECTRONIC COUNTING

circuits
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devices

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The bulk of the information contained in this book is based on material supplied by B. S. Cowle and J. E. Gilliam of the Mullard Central Application Laboratory. The chapter on numerical indicator tubes is based on material supplied by B. Butler of the Mullard Industrial Electronics Division.

The chapter on the language of logic is based on similar chapters in the Electronics Trainer Manual Part VIII produced by the International Centre for the Furtherance of Science Teaching in co-operation with R. H. Grigg of the Military College of Science, Shrivenham.

FOREWORD

The increasing use of mechanisation and automation in factories has given rise to an increased interest in counting. Whether the application is in monitoring the position of a machine tool by digital means, or in packing a certain number of items in a box, a problem of counting arises. In many laboratory instruments too—such as frequency counters, timers and digital voltmeters—the basic function is that of counting.

Electronics, particularly with transistors and integrated circuits, has revolutionised counting equipment, and the present book is intended to help engineers to use electronics to solve their counting problems as simply or as cheaply as possible. The book contains many practical circuits, but it also contains a great deal of theoretical information from which the reader can design a counter to meet his own particular needs.

CONTENTS

CHAPTER 1

INTRODUCTION

Since the dawn of civilisation, man has found it necessary to count; that is, to have a method of representing quantities or measures and of manipulating them to perform functions of addition, subtraction, multiplication and division. Not unreasonably, he found that his fingers provided an excellent physical aid for registering any counting exercise he was doing in his head, and it is from this that the decimal system developed.

The decimal system may be expressed fully in mathematical terms as follows, by considering the number 147 as an example. This is the conventional shorthand way of expressing a decimal number. The longhand way of writing the same number is $1 \times 10^2 + 4 \times 10^1 + 7 \times 10^0$. The ten is known as the base, or radix, of the system and the indices indicate the power to which the base is raised. The base and the particular index to which it is raised are called the weight; that is, the least significant weight is 10^0 which is 1, the next is 10^1 which is 10, and so on. The numbers by which each weight is multiplied are called digits. In practice, only the digits of the system are written, the weights being implied.

Once the full way of writing a number to the base 10 is understood, it is a simple step to express the same number to any base one chooses. Some examples are given below.

$$147 = 1 \times 10^2 + 4 \times 10^1 + 7 \times 10^0 \qquad\qquad = (147)_{10}$$
$$= 2 \times 8^2 + 2 \times 8^1 + 3 \times 8^0 \qquad\qquad = (223)_8$$
$$= 1 \times 5^3 + 0 \times 5^2 + 4 \times 5^1 + 2 \times 5^0 \qquad = (1042)_5$$
$$= 1 \times 2^7 + 0 \times 2^6 + 0 \times 2^5 + 1 \times 2^4 + 0 \times 2^3 + 0 \times 2^2 +$$
$$+ 1 \times 2^1 + 1 \times 2^0 = (10010011)_2$$

It is evident from the last example that the digits of the system using a base of two are either one or nought, and this is true for any number expressed to the base of two.

A list of powers of two, together with their equivalent decimal numbers, is given in Table 1.

Numbers expressed to the base of two are useful for electronic counting systems because electronic circuits which can be set in one of two states are made very simply, whereas circuits with more than two states, although possible, are much more complex and less reliable. The counting system

using a base of two is called the binary system and each '1' or '0' is called a *bit*, this being a contraction of *binary digit*. The number of bits in the

TABLE 1

Powers of Two together with their Equivalent Decimal Numbers

$2^0 = 1$	$2^5 = 32$	$2^{10} = 1024$
$2^1 = 2$	$2^6 = 64$	$2^{11} = 2048$
$2^2 = 4$	$2^7 = 128$	$2^{12} = 4096$
$2^3 = 8$	$2^8 = 256$	$2^{13} = 8192$
$2^4 = 16$	$2^9 = 512$	$2^{14} = 16384$

binary form of the decimal number 147 is eight, as shown above, and the highest decimal number which can be obtained with eight bits is 255.

The binary code discussed so far is not the only code which is expressed in two-state bits. All counting codes with two-state bits, however, fall into one of two classes—weighted and unweighted. A weighted code is one in which a '1' bit is allotted different values depending upon its position in the number. For example, the above binary code is weighted; a '1' in the first position is worth 1, a '1' in the second position is worth 2, a '1' in the third position is worth 4 and so on. The order of bits in un-weighted codes changes in such a way as to make this sort of weighting meaningless.

A system in which binary-type elements are connected together to count as though to a base of ten is called a Binary Coded Decimal system, BCD for short. BCD is of major importance since it provides the link between the counting system used by the machine and that used by man.

Weighted Codes

There are several weighted BCD codes, but the initial problems in forming BCD are common to all systems. The first problem is to make the system repeat itself after ten counts. If four binary elements are connected in series, sixteen separately identifiable states exist, as shown in Table 2, but for a decade counter, only ten states are required. The problem, therefore, is to find a method of restoring the counter to the 0 0 0 0 state after ten counts instead of sixteen. This is achieved by gating techniques which are discussed fully in subsequent chapters of this book. The second problem is to allocate weights to each column of the counting sequence table in such a way that the sum in any row is equal to the decimal value which that row represents.

Two common weighted BCD codes are given in Table 3. The procedure for associating a binary combination in the table with its appropriate decimal number is called 'decoding'. It is unimportant where the gating

operations occur to shorten the cycle to ten, provided that the rows may be decoded to give the correct decimal number.

TABLE 2
Binary Table

Decimal Number	Binary States			
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

TABLE 3
Two Weighted BCD Codes

| Decimal Number Weights | 1248BCD | | | | Weights | 1242BCD | | | |
	8	4	2	1		2	4	2	1
0	0	0	0	0		0	0	0	0
1	0	0	0	1		0	0	0	1
2	0	0	1	0		1	0	0	0
3	0	0	1	1		1	0	0	1
4	0	1	0	0		1	0	1	0
5	0	1	0	1		1	0	1	1
6	0	1	1	0		1	1	0	0
7	0	1	1	1		1	1	0	1
8	1	0	0	0		1	1	1	0
9	1	0	0	1		1	1	1	1

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Unweighted Codes

Unweighted codes are used at times when their special features are advantageous. The unweighted codes most frequently encountered are known as cyclic progressive codes. The special feature of these codes is that only one bit changes between consecutive states in a counting sequence. This overcomes ambiguities which could arise when several bits try to change simultaneously. For example, if a disc used for monitoring the rotation of a shaft were coded in 1248BCD, when the shaft moved from position 7 to position 8, all the digits would change. If the disc were stopped somewhere between these two coded positions, a wrong reading could be obtained. This is particularly likely if there is any misalignment between the disc and the sensing elements which transmit the code on the disc to the display. One example of a cyclic progressive code which repeats itself after ten counts is given in Table 4.

TABLE 4
Sequence of a Cyclic Progressive Code

Decimal Number

0	0	0	1	0
1	0	1	1	0
2	0	1	1	1
3	0	1	0	1
4	0	1	0	0
5	1	1	0	0
6	1	1	0	1
7	1	1	1	1
8	1	1	1	0
9	1	0	1	0

One-out-of-ten Code

The one-out-of-ten code is one which has ten bits, only one of which may in the '1' state at any time. This code is shown in Table 5. If ten binary elements are connected in such a way that the output of each feeds the input of the next, to form a ring, a counter is formed which operates in accordance with this table. This type of counter is known as a 'ring counter'.

TABLE 5
Sequence of the 1-out-of-10 Code
Decimal Number

0	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0
2	0	0	1	0	0	0	0	0	0	0
3	0	0	0	1	0	0	0	0	0	0
4	0	0	0	0	1	0	0	0	0	0
5	0	0	0	0	0	1	0	0	0	0
6	0	0	0	0	0	0	1	0	0	0
7	0	0	0	0	0	0	0	1	0	0
8	0	0	0	0	0	0	0	0	1	0
9	0	0	0	0	0	0	0	0	0	1

Twisted-ring or Johnson Code

If only five binary elements are connected to form a ring with one of the inter-stage connections inverted, a twisted-ring, or Johnson, counter is formed. The twisted-ring, or Johnson, code is shown in Table 6. This code has the advantage of needing fewer counting elements than the one-out-of-ten code, but is more difficult to decode. The twisted-ring code differs from the one-out-of-ten code in that more than one element may be a '1' at any time.

TABLE 6
Sequence of the Twisted-ring, or Johnson, Code
Decimal Number

0	0	0	0	0	0
1	1	0	0	0	0
2	1	1	0	0	0
3	1	1	1	0	0
4	1	1	1	1	0
5	1	1	1	1	1
6	0	1	1	1	1
7	0	0	1	1	1
8	0	0	0	1	1
9	0	0	0	0	1

CHAPTER 2

THE LANGUAGE OF LOGIC

A little over a hundred years ago, 'logical' or 'Boolean' algebra was developed by George Boole (Refs. 1 and 2) to simplify complex logical propositions, and Boolean algebra now plays an important part in the analysis and logic design of counting systems.

The Logic of Classes

In mathematical logic, a 'class' is defined as a group of elements, all of which possess at least one characteristic in common. From this definition, it follows that a complementary class can exist in which no member possesses the common characteristic. Both classes together may be taken to form the particular universal class under consideration. It is convenient to illustrate these ideas with the aid of a 'Venn diagram' as shown in Fig. 1.

The area within the square represents the universal class being considered. This class may be divided into a number of sub-classes, two in this case; class A contained within the circle and class Ā outside the circle (Fig. 1a). A bar is placed above the variable to denote the complement.

The 'logic of classes' is concerned with the relations between various sub-classes that may exist within a particular universal class. The complementary class has been introduced already, but it will be clear that the operations of 'intersection' and 'union' can also occur between sub-classes.

To clarify these ideas, the following example is considered:

A certain universal class is defined as a group of students, and is represented by the total area within the square. Two sub-classes exist in the group of students as shown in the 'Venn' diagrams of Figs. 1b, 1c, 1d, 1e and 1f.
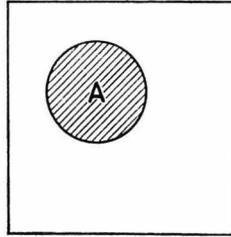
Notice that when 'intersection' occurs (Fig. 1e), the students are members of both A AND B. Intersection is denoted by a full stop thus: A.B. Since there is no change in the intersecting area, it is equally true to state that the students are members of both B AND A; hence
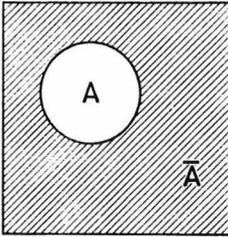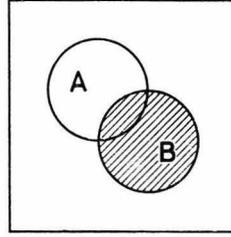
$$A.B = B.A.$$

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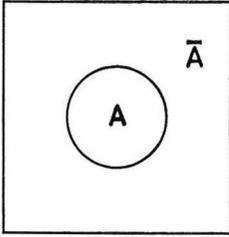
Fig. 1a—Venn diagram

Fig. 1b—Some are boys with brown hair
Shaded area = class A

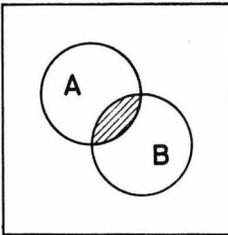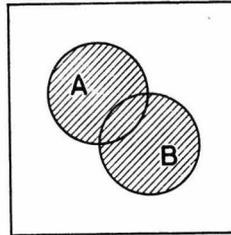Fig. 1c—The remainder are NOT boys
with brown hair. Shaded area= class $\bar{A}$

Fig. 1d—Some are boys with blue eyes.
Shaded area = class B

Fig. 1e—Some are boys with brown
hair AND blue eyes. Shaded area =
intersection of A and B

Fig. 1f—Some are boys with brown hair
OR blue eyes OR both. Shaded area =
union of A and B

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For the case of 'union' (Fig. 1f), the students are members of A or B or both, and this function is represented by a plus sign: $A+B$. Clearly, the area remains unaltered for $B+A$; therefore

$$A+B = B+A.$$

Obviously the order in which the variables are placed has no significance.

In the diagram for intersection (Fig. 1e), the area NOT shaded represents NOT (A AND B) which may be written as $\overline{A.B}$. The area shaded in Fig. 1g is NOT A OR NOT B (written as $\bar{A}+\bar{B}$) and is equivalent to the area NOT shaded in Fig. 1e. Thus:

$$\bar{A}+\bar{B} = \overline{A.B}.$$

Both diagrams are shown side by side to aid comparison. A similar proof can be obtained from Fig. 1f for $\bar{A}.\bar{B} = \overline{A+B}$, as shown again for clarity in Figs. 1i and 1j.

These two proofs confirm de Morgan's theorem which is extremely important in Boolean algebra. De Morgan's theorem is explained fully in the section on theorems later in this chapter.
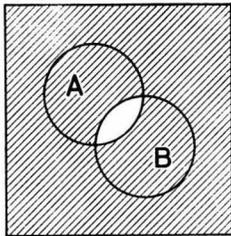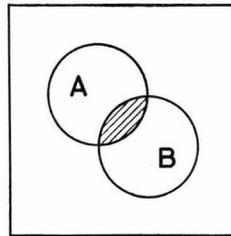
Fig. 1g—Shaded area $= \overline{A}+\overline{B}$
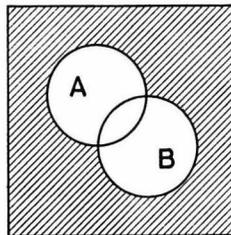
Fig. 1h—Unshaded area $= \overline{A.B}$

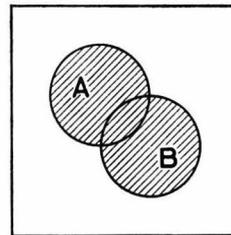Fig. 1i—Shaded area $= \overline{A}.\overline{B}$

Fig. 1j—Unshaded area $= \overline{A+B}$

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The Logic of Propositions

The theorems of Boolean algebra apply equally either to the logic of classes or to the logic of propositions, but in the latter, the emphasis is placed on whether a given statement is true or false. In compound logical propositions, two basic connectives are used, and since these are similar to the operations of intersection and union previously described, the same symbols will be used. The basic connectives are:

(a) AND, formally known as conjunction, written as A.B.

(b) OR, formally known as disjunction, written as A+B.

(In textbooks and current literature many different symbols are used for the basic connectives.)

'Conjunction' is the proposition that both A AND B are true, while 'disjunction' is the proposition that A OR B OR both are true. For example, the statement "Today is Tuesday and it is raining" can be represented as follows:

Let A = "Today is Tuesday" and B = "it is raining". If C = the complete statement, then C = A.B.

When is the complete statement true? This can be established by tabulating all the possible combinations of truth or falsity for A and B, and deciding the particular conditions under which C is true, as shown in Table 7.

TABLE 7
Possible Combinations of Truth or Falsity

A	B	C
False	False	False
False	True	False
True	False	False
True	True	True

Values can be assigned to these two possibilities and normally a '1' is used to denote the value of a true statement, and a '0' the value of a false statement. Under these conditions the table is that shown in Table 8.

TABLE 8
Possible Combinations of Truth or Falsity Expressed with Values of '1' and '0'

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

Such a table is known as a "Truth Table", and the proof is called a proof by the method of perfect induction. Clearly here the complete statement is true only when A AND B are true. That is, $C = A.B$.

A similar procedure can be adopted for disjunction, and the equation $A+B = C$ may be obtained from a suitable proposition such as "There is a voltage on terminal number 3 or on terminal number 7". The truth table is given in Table 9.

TABLE 9
Truth Table for Disjunction

A	B	C
0	0	0
1	0	1
0	1	1
1	1	1

In this case the complete statement is true when either A OR B is true. That is, $C = A+B$.

For the operation of complementing or negating, a bar is placed above the variable, and the truth table is that shown in Table 10.

TABLE 10
Truth Table for Complementing

A	Ā
0	1
1	0

Postulates

Only a summary of the 'postulates' (that is, fundamental conditions) is given here since the truth of these is self-evident. The eight postulates are as follows.

A variable may assume one of two values: 0 or 1;
The complement of 0 is 1 and vice versa;

$$1.1 = 1, \qquad 0+0 = 0;$$
$$1.0 = 0.1 = 0, \qquad 0+1 = 1+0 = 1;$$
$$0.0 = 0, \qquad 1+1 = 1.$$

The postulates form the basis of a number of theorems which allow expressions to be manipulated and simplified. Most theorems in Boolean algebra fall into pairs, each expression being the 'dual' of the other. In order to obtain the dual of an expression, it is necessary to exchange AND for OR and to exchange 0 for 1. An example will serve to illustrate the

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procedure, but in fact the last six postulates given above are presented in dual pairs.

The dual of

$$0.A+B.\bar{C}+1$$

is

$$(1+A).(B+\bar{C}).0.$$

It should be noted that normally the AND function takes precedence over the OR function in the absence of any other information. It is, therefore, necessary to add brackets to the dual expression to avoid any ambiguity.

Theorems

In an expression such as $A.B+\bar{A}.C+D.(\bar{B}+\bar{C})+\bar{D}.E$ there are five variables—A, B, C, D and E—and nine 'literals'. A literal is defined as each appearance of a variable or of its complement.

To obtain the complement of an expression, it is necessary to exchange AND for OR, to exchange 0 for 1 and to complement all literals.

The complement of

$$0.A+B.\bar{C}+1$$

is

$$(1+\bar{A}).(\bar{B}+C).0.$$

Where possible, the following theorems are presented in dual pairs. It may then be shown that, if the first expression is true, the dual must also be true. In order to prove this point, both expressions for theorem 1 will be verified using the method of perfect induction.

Theorem 1a) $A.0 = 0$;   Theorem 1b) $A+1 = 1$

Proof for theorem 1a: $A.0 = 0$

If $A = 0$ then $0.0 = 0$

If $A = 1$ then $1.0 = 0$

Both are postulates and are true, hence theorem 1a is true.

Proof for theorem 1b: $A+1 = 1$

If $A = 0$ then $0+1 = 1$

If $A = 1$ then $1+1 = 1$

Both are postulates and are true, hence theorem 1b is true.

A similar proof may be obtained for the following simple theorems:

Theorem 2a) $A.1 = A$;   Theorem 2b) $A+0 = A$.

Theorem 3a) $A.A = A$;   Theorem 3b) $A+A = A$.

Theorem 4a) $A.\bar{A} = 0$;   Theorem 4b) $\bar{A}+A = 1$.

Theorem 5a) $A.B = B.A$;   Theorem 5b) $A+B = B+A$.

Theorem 5, the "Commutative Law", states that the order in which the variables are placed is not significant. This was shown to be true by means of Venn diagrams in the previous section.

The remaining theorems can all be proved by constructing a truth table which shows all the possible combinations of the values of the variables involved. Theorem 6, the "Associative Law", will be taken as an example to demonstrate the method.

Theorem 6a) $A.B.C = A.(B.C) = (A.B).C$
Theorem 6b) $A+B+C = A+(B+C) = (A+B)+C$
It is required to prove that: $A.(B.C)=(A.B).C$
The truth table for this expression is given in Table 11.

TABLE 11
Truth Table for Theorem 6a

A	B	C	(B.C)	(A.B)	A.(B.C)	(A.B).C
0	0	0	0	0	0	0
1	0	0	0	0	0	0
0	1	0	0	0	0	0
1	1	0	0	1	0	0
0	0	1	0	0	0	0
1	0	1	0	0	0	0
0	1	1	1	0	0	0
1	1	1	1	1	1	1

The first three columns provide all the possible combinations of the variables, and the other columns are derived by appropriate combinations of the values of the variables involved. Since the last two columns are identical in all respects the expression is valid.

Theorem 7a) $\overline{A.B.C} = \bar{A}+\bar{B}+\bar{C}$;
Theorem 76) $\overline{A+B+C} = \bar{A}.\bar{B}.\bar{C}$.

In the previous section, Venn diagrams were used to verify de Morgan's theorem, which is stated above. The result is very important and should be noted carefully. It may be stated in a more general form as follows:

$$f(A,B,C, \text{ AND OR}) = f(\bar{A},\bar{B},\bar{C}, \text{ OR AND})$$

The symbol f denotes that the complement of the function is required; by applying the normal rules, AND is exchanged for OR and each literal is complemented. For example:

$$\overline{(\bar{A}.B+\bar{C}).D} = (A+\bar{B}).C+\bar{D}.$$

Two more theorems are:

Theorem 8a) $A.(A+B) = A$;   Theorem 8b) $A+(A.B) = A$.
Theorem 9a) $(A+B).(A+\bar{B}) = A$;   Theorem 9b) $(A.B)+(A.\bar{B}) = A$.

The "Distributive Law" given in theorem 10, below, is also very important, and requires careful attention:

B

Theorem 10a) $A.B+A.C = A.(B+C)$;
Theorem 10b) $(A+B).(A+C) = A+B.C$.

In theorem 10a the procedure is similar to normal algebraic factorising, but theorem 10b shows that the operations of AND and OR do not have precisely the same meaning as multiplication and addition in classical algebra, although the functions are frequently described by the terms "product" and "sum" respectively. Furthermore, an expression such as $A.B+C.\dot{D}$ is termed a "sum of products", while $(A+B).(C+D)$ is called a "product of sums".

In Boolean algebra there are four forms of expression that are of particular interest:

Expanded sum of products.   Expanded product of sums.
Minimum sum of products.   Minimum product of sums.

The expanded forms are often useful for the analysis and simplification of Boolean functions and their associated circuitry, while the minimum forms are of interest because these are most frequently used as the actual basis for the required circuits. In practice, however, the minimum may be defined in several different ways, largely dependent upon the type of logical circuit being used. For instance, with integrated circuits that use diode-transistor logic, the minimum should be defined as the smallest number of integrated circuits. If the Boolean function is complex, it is not always easy to determine a minimum by algebraic manipulation, and other methods of simplification must be adopted.

In order to obtain the expanded sum of products, theorem 9b is used, and all the possible combinations of the missing variables are supplied to each product as shown in the example below.

$$A.\bar{B}.C+A.\bar{C}.D = A.\bar{B}.C.D+A.\bar{B}.C.\bar{D}+A.\bar{C}.D$$
$$= A.\bar{B}.C.D+A.\bar{B}.C.\bar{D}+A.B.\bar{C}.D+A.\bar{B}.\bar{C}.D.$$

On the first line, $A.\bar{B}.C$ expands into two terms when the missing variable is supplied both as D and $\bar{D}$, and in the same way two further terms are formed from $A.\bar{C}.D$ by adding B and $\bar{B}$.

A similar operation is carried out for the expanded product of sums, in this case all the possible combinations of the missing variables being added to each sum. Thus, by expansion,

$$(A+\bar{C}).(B+\bar{C}) = (A+B+\bar{C}).(A+\bar{B}+\bar{C}).(\bar{A}+B+\bar{C}).$$

CONTACT SWITCHING CIRCUITS

In any logic switching circuit the particular conditions representing '0' and '1' must be clearly defined since the assignment of values has a profound effect, not only on the Boolean function representing a given circuit but also on the circuit associated with a particular function. The choice does

not, however, affect the algebra or its manipulations, but merely the interpretation placed on the variables and their values.

In general, the Boolean function describing a circuit sets down conditions in which a signal will be transmitted through the system. The normal convention adopted for a contact switching circuit is that a closed circuit is represented by '1' and an open circuit by '0'. Under these conditions, two switches wired in series will perform the AND function as shown in Fig. 2 and it may be seen that the maximum transmission is obtained between p and q when the circuit is closed.
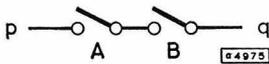
TABLE 12

Truth Table for AND Circuit

A	B	Circuit State
0	0	0 = Open
1	0	0 = Open
0	1	0 = Open
1	1	1 = Closed

Fig. 2—AND circuit

The action of the circuit is illustrated in Table 12, and clearly maximum transmission implies a low impedance path between p and q permitting an easy flow of current through the circuit.

Fig. 3 shows the parallel arrangement of switches required for the OR function and Table 13 shows the thruth table.
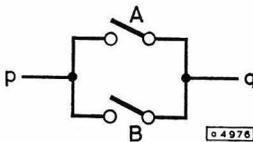
TABLE 13

Truth Table for OR Circuit

A	B	Circuit State
0	0	0 = Open
1	0	1 = Closed
0	1	1 = Closed
1	1	1 = Closed

Fig. 3—OR circuit

The operation of complementing means that the circuit is closed when the switch is NOT operated as illustrated in Fig. 4 and Table 14.

TABLE 14
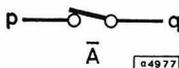
Truth Table for Complementing Circuit

A	$\bar{A}$	Circuit State
0	1	1 Closed
1	0	0 Open

Fig. 4—NOT circuit

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It is now possible to interpret the theorems of Boolean algebra in terms of switching circuits, as the following examples show.

Theorem 3 is shown in Fig. 5. Theorem 3a states that $A.A = A$ and theorem 3b states that $A+A = A$.

From Fig. 5 it may be seen that theorem 3 states that identical switches wired in series or in parallel can be replaced by a single switch.

It should be emphasised that the literals used in any theorem can represent single variables or complex expressions. For instance, theorem 3 may be employed to simply the following expression:

$$(\bar{A}.C.C+\bar{B}).(\bar{A}.C+\bar{B}+\bar{B}) = (\bar{A}.C+\bar{B}).(\bar{A}.C+\bar{B}+\bar{B})$$
$$= (\bar{A}.C+\bar{B}).(\bar{A}.C+\bar{B})$$
$$= (\bar{A}.C+\bar{B}).$$
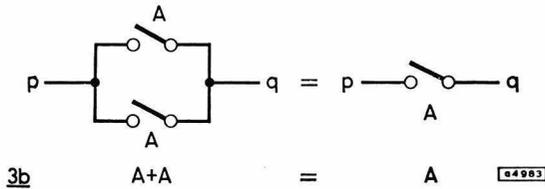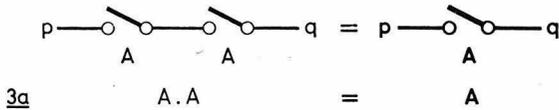
Fig. 5—Circuits for theorem 3

Theorem 8a (Fig. 6) states that any circuit consisting of a switch in series with a parallel circuit containing the same switch, may be replaced by a circuit consisting of the switch alone. Theorem 8b states that any circuit
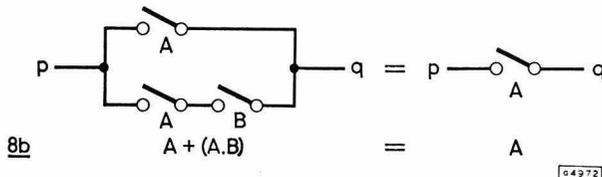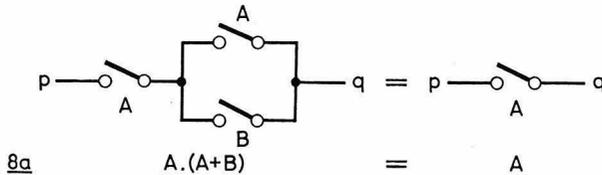

Fig. 6—Circuits for theorem 8

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consisting of a switch wired in parallel with a series circuit containing the same switch, may be replaced by a circuit consisting of the switch alone.

If the logic convention employed is inverted, that is to say a closed circuit is represented by '0' and an open circuit by '1', then, for a given circuit arrangement, the AND and OR functions are interchanged. For example, the parallel arrangement of switches in Fig. 7 is required for the AND function, while a series circuit is necessary for the OR function as shown in Fig. 8.
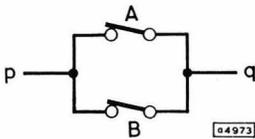
Fig. 7—AND circuit—Inverted Logic

TABLE 15

Truth Table for AND Circuit—Inverted Logic

A	B	Circuit State
0	0	0 = Closed
1	0	0 = Closed
0	1	0 = Closed
1	1	1 = Open
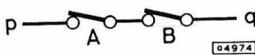
Fig. 8—OR circuit—Inverted Logic

**TABLE 16**

Truth Table for OR Circuit—Inverted Logic

A	B	Circuit State
0	0	0 = Closed
1	0	1 = Open
0	1	1 = Open
1	1	1 = Open

From the truth tables given in Tables 15 and 16, it is clear that minimum transmission or maximum hindrance is obtained when the circuit is open, and this implies a high impedance path between p and q.

A similar result can be obtained without inverting the logic if the Boolean function is complemented, as illustrated by de Morgan's theorem in Fig. 9 overleaf.
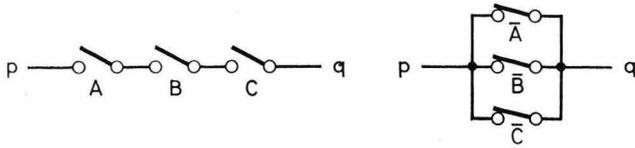
The complement of A.B.C is $\overline{A.B.C} = \overline{A}+\overline{B}+\overline{C}$
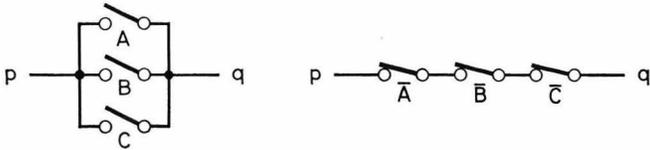
The complement of A+B+C is $\overline{A+B+C} = \overline{A}.\overline{B}.\overline{C}$

Fig. 9—Illustration of complements

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BASIC COUNTING ELEMENTS

The logic circuits described in Chapter 2 may be realised in a variety of ways by the use of active or passive electronic components in discrete or integrated form.

The logic states associated with electronic logic elements may be defined as '1' for the presence of a voltage and '0' for the absence of any voltage. Other definitions are possible, but for the purpose of this book the following conventions will be adopted:

Logical State	Positive Logic	Negative Logic
1	+ High	− High
0	0 Low	0 Low

LOGIC GATES
Diode AND Gates

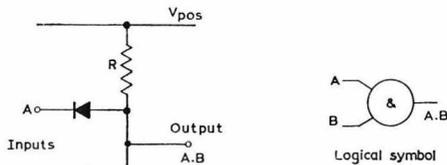Examination of the circuit shown in Fig. 10 shows that, if either or both

Fig. 10—Diode AND gate for positive logic

TABLE 17
Truth Table for Positive Logic AND Gate

Inputs		Output
A	B	
0	0	0
0	1	0
1	0	0
1	1	1

inputs are held at zero potential, the current flowing in resistor R will pass through those input diodes whose cathodes are at zero potential,

and the output will be clamped at near zero potential. The actual "low" voltage output under these conditions will be the forward voltage drop across one diode above zero. The forward voltage drop across one diode is termed V_f. For germanium diodes, this "low" voltage output is 0·2 to 0·4V; and for silicon diodes, it is 0·5 to 0·8V. The value of the forward voltage drop depends on the current level and on the junction temperature. As the junction temperature is increased, the value of the forward voltage for a given current falls at a rate of approximately 2mV/degC.

If both inputs to the gate shown in Fig. 10 are made positive, the diodes are non-conducting and the output will be positive. The circuit therefore provides an AND function for positive signals as is shown by the truth table given in Table 17.

For negative signals, a similar gate is used in conjunction with a negative supply, but with the diodes reversed. A diode AND gate for negative signals is shown in Fig. 11. In this circuit, the output is zero when either A or B is absent and negative when A and B are present as shown in the truth table given in Table 18. It can be seen that the logical symbol and the truth table are the same for negative and positive logic.
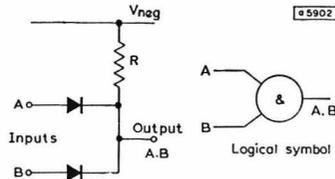

Fig. 11—Diode AND gate for negative logic

TABLE 18
Truth Table for Negative Logic AND Gate

Inputs		Output
A	B	
0	0	0
0	1	0
1	0	0
1	1	1

Diode OR Gate

The circuit for a diode OR gate is shown in Fig. 12 and its truth table is given in Table 19. In this circuit, if either input is made positive, the input diode is forward-biased, and the output is raised to almost the same

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potential level as the input, the only voltage drop being the forward voltage drop of the diode. This circuit operates as an OR gate because making either A OR B OR both positive causes a positive output to appear.

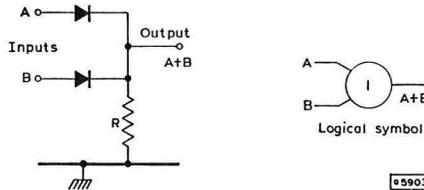If the diodes shown in Fig. 12 are reversed, the circuit operates as an OR gate for negative signals.

Fig. 12—DIODE OR gate for positive logic

TABLE 19

Truth Table for Diode OR Gate

| Inputs		Output
A	B	
0	0	0
0	1	1
1	0	1
1	1	1

Interconnecting Diode Gates

If diode AND gates are cascaded, care must be taken to ensure that the shift in the final output voltage due to the combination of the forward voltages of the diodes does not produce an erroneous logical output. Diode AND gates may be cascaded where intermediate outputs are required, provided that suitable precautions are taken. The way in which forward voltages may be built up is illustrated in Fig. 13, which also shows methods of restoring the voltage to the required zero level. In this description, all inputs are assumed to be at zero.

If a forward-biased diode is used to remove the voltage shift, as in gates 1 and 2, no further AND gates can be connected to the output of the voltage-shifting diode since the current passed through the diode of this added gate would reverse-bias the shifting diode.

In the low state, the output of gate 3 is $2V_t$ above zero. Resistors R_1, and R_2 form a potential divider, and the resistor values are chosen so that the low-state output at the junction is zero or slightly negative. A capacitor may be connected across resistor R_1 to preserve the edges of

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the switching waveforms. This capacitor is known as a "speed-up" capacitor.

OR gates may also be cascaded, but at every stage the output voltage
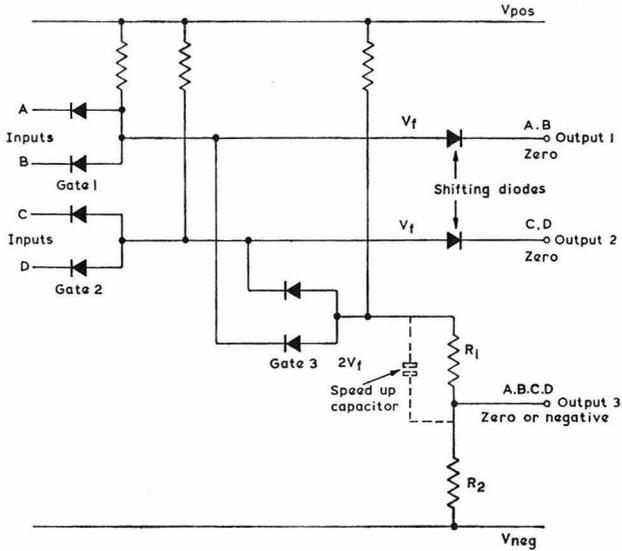
Fig. 13—Two methods of overcoming build-up of forward voltage drops

in the '1' state is reduced by V_f. This limits the number of stages which can be connected together. Also, in cascading OR gates, it must be noted that the current to all the gates in the chain must be supplied from the input signal.

A number of AND gates can feed an OR gate, but OR gates may not feed an AND gate, since the OR gate does not normally have a sufficiently low impedance in the '0' state to maintain the logic level.

Diode-Transistor Logic Gates (DTL)
A detailed design procedure for diode-transistor gates is given in Appendix 1. In Chapter 2, the concept of the NOT function was introduced. This function is one of signal inversion as shown in the truth table given in Table 20. A logical '0' at the input produces a '1' at the output and vice-versa. An n-p-n transistor connected as shown in Fig. 14 performs a NOT function. The value of R_s is chosen so that the base current is limited to a safe value. The value of R_c is chosen to ensure that the transistor is saturated with the minimum level of positive ('1' state) input and that

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sufficient current is supplied to the succeeding circuit when the transistor is switched off. Typical component values for a circuit operating from a 6V supply are $R_s = 5 \cdot 6k\Omega$ and $R_c = 2 \cdot 2k\Omega$.

TABLE 20

Truth Table for an Inverter Gate

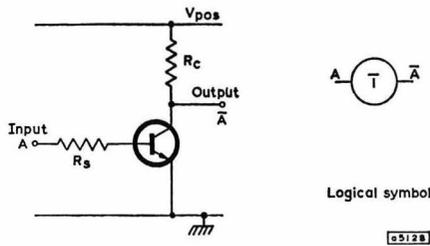| Input A	Output $\bar{A}$
0	1
1	0

Fig. 14—NOT Circuit

The equivalent NOT circuit for negative logic uses a p-n-p transistor in conjunction with a negative supply rail. NOT circuits, or inverters, such as these may be combined with diode gates to give power gain, reconstitution of voltage levels and isolation between stages. A diode AND gate feeding a transistor inverter provides a NOT AND, function and a diode OR gate with a transistor inverter gives a NOT OR function. These are generally referred to as NAND and NOR gates respectively. When inverted logic is used—that is, when zero voltage represents a logical '1' and a positive voltage represents a logical '0'—the NAND gate shown in Fig. 15 performs a NOR function.

It will have been seen by now that to convert a circuit from positive to negative logic, the diodes are reversed, n-p-n transistors are replaced by p-n-p types, and positive supply lines are replaced by negative lines, and vice versa. With this in mind, and to avoid repetition, only circuits for positive logic will be considered in the future discussion.

DTL NAND Gates

A basic NAND gate in Diode-Transistor-Logic form is shown in Fig. 15. The truth table for this circuit is given in Table 21.

In this circuit, voltage-shifting elements have been omitted. By

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de Morgan's theorem, the output of the NAND gate, $\overline{A.B}$, is equivalent to $\bar{A}+\bar{B}$. In counting circuits, it should therefore be noted that a negative-going output is obtained when both inputs are made positive. It is this negative edge that is frequently used as a trigger signal. In the '1' state,
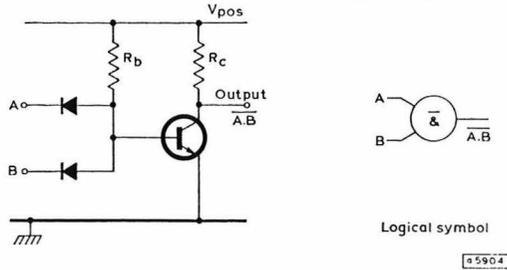

Fig. 15—Basic DTL NAND gate

TABLE 21
Truth Table for a NAND Gate

Inputs		Output
A	B	
0	0	1
0	1	1
1	0	1
1	1	0

the transistor base current is provided by resistor R_b, as shown in Fig. 15. When an input is held at zero, this current is passed through the input diode and absorbed in the source. It is important to remember that, when the input is in the '0' state, the voltage at the transistor base is the low-state input voltage. If this circuit is fed from a transistor, this voltage could be the saturation collector-emitter voltage of the transistor (100 to 200mV) plus the forward diode voltage drop. This value must not be sufficient to turn the NAND gate on, and precautions to prevent this may be necessary.

When a silicon transistor is used in the NAND gate, the base must be taken positive by some 500mV before conduction occurs. If germanium input diodes are used in conjunction with the silicon transistor, the forward voltage of the diode is normally sufficiently small to ensure that the transistor remains cut off when the input is held at zero. With silicon diodes, the forward diode voltage is of the same order as the transistor base-emitter voltage and therefore other circuit techniques must be used to ensure satisfactory circuit operation.

Two methods of d.c. protection are shown in Fig. 16. These circuits have the effect of increasing the noise immunity of a stage.
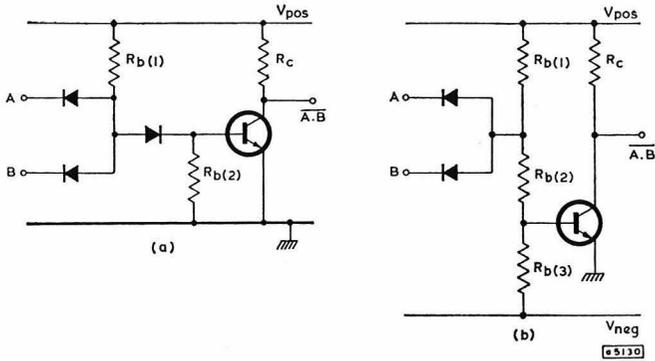
24

Fig. 16—NAND gates with increased noise immunity

DTL NOR Gates

The NAND gate may be converted into a NOR gate, as shown in Fig. 17. The truth table of a NOR gate is given in Table 22. Here the transistor is on when either input is made positive. The function performed is $\overline{A+B}$, which is equivalent to $\bar{A}.\bar{B}$.

Table 22
Truth Table for a NOR Gate

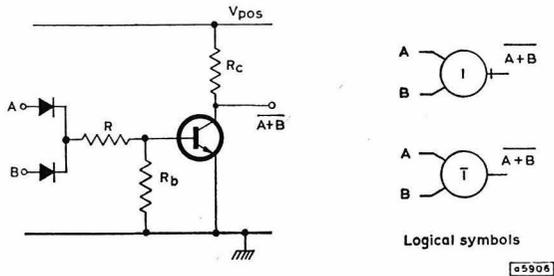|	Inputs	Output
A	**B**	
0	0	1
0	1	0
1	0	0
1	1	0

Fig. 17—Basic NOR gate

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The noise immunity of this type of gate can also be increased by means of additional diodes or by the use of a negative supply voltage as shown in Fig. 18.
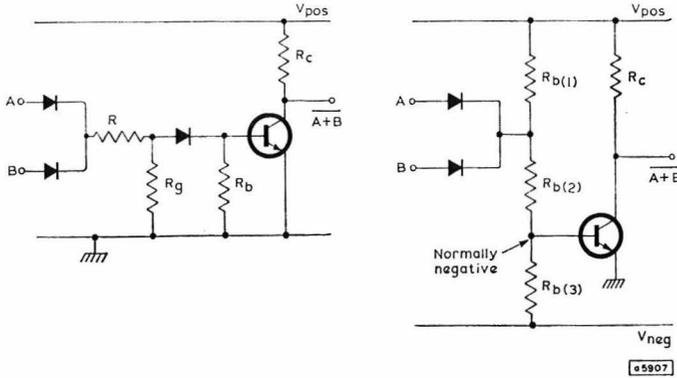

Fig. 18—NOR gates with increased noise immunity

Integrated Circuit NAND Gates

The NAND element is an extremely versatile logic element and a wide range is available in integrated circuit form. The circuit of a typical DTL integrated circuit NAND gate is shown in Fig. 19. The node connections are provided to enable further input-expanding diodes to be connected externally.
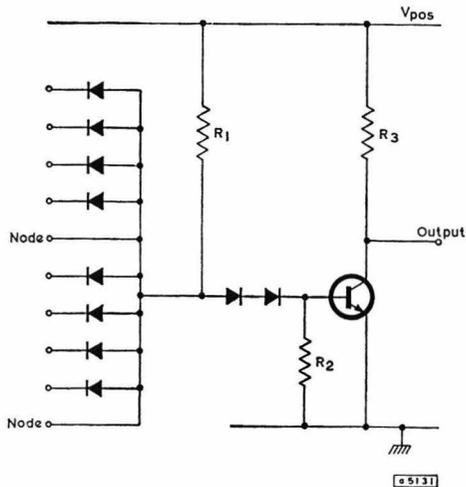

Fig. 19—Eight input NAND gate with two nodes (FCH111)

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Interconnection of DTL NAND Gates (Wired-OR)

An interesting interconnection between NAND gates, giving the NOR function at the output, is shown in Fig. 20.

The output from such a circuit connection is zero when A and B are positive or when C and D are positive, or when all four inputs are positive. The logic output is thus $\overline{A.B+C.D}$ which may be expanded to $(\bar{A}+\bar{B}).(\bar{C}+\bar{D})$ or $\overline{A.B.C.D}$. This method of connection is useful in reversible counters where a function of the form $Q.F+\bar{Q}.\bar{F}$ is required in interstage coupling. This function can easily be generated by means of two NAND gates connected as shown in Fig. 20, the inputs of one being fed with $Q.\bar{F}$ and the inputs of the other with $\bar{Q}.F$. The output is then

$$\overline{Q.\bar{F}+\bar{Q}.F}$$

which, by using de Morgan's theorem can be expressed as

$$\overline{Q.\bar{F}}.\ \overline{\bar{Q}.F},$$

which, in turn, can be simplified to

$$(\bar{Q}+F).(Q+\bar{F}).$$

This may be expressed finally as

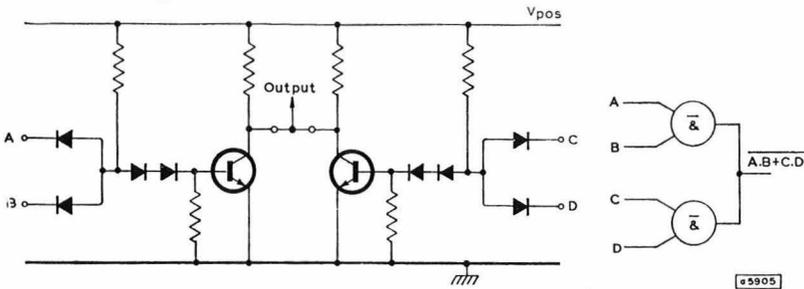$$\bar{Q}.\bar{F}+Q.F$$

which is the required function.

Fig. 20—Wired OR connection of NAND gates. Outputs of NAND gates are effectively coupled via an AND gate, formed by the transistors together with the combined collector loads. The output can thus be written: $\overline{A.B.C.D}$, which transforms to $\overline{AB+CD}$.

When this connection is used, it must be appreciated that two collector resistors are connected in parallel and that either transistor may have to conduct the current supplied by both load resistors in addition to the external load. Some integrated circuit gates are supplied without collector resistors. An external resistor may then be used, the value of which may be chosen to minimise dissipation, or a gate without a collector resistor can be used in conjunction with a gate which has a collector resistor.
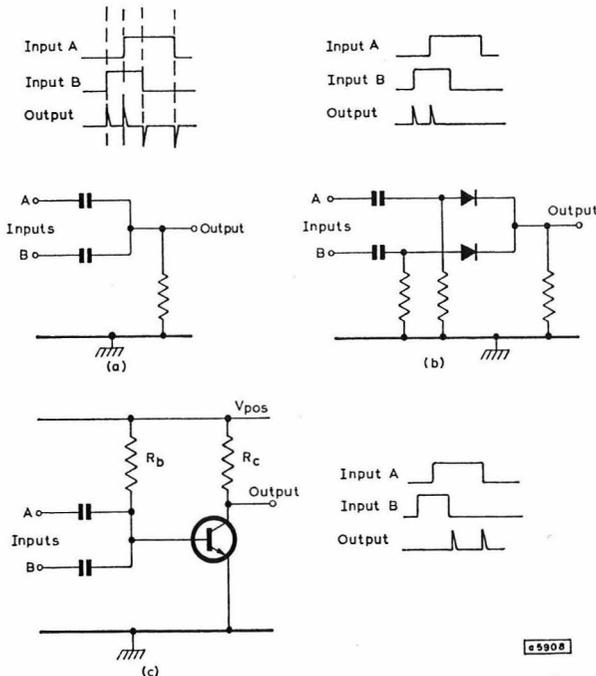
27

NAND and NOR gates may be cascaded in any sequence. An example of a half-adder using NAND and NOT elements is shown in Fig. 21. (A half-adder forms the sum of two binary numbers without a carry input.)

The number of diode inputs which a gate may have is limited in general by the speed requirements of the system. Circuits having up to ten inputs are common.
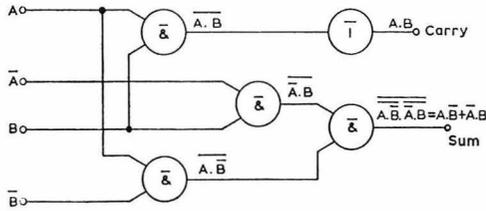
Fig. 21—Half adder

Fig. 22—Examples of capacitive gates (a) Basic capacitive OR gate (b) Capacitor-diode OR gate (c) Capacitor-transistor gate

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Capacitive Gates

Sometimes it is useful to make an OR gate which is sensitive only to the edges of pulses. Capacitive gates may be used for this purpose, and the exact function performed by these gates can be modified by the addition of diodes or transistors. The gates and waveforms shown in Fig. 22 are self-explanatory. In the gate shown in Fig. 22c, the transistor is normally held saturated by the current in resistor R_b. Positive inputs are differentiated by the input CR combination formed by the input capacitor and the input resistance of the transistor.

Resistor-Transistor Logic (RTL)

The NOR function can be performed by the use of a circuit of the type shown in Fig. 23. Resistors are used as input isolating elements in this
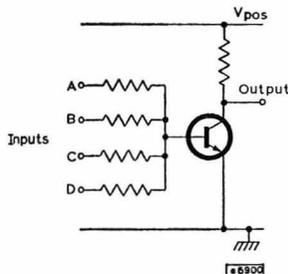

Fig. 23—Resistor—transistor NOR gate

case, and the values are chosen so that a positive voltage equivalent to a logical '1' on any input provides sufficient base current to turn the transistor on.

Directly Coupled Transistor Logic (DCTL)

A particular feature of silicon transistors lies in the large difference between the forward base-emitter and the collector saturation voltages. The saturation voltage is usually about 100mV or even less for both germanium and silicon transistors, but the forward base-emitter voltage of a silicon transistor is about 600 to 700mV compared with 200 to 300mV for a germanium transistor. Thus, if the collector of one silicon transistor directly feeds the base of another, the second transistor is safely held off when the first is in saturation.. Use of this property is made in the design of directly coupled transistor logic gates and bistable elements. The differences between the base-emitter voltage and the collector saturation voltage of germanium transistors is far less, and therefore they are not

c

suitable for such very simple directly coupled circuits.

The example shown in Fig. 24 is a DCTL NOR gate. If any base is made positive, that transistor is saturated and the output is held at $V_{CE(sat)}$.
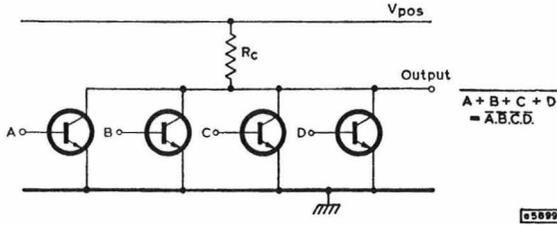

Fig. 24—Directly coupled transistor NOR gate

For the output to be positive, all inputs must be zero. If the output of this gate is connected to the input of a similar gate, the logic levels obtained are defined as $V_{CE(sat)}$ for a logical '0' and V_{BE} for a logical '1'.

Transistor-Transistor Logic (TTL)

Transistor-transistor logic lends itself to integrated circuit techniques. The circuit of a TTL NAND gate is shown in Fig. 25. Direct coupling is used
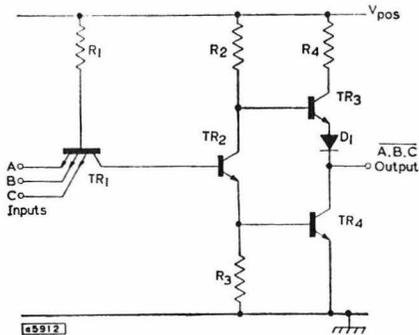
Fig. 25—Circuit configuration of TTL NAND gate

between transistors and the output impedance is low in both the '1' and the '0' states because of the action of the "totem-pole" output stage formed by TR_3 and TR_4. The gate operates as follows. If any input is low, the current in R_1 is conducted, via the base-emitter diode of TR_1 , to the zero potential line. No collector current flows, therefore TR_2 is held in the OFF condition and so is TR_4. The collector potential of TR_2 is high, and current flows via R_2 into the base of TR_3 , keeping it

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switched on. The output voltage is therefore high. If all the input potentials are high, TR_1 provides the base current drive for TR_2. The emitter current of TR_2 turns TR_4 on and the output is therefore held at the collector-to-emitter saturation voltage. Under this condition, TR_3 is cut off because the collector-to-emitter voltage of TR_2 is insufficient to overcome the base-emitter voltage of TR_3 plus the forward voltage drop of D_1. The circuit is suitable for driving capacitive loads. The typical stage delay of 13ns makes TTL suitable for operation in high speed systems. The logic swing of a TTL gate is very good—not less than 2·4V for a logical '1'.

Propagation Delay

The propagation delay is the time which elapses between a signal entering one gate and entering the next gate in the series. It is sometimes referred to as the "stage delay" and is usually measured by connecting three gates in series as shown in Fig. 26. The first gate is used to standardise the input pulse to the second gate. If t_1 and t_2 are the times indicated in Fig. 26,

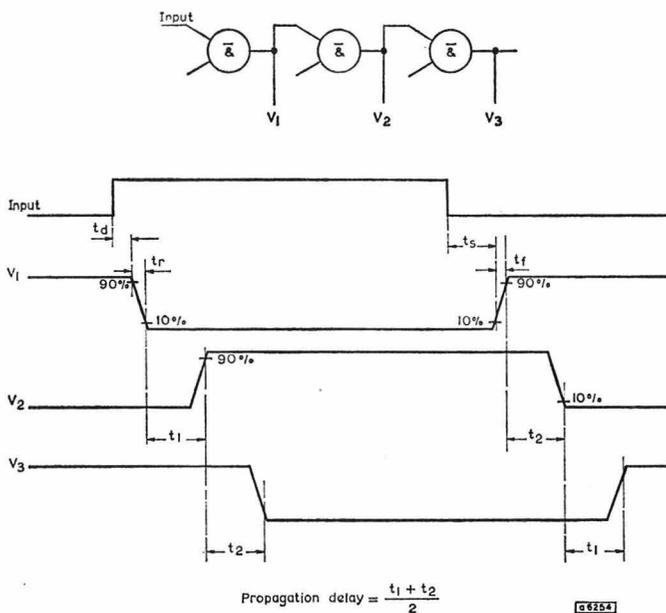$$\text{Propagation delay} = \frac{t_1 + t_2}{2}$$

Fig. 26—Propagation delay

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the propagation delay can be expressed as

$$\frac{t_1+t_2}{2}$$

The waveforms shown in Fig. 26 show that the propagation delay is independent of rise and fall times. The rise and fall times, the storage time (t_s) and the turn-on delay (t_d) affect the maximum operating pulse repetition frequency. Propagation delay is normally measured with each gate loaded to full fan-out.

Signal Noise Immunity (SNI)

Signal noise immunity (SNI) is a very important factor in the design of logic circuits. It is concerned with ensuring that the logic elements are not triggered by spurious signals, or noise, in the system.

Two signal noise immunity figures are frequently encountered when dealing with logic elements—one associated with the "low" input state, and the other with the "high" input state. These two values are illustrated in Fig. 27. The value associated with the "low" input state is frequently
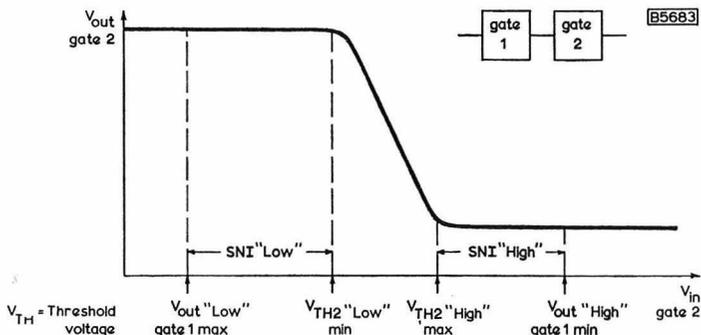

Fig. 27—Transfer characteristic illustrating signal noise immunity

less than that associated with the high input state. The effects of noise pulses on these two input states are different because in the "low" input state the source is a low impedance, whereas in the "high" input state, the source is usually the collector resistance of the previous stage.

The signal noise immunity figure associated with the "low" input state is the difference between the maximum "low" output stage voltage and the minimum "low" input threshold voltage, and the figure for the "high" input state is the difference between the minimum "high" output state voltage and the maximum "high" input threshold voltage. These points are shown on the typical transfer characteristic given in Fig. 27.

The signal noise immunity figure therefore indicates that interference pulses up to these values may appear at the input without the possibility

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of the gate changing state.

As the voltage levels mentioned above are temperature-sensitive, the signal noise immunity is also temperature-dependent. A graph showing typical variations of d.c. levels with temperature is given in Fig. 28.
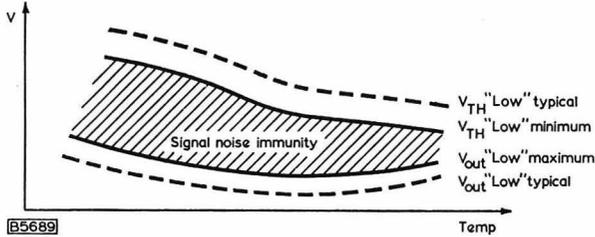

Fig. 28—Variation of d.c. levels with temperature

BISTABLE ELEMENTS

If two RTL NOR stages are connected together in such a way that the output of each feeds the input of the other, a bistable element is produced. Such an arrangement is shown in Fig. 29.
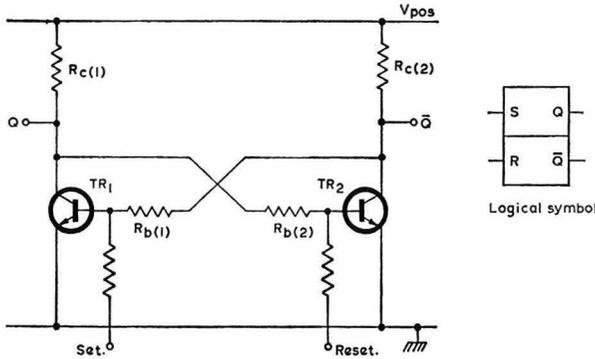
Fig. 29—Bistable circuit with resistive cross-coupling

If transistor TR_1 is in a conducting state, the collector voltage is low and, provided there is sufficient base drive, the value of the collector voltage will be the saturation voltage $V_{CE(sat)}$—normally about 100 to 200mV. The base of TR_2 is, therefore, also held at this low voltage, and TR_2 is cut off. Since no collector current flows in this stage, the collector voltage is high, and current flows through $R_{c(2)}$ and $R_{b(1)}$ to the base of TR_1, maintaining TR_1 in conduction. The circuit remains in this stable state until TR_1 is cut off by application of a negative voltage to its base,

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or TR_2 is made to conduct by means of a positive base voltage. If the stage is disturbed in either of these ways, the collector current of TR_1 is reduced, causing a rise in collector voltage. Because of this rise, transistor TR_2 receives a base current drive, forcing it to conduct heavily and causing the collector voltage to fall, thereby reducing the base current in TR_1 still further. Eventually TR_1 will be cut off and TR_2 will be saturated. The bistable stage is then in its other stable state. The voltage to which the collector of the OFF transistor rises is fixed by the values of R_c and R_b which are, in turn, determined by the required voltage and current output levels, the speed of operation required and the gain of the transistors. The conditions for choosing these resistors in the ON state are shown in Fig. 30.
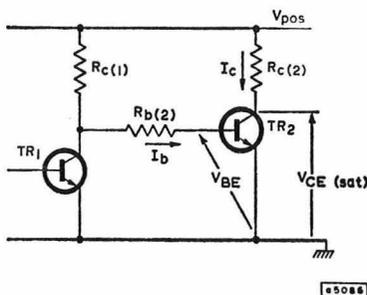

Fig. 30—Circuit showing conditions for choosing resistor values in the ON state

The value of collector current is chosen by system considerations, such as the drive current required for subsequent stages. If $I_{c(U)}$ is the collector current flowing without external load and $I_{c(L)}$ is the maximum load current, then

$$I_{c(U)} = \frac{V_{pos} - V_{CE(sat)}}{R_{c(2)}},$$

and the minimum base current that can be tolerated is

$$\frac{I_{c(U)} + I_{c(L)}}{h_{FE}}$$

In practice, a higher base current than this minimum is always used to ensure that the ON device is fully saturated and to provide higher switching speeds. This higher base current is generally known as "base overdrive". If γ is the overdrive factor, the design value of current gain is h_{FE}/γ. The

maximum value of base resistor $R_{b(2)}$ is, therefore, given by:

$$R_{b(2)max} = \frac{V_{pos} - V_{BE}}{I_{c(U)} + I_{c(L)}} \cdot \frac{h_{FE}}{\gamma} - R_{c(1)}$$

An overdrive factor of at least 2 is desirable.

DTL R-S Bistable Element (R-S Flip-Flop)

If two DTL NAND gates are cross-coupled in a similar manner to the previous example, a bistable element is obtained whose output voltage swing is greater than that of the resistive-coupled circuit. This is known as a set-reset or R-S bistable circuit. This greater voltage swing is obtained because the base current of the ON transistor is supplied by the gating resistor and is not passed through the collector load resistor. The method of connecting the bistable element is shown in Fig. 31. Diodes D_5 and D_6 are voltage-shifting diodes. Resistors R_5 and R_6 provide a discharge path for the stored base charge, thereby reducing the turn-off time.
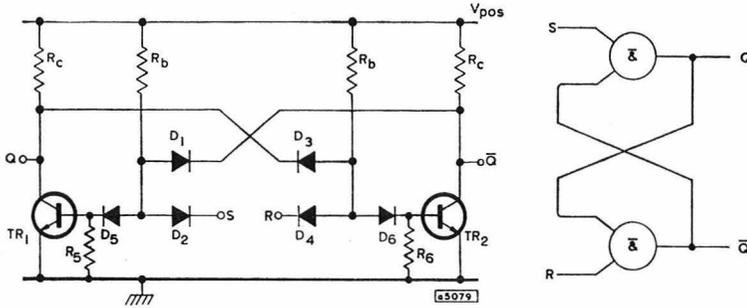
Fig. 31—Set-reset DTL bistable circuit

TABLE 23

Truth Table of DTL Bistable Element

R	S	Q	$\overline{Q}$
0	0	1	1
1	0	1	0
0	1	0	1
1	1	No change	

The DTL bistable element is set or reset by applying a voltage to the S or R terminal respectively. The voltage may either be negative or zero. The truth table of this bistable element is given in Table 23.

Triggered or T Bistable Element for Counters (T Flip-Flop)

The requirement of the triggered bistable circuit is that it should change state at each input pulse. This action is achieved by the use of some form of steering circuit.

One of the simplest forms of triggered bistable element is shown in Fig. 32. This is a resistive-coupled bistable circuit to which two capacitors —C_1 and C_2—have been added as triggering components. If it is assumed
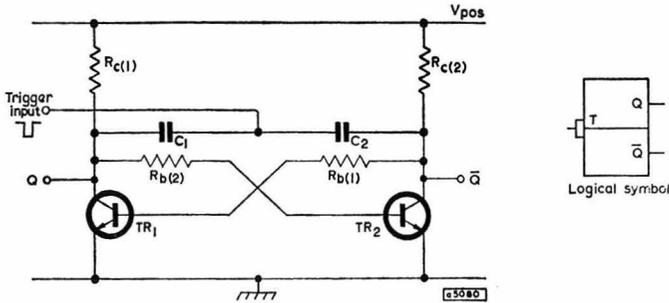

Fig. 32—Simple triggered bistable circuit

that TR_1 is on and TR_2 is off and that a negative pulse is applied to the trigger input, this pulse will be fed to both collectors via capacitors C_1 and C_2. Since TR_1 is on, and therefore has a low impedance, the pulse has no effect on its collector. Transistor TR_2, however, is off, and the input pulse is therefore passed via C_2 and $R_{b(1)}$ to the base of TR_1. This
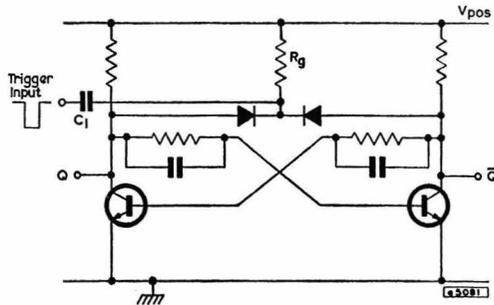

Fig. 33—Diode-steered bistable circuit

causes the base current of TR_1 to be reduced so that the bistable circuit changes state. Transistor TR_2 is now on, and the next pulse causes the bistable circuit to change state again. This type of circuit is only suitable for low operating speeds.

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Another type of bistable circuit is shown in Fig. 33. The operation of this circuit is similar to that of Fig. 32 except that diodes are used to steer the trigger pulses. A discharge path for capacitor C_1 is provided by resistor R_g.

The recommended method of triggering is shown in Fig. 34. Two
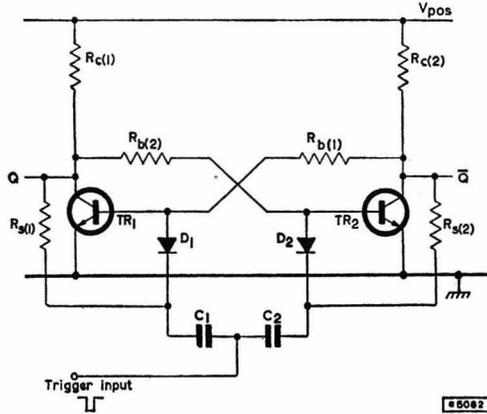
Fig. 34—Steered bistable circuit

steering gates are formed by $R_{s(1)}$, D_1, C_1 and $R_{s(2)}$, D_2, C_2. If TR_1 is on and TR_2 is off, the collector voltage of TR_2 is high and therefore D_2 is reverse-biased through $R_{s(2)}$. Diode D_1, however, is not subjected to such a reverse bias and a negative edge arriving at the trigger input is steered by the diode to the base of TR_1. The bistable circuit changes state, and D_1 becomes reverse-biased. The next input pulse is steered to TR_2 and the bistable circuit reverts to its original state. Such stages may

Fig. 35—Steered DTL bistable circuit

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be cascaded, the Q or Q̄ output of one stage being connected to the trigger input of the next. This type of trigger steering circuit may be used equally well with the DTL bistable element as sho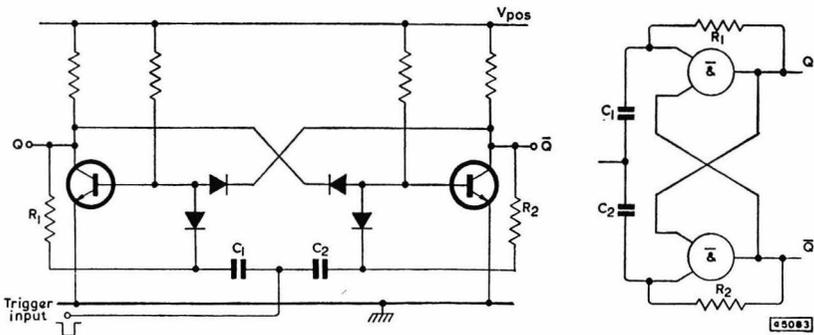wn in Fig. 35. Such an element may be made from a dual NAND gate, the triggering capacitors C_1 and C_2, and steering resistors R_1 and R_2, being added externally. Quadruple gates are also available which provide the facility of making two bistable circuits from one package.

Refinements in Bistable Element Design

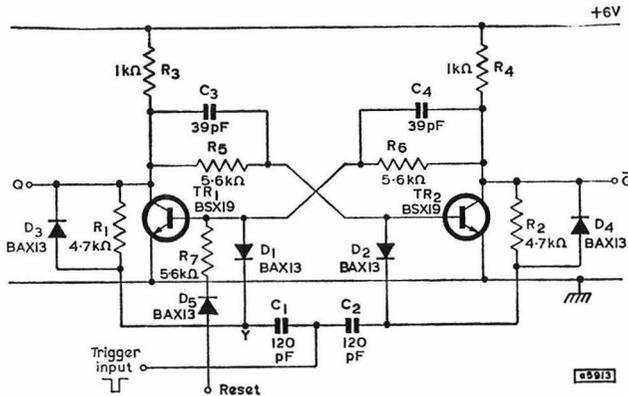A practical binary counting bistable element with a reset facility is shown in Fig. 36.

Fig. 36—Triggered bistable circuit with speed-up capacitors and recovery diodes

A detailed discussion of design procedures for bistable stages is to be found in Appendix 2. To obtain the maximum counting speed from a bistable circuit, several refinements can be made. The simplest of these is the addition of cross-coupling capacitors to provide a fast transfer of charge, thereby increasing switching speed. The capacitors, usually of about 50pF or less, are called "speed-up" capacitors. The speed-up capacitors are shown as C_3 and C_4 in Fig. 36.

A limitation on counting speed is imposed by the recovery or discharge time of the steering circuits C_1R_1 and C_2R_2. If the trigger input is fed with square-wave signals, the negative edges cause the bistable circuit to trigger, whilst positive edges are blocked by D_1 and D_2 and therefore have no effect. When a negative edge appears at the trigger input, the appropriate steering diode conducts and its associated capacitor becomes positively charged. If transistor TR_1 is on, and its collector potential is low, when a positive edge appears at capacitor C_1, this capacitor begins

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to discharge via R_1 and R_3 to return point Y to zero potential. The discharge time is limited by R_1. If the voltage at Y has not returned to zero before the negative edge after next, the sensitivity of the stage is reduced and irregular triggering may result at the highest counting rate. Diodes D_3 and D_4 are inserted to overcome this effect by giving a low-resistance discharge path to C_1 and C_2. Transistor turn-on and turn-off times also limit the maximum operating speeds of gates and bistable elements.
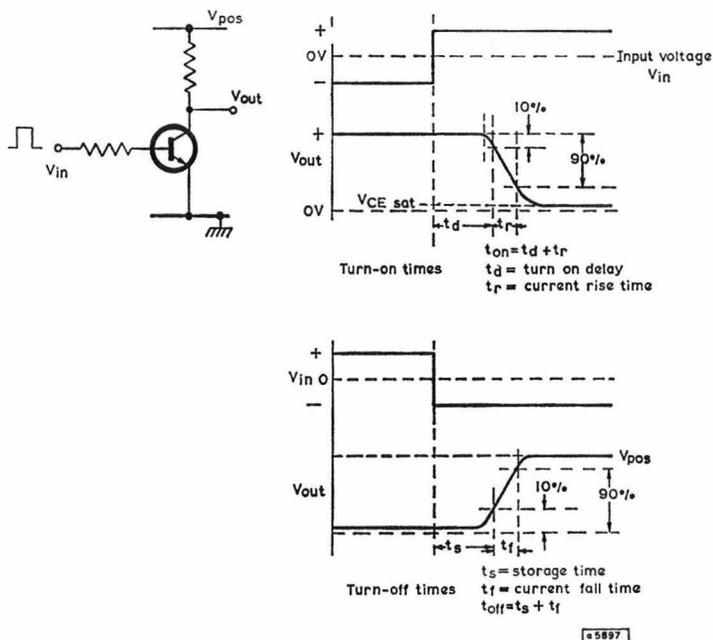
Fig. 37—Transistor turn-on and turn-off times

The delays and rise times observed in switching a transistor on and off are illustrated in Fig. 37. Some of the factors that affect the switching times of gates and bistable elements are given below.

1. Stray or circuit capacitance at the output increases the rise and fall times.
2. Stray capacitance at the input necessitates a greater drive current to produce a given switching speed.
3. The extent to which the transistor was saturated in the ON state affects the storage, or desaturation time (t_s).
4. A high negative potential at the base prior to switching on increases the turn-on delay (t_d).

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5. The voltage swing required from the output governs the collector voltage rise time. Clamping can limit the voltage swing and therefore reduce the rise time. This technique may be used in conjunction with a high supply voltage, giving a high aiming potential from which to charge circuit capacitances during the initial part of the collector voltage excursion.

6. Large forward and reverse transient base currents, as supplied by the speed-up capacitors, give fast switching times. After switching, the forward current or reverse voltage should be reduced to minimise the effects of (3) and (4) above.

Various techniques which may be used to increase switching speeds are shown in Figs. 38, 39 and 40. Steering circuits are omitted for clarity.
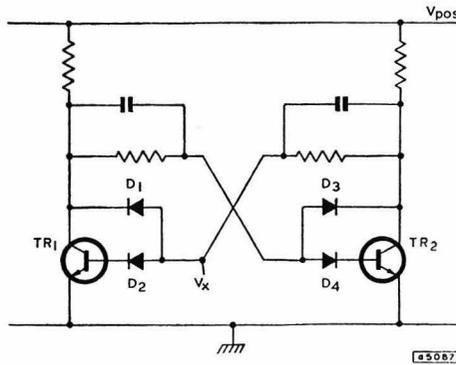

Fig. 38—Method of increasing switching speed by preventing saturation

Examination of the circuit in Fig. 38 reveals that when TR_1 is on, the collector voltage attempts to fall to $V_{CE(sat)}$. The voltage at V_x, however, is V_{BE} plus the forward voltage of D_2. If the collector voltage falls to a value $V_x - V_f$ (where V_f is the forward diode voltage drop), D_1 becomes forward-biased and some of the base current is diverted through this path. Transistor TR_1 is thereby prevented from entering saturation. The storage time, t_s, is thus reduced to a minimum. A further advantage is that during the turn-on time, heavy base drive is supplied by the speed-up capacitors.

A method of reducing the collector voltage rise time is illustrated in Fig. 39. When the collector voltage of either transistor rises, the corresponding collector-emitter capacitances and stray capacitance are charged, via the collector resistors, $R_{c(1)}$ or $R_{c(2)}$, to a high aiming potential; namely, the supply voltage. When the collector voltage reaches a value $(V_f + 3)$ volts, the catching diode D_1 or D_2 is forward-biased and

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the collector voltage is clamped. The collector voltage rise time is thus reduced.

A method of reducing the turn-on delay is shown in Fig. 40. Diodes D_1 and D_2 prevent the base potential becoming excessively negative during switch-off. The base voltage is caught at V_f and the turn-on delay on the next transition is therefore reduced.
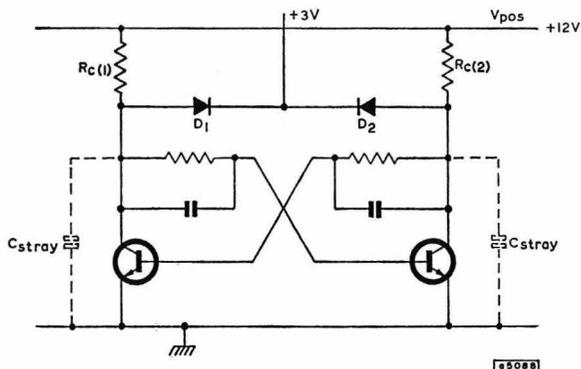
Fig. 39—Method of increasing switching speed by reducing collector voltage rise time with a collector diode clamp
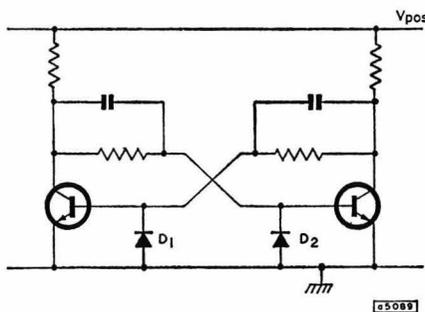
Fig. 40—Method of increasing switching speed by reducing turn-on delay with a reverse base-voltage diode clamp

Store Bistable Circuit

The set-reset, or R-S, bistable circuit has been discussed in both resistive-coupled and diode-coupled forms. An extension of the R-S bistable circuit is the gated R-S circuit shown in Fig. 41.

Diodes D_1 and D_2 are voltage-shifting diodes. Diodes D_3 and D_5 form an AND gate with $R_{g(1)}$ as do D_4 and D_6 with $R_{g(2)}$. If the "Inhibit" terminal, I, is held at a low potential, voltages applied to R and S have no effect. If, however, a positive voltage is applied to I, the bistable

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circuit may be set and reset by applying signals to the R and S terminals. When R is made positive or open circuit and S is held at low potential, the circuit sets to the '1' state; that is, a high potential appears at Q. Resetting to '0' is effected by applying a low signal to R and a positive or open-circuit signal to S. Terminals R and S must not simultaneously be made positive or open circuit if I is also at high potential, since this causes Q and $\bar{Q}$ to be zero at the same time, and when the inhibit line is returned to zero the state of the bistable circuit is indeterminate.

This type of circuit can be used as a store bistable element. If the Q and $\bar{Q}$ outputs of a counting bistable element are connected to the R and S terminals, each time the I terminal is taken positive, the store bistable
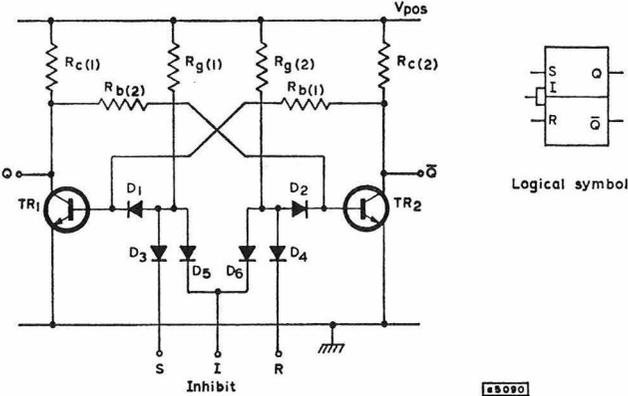
Fig. 41—Gated R-S bistable element (store bistable circuit)

element assumes the same logic state as the counting bistable element. When the positive voltage is removed from the I terminal, the information stored remains unaltered until the next time the I terminal is made positive. The only loading applied by this bistable element to the counting bistable element is that imposed by the input diode AND gates.

Clocked Bistable Circuits

Clocked bistable circuits do not change state when the logical levels at their inputs are changed, but change state only upon the arrival of a clock pulse. These elements find their chief application in synchronous counters, which have the advantage over asynchronous counters of avoiding ambiguities when sampled during a count, as explained in Chapter 5.

In a clocked system, the clock pulses are denoted n, n+1, n+2 and so on, where n means the present time, n+1 means the next bit time and so on. The present state of the bistable circuit may therefore be defined as Q_n,

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the state after the next clock input as Q_{n+1} and so on. The condition of the logical inputs before the clock pulse determines the next state of the bistable circuit, according to its truth table. The bistable circuit takes up the required state when the next clock pulse arrives, but, depending upon the type of bistable circuit, the required state may be reached as a result of the leading edge or the trailing edge of the clock pulse. The term Q_{n+1} therefore defines the state of the bistable circuit at a time $t+s$, when t is the time of the active portion of the clock pulse in defining the output and s is the settling time of the bistable circuit.

Staticiser

A staticiser is a particular type of bistable element which performs a store operation similar to that of the store bistable circuit described above. The staticiser circuit, however, uses one control line and a clock line. The logical symbol for a staticiser is shown in Fig. 42a and the truth table is given in Table 24. The states are those after the action of a command pulse. The staticiser takes up its final state at the leading edge of the command pulse. The control line information must be present until the command pulse is removed.

The circuit diagram of a staticiser is given in Fig. 43.
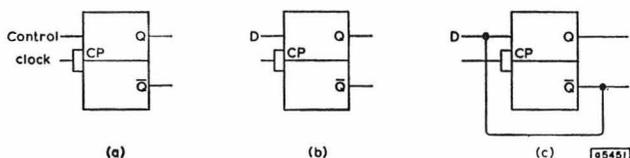
Fig. 42—Staticiser and D bistable elements
(a) logical symbol for staticiser   (b) logical symbol for D bistable element
(c) D bistable element connected to operate as a T bistable element

TABLE 24
Truth Table for a Staticiser

Control	Q	$\bar{Q}$
0	0	1
1	1	0

D Bistable Element (D Flip-Flop)

The D bistable element is a further form of staticiser, available in integrated circuit form. The truth table for a D bistable circuit is given in Table 25, and the logical symbol is shown in Fig. 42b. The bistable circuit takes up its final state after the leading edge of the clock pulse, and a change of information on the D line during the clock pulse has no effect. If the D input is connected to the $\bar{Q}$ output, as shown in Fig. 42c,

the bistable circuit changes state on each clock pulse; that is, it operates as a triggered, or T, bistable circuit. This form of operation is not possible with the basic staticiser circuit shown in Fig. 43.
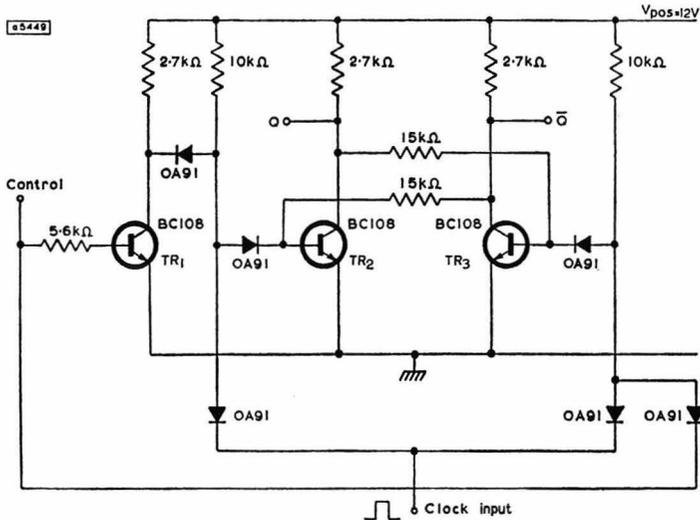
Fig. 43—Staticiser circuit

TABLE 25
Truth Table for D Bistable Element

Clock	D	Q_{n+1}	$\bar{Q}_{n+1}$
0	0	Q_n	$\bar{Q}_n$
0	1	Q_n	$\bar{Q}_n$
1	0	0	1
1	1	1	0

Clocked R-S Bistable Circuit (Clocked R-S Flip-Flop)
In its simplest form, the clocked R-S bistable element is a triggered bistable circuit with the gating resistors for the steering circuits disconnected from the collectors. Such a circuit is shown in Fig. 44. The truth table for this circuit is given in Table 26. This circuit can be converted to operate as a D bistable element by connecting the control signal to $R\bar{Q}$ and its inverse via a transistor such as TR_1 in Fig. 43 to SQ.

The states shown in Table 26 are those after a complete clock pulse.

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The information supplied to the SQ and R$\bar{\text{Q}}$ inputs determines the state the bistable circuit will assume after a complete positive clock pulse.
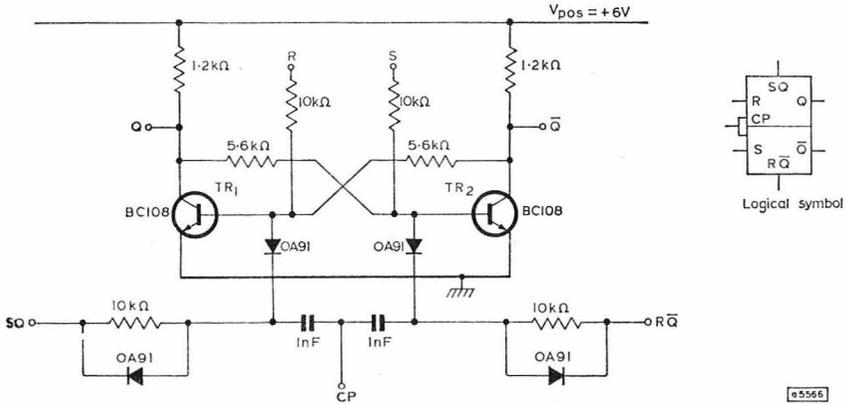

Fig. 44—Basic clocked R-S bistable element

TABLE 26

Truth Tables for Clocked R-S Bistable Element

SQ	R$\bar{\text{Q}}$	$Q_{(n+1)}$	$\bar{Q}_{(n+1)}$
0	0	not defined	
0	1	1	0
1	0	0	1
1	1	Q_n	Q_n (no change)
R	S	Q	$\bar{Q}$
0	0	no change	
0	1	1	0
1	0	0	1
1	1	0	0 (prohibited)

The steering mechanism is the same as for the normal triggered bistable circuit, but the steering voltages are obtained from external sources such as DTL gates. It should be noted that an '0' on the R$\bar{\text{Q}}$ or SQ inputs is an "enable" signal.

Connecting R$\bar{\text{Q}}$ to $\bar{\text{Q}}$ and SQ to Q converts this circuit to a triggered bistable circuit. Although direct set and reset functions are possible by application of signals to the base terminals, an alternative method, using two extra transistors, is shown in Fig. 45. Resistive inputs are shown, but diode inputs providing an AND or OR function on the set and reset inputs
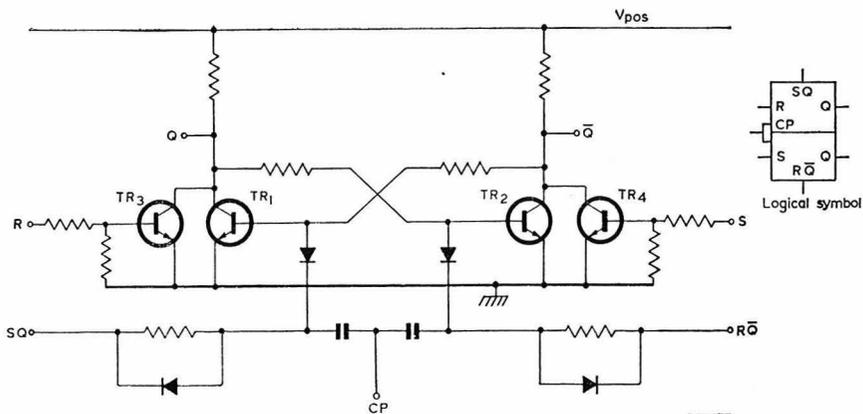
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Fig. 45—Practical clocked R-S bistable element

are equally suitable. The direct set and reset inputs operate regardless of whether a clock signal is present or not and override the SQ and R$\overline{\text{Q}}$ inputs.

When the R input is made positive, transistor TR_3 saturates and the collector voltage of TR_1 is returned to zero. Transistor TR_2 is therefore cut off and the circuit is set to the '0' state. The effect of a signal on the S terminal in setting a '1' is similar. Setting and resetting by the use of shunt transistors on the bases is also possible, as illustrated in Fig. 46. A positive signal on S sets a '1' in Q.

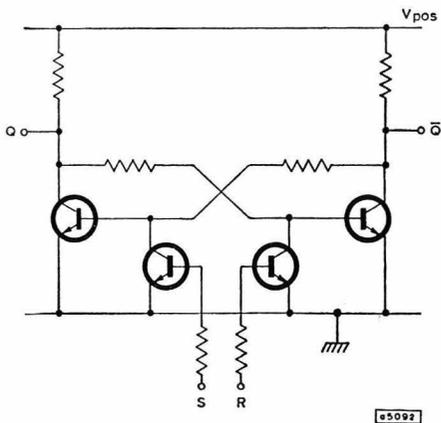
Fig. 46—Alternative set and reset connections

The J-K Bistable Circuit (J-K Flip-Flop)

The J-K bistable circuit is a more complex device than those previously discussed. This was first described by M. Phister (Ref. 3). It offers all the

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functions of R-S, clocked R-S and T bistable elements. It can operate in clocked or unclocked systems and is therefore a very versatile element.

For reasons of economy, it is not a practical proposition to build J-K bistable circuits from discrete components. The advent of silicon integrated circuits, however, has made possible the construction of complex semiconductor arrays at an economic price with the added advantages of very small physical size and high reliability.

Two truth tables are necessary, one showing the effect of the R and S inputs and the other showing the effect of the J and K inputs. These are given in Tables 27 and 28. The S and R inputs operate independently of a clock but, in Table 28, the states shown are those just after the clock pulse has taken effect. Depending upon the circuit design, the output may change state at the leading or trailing edge of the clock pulse. The pin numbers refer to the FCJ101 and FCJ102 devices. Two logical symbols for J-K bistable elements are shown in Fig. 47.

TABLE 27
Set and Reset Truth Table for J-K Bistable Circuit

S_1 (S)	S_2 (R)	Q_{n+1} (pin 10)	$\bar{Q}_{n+1}$ (pin 5)
0	0	1	1
1	0	1	0
0	1	0	1
1	1	Q_n	$\bar{Q}_n$ (no change)

TABLE 28
Truth Table for J and K Inputs of J-K Bistable Circuit

J	K	Q_{n+1} (pin 10)	$\bar{Q}_{n+1}$ (pin 5)
0	0	Q_n	$\bar{Q}_n$ (no change)
0	1	0	1
1	0	1	0
1	1	$\bar{Q}_n$	Q_n (reversal of state)

In operation, if all the J and K inputs and the S and R inputs are open-circuited or positive, the J-K bistable circuit operates as a triggered bistable circuit, changing state on each clock pulse.

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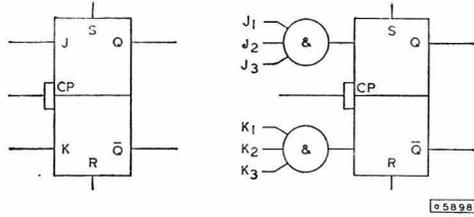Fig. 47—Logical symbols for J-K bistable elements

The FCJ101 and FCJ102 devices are examples of integrated J-K bistable circuits. Their circuit diagram is shown in Fig. 48. Information is set into the circuit at the leading edge of the clock pulse and the output changes state at the trailing edge. No limitations are usually placed on
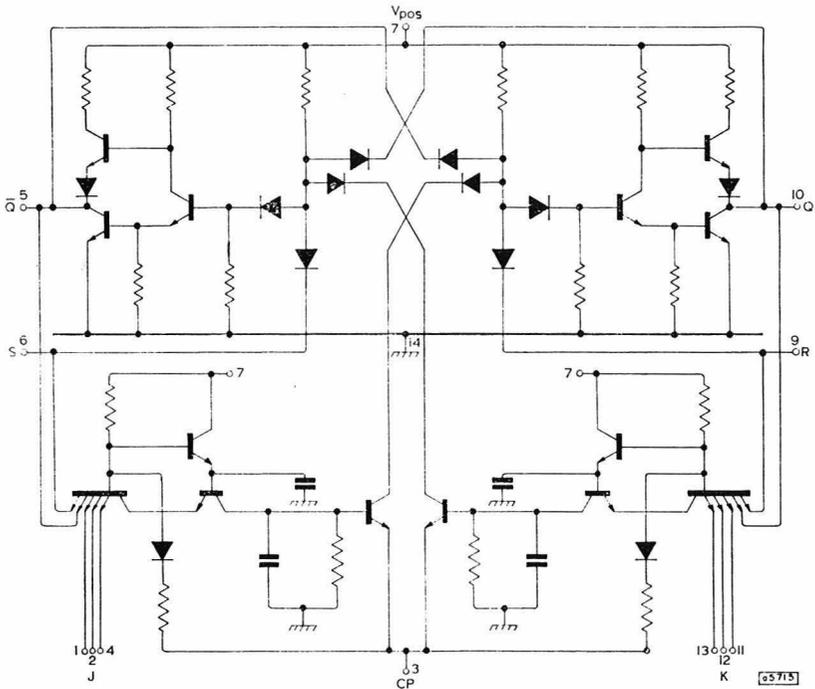

Fig. 48—Circuit diagram of integrated multiple-input J-K bistable element

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the rise time of the leading edge of the clock pulse. The trailing edge however, must have a fall time of less than 100ns. Gating functions to control the action of the circuit are possible by means of the three-input AND gates on each of the J and K inputs. By this means, gating to obtain special counts, for example, can easily be achieved. Circuits showing the use of the J-K bistable circuit are given in later chapters.

P-N-P/N-P-N Complementary Transistor Bistable Circuits

The use of complementary transistors enables a simple bistable element to be built. The basic circuit arrangement for a p-n-p/n-p-n switch is shown in Fig. 49. A trigger voltage of the form shown, applied to the trigger terminal A or B, switches the bistable element on.
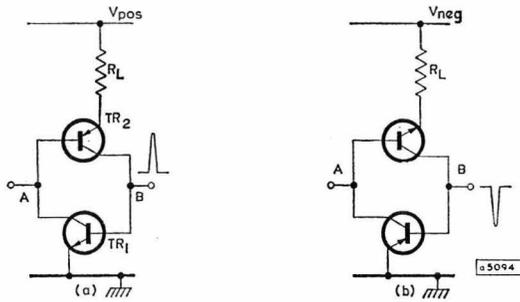

Fig. 49—P-N-P/N-P-N bistable elements

If a positive pulse is applied to terminal B of the circuit in Fig. 49a transistor TR_1 conducts and collector current flows. This current is fed to the base of TR_2 which also switches on. The collector current of transistor TR_2 flows in the base of TR_1 causing an increase in the collector current of TR_1. This cumulative action causes both transistors to conduct heavily, and current is limited only by R_L. The action of negative trigger voltages on the A terminal is similar. The operation of the circuit shown in Fig. 49b is similar to that in Fig. 49a but with the polarities of the signals reversed.

To switch the device off, it is necessary to remove the base current of TR_1 and TR_2. Thus, with the simple circuit, it is necessary for the trigger pulse source to absorb the whole of the loop current, which could be almost as high as the load current. An alternative method of switching off is to reduce the collector voltage to a value below the holding voltage for the circuit. The holding voltage is the minimum voltage required to keep the switch in the stable ON condition.

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To build a practical counter, the basic circuit must be modified in order to incorporate triggering circuitry. A suitable arrangement is shown in Fig. 50. A chain of complementary-pair stages is shown, with a pulse-steering circuit, in Fig. 51. Such a circuit is suitable for use as a ring counter.
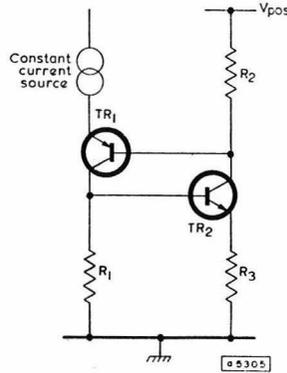
Fig. 50—Practical p-n-p/n-p-n bistable circuits
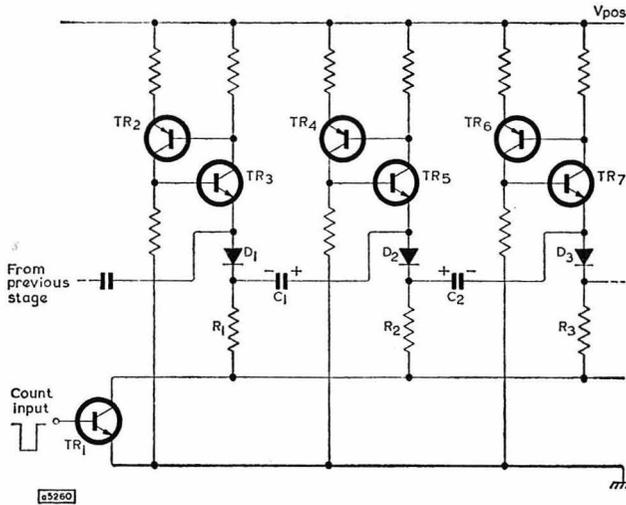
Fig. 51—A chain of complementary-pair stages suitable for a ring counter, showing polarities to which capacitors become charged during a count pulse

When the centre stage (TR_4 and TR_5) is conducting, the emitter current of TR_5 flows through TR_1, and capacitors C_1 and C_2 are charged with the polarities shown. If TR_1, is now turned off by the count input pulse, the current in TR_4 and TR_5 is interrupted and the stage is turned off.

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Capacitor C_1 discharges through R_1, R_2 and D_2, but capacitor C_2, being charged with the opposite polarity to that of C_1, remains charged. Transistor TR_1 is turned on again, making the emitter of TR_7 negative with respect to the base. The pair formed by TR_6 and TR_7 is, therefore, turned on.

Thus, at each input pulse, the conducting p-n-p/n-p-n pair is switched off and the next pair to the right is switched on.

Thyristors

The thyristor is a semiconductor power switch. It is usually, though not necessarily, a far larger semiconductor device than the switching transistors discussed so far. It operates in a similar manner to the p-n-p/n-p-n circuit of Fig. 49. The equivalence of the thyristor to the two-transistor circuit is illustrated in Fig. 52.
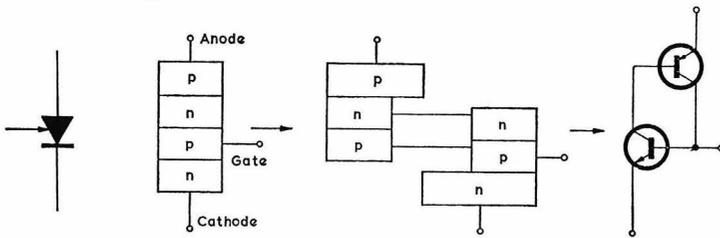

Fig. 52—Thyristor structure and transistor equivalent

In the OFF state, the loop gain of the device is so low that no anode current, other than a very small leakage current, can flow. When a positive pulse of short duration is applied to the gate terminal, however, the loop gain is raised to unity and regenerative action causes the device to switch on. All three junctions are then forward-biased, and the current is limited only by the anode load. Under these conditions, the voltage across the thyristor is very low, being of the same order as the base-emitter voltage of a transistor.

To return the thyristor to the OFF state, it is necessary to apply a reverse bias to the anode for long enough to allow the junctions to recover from the effects of carrier storage. Alternatively, the anode current may be reduced to a value below the minimum holding current. The holding current is that current below which the internal loop gain is less than unity and therefore, in this region, regenerative switching does not occur.

The circuit shown in Fig. 53 consists of two thyristor sections connected in such a manner that switching off the first triggers the second.

If CSR_1 has been turned on by a positive pulse at the reset input and CSR_2 is off, diode D_1 will be reverse-biased by the anode voltage of

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CSR_2, but the reverse bias on D_2 will be very small—only the conduction voltage of CSR_1. A positive input .pulse applied to the count input terminal causes D_2 to conduct and, provided the amplitude of the pulse is less than V_{pos}, D_1 remains reverse-biased. The input pulse therefore passes through D_2 and C_3 to the gate of CSR_2 which is triggered to the ON state. The anode voltage of CSR_2 then falls sharply and a negative voltage step is applied, via C_4 and C_2, to the anode of CSR_1. Thyristor CSR_1 is thereby turned off, and CSR_2 remains on. For this circuit to operate, the input pulse must be supplied from a low-impedance source,
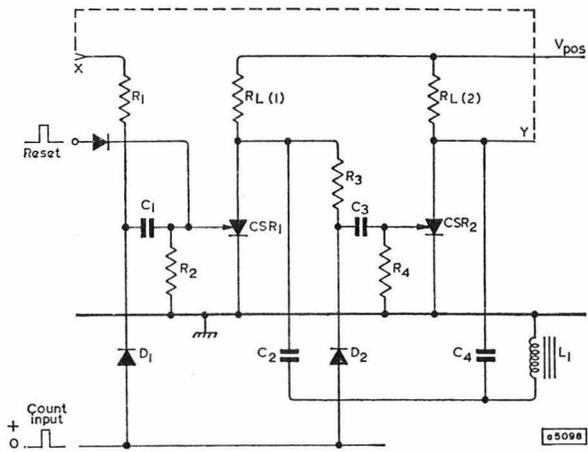
Fig. 53—Transfer between two thyristor stages

and must be of limited duration. The inductor L_1 is inserted as a load across which the turn-off commutation pulses are developed.

A number of these stages may be connected in the form of a ring counter, point X of the first stage being connected to point Y of the last. With this type of circuit it is possible to have more than one stage in a ring ON at the same time; thus, if each stage is provided with a reset input, shift register action is achieved.

Silicon Controlled Switch
The silicon controlled switch is a p-n-p-n structure, similar to a thyristor, but with a second gate for switching off. The two-transistor analogy, as illustrated in Fig. 54, is applicable, and all four connections are available.

Silicon controlled switches are available with high voltage ratings between anode and cathode and between anode and anode gates, and are

suitable for use as counting elements at speeds up to about 100kHz and as numerical indicator tube drivers. In the numerical indicator tube driving application, because the silicon controlled switch is a latching element (that is, a bistable device), it may also be used as a store.
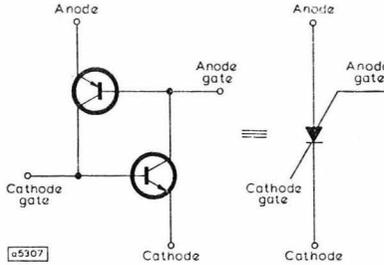
Fig. 54—Silicon controlled switch
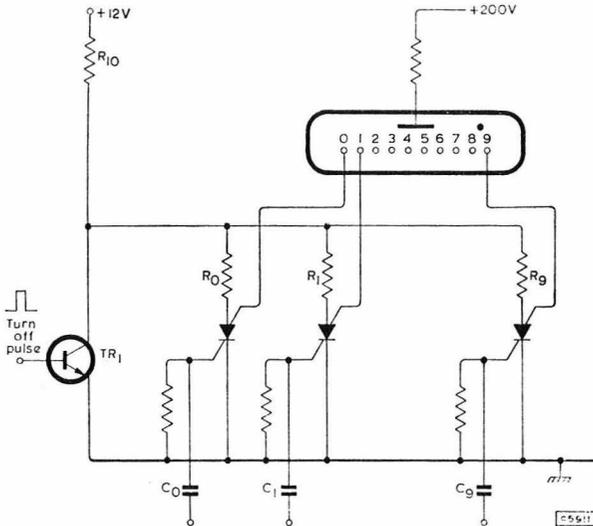
Fig. 55—Method of using silicon controlled switches in conjunction with a numerical indicator tube

The circuit given in Fig. 55 shows a method of using silicon controlled switches in conjunction with a numerical indicator tube. The operation of the circuit is as follows.

If all the silicon controlled switches are off, the anodes are biased to $+12V$ via R_{10} and R_{0-9}. A positive pulse appearing at one cathode gate turns that stage on and, due to internal gain, the device remains in

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the ON condition. The anode potential of the ON stage falls to the holding voltage (about 1V) and the anode gate voltage falls to near zero ($V_{CE(sat)}$ of the n-p-n section). One numerical indicator tube cathode is therefore switched on.

To switch off, the potentials on all anodes are reduced to below the holding voltage by a pulse applied via TR_1. A decimal ring counter using this type of device is discussed in Chapter 6.

Cold Cathode Trigger Tubes

The cold cathode trigger tube is a gasfilled switching element containing four, or occasionally five, electrodes. A schematic diagram of the element is given in Fig. 56.
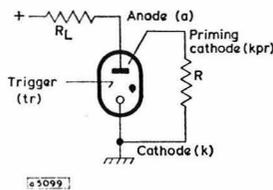

Fig. 56—Trigger tube

In operation, a voltage which is high, but insufficient to cause a discharge to begin, say 200V, is applied across the main anode-cathode gap. The priming cathode, which is sited behind the anode, is connected via a current-limiting resistor, R, of high resistance—usually 10 to 20MΩ— to the cathode or negative supply line. Since the gap between anode and priming cathode is small, this gap breaks down and a small current-limited discharge is set up. As a result of this discharge, some degree of ionisation occurs in the tube, the purpose of which is to provide reliable triggering performance. If the trigger electrode is now made sufficiently positive with respect to the cathode to cause a discharge across the trigger-cathode gap, extra ionisation occurs which reduces the striking potential of the main anode-cathode gap. This gap now breaks down and the discharge is maintained in the main anode-cathode gap. In this conducting state, the anode current is limited by the resistor R_L and the anode-to-cathode voltage remains constant at the maintaining voltage of the tube. Once in the conducting state, the trigger electrode has no further effect, and the glow can be extinguished only be reducing the anode current or by reducing the anode voltage below the maintaining voltage. Some tubes have two separate trigger electrodes for independent triggering from separate sources.

A useful method of triggering a cold cathode trigger tube is known as the "pulse plus bias" technique. A circuit using this technique to trigger Z700U tubes is shown in Fig. 57.
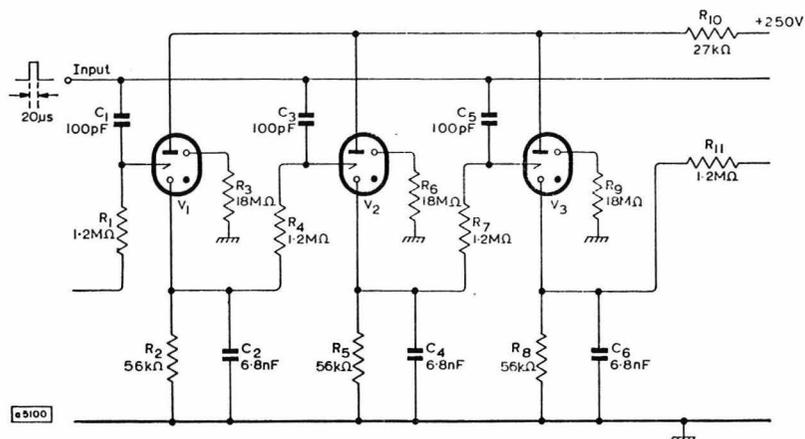

Fig. 57—Pulse plus bias transfer mechanism using Z700U cold cathode trigger tubes

If V_1 is assumed to be conducting and has a maintaining voltage of say 115V, the total voltage drop across R_2 and R_{10} is (250—115)V or 135V, giving a cathode current of approximately 1·6mA. For the purpose of this explanation, priming currents are neglected. The other tubes are assumed to be off. The cathode voltage of V_1 is therefore 1·6mA multiplied by 56kΩ; that is, approximately 90V, and this voltage is applied to the trigger of V_2 as a bias. For ignition of V_2 however, a pulse voltage of at least 172V is required. Tube V_2 is, therefore, off, and since no cathode current flows, there is no bias applied to the trigger of V_3.

When a 100V pulse is applied to the input line, it is fed via the 100pF coupling capacitors C_1, C_3 and C_5, to all the trigger electrodes. Because of the bias at the trigger of V_2, this 100V pulse raises the trigger electrode voltage of V_2 to 190V, causing the tube to turn on. No other tube has a standing bias and therefore only V_2 turns on. Capacitor C_4 was initially discharged and the cathode of V_2 was at zero voltage. The anode-to-cathode voltage of V_2 now falls rapidly to the maintaining voltage, and the voltage of the common anode supply line is reduced from its original value of some 210V to about 115V. The cathode of V_1 is held at a positive potential of 90V by the charge on C_2 and, therefore, since the voltage across V_1 is only some 25 to 30V, which is well below the maintaining voltage, tube V_1 is extinguished. The pulse now disappears. Because of

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the cathode current of V_2, capacitor C_4 charges to about 90V, the common anode line rises again to about 210V and a bias is applied to the trigger of V_3. Tube V_1 is now off, and only V_2 is on. The next input pulse causes V_3 to be triggered and V_2 to be extinguished. A number of these stages connected so that the cathode of the last biases the trigger of the first, form a ring counter. More elaborate circuits using cold cathode trigger tubes are discussed in Chapter 6.

DECADE SELECTOR AND COUNTING TUBES

Only the structure and operation of decade selector and counting tubes are described in this chapter. Detailed circuit design is included in Chapter 6. The tubes contain thirty cathodes equally spaced in a circle around a central anode disc. The structure is enclosed in a glass envelope which contains a mixture of inert gases at low pressure.

The cathodes are arranged in three groups of ten, termed main cathodes k_1, k_2, k_3 etc., guide-A cathodes GDA_1, GDA_2, GDA_3 etc. and guide-B cathodes GDB_1, GDB_2, GDB_3 etc. All the guide-A cathodes are connected together and brought out to a single pin, and similarly, the guide-B cathodes are connected to another single pin. The main cathodes and the anode are all brought out separately. A schematic diagram of the tube is shown in Fig. 58.
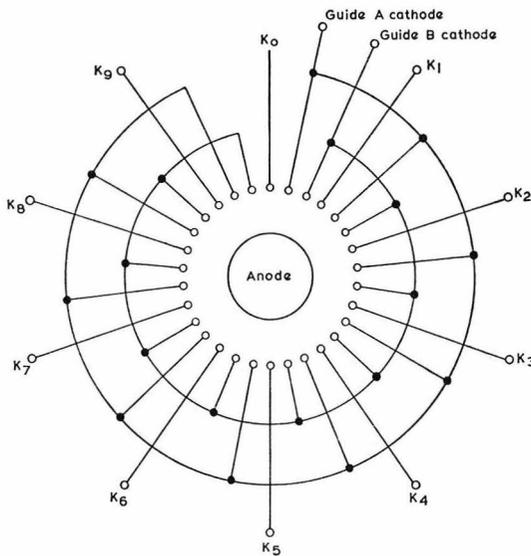

Fig. 58—Electrode layout in decade counter tube

In operation, a glow discharge is set up between the anode and one cathode, and this glow is visible through the top of the envelope. By the use of a suitable drive circuit, the glow is made to travel from one main cathode to the next at each input count pulse. Fitting an escutcheon around the tube enables the position of the glow to be read off in the positions 0 to 9, thus giving a visual read-out of the count reached.

The transfer of the glow from one main cathode to the next is effected as follows. Both the guide-A potential and the guide-B potential are normally positive. A negative pulse is applied to the guide-A cathodes, causing a transfer of the glow from the conducting main cathode to the adjacent guide-A cathode. The negative pulse is now removed, but simultaneously a negative pulse is applied to the guide-B cathodes. The glow is now transferred from the guide-A to the adjacent guide-B cathode. When the guide-B pulse is removed, since the guide-A pulse is now positive, the glow transfers to the nearest main cathode (the next in sequence) which is at low potential.

If cathode resistors are inserted, as shown in Fig. 59, a voltage read-out from the conducting cathode may be obtained. A method of generating the consecutive drive pulses, and for forward and reverse counting, is given in Chapter 6.
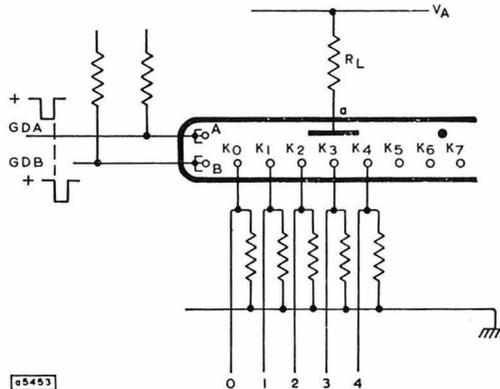

Fig. 59—Basic decade counter tube circuit

OTHER COUNTING ELEMENTS

It is possible to use a variety of other elements to perform counting and gating functions. One example is the magnetic core, as used for storing information in computers. This type of element may be used to build ring counters and shift registers, but has no special advantage except when used in computers.

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INDICATORS

Whilst several forms of indicator, such as meters, edge-lit indicators, etc. have been used as the read-out elements for counting circuits, probably the most economical and satisfactory solution is the numerical indicator tube. This is a cold cathode tube containing one anode and a set of ten cathodes. Each cathode is shaped to form a numeral or, in some cases, a letter or symbol, and when a glow is set up on the required cathode, the numeral is visible through the glass envelope. Details of the structure and use of these tubes are given in Chapter 11.

CHAPTER 4

PULSE SHAPING CIRCUITS

For most counting circuits to operate satisfactorily, a well defined input pulse shape is required. The most important characteristics are the rise and fall times of the pulse edges, and the amplitude of the pulse. The information to be counted, however, may come from any of a variety of sources, and may therefore require amplification or shaping, or both.

SIMPLE PULSE SHAPING CIRCUITS
The simplest form of pulse shaper is the squaring amplifier, the basic circuit of which is shown in Fig. 60.
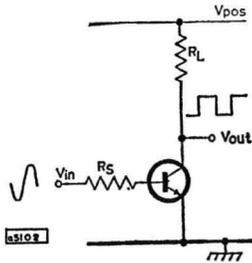
Fig. 60—Squaring amplifier   Fig. 61—Projected cut-off
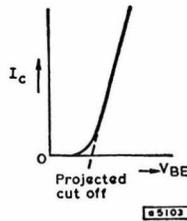
For operation in the linear region, with small signals, a variation δV_o in output voltage of a transistor amplifier of this type is given by:

$$\delta V_o = \delta I_b h_{FE} R_L.$$

The variation δI_b in base current is given by:

$$\delta I_b = \frac{\delta V_{in}}{R_s + r_{bb'} + (1 + h_{FE}) r_e},$$

where r_e and $r_{bb'}$ are the internal emitter and base resistances.

For the transistor to enter the saturated condition, if $V_{CE(sat)}$ is assumed to be negligible compared with V_{pos}, the collector current must be:

$$I_{c(sat)} = \frac{V_{pos}}{R_L}, \qquad \ldots(1)$$

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and the corresponding base current must be:

$$I_{b(sat)} = \frac{I_{c(sat)}}{h_{FE}}. \qquad \ldots(2)$$

Therefore, by combining Eq.1 and Eq. 2,

$$I_{b(sat)} = \frac{V_{pos}}{R_L h_{FE}}. \qquad \ldots(3)$$

To produce this base current, the required input voltage is given by:

$$V_{in} = I_{b(sat)}\{R_s + r_{bb'} + (1 + h_{FE})r_e\} + V_{BE}.$$

The value of V_{BE} is the minimum value of base-emitter voltage necessary to produce a flow of collector current. The more usual value taken for V_{BE} is the projected cut-off value shown in Fig. 61, and this value is used here.

To cut the transistor off, it is necessary only to reduce the base voltage to below the cut-off value. The input voltage swing necessary to travel from the saturated to the cut-off state (from V_1 to V_2 in Fig. 62) is therefore given by:

$$\delta V_{in} = I_{b(sat)}\{R_s + r_{bb'} + (1 + h_{FE})r_e\}.$$

Therefore, substituting for $I_{b(sat)}$ from Eq. 3

$$\delta V_{in} = \frac{V_{pos}\{R_s + r_{bb'} + (1 + h_{FE})r_e\}}{h_{FE}R_L} \qquad \ldots(4)$$

The value of r_e is $0 \cdot 025/I_e$ at 25°C, and the value used is the peak-current value. Note must also be taken that, in the above equations, the value of h_{FE} used is that which applies to the saturated state. Substitution of numerical values in Eq. 4 gives an indication of the effects of the fall in h_{FE} and the assumption of a low value of r_e.

Let:

V_{pos}	= 12V
h_{FE} (for saturation)	= 30
R_s	= 1kΩ
$r_{bb'}$	= 50Ω
R_L	= 1kΩ

From Eq. 1

$$I_{c(sat)} = \frac{V_{pos}}{R_L} = 12\text{mA},$$

corresponding to a value of r_e of $2 \cdot 08\Omega$, and from Eq. 4

$$\delta V_{in} = \frac{12\{1000 + 50 + (1 + 30) \times 2 \cdot 08\}}{30 \times 1000} = 0 \cdot 46\text{V}.$$

This gives an indicated voltage gain of 12/0·46, or 26·5, in the active region. The value of R_s may be reduced, thus giving a higher voltage gain, but the minimum value depends on the maximum source current which can be taken, and on the maximum permitted base current.
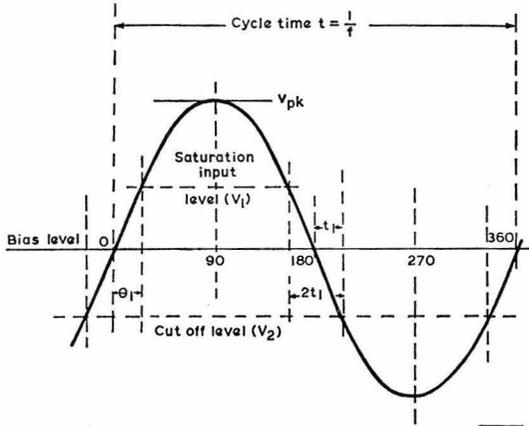
Fig. 62—Sine-wave input signal

If now a stage such as this is fed with a sine-wave signal of sufficient amplitude, the stage will be driven into saturation and cut-off on each cycle. The bias should be arranged so that the stage is in the active region when the sine-wave input signal passes through zero, thereby using the most rapidly changing part of the sine-wave as shown in Fig. 62.

The time spent in the active region may be calculated as follows. In time t, the input swings through one complete cycle, 360° or 2π radians. The voltage V_1 at any instant, corresponding to an angle θ_1 radians, is given in terms of the peak voltage v_{pk}, as:

$$V_1 = v_{pk} \sin\theta_1$$

that is,

$$\theta_1 = \sin^{-1}\left(\frac{V_1}{v_{pk}}\right).$$

The total active angle corresponding to the rise time from cut-off to saturation input level, $2t_1$ in Fig. 62, is given by

$$2t_1 = 2 \sin^{-1}\left(\frac{V_1}{v_{pk}}\right).$$

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Therefore, the total active time is given by

$$2t_1 = \frac{2\theta_1}{2\pi}t = \frac{t}{\pi}\sin^{-1}\left(\frac{V_1}{v_{pk}}\right).$$

This assumes that the input voltages from cut off to saturation are symmetrically disposed about the bias point. Deviation from this in practice causes negligible error in the calculated results.

For the example quoted above, V_1 was found to be 0·23V. For a 10kHz sine-wave signal having a peak voltage of 5V,

$$t = \frac{1}{f}$$
$$= \frac{1}{10 \times 10^3}$$
$$= 100\mu s$$

and the active time, $2t_1$, is thus given by

$$2t_1 = \frac{100 \times 10^{-6}}{\pi} \cdot \sin^{-1} \frac{0\cdot 23}{5} \text{ seconds}$$
$$= 1\cdot 45\mu s.$$
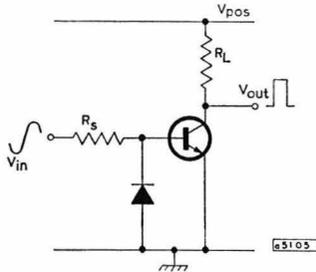
Fig. 63—Squaring amplifier with base clamp

While the ratio between the peak voltage and the voltage δV_{in} is large, the active time is inversely proportional to the peak voltage. Very large signals cannot be used without special protective circuits, however, since, in the reverse bias condition, there is danger of damaging the base-emitter junction. This can be avoided by connecting a diode between base and emitter as shown in Fig. 63. Switching times can also be reduced by limiting the collector voltage swing, by using a lower supply voltage or by using a diode clamp.

The above analysis assumes that the transition frequency, f_T, of the transistor used is much higher than the operating frequency, and that the desaturation time is not significant compared with the periodic time $1/f$.

REGENERATIVE PULSE SHAPING CIRCUITS

Regenerative pulse shaping circuits are circuits in which positive feedback is used to ensure fast switching. The most commonly used of these is the Schmitt trigger circuit. This is a bistable circuit which changes state in accordance with the d.c. input level, producing a fast switching action irrespective of the rate of change of the input voltage. A Schmitt trigger circuit is shown in Fig. 64. It may be seen that TR_1 is on if the input voltage is more positive than $V_E + V_{BE}$, and off when V_{in} is less than $V_E + V_{BE}$.
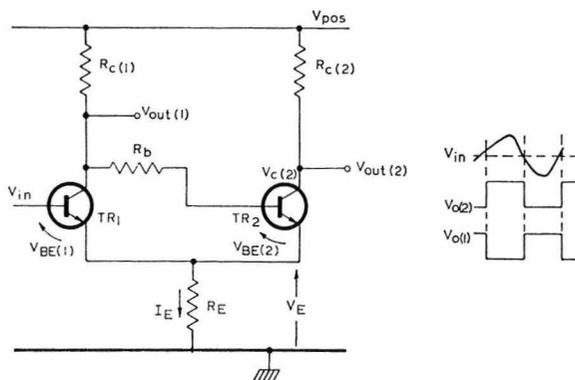

Fig. 64—Basic Schmitt trigger circuit

Transition Points

The Schmitt trigger circuit is a backlash circuit and operates as follows. If the value of V_{in} in Fig. 64 is high and transistor TR_1 is saturated, the base of TR_2 is held at the value of $V_{CE(sat)}$ for TR_1 and is therefore cut off. As V_{in} is reduced, a point is reached where TR_1 comes out of saturation and the collector voltage begins to rise. Transistor TR_2 then begins to conduct, causing V_E to rise and thereby turning TR_1 off sharply due to cumulative action. This is the first transition point, $V_{in(off)}$.

The circuit is now in its other stable state, with TR_1 cut off and TR_2 saturated. Normally, in this stable state, the base current of TR_2 is much higher than necessary to keep TR_2 saturated. If V_{in} is now raised, TR_1 begins to conduct and the emitter potential rises following V_{in}. Some of the current in R_E flows in TR_1 and therefore the emitter current of TR_2 is reduced. The collector voltage of TR_1 is falling and the emitter voltage is rising. Both of these factors tend to cut TR_2 off. Once V_{in} is high enough to bring TR_2 out of saturation, the circuit becomes unstable and reverts to the condition with TR_2 cut off and TR_1 saturated. This is

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the second transition point, $V_{in(on)}$. The difference between $V_{in(on)}$ and $V_{in(off)}$ is known as the backlash.

The input voltages at the transition points are given approximately by the following equations:

$$V_{in(off)} \simeq \frac{V_{pos}}{1 + \dfrac{h_{FE(1)}R_{C(1)}}{(1+h_{FE(1)})R_E}} + V_{BE(1)} \; ;$$

$$V_{in(on)} \simeq \frac{V_{pos}[h_{FE(2)}(R_{C(1)}+R_{C(2)})-R_b]-R_{C(2)}h_{FE(2)}V_{BE(2)}}{h_{FE}(R_{C(1)}+R_{C(2)})-R_b + \dfrac{R_{C(1)}R_{C(2)}h_{FE(2)}}{R_E}} + V_{BE(1)},$$

where $V_{BE(1)}$ and $V_{BE(2)}$ are the normal conduction values at the operating currents.

The value $V_{in(on)}$ is a function of the loop gain of the circuit, and depends, in practice, mainly on R_b and $h_{FE(2)}$.

As the difference between $V_{in(off)}$ and $V_{in(on)}$ decreases, the rise and fall times of the output waveforms increase until a point is reached where $V_{in(off)}$ is equal to $V_{in(on)}$. At this point, the circuit ceases to operate as a bistable element and becomes a linear amplifier.

The figures shown in Table 29 show the calculated and measured values for three prototype circuits. The effects of h_{FE} and R_b on backlash and switching times are shown. It can be seen from the table that a good degree of agreement is obtained between the measured and calculated figures, although the errors are larger in the low-voltage circuit. This is due to slight inaccuracies in the value assumed for V_{BE}.
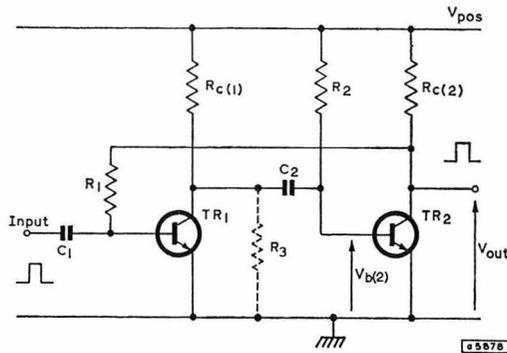

Fig. 65—Monostable circuit

TABLE 29

Performance of Schmitt Trigger Circuits

Circuit Details	R_b	$V_{in(off)}$		$V_{in(on)}$		t_r	t_f
		Calc	Meas	Calc	Meas		
	kΩ	V	V	V	V	ns	ns
Transistor = BC108	2·2	6·6	6·5	8·4	8·4	100	25
$h_{FE} \simeq 200$	10	6·6	6·5	8·4	8·3	400	150
$R_{C(1)} = R_{C(2)} = R_E = 1kΩ$	56	6·6	6·5	8·0	8·0	2000	400
$V_{pos} = 12V$	100	6·6	6·5	7·6	7·5	5000	600
Transistor = BSX19	2·2	6·6	6·6	8·4	8·4	20	30
$h_{FE} \simeq 25$	10	6·6	6·6	7·9	7·8	100	100
$R_{C(1)} = R_{C(2)} = R_E = 1kΩ$	22	6·6	6·6	6·9	6·8	200	200
$V_{pos} = 12V$	56 ←———————— linear —————————→						
Transistor = BSX19	2·2	3·5	3·6	4·4	4·3	25	18
$h_{FE} \simeq 25$	5·6	3·5	3·6	4·2	4·1	60	40
$R_{C(1)} = R_{C(2)} = R_E = 1kΩ$	10	3·5	3·6	4·0	3·9	150	120
$V_{pos} = 6V$	15	3·5	3·6	3·9	3·7	400	300
	22 ←———————— linear —————————→						

PULSE FORMING CIRCUITS
Several types of pulse forming circuit may be built using electronic components. One of the most useful of these in counting applications is the monostable, or delay, circuit.

Monostable Circuits
Monostable circuits are used to generate a pulse of defined width from an input triggering edge. A monostable circuit is shown in Fig. 65. The operation of this circuit is as follows.

Transistor TR_2 is normally held in the saturated state by the current passing through resistor R_2, and the output of TR_2 is at $V_{CE(sat)}$. The base of TR_1 is therefore held near zero voltage and TR_1 is cut off. When a positive pulse is applied to the input, TR_1 is turned on and the collector voltage falls. This fall in voltage is transmitted via C_2 to the base of TR_2, and TR_2 is cut off. The resultant rise in the collector voltage of TR_2 is passed to the base of TR_1 to hold it in the ON condition. Capacitor C_2 now charges via R_2 towards a value V_{pos}. Once the base voltage of TR_2 reaches some 600mV above zero, TR_2 begins to conduct and the circuit reverts to its stable state.

During the quasi-stable state, $V_{b(2)}$ is made negative by an amount

the second transition point, $V_{in(on)}$. The difference between $V_{in(on)}$ and $V_{in(off)}$ is known as the backlash.

The input voltages at the transition points are given approximately by the following equations:

$$V_{in(off)} \simeq \frac{V_{pos}}{1 + \dfrac{h_{FE(1)}R_{C(1)}}{(1+h_{FE(1)})R_E}} + V_{BE(1)} \; ;$$

$$V_{in(on)} \simeq \frac{V_{pos}[h_{FE(2)}(R_{C(1)}+R_{C(2)})-R_b]-R_{C(2)}h_{FE(2)}V_{BE(2)}}{h_{FE}(R_{C(1)}+R_{C(2)})-R_b + \dfrac{R_{C(1)}R_{C(2)}h_{FE(2)}}{R_E}} + V_{BE(1)},$$

where $V_{BE(1)}$ and $V_{BE(2)}$ are the normal conduction values at the operating currents.

The value $V_{in(on)}$ is a function of the loop gain of the circuit, and depends, in practice, mainly on R_b and $h_{FE(2)}$.

As the difference between $V_{in(off)}$ and $V_{in(on)}$ decreases, the rise and fall times of the output waveforms increase until a point is reached where $V_{in(off)}$ is equal to $V_{in(on)}$. At this point, the circuit ceases to operate as a bistable element and becomes a linear amplifier.

The figures shown in Table 29 show the calculated and measured values for three prototype circuits. The effects of h_{FE} and R_b on backlash and switching times are shown. It can be seen from the table that a good degree of agreement is obtained between the measured and calculated figures, although the errors are larger in the low-voltage circuit. This is due to slight inaccuracies in the value assumed for V_{BE}.
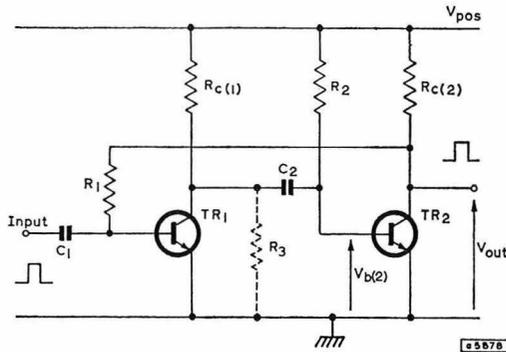

Fig. 65—Monostable circuit

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TABLE 29

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Circuit Details	R_b	$V_{in(off)}$		$V_{in(on)}$		t_r	t_f
		Calc	Meas	Calc	Meas		
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$V_{pos} = 12$V	100	6·6	6·5	7·6	7·5	5000	600
Transistor = BSX19	2·2	6·6	6·6	8·4	8·4	20	30
$h_{FE} \simeq 25$	10	6·6	6·6	7·9	7·8	100	100
$R_{C(1)} = R_{C(2)} = R_E = 1$kΩ	22	6·6	6·6	6·9	6·8	200	200
$V_{pos} = 12$V	56 ←			linear			→
Transistor = BSX19	2·2	3·5	3·6	4·4	4·3	25	18
$h_{FE} \simeq 25$	5·6	3·5	3·6	4·2	4·1	60	40
$R_{C(1)} = R_{C(2)} = R_E = 1$kΩ	10	3·5	3·6	4·0	3·9	150	120
$V_{pos} = 6$V	15	3·5	3·6	3·9	3·7	400	300
	22 ←			linear			→

PULSE FORMING CIRCUITS

Several types of pulse forming circuit may be built using electronic components. One of the most useful of these in counting applications is the monostable, or delay, circuit.

Monostable Circuits

Monostable circuits are used to generate a pulse of defined width from an input triggering edge. A monostable circuit is shown in Fig. 65. The operation of this circuit is as follows.

Transistor TR_2 is normally held in the saturated state by the current passing through resistor R_2, and the output of TR_2 is at $V_{CE(sat)}$. The base of TR_1 is therefore held near zero voltage and TR_1 is cut off. When a positive pulse is applied to the input, TR_1 is turned on and the collector voltage falls. This fall in voltage is transmitted via C_2 to the base of TR_2, and TR_2 is cut off. The resultant rise in the collector voltage of TR_2 is passed to the base of TR_1 to hold it in the ON condition. Capacitor C_2 now charges via R_2 towards a value V_{pos}. Once the base voltage of TR_2 reaches some 600mV above zero, TR_2 begins to conduct and the circuit reverts to its stable state.

During the quasi-stable state, $V_{b(2)}$ is made negative by an amount

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approximately equal to the fall in the collector voltage of TR_1. The time taken for $V_{b(2)}$ to rise again to the point where TR_2 begins to conduct is governed by C_2R_2 and the aiming potential. The general expression governing a charging CR circuit is:

$$v = V(1 - e^{\frac{-t}{CR}}),$$

where v is the instantaneous voltage at time t, and V is the total aiming potential. Manipulating this equation to give an equation for t gives:

$$t = -CR \log_e\left(1 - \frac{v}{V}\right) \qquad \ldots(5)$$

If it is assumed that $V_{b(2)}$ is taken negative by the full supply voltage and that TR_2 begins to conduct when $V_{b(2)}$ reaches zero, the equation becomes.

$$t = -C_2R_2 \log_e\left(1 - \frac{V_{pos}}{2V_{pos}}\right)$$
$$= C_2R_2 \log_e 0\cdot5.$$

Therefore

$$t = 0\cdot69\, C_2R_2 \qquad \ldots(6)$$

where t is the pulse width of the monostable circuit.

In circuits designed to operate from high voltage supplies, precautions must be taken to ensure that the maximum allowable value of reverse base-emitter voltage of TR_2 is not exceeded. A simple method of achieving this is to connect a resistor R_3 from the collector of TR_1 to the zero potential line, forming a potential divider with $R_{C(1)}$ as shown dotted on Fig. 65.

The collector voltage swing of TR_1 is thereby restricted to

$$V_{C(1)} = \frac{V_{pos}R_3}{R_{C(1)} + R_3}.$$

Eq. 5 now becomes:

$$t = -C_2R_2 \log_e\left(1 - \frac{V_{C(1)}}{V_{pos} + V_{C(1)}}\right).$$

Therefore, by substitution,

$$t = -C_2R_2 \log_e\left(1 - \frac{R_3}{R_{C(1)} + 2R_3}\right). \qquad \ldots(7)$$

Two practical examples are given in Table 30. The input pulses to both circuits have amplitudes of greater than 2V and durations of greater than 1μs.

The pulse width, or delay, of the first circuit is calculated by using Eq. 6, and that of the second circuit is calculated by using Eq. 7.

Monostable circuits giving pulse durations of less than 100ns may be built using BSX19 or BSX20 transistors.

TABLE 30
Details of Two Practical Monostable Circuits

	First Circuit	Second Circuit	
Transistor type	BC108	BC108	
V_{pos}	6	20	V
$R_{C(1)}$	2·2	10	kΩ
$R_{C(2)}$	1·0	5·6	kΩ
R_1	10	27	kΩ
R_2	10	22	kΩ
R_3	Omitted	3·3	kΩ
C_1	100	100	pF
Time for various values of C_2			
1nF	7	4·8	μs
2·2nF	15	10	μs
4·7nF	33	23	μs
10nF	70	48	μs
47nF	330	230	μs
100nF	700	480	μs
1000nF	7000	4800	μs

CHAPTER 5

BINARY COUNTERS

The basic form of electronic counter is the binary counter. This type of counter uses bistable stages to their full capacity, but it is not normally used where information is to be transmitted to human operators. Because the binary system is used in computers and calculating machines, some typical circuits are described in this chapter.

In this chapter, and in subsequent chapters, counters are broadly divided into two classes—synchronous and asynchronous. In synchronous counters, all stages are acted upon simultaneously under the command of a clock pulse. By this method, ambiguous transitional states are avoided and, in general, maximum counting speed is achieved. These circuits do not, however, necessarily offer the most economic solutions to counting problems.

Two types of asynchronous counter exist. In the first type, the output of one stage triggers the next, and so on through the counter. This type is called the 'ripple-through' type. In setting the last stage of a ripple-through counter, the total delay is equal to the sum of all the stage delays of the counter.

In the second type of asynchronous counter, gates are used and the delay in the information path may vary for different numbers, because different numbers may use different routes within the counter. In these counters, the delays are generally less than those in ripple-through counters and some information may actually be transferred synchronously. This is sometimes known as semi-synchronous operation.

BINARY UP COUNTER

A binary counter consists of a number of bistable elements cascaded in such a way that a change from the '1' state to the '0' state in one bistable element causes the next element in the chain to change its state.

The capacitively steered bistable circuit discussed in Chapter 3 is triggered only by the negative-going edge of an input pulse, a positive-going edge having no effect. Thus, if a chain of such elements is built up by connecting the 'true' or 'Q' output of each bistable circuit to the trigger input of the next, a binary up counter results.

A schematic diagram of such a counter is shown in Fig. 66. This

counter consists of four bistable circuits and has a total count capacity of sixteen states. The reset input of each bistable element is connected via an isolating diode and current limiting resistor to a common reset line. When this line becomes positive, all the bistable elements are reset to the zero state.
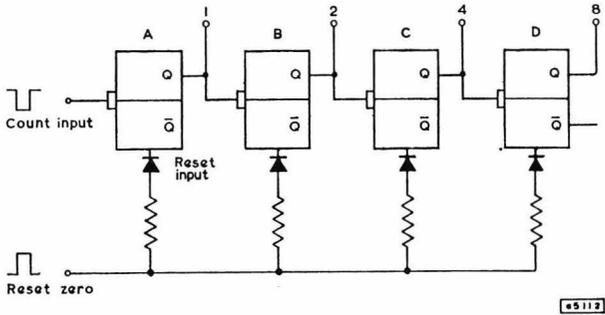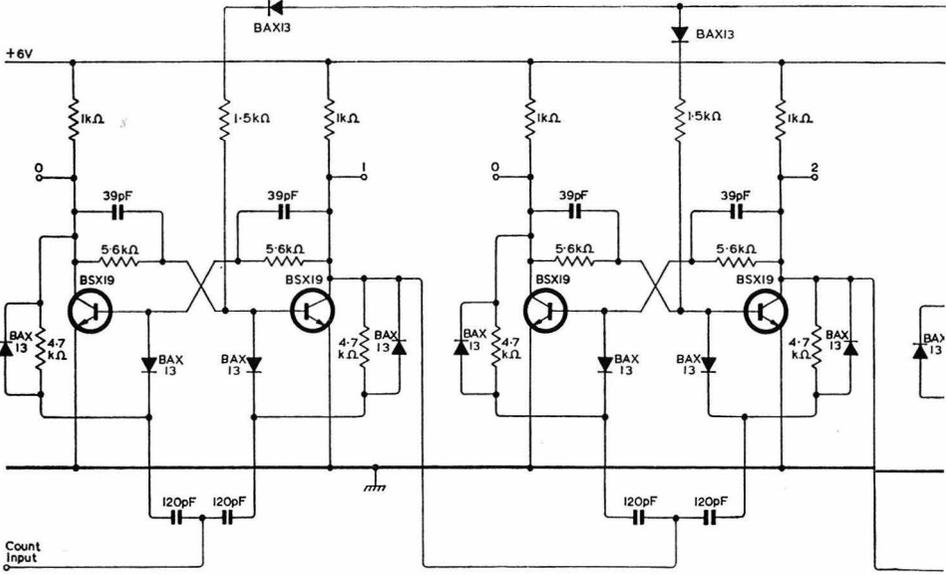

Fig. 66—Four-stage ripple-through binary up counter with reset

Any number of stages may be cascaded in this way to give a larger count capacity. The total count capacity of n stages is 2^n states. The truth table for the counter shown in Fig. 66 is given in Table 31. The sixteenth input pulse causes all the bistable circuits to reset to zero, enabling the counting cycle to begin again. A practical circuit for a counter of this type for counting at speeds up to 5MHz is shown in Fig. 67.

BINARY DOWN COUNTER

A binary down counter counts in a reverse binary sequence. The binary numbers 0 to 7 written in reverse order are shown in Table 32.

Examination of this table shows that the A bistable stage is triggered on every input pulse, the B bistable stage is triggered when the output of A changes from '0' to '1' and C is triggered when B changes from '0' to '1'. Thus, if a counter is made up of cascaded binary stages where the trigger input of each stage is fed from the inverted ($\bar{Q}$) output of the previous stage, a binary down counter results. Such a counter, extended to five stages, is shown in Fig. 68.
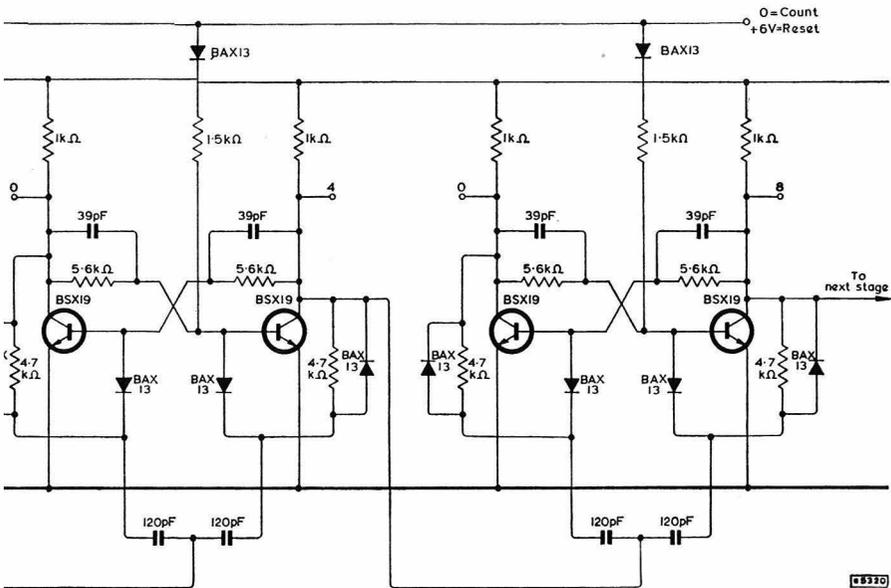
Fig. 67—Practical binary counter

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TABLE 31
Truth Table for the Simple Binary Up Counter shown in Fig. 66

No. of Count Input Pulses	Counter Outputs				Logical state
	D	C	B	A	
0	0	0	0	0	$\bar{A}.\bar{B}.\bar{C}.\bar{D}$
1	0	0	0	1	$A.\bar{B}.\bar{C}.\bar{D}$
2	0	0	1	0	$\bar{A}.B.\bar{C}.\bar{D}$
3	0	0	1	1	$A.B.\bar{C}.\bar{D}$
4	0	1	0	0	$\bar{A}.\bar{B}.C.\bar{D}$
5	0	1	0	1	$A.\bar{B}.C.\bar{D}$
6	0	1	1	0	$\bar{A}.B.C.\bar{D}$
7	0	1	1	1	$A.B.C.\bar{D}$
8	1	0	0	0	$\bar{A}.\bar{B}.\bar{C}.D$
9	1	0	0	1	$A.\bar{B}.\bar{C}.D$
10	1	0	1	0	$\bar{A}.B.\bar{C}.D$
11	1	0	1	1	$A.B.\bar{C}.D$
12	1	1	0	0	$\bar{A}.\bar{B}.C.D$
13	1	1	0	1	$A.\bar{B}.C.D$
14	1	1	1	0	$\bar{A}.B.C.D$
15	1	1	1	1	$A.B.C.D$
16	0	0	0	0	$\bar{A}.\bar{B}.\bar{C}.\bar{D}$

TABLE 32
Truth Table for Binary Down Counter

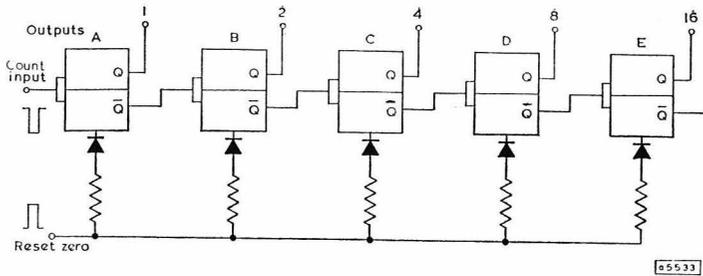| No. of Count Input Pulses	Counter Outputs		
	C	B	A
7	1	1	1
6	1	1	0
5	1	0	1
4	1	0	0
3	0	1	1
2	0	1	0
1	0	0	1
0	0	0	0
7	1	1	1

Fig. 68—Binary down counter with reset

SYNCHRONOUS BINARY COUNTERS

In each bistable stage, there is some delay between the application of the input pulse and the instant when the stage settles in its new state. In the cascaded counters discussed so far, these 'ripple-through' delays become cumulative. This effect is illustrated in Fig. 69. In many applications, this ripple-through delay is not important, but in applications where the counter can be sampled at any time during the counting process, errors may be introduced in the information taken from the counter. These errors can be avoided by sampling the counter only between input pulses after the maximum ripple-through delay has occurred, although
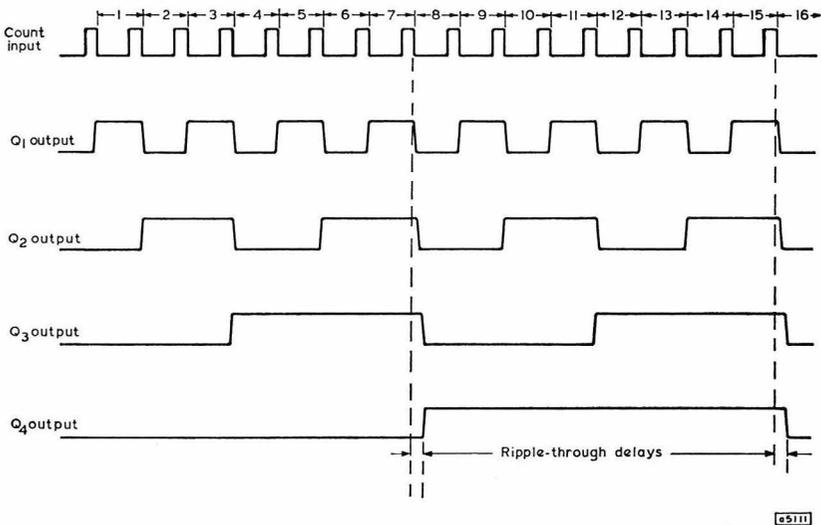
Fig. 69—Binary counter output waveforms showing ripple-through delays in turning Q_4 on and off

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this can only be done if the total delay is less than the minimum time be-tween successive inputs. A much better way is to use synchronous counting circuits.

Synchronous counters have a further advantage where feedback gating is used (as discussed in Chapters 7 and 8) because ripple-through delays would limit the maximum operating speed of the counter. In synchronous, or parallel, counters, delays are minimised by feeding the input trigger pulse to all bistable stages simultaneously, via gating circuits which ensure that only the appropriate stages are triggered by each count pulse.
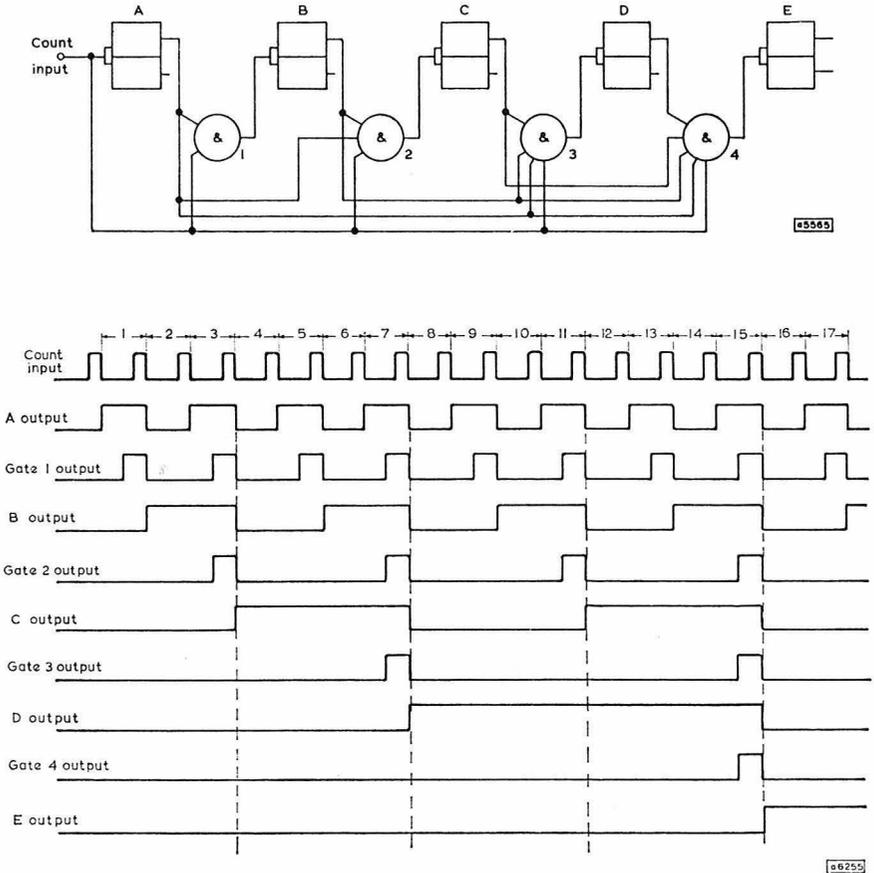
Fig. 70—Simple synchronous binary counter and associated output waveforms for first half of count cycle of 32 pulses

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By examination of the table of counter outputs shown in Table 31, the triggering conditions for each stage can be found as follows:
1. A is triggered for every input pulse.
2. B is triggered for input pulses arriving when A is present.
3. C is triggered for input pulses arriving when A and B are present.
4. D is triggered for input pulses arriving when A, B and C are present.

To provide a simple synchronous counter, it is, therefore, necessary to provide the following gating functions:

Trigger A : Input pulse (P)
Trigger B : A AND P (A.P)
Trigger C : A AND B AND P (A.B.P)
Trigger D : A AND B AND C AND P (A.B.C.P)
Trigger n : A AND B AND C AND D . . . (n–1) AND n AND P
$$(A.B.C.D . . . . . (n–1). n.P)$$

It may be seen that the loading on the trigger pulse source increases as the number of stages increases, as does the loading on the output of the bistable elements, particularly those early in the chain. A long counter of this type requires a considerable number of extra components.

A synchronous counter of the above type using triggered bistable elements is shown in Fig. 70. Similar circuits can be made from clocked R–S or J–K bistable elements; for example, a synchronous binary counter using J–K bistable circuits is shown in Fig. 71. The waveforms for this counter are shown in Fig. 72.
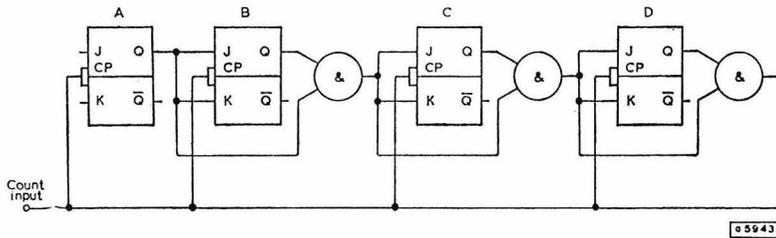

Fig. 71—Synchronous binary up counter using J-K bistable elements

REVERSIBLE BINARY COUNTER

By combining the up and down counters, with suitable gating, a reversible counter may be constructed. A four-stage counter of this type is shown, in logic diagram form, in Fig. 73. When the up line potential is positive and the down line potential is zero, pulses from the Q outputs are fed, via AND gates 1, 2 and 3 and OR gates 4, 5 and 6 to the bistable trigger inputs, resulting in up counting. If the up line is at zero potential and the down line is positive, the trigger signals are fed from the Q̄ outputs via gates 7, 8 and 9, resulting in down counting.
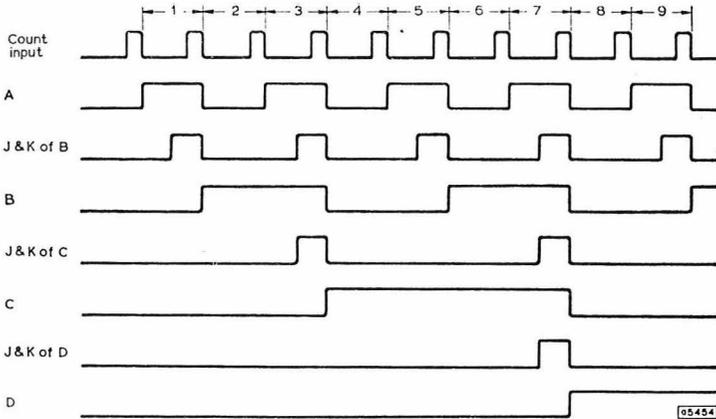
75

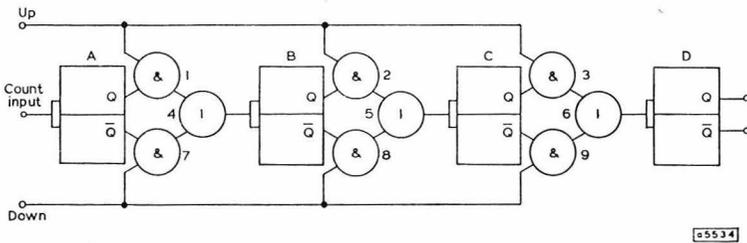Fig. 72—Waveforms for synchronous binary up counter shown in Fig. 71

Fig. 73—Basic reversible binary counter

alternative method of achieving the same result by the use of DTL logic, is shown in Fig. 74. The wired-OR connection at the output NAND gates is described in Chapter 3. Because of the inversion pro- in the NAND gates, the trigger pulses for the up count are taken from outputs, and those for the down count are taken from the Q outputs.
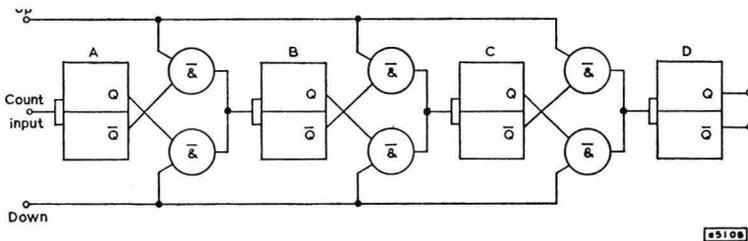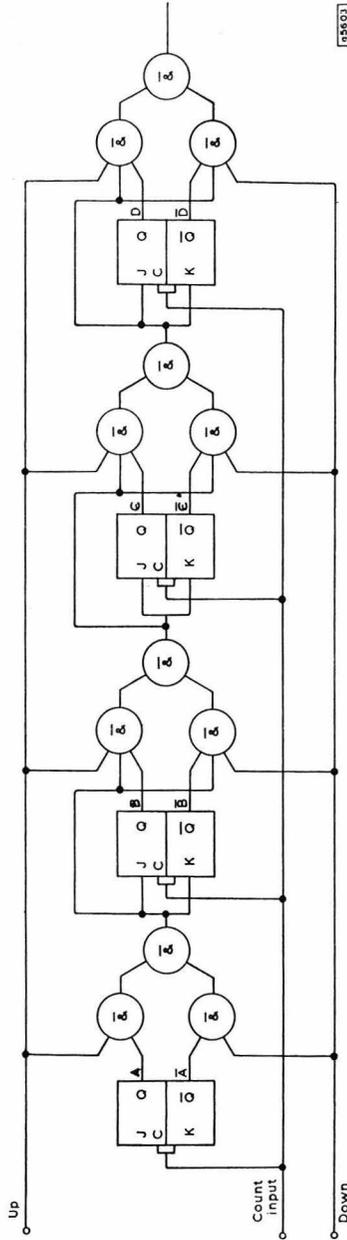

Fig. 74—Reversible binary counter using NAND logic

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Fig. 75—Reversible synchronous binary counter

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In both these circuits it is necessary that, in changing from up to down counting, or vice versa, the rate of change of voltage applied to the control lines is low enough to prevent the bistable circuit trigger inputs from responding.

These problems can be solved by using a synchronous circuit such as that shown in Fig. 75. The waveforms for this circuit are given in Fig. 76. When this circuit is used, the control line potentials must not be changed during a count input pulse.
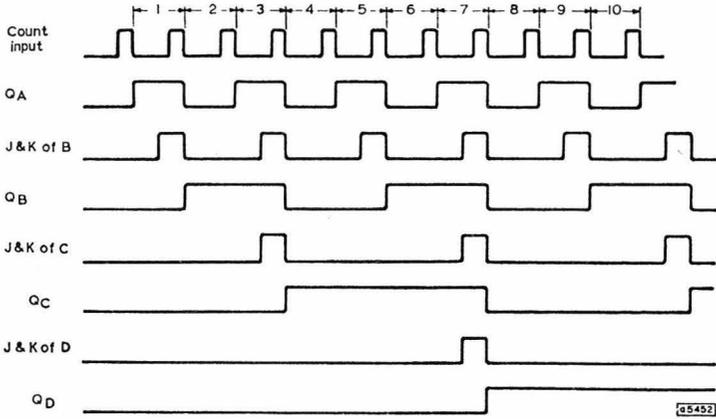

Fig. 76—Waveforms for reversible synchronous binary counter

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RING COUNTERS

The basic principles of ring counters have been explained in Chapter 1. In the present chapter, several examples of ring counters are given, together with detailed design information.

The simplest form of ring counter is the one-out-of-ten type, in which there are ten electronic switches, only one of which is permitted to be closed at any time. When a count pulse is received, the conducting switch is opened, or made non-conducting, and the switch adjacent to it is closed. A continuous train of count pulses, therefore, causes the position of the closed switch to step along the row. If the output of the tenth switch is connected to the input of the first switch, a continuous ring is formed, the elements of which represent the figures nought to nine, in order round the ring. This ring, therefore, represents one decade—the units decade—of the total count. More significant decades—tens, hundreds, thousands and so on—may be made by applying a 'carry' pulse, generated at the same time as the 'nought' switch closes, to the input of another decade ring.

ONE-OUT-OF-TEN RING COUNTER USING J-K BISTABLE ELEMENTS

A ring counter, in which ten J-K bistable elements are used as the electronic switches, is shown in Fig. 77. If integrated circuits of the FC range
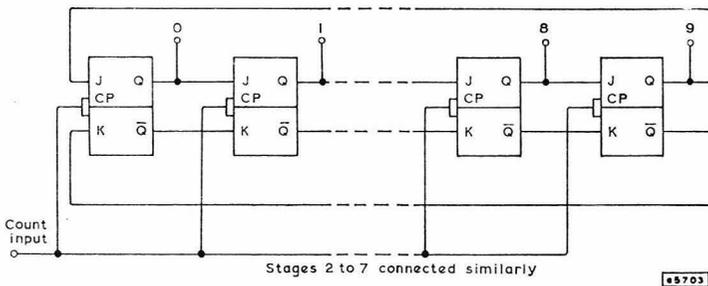

Fig. 77—A ring counter using J-K bistable elements

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are used to make this ring counter, its performance is as shown in Table 33.

TABLE 33
Performance of Ring Counter using J-K
Bistable elements of the FC range

Maximum operating frequency $\geqslant$ 10MHz
Supply voltage $= 6V \pm 10\%$
Drive pulse
      amplitude $= 4V$
      rise time $< 50ns$
      fall time $< 50ns$

RING COUNTER USING SILICON CONTROLLED SWITCHES

As discussed in Chapter 3, the silicon controlled switch is a device which has two stable states—on and off. Unlike the transistor, it continues to conduct after the input drive current has been removed. It can be switched off by driving the anode gate positive or reducing the voltage on the cathode gate below the base-emitter cut-off voltage, which is about $+0.7V$. Turn off may also be effected by reducing the anode voltage or current below the holding values.
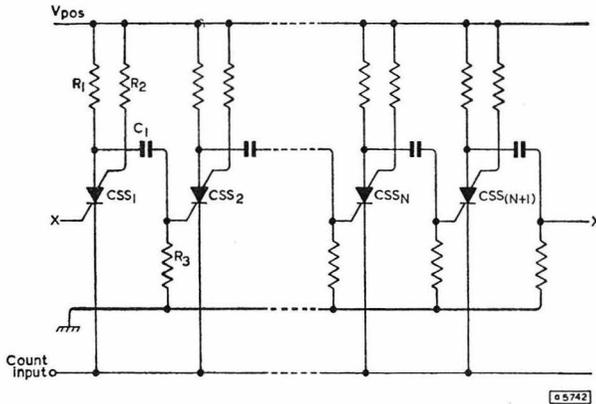

Fig. 78—Silicon controlled switches connected as a ring counter

The silicon controlled switch is used to its best advantage in a ring counter configuration where each device switches a number in a numerical indicator tube. In this configuration, no decoding is required and the controlled switch acts as its own store.

The principle of operation of a silicon controlled switch ring counter may be explained by means of Fig. 78. When CSS_1 is conducting, all others are switched off. When a count pulse arrives, all devices, whether on or off, are switched off because their cathodes have been made positive with respect to their cathode gates. When the count pulse disappears,

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all devices are left switched off with the exception of CSS_2, whose cathode gate is temporarily positive while the charge on capacitor C_1 adjusts itself to the new d.c. conditions. The anode potential of CSS_1 changes from about 1V (the ON state) to $+V_{pos}$ (the OFF state). Having been triggered, CSS_2 remains in the conducting state even after the drive from C_1 ceases. Further count pulses cause each stage of the ring counter to conduct sequentially in a similar manner.
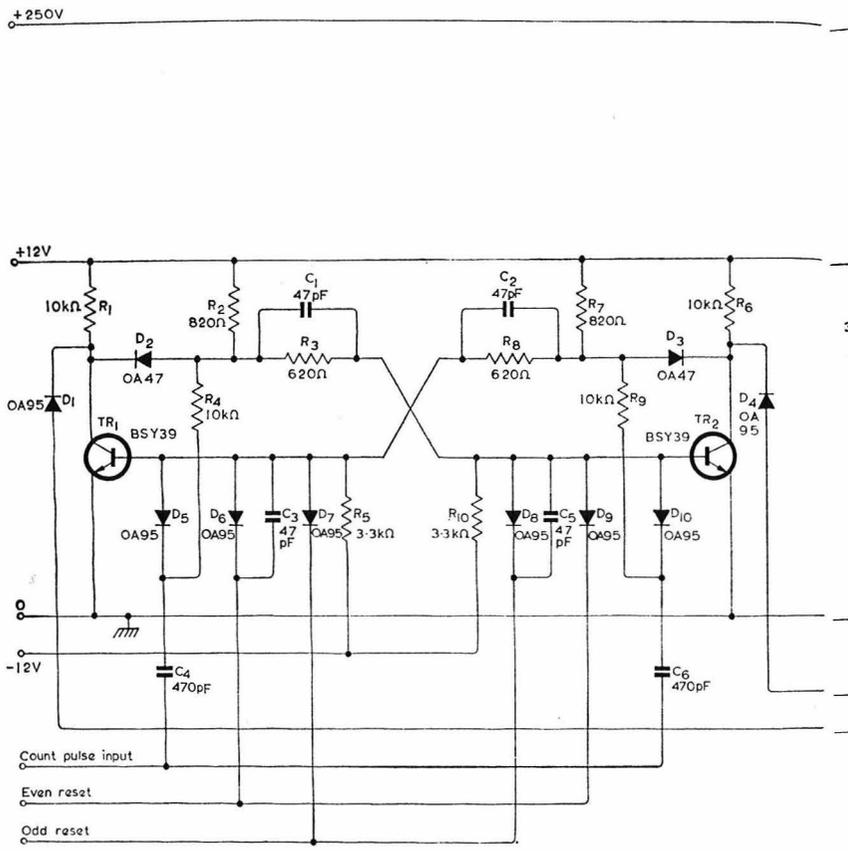
In practice, such a system is not feasible, mainly because of speed limitations. For instance, it is the leading edge of the count pulse which turns each silicon controlled switch off and initiates the discharge trigger voltage across R_1. If the count pulse is long, this voltage will have disappeared before the arrival of the trailing edge of the pulse restores the cathode to zero voltage—a necessary state if the trigger voltage is to be effective.

A better scheme is shown in Fig. 79. The principle of this system is that the cathode voltage of the silicon controlled switch which is to be triggered next is made zero at the same time as the trigger voltage is initiated by the turning off of the previous silicon controlled switch. This is achieved by driving alternate cathodes between zero voltage and some positive voltage on the application of each count pulse. This is easily effected by using the count pulse to drive a bistable stage and connecting the outputs of the bistable circuit to alternate silicon controlled switch cathodes. The circuit incorporates a facility for setting any number in the numerical indicator tube which operates in the following manner.

Suppose it is required to set a '0' in the numerical indicator tube. A negative pulse, with an amplitude of 12V and a duration of 20µs, is applied to the 'Even reset' line. This turns TR_1 and TR_2 off simultaneously via D_6 and D_9. At the end of this pulse a positive-going spike is fed via C_3 to the base of TR_1. Transistor TR_1 is therefore turned on. Transistor TR_2 is not affected by this spike because there is no capacitor across D_9. This primes all the even-numbered silicon controlled switches. Now a positive pulse with an amplitude of 12V and a duration of 2µs is applied to the '0' line. This pulse triggers the cathode gate, the silicon controlled switch turns on and the '0' is illuminated in the indicator tubes. The performance of the circuit is given in Table 34.

TABLE 34
Performance of Silicon Controlled Switch Ring Counter

Maximum frequency	= 50kHz
Count pulse (negative-going)	
amplitude	= 5V
duration	= 10µs
rise and fall times	< 200ns

+250V

+12V

10kΩ R₁

R₂ 820Ω

C₁ 47pF

R₃ 620Ω

C₂ 47pF

R₈ 620Ω

R₇ 820Ω

10kΩ R₆

D₂ OA47

D₃ OA47

OA95 D₁

TR₁ BSY39

R₄ 10kΩ

10kΩ R₉

D₄ OA 95

TR₂ BSY39

D₅ OA95

D₆ OA95

C₃ 47 pF

D₇ OA95

R₅ 3·3kΩ

R₁₀ 3·3kΩ

D₈ OA95

C₅ 47 pF

D₉ OA95

D₁₀ OA95

0

/77/

C₄ 470pF

C₆ 470pF

-12V

Count pulse input

Even reset

Odd reset

Tolerances: Resistors ± 10%, Capacitors ± 20%. Voltages ± 5%

Fig. 79—Practical ring counter using

silicon controlled switches

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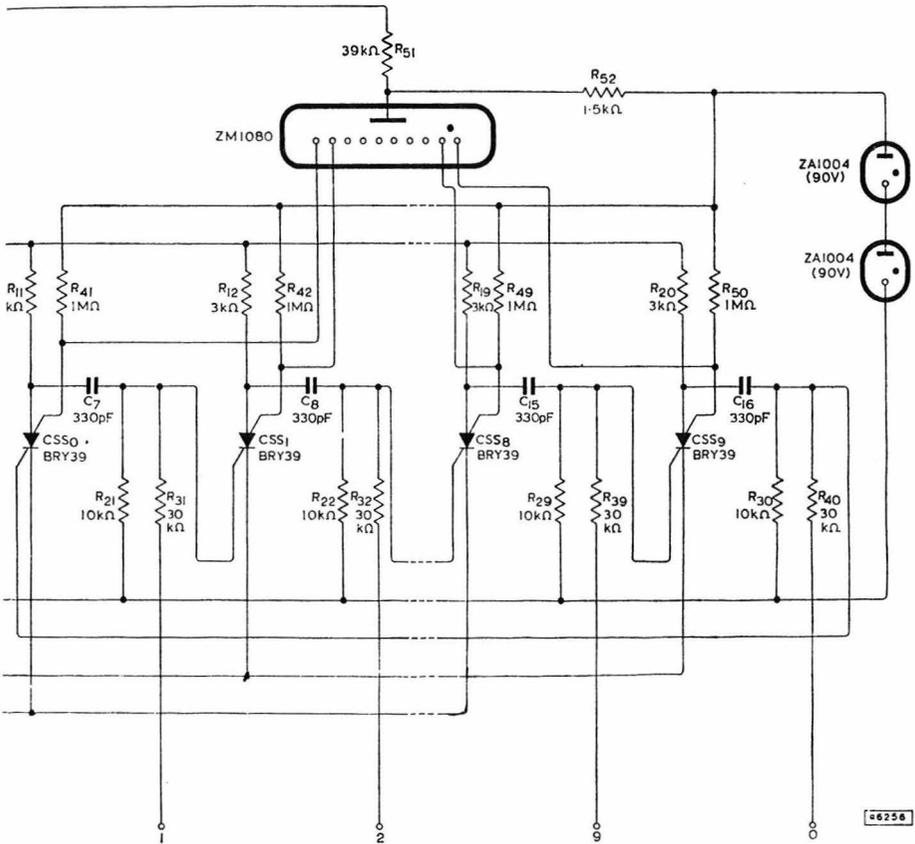
RING COUNTER USING P-N-P/N-P-N COMPLEMENTARY PAIRS

The operation of the complementary-pair bistable circuit has been fully discussed in Chapter 3. In the present chapter, a reversible ring counter using complementary pairs is described. The basic p-n-p/n-p-n switch used in this counter is shown in Fig. 80. The object of the constant-
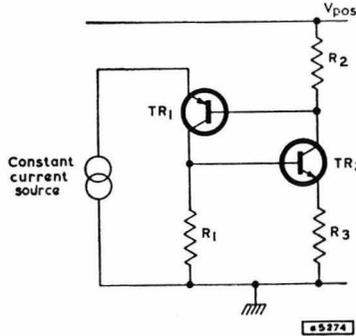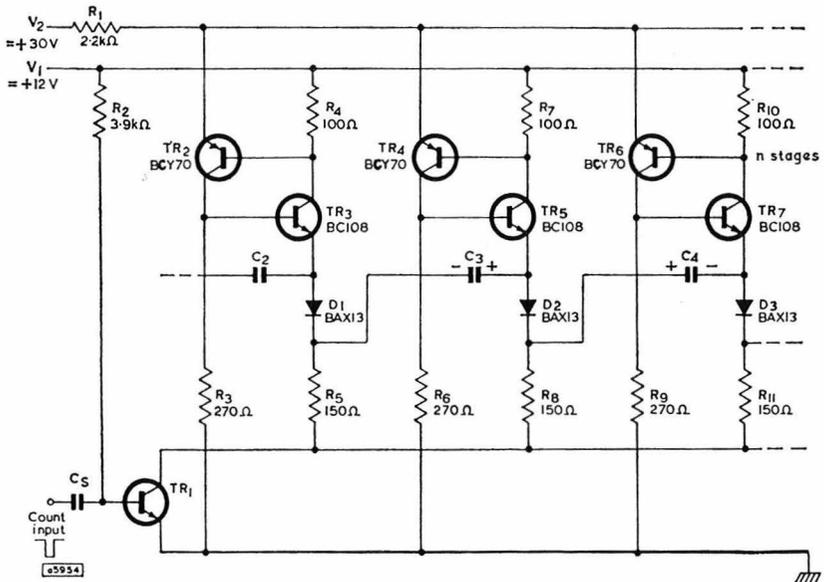

Fig. 80—Basic p-n-p/n-p-n switch

Fig. 81—Three stages of the complementary pair counter

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current source is to ensure that, when the switch is in the ON state, neither transistor is saturated. The current source achieves this by establishing a fixed potential across resistor R_1, so that the emitter and base potentials of TR_2 are known. The current in R_3 is fixed by emitter follower action in TR_2, and this current flows in R_2, thereby defining the collector potential of TR_2. By suitable choice of resistor values and current source, both transistors are kept out of saturation. This is important in order to ensure that switching times are kept to a minimum.

Three stages of the counter are shown in Fig. 81. When the centre stage is conducting, capacitors C_3 and C_4 are charged and the arrival of a count pulse causes C_3 to discharge, turning the next stage on as explained in Chapter 3.

Reversible P-N-P/N-P-N Counter

By providing a second drive and steering circuit as shown in Fig. 82, the counter is made reversible. The performance of this counter when constructed with the component values shown is given in Table 35.

TABLE 35

Performance of Complementary Pair Counter

	BSX19 BSY40	BC108 BCY70
Maximum frequency	6MHz	1MHz
Current	20mA	20mA
Drive pulse		
amplitude	2V	2V
fall time	10ns	<20ns
rise time	100ns	100ns

ONE-OUT-OF-TEN RING COUNTER USING TRIGGER TUBES

Two stages of a ring counter using gasfilled trigger tubes, such as the Z700U, are shown in Fig. 83. Each tube is continually primed by the discharge across the anode-to-priming cathode gap of the trigger tube. Stepping is effected by means of a pulse plus bias system. If, for example, tube V_1 is conducting, the current through that tube flows through the cathode resistor R_{13} and develops a voltage of about 60 to 90V across it. This voltage appears at the trigger of V_2 and forms the bias for the next count pulse. If now a pulse of the order of $+100V$ and having a fairly short rise time is applied to the trigger electrode of each tube via a capacitor, the amplitude of this pulse is insufficient to trigger any tube except V_2, whose
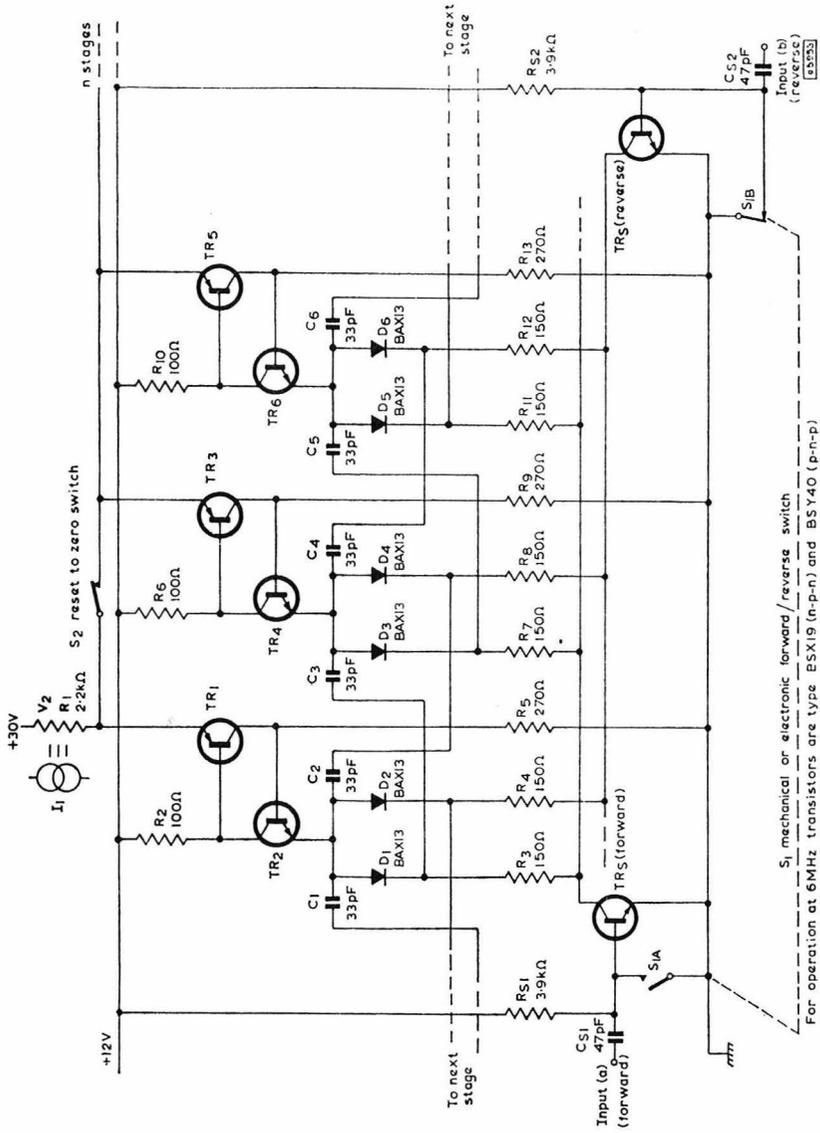
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Fig. 82—Reversible ring counter using p-n-p/n-p-n complementary pairs

trigger is already at the cathode potential of tube V_1. Therefore, V_2 conducts. The current now drawn by V_1 and V_2 increases the potential drop across R_4, so that the voltage on the line to the right of R_4 is reduced. This, together with the voltage dropped across R_{12} and R_{13} (which is unable to change instantly because of the presence of C_6 and C_7) causes V_1 to be extinguished.
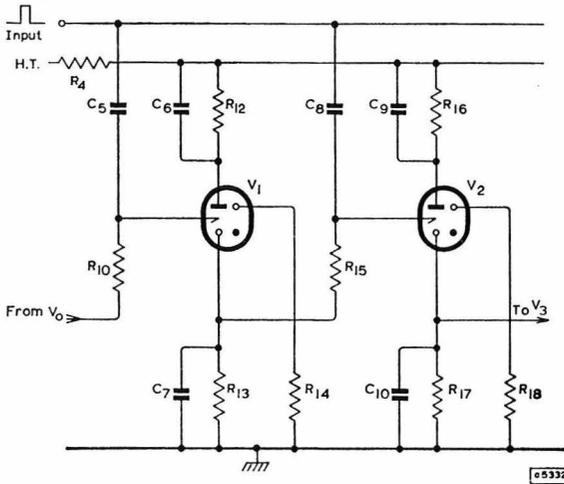

Fig. 83—Two stages of a ring counter using trigger tubes

A complete decade circuit including a numerical indicator tube display, a carry stage, and start and reset facilities, is shown in Fig. 84. The operating details of the counter are given in Table 36. Each cathode of the numerical indicator tube (type ZM1020 or ZM1080) is connected to the anode of the appropriate Z700U trigger tube. Thus, when a tube is triggered, the fall in potential at its anode causes the correct cathode of the numerical indicator tube to conduct and display the appropriate number.

TABLE 36

Operating Details of Counter shown in Fig. 84

Operating frequency	= 1kHz
Drive pulse amplitude	= 70 to 100V

Tube V_{10} generates the carry pulse to the next decade and is in a self-extinguishing circuit. When V_9 is triggered, a bias voltage is applied to the trigger of V_{10}. The next input pulse, in conjunction with this bias, overcomes the trigger-cathode breakdown voltage, and V_{10} is

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Fig. 84—One decade of a decimal counter using Z700U trigger tubes
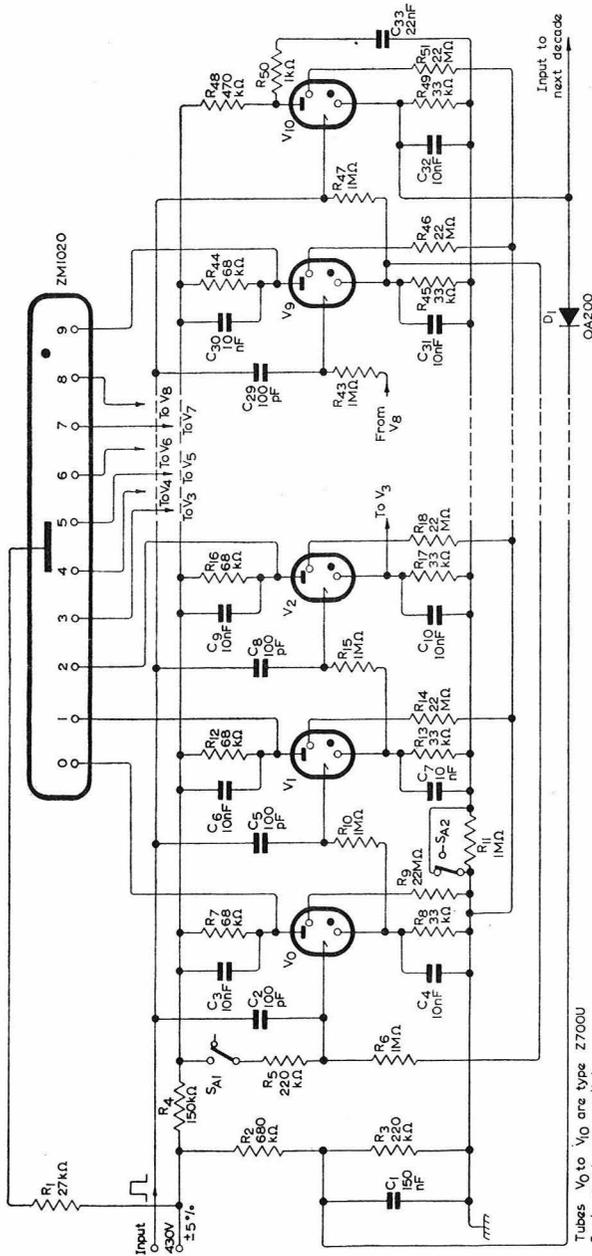
Tubes V_0 to V_{10} are type Z700U
S_A is reset-zero switch
Stages 3 to 8 are the same as stage 2, and have been omitted from the drawing
All capacitors 500V rating. All resistors $\frac{1}{2}$ W

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triggered. This pulse is also the "carry-to-zero" pulse and triggers V_0. Capacitor C_{33} discharges through V_{10}, generating a positive pulse at the cathode which becomes the input pulse to the next decade. The amplitude of this pulse is limited by the catching diode D_1. When C_{33} has discharged to such a voltage that the anode-to-cathode voltage of V_{10} is below the maintaining voltage (116V), V_{10} is extinguished.

The function of the start/reset switch, S_A, is twofold. When the circuit is first switched on, or when a count has been completed, any tube may be in the triggered condition. To set the counter to zero, the start/reset switch is closed. S_{A2} introduces a 1MΩ resistor into the common negative line of all tubes except V_0, thus reducing the current in all stages except the first to a value below the holding current and thereby extinguishing all tubes other than V_0. Simultaneously, S_{A1} applies a trigger pulse to V_0 via R_5, to trigger V_0 if it has not already been triggered.

Some care should be taken in arranging the components and wiring of the circuit, or non-sequential stepping may occur. In general, the connections between the leads of the trigger tube and adjacent passive components should be short, particularly the priming cathode lead.

Reversible Operation

The ring counter described above may be made to count in a reverse, as well as a forward, direction by the use of a modified trigger tube such as the Z700W. This tube has two trigger electrodes, but is otherwise identical to the Z700U. A reversible ring counter circuit using the Z700W is shown in Fig. 85. The circuit is fundamentally the same as that of the unidirectional circuit shown in Fig. 84, with the addition of the couplings between the cathodes and second trigger electrodes. The extra tube (V_{11}) is necessary to generate the carry pulse to the next decade.

ONE-OUT-OF-TEN RING COUNTER USING Z504S DECADE SELECTOR AND COUNTING TUBES

A detailed description of the operation of the Z504S counting tube is given in Chapter 3. Briefly, this tube is a cold-cathode gasfilled discharge tube, having a central anode in the form of a disc, around which are symmetrically placed ten main cathode electrodes. Between each main cathode, a guide-A cathode and a guide-B cathode are interposed. The discharge is caused to step from one main cathode to the next by inducing it to step first to the guide-A cathode, then to the guide-B, and finally to the next main cathode. The mechanism by which the discharge changes position is to drive first the guide-A cathodes and then the guide-B cathodes negative for a short time one after the other. The limits to which the guide pulses must conform are shown in Table 37.
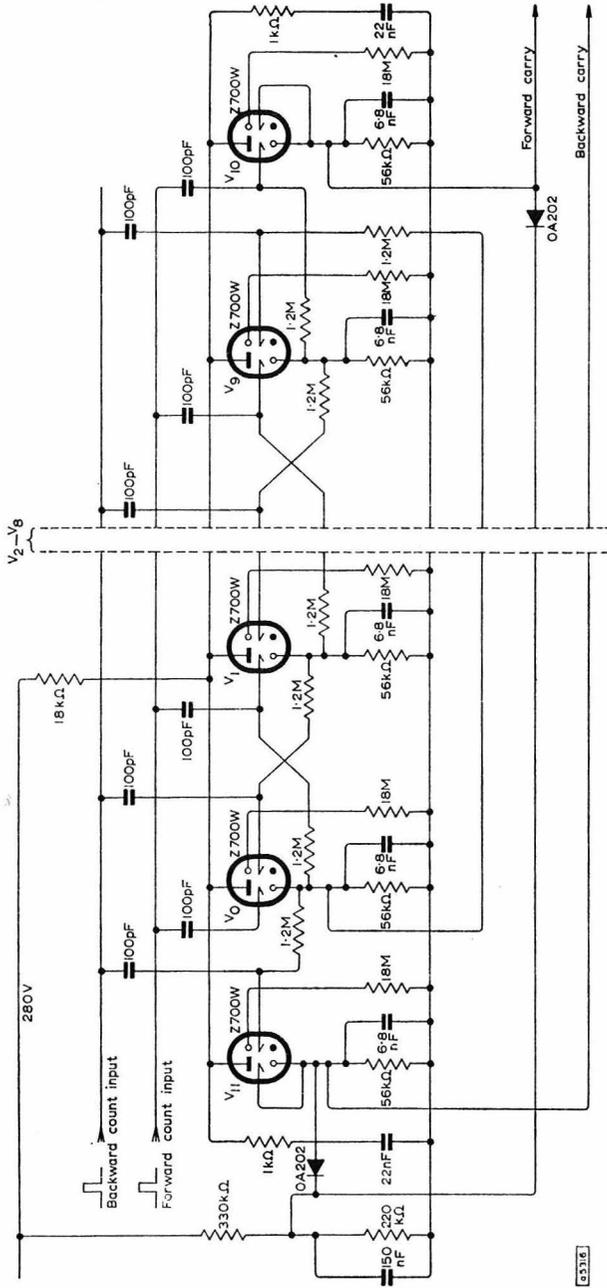
Fig. 85—A reversible decade ring counter using Z700W trigger tubes
(Numerical indicator tube driving circuitry not shown)

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TABLE 37

Recommended Characteristic Operating Range of Decade Selector and Counting Tubes type Z504S

|	
Nominal anode current	$330\mu A$
Minimum dwell time:	
guide-A cathode	$60\mu s$
guide-B cathode	$60\mu s$
main cathode	$75\mu s$
Negative guide voltage for transfer:	
minimum	45V
maximum	$(140 - V_{GDB})V$
Positive guide supply voltage:	
main cathode dwell time $>$ 1ms	minimum 25V
main cathode dwell time $\leqslant$ 1ms	minimum 35V
	maximum 50V
Maximum negative bias voltage on any main cathode	$-14V*$
Maximum positive voltage excursion on any main cathode	$(V_{GDB} - 10)V$
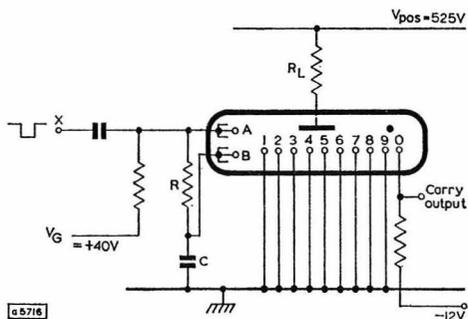
Fig. 86—Basic R-C integrator network

Integrated Pulse Drive

One method of generating drive pulses is to use a capacitor-resistor integrating circuit. This method is known as integrated pulse drive. The basic integrator input circuit is shown in Fig. 86. When an input signal consisting of a negative rectangular pulse of 100V is applied to point X, the guide-A potential immediately falls by the amplitude of the applied pulse (see Fig. 87). The discharge in the tube then transfers from the main cathode to its adjacent guide-A cathode. The capacitor C begins to

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*Where a 14V negative bias is used with guide-B rest periods of less than 120μs the minimum recommended negative guide voltage for transfer should be increased to $-60V$.

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charge with a time-constant CR, from the positive guide bias level towards the potential of the guide-A cathodes. When the input pulse at point X ends, the guide-A potential rises again to the positive guide bias level, and the anode rises towards a potential which is equal to the sum of the maintaining voltage and the positive guide bias (that is, $V_m + V_G$).

Now, if the guide-B cathodes are at the guide-A potential when the guide-A pulse ends, the potential difference between the anode and the guide-B cathodes is increased toward $V_m + V_G + V_{pulse}$, and the discharge transfers from the guide-A cathode to the adjacent guide-B cathode. The discharge now rests on this cathode and the capacitor C discharges exponentially back to the positive guide bias level—with a corresponding rise in anode voltage. When the guide-B cathode becomes sufficiently positive, and the anode voltage has risen sufficiently for breakdown to occur between the anode and the next main cathode, the discharge transfers to this main cathode. The transfer from one main cathode to the next is now complete, and the circuit is ready for a further input pulse.
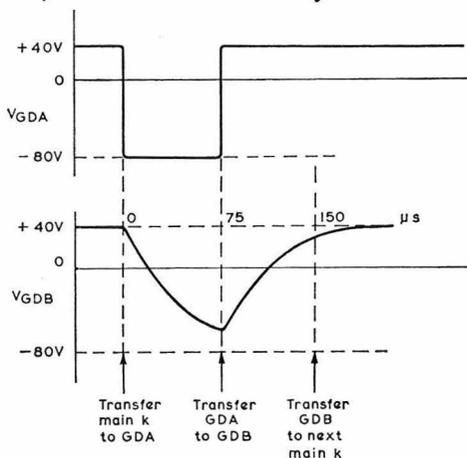

Fig. 87—Guide-A and B pulses

Transistor Drive Circuit

The first counting tube in a system is required to operate from an external signal source, and is therefore driven by a pulse-shaping circuit which provides a negative pulse of defined amplitude and width, which is suitable for direct application to the guide-A cathodes (assuming clockwise rotation). The integrator circuit which has been described has only to generate a delayed pulse for guide-B cathodes.

A transistor drive circuit is shown in Fig. 88. The circuit consists of a monostable circuit which, when triggered, produces a pulse of defined

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Fig. 88—Transistor drive circuit

amplitude and duration (100V, 100μs). This pulse is then used to produce the two pulses required to drive the guide electrodes. The monostable circuit is in its stable state when TR_1 is saturated and TR_2 is cut off. The collector voltage of TR_2 is 100V. When a count pulse is applied to the input, the monostable circuit is triggered. The count pulse must be negative-going and must have an amplitude of about 5V if its rate of rise is no greater than 4V/μs. With a steeper edge, a smaller amplitude can be tolerated. Once the circuit has been triggered, the waveform at the collector of TR_2 changes as shown in Fig. 89.

Fig. 89—Voltage waveforms at various points in the drive circuit

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Both guides are normally maintained at $+40V$ by the potential divider R_7, R_8. When the monostable circuit is triggered, the waveform at the collector of TR_2 is coupled via the capacitor C_3 to the guide circuits. The guide-A waveform is as shown in Fig. 89. Capacitor C_4 and resistor R_{11} differentiate the signal, producing the guide-B waveform shown in the same figure. The purpose of the diode D_1 is to prevent the voltage on the guide cathodes from rising above $+40V$ when the circuit is restored to normal. The arrival of these guide waveforms provides suitable conditions to transfer the glow from one cathode to the adjacent cathode, the transfer taking place in the desired direction.

Resetting
Resetting facilities are obtained by the addition of the circuitry shown in Fig. 90. Closing switch S_1 causes a large negative pulse to appear at the cathode, forcing the glow to transfer to that electrode.
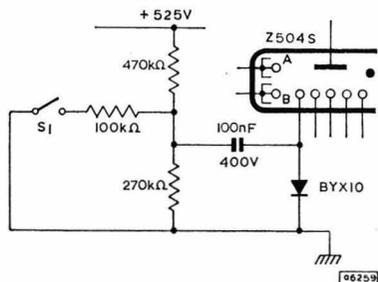
Fig. 90—Additional circuitry for resetting

Coupling Circuits
When decade counting tubes are used in a series chain to give an indication representing two or more significant figures, provision must be made for coupling the output from one counting tube to the input of the next. By means of this coupling circuit, the "units" counter passes a signal after each count of ten to the "tens" counter, and so on. A block schematic diagram of a complete counter is shown in Fig. 91.

The problems posed by the coupling circuits are, to a great extent, similar to those encountered in the drive circuit discussed earlier. From the single pulse on the resistor in the circuit of cathode k_o, two negative pulses have to be generated to drive the guide electrodes of the subsequent counting tube. A circuit capable of performing such a function is shown in Fig. 92.

In this circuit, the BSX21 transistor is normally in the OFF state with a collector potential of 100V defined by the potential divider R_2R_3. When

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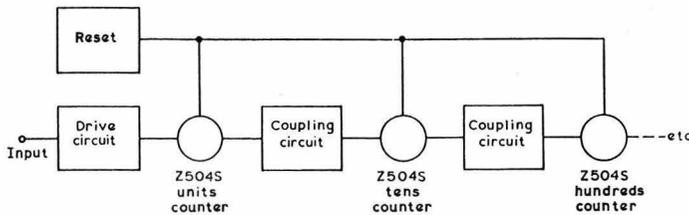
Fig. 91—Block schematic diagram of interstage coupling
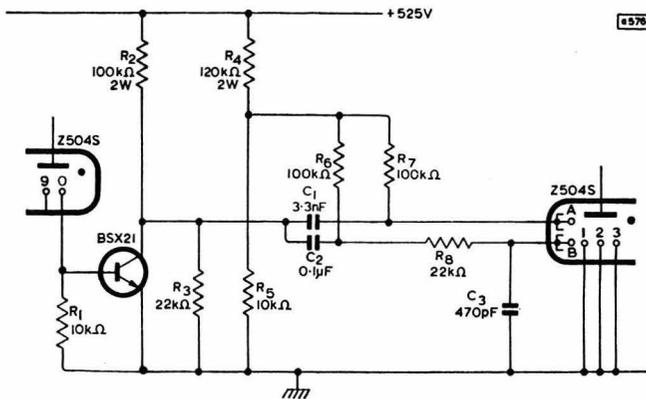
Fig. 92—Coupling circuit using a transistor type BSX21

the discharge of the left-hand stepping tube transfers to the k_o cathode, the current drawn by the electrode passes into the base of the transistor, driving it into saturation. Both guide cathodes are held at $+40V$ by the potential divider R_4, R_5. When the transistor switches into saturation, the change in collector voltage is coupled to the guide-A and B cathodes of the next tube by C_1 and C_2, their potential changing from $+40V$ to $-70V$. The voltage change on the guide-B cathode is delayed on that of the guide-A cathode by the network C_3, R_8, thereby ensuring that the discharge transfers in the forward direction. This is illustrated in Fig. 93. The guide-A cathode returns to $+40V$ controlled by the time-constant C_1R_7. The guide-B cathode returns to $+40V$ on the longer time-constant C_2R_6. This difference in time-constant ensures that the discharge of the guide-A cathode extinguishes before that of the guide-B cathode thereby preventing the discharge from transferring back to the original cathode.

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The discharge transfers to the next cathode as the guide-B voltage rises to a more positive (about +10V) potential than the cathode. When the counter is running at its maximum speed, the discharge transfers from the k_0 electrode before either the guide-A cathode or the guide-B cathode has recovered (see Fig. 93). However, the discharge in the next stepping tube has time to transfer from the guide-A electrode to the guide-B cathode by virtue of the fast recovery of the guide-A potential. Therefore, when the transistor turns off and the guides return very quickly to a positive voltage the discharge is transferred forward to the next cathode.
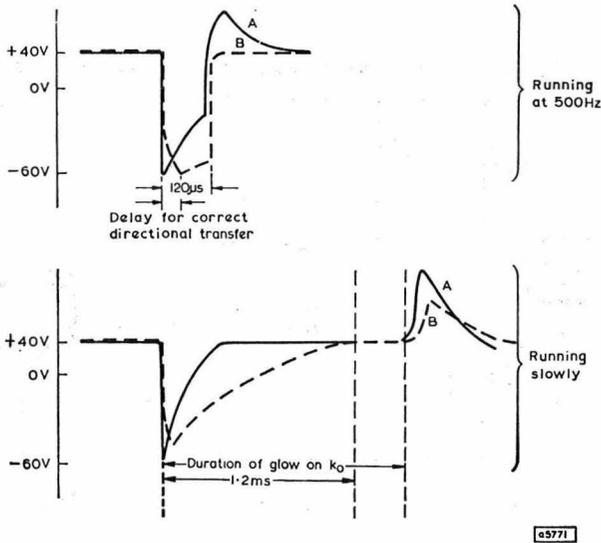
Fig. 93—Voltage waveforms on the guide electrodes for fast and slow running

Sine-wave Drive

For sine-wave drive, the counting tube is connected in a circuit such as that shown in Fig. 94. Rotation of the glow is achieved, as already explained, by the application of suitable negative pulses to the guide-A and guide-B cathodes. The "negative pulses" in the sine-wave drive circuit are the negative half-cycles of two sine-waves with a suitable phase difference. For clockwise rotation, the leading sine-wave is applied to the guide-A cathode, and the lagging sine-wave to the guide-B cathode as shown in Fig. 94.

The input to the drive circuit should be between 40 and 70V, r.m.s., with a maximum frequency of 4kHz. The phase lag for the guide-B

cathodes is obtained by means of a conventional phase-shift circuit, with the value of the capacitor C chosen in accordance with the input frequency as given by the following equation

$$C = \frac{5}{f}$$

where C is in μF and f is in Hz.

Since the circuit depends on a specific phase shift, then once the capacitor value has been chosen for a particular frequency, only very small departures from this frequency can be permitted.

A positive guide bias of 8 to 10V is required with this form of drive, and not the value of 40V which has been recommended in the discussion of tube requirements for pulse operation. The reason for this is that the positive half-cycles of the sine-wave constitute, in effect, a sufficiently large positive guide bias. The bias of 8 to 10V ensures an equal period of rest on all cathodes.
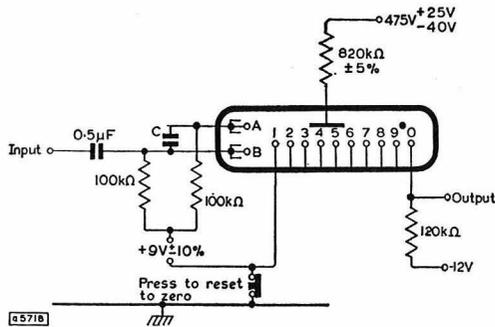
Fig. 94—Sine-wave drive circuit for clockwise rotation

BINARY CODED DECIMAL COUNTERS

The counters discussed in Chapter 6 were of the normal decimal type; that is, they were counters with ten devices per decade—one for each decimal digit. A counter which counts to some number, n-1, and then resets to zero is known as a "modulo-n" counter. The minimum requirement for a modulo-n counter is that it should be a circuit with n discrete, recognisable states, and one of the simplest forms of such circuits consists of several binary stages connected in series, or cascade, to form a binary counter as described in Chapter 5.

A four-stage binary counter has a counting capacity of 16 states, after which it reverts to the first state. If such a counter is prevented, by feedback, from counting more than 9, a binary-coded-decimal (BCD) counter results.

In this chapter, some of the possible methods of gating binary stages to perform the function of counting through 10 states (0 to 9) in 1248, 1245 and 1242 codes are discussed. Both asynchronous and synchronous counters are shown, and circuits for reversible counters are also included.

COUNTERS USING DISCRETE COMPONENTS

Asynchronous Counters

A four-stage binary counter is shown in block form in Fig. 95. The first ten states of the four bistable elements are given in Table 38.
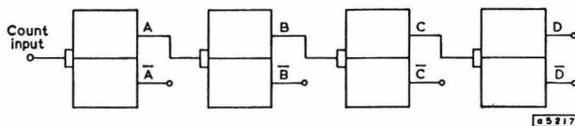

Fig. 95—Four-stage ripple-through asynchronous binary counter

In order to make a BCD counter from the four binary stages, the states corresponding to numbers 10 to 15 (binary 1010 to 1111) must be inhibited and the counter must be made to return from the '9' state to zero. By examination of Table 38, the following deductions can be made.

(1) A changes state at each input pulse.
(2) B changes state each time A changes from '1' to '0' unless D is already present (state 9 to state 0).

(3) C changes state each time B changes from '1' to '0'.
(4) D is reset from '1' to '0' at the next count pulse after A and D are '1' simultaneously; that is, the transition from 9 to 0; D is '0' for all transitions of A from '1' to '0', except in the change from 7 to 8.

TABLE 38
The First Ten States of the Four-bistable Circuit

	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

For a counter to behave according to this truth table, the output of A must be prevented from triggering B (and therefore C) after the eighth input pulse, and the tenth pulse must reset D from '1' to '0'. The basic logic diagram for such a counter is shown in Fig. 96 Gate 1 prevents B from being triggered if $\bar{D}$ is not present (D = '1') and gate 2 steers the output of A to reset D when D = 1.
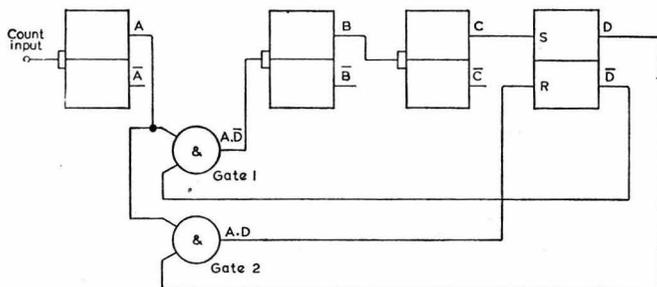

Fig. 96—Ripple-through 1284 BCD counter

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The bistable elements used in Fig. 96 are assumed to change state on a transition from '1' to '0' of the trigger input. That is, if a positive voltage is assumed to represent a logical '1', the bistable element triggers on a negative-going or falling edge. Stage D is used as a Set/Reset bistable element and it, too, is set and reset by negative-going edges.

In practice, the circuit shown in Fig. 96 can be simplified slightly. If every transition of A from '1' to '0' is allowed to set D to the '0' state, then, since D is in the '0' state for numbers 0 to 7, these states would not be disturbed. On the transition from 7 to 8, D is first set to zero, giving a state $\bar{A}.\bar{B}.C.\bar{D}$, then, after a delay due to gate 1, B is triggered, giving the state $\bar{A}.\bar{B}.C.\bar{D}$; and finally, after the delay of the B stage, C is triggered, giving the state $\bar{A}.\bar{B}.\bar{C}.\bar{D}$, and the change in the output of C sets D to 1. The counter therefore reaches the correct state $\bar{A}.\bar{B}.\bar{C}.D$. The next transition of A from '1' to '0' occurs at the tenth input pulse, when resetting
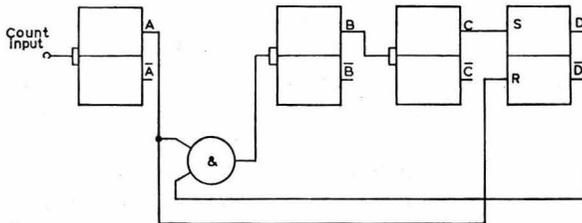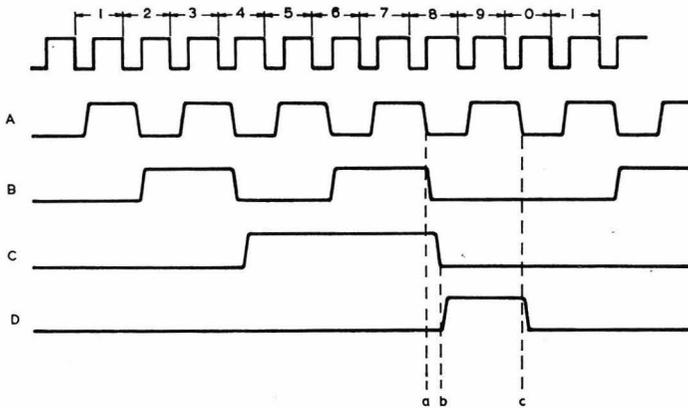
Fig. 97—Block diagram and waveforms of BCD counter using single gate

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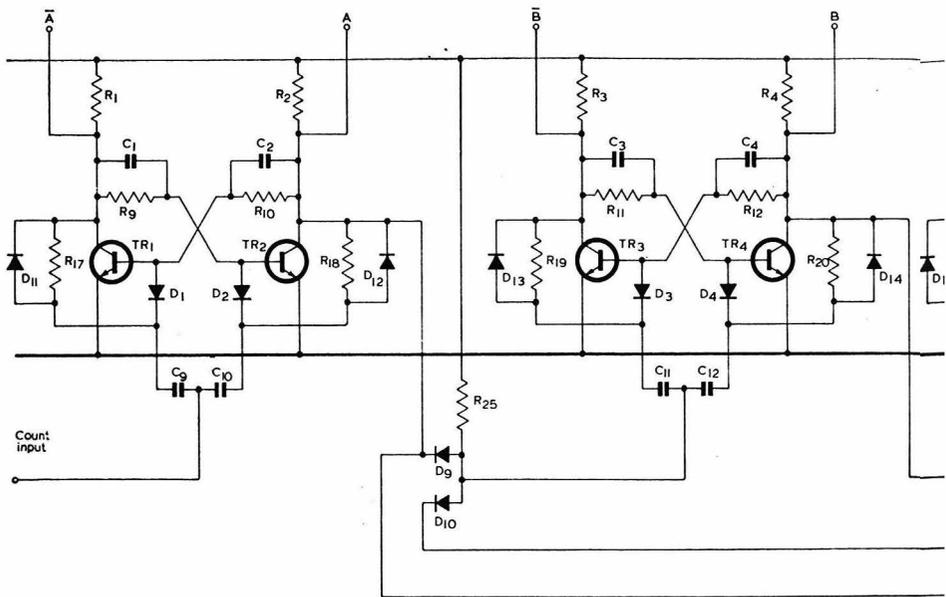
TR₁–TR₈	BC108	BSX19
Supply voltage	12V	6V
D_1–D_{10}	OA91	BAX13
D_{11}–D_{18}	omitted	BAX13
R_1–R_8	3·3kΩ	680Ω
R_9–R_{16}	8·2kΩ	2·2kΩ
R_{17}–R_{24}	6·8kΩ	1·5kΩ
R_{25}	6·8kΩ	1·8kΩ
C_1–C_8	omitted	22pF
C_9–C_{16}	820pF	82pF

Fig. 98—Practical asynchronous BCD counter

D to '0' is required by the truth table. Gate 2 may be omitted if the R and S terminals are a.c. coupled; that is, if stage D is a triggered bistable circuit in which the input is split. The resulting counter circuit and waveforms are shown in Fig. 97. At time 'a', stage D is reset to zero; at time 'b', C sets D; and at time 'c', D is reset directly by A. It will be seen that the 'set' delay for D is much longer than the 'reset' delay.

A practical ripple-though BCD counter using a single gate is shown in Fig. 98. Two versions of the circuit are given, one using the BC108 transistor operating at a maximum counting rate of 100kHz and the other using the BSX19 transistor with a maximum counting rate of at least 10MHz. The performance of this circuit is given in Table 39. Practical bistable circuits using the BSX19 and BSX20 have been made

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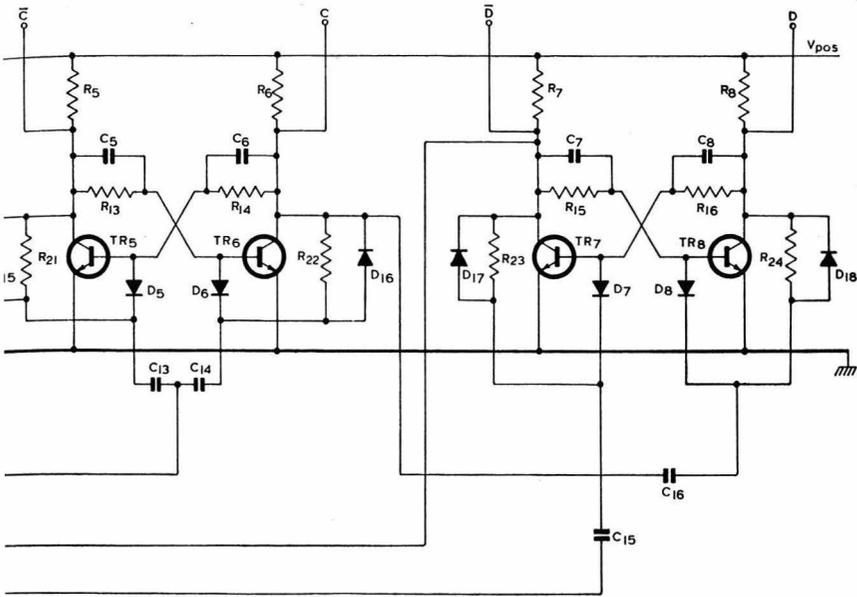
TABLE 39

Operating Conditions for Circuit shown in Fig. 98

	BC108	BSX19
Transistor type	BC108	BSX19
Input pulse requirement		
Amplitude		
maximum	8V	5V
minimum	3V	2·5V
Voltage fall time		
maximum	10μs	75ns
minimum	< 5ns	< 5ns
Max counting rate		
unloaded bistable stage	160kHz*	20MHz
decade counter	100kHz*	> 10MHz
Outputs		
Amplitude	8V	4·5V
Voltage fall time	70ns	15ns
Voltage rise time	100ns†	70ns†

*The addition of OA91 recovery diodes and 39pF speed-up capacitors to the BC108 circuit increases the counting rate to over 1MHz.
†These times depend upon the capacitive loading.

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to operate at frequencies in excess of 30MHz, and decade counting rates of 20MHz can be achieved with careful design and layout.

The ripple-through delay of the B and C stages has a limiting effect on the maximum counting speed of this type of BCD counter. Some improvement is obtained by including a gate which can detect the 7 state, and using its output to set D. The operation of this gate (gate 3 of Fig. 99) is as follows.

If the counter is in the 6 state (binary 0110), then the next input pulse sets stage A to '1', making the state of the counter 0111. The output of gate 3 is now logical '1', which has no effect on D. The eighth input pulse
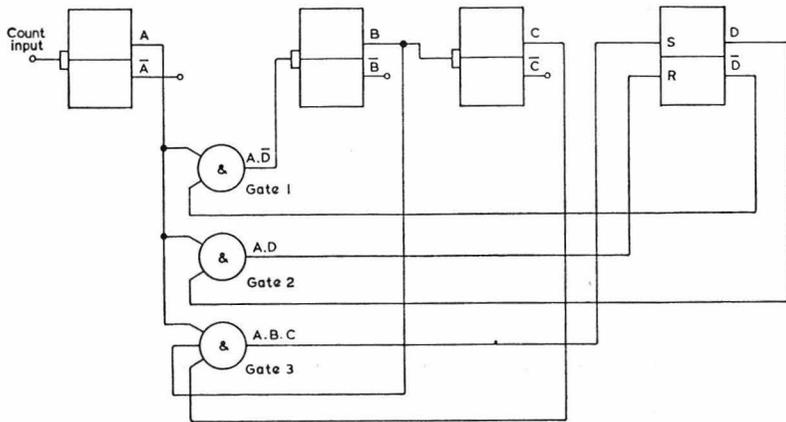
Fig. 99—Semi-synchronous BCD counter
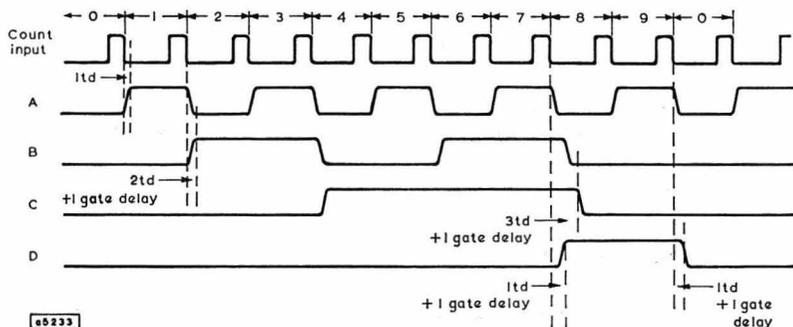
Fig. 100—Waveforms for semi-synchronous BCD counter

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resets stage A to zero, and the output of gates 1 and 3 also falls to the '0' state, setting D to '1' immediately and simultaneously resetting B, thereby making the total state of the counter 1100. This state is only transient, because after the B stage delay, C is reset to give a correct counter state 1000. The ripple-through delays of stages B and C in setting D are therefore eliminated. The waveforms and relative phasing are shown in Fig. 100. Gate 2 is not essential to the operation of the circuit, but the operation of the counter becomes a little more critical if it is removed.

This type of circuit arrangement can give an improvement in counting speed of some 35% over the simple circuit shown in Fig. 98. In a particular example using BSX19 transistors, the counting rate was increased from 16MHz to 22MHz by using the three-gate circuit.

Synchronous Unidirectional BCD Counter

In a synchronous counter, the count, or clock, pulses are fed to all bistable stages at the same time, and gates are employed to determine which stages will respond to the count input pulses according to the overall state of the counter. From the 1248 code shown in Table 40 the triggering requirements for each of the bistable stages may be determined.

TABLE 40

Truth Table for 1248 Code

	D	C	B	A
Weights	8	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Examination of the truth table shown in Table 40 reveals the following:

(1) A changes state at each input pulse.

(2) B sets to '1' following conditions A.B̄.C̄.D̄ or A.B̄.C.D̄. This may be reduced to A.B̄.D̄.

(3) B resets to '0' following condition A.B.C̄.D̄ or A.B.C.D̄. This may be reduced to A.B.D̄, but since A.B.C.D and A.B.C̄.D never appear, it may be further reduced to A.B.

(4) C sets to '1' following condition A.B.C̄.D̄, but since A.B.C̄.D never appears this may be reduced to A.B.C̄.

(5) C resets to '0' following condition A.B.C.D̄, but since A.B.C.D never appears, this may be reduced to A.B.C.

(6) D sets to '1' following condition A.B̄.C̄.D̄, but since A.B.C.D never appears, this may be reduced to A.B.C.

(7) D resets to '0' following condition A.B̄.C̄.D, but this may be reduced to A.D, since this is the only time when A and D appear together in the truth table.

In a practical circuit of a clocked R-S bistable element, a logical '0' on the S or R inputs is an 'enable' signal. Thus, what is really required on the set B terminal, for example, is $\overline{A.B̄.D̄}$. This is conveniently achieved by using NAND gates rather than AND gates. The logic diagram of such counter is shown in Fig. 101. The A stage in this counter is a normal triggered bistable circuit with internal steering. The remainder of the stages are clocked R-S bistable elements. A typical circuit of such an element, together with the NAND gates required for setting the SQ and RQ̄ terminals, is shown in Fig. 102. The truth table for a clocked R-S bistable element after each count pulse (that is, after each negative-going edge) is shown in Table 41.
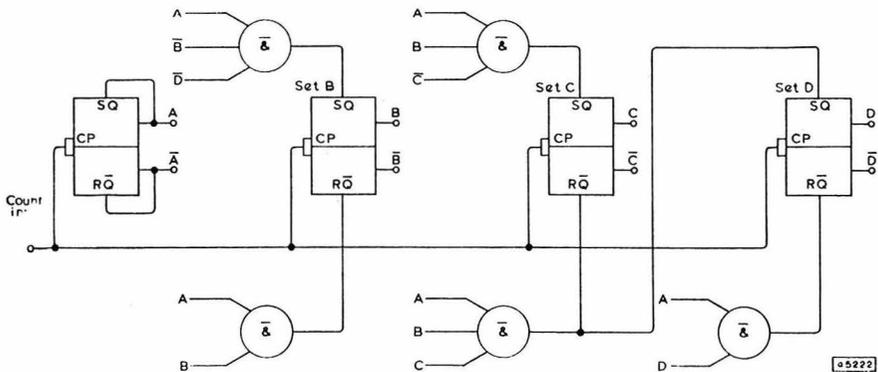

Fig. 101—Synchronous 1248 BCD counter using clocked R-S bistable elements

Fig. 102—Clocked R-S bistable element with NAND gates

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TABLE 41

Truth Table for Clocked R-S Bistable Element

SQ	RQ̄	$Q_{(n+1)}$	$\bar{Q}_{(n+1)}$
0	0	not defined	
0	1	1	0
1	0	0	1
1 -	1	Q_n	$\bar{Q}_n$ (no change)

Asynchronous 1242 BCD Counter

By means of different gating between stages, a counter may be made to operate in a code where the bistable stages have weights of 1, 2, 4, 2 respectively. The truth table of such a counter is shown in Table 42. The circuit for a counter of this type is given in Fig. 103. The OR gate 4 could be dispensed with by feeding the outputs of gates 2 and 3 into the capacitive set and reset terminals of stage D as shown in Figs. 96, 97 and 98.

An alternative truth table for a 1242 code is shown in Table 43. The circuit of a counter which counts according to this truth table is given in Fig. 104. This counter uses standard triggered bistable circuits and the feedback path is connected directly to the bases of the transistors associated with the $\bar{Q}$ outputs of stages B and C. The type of counter shown
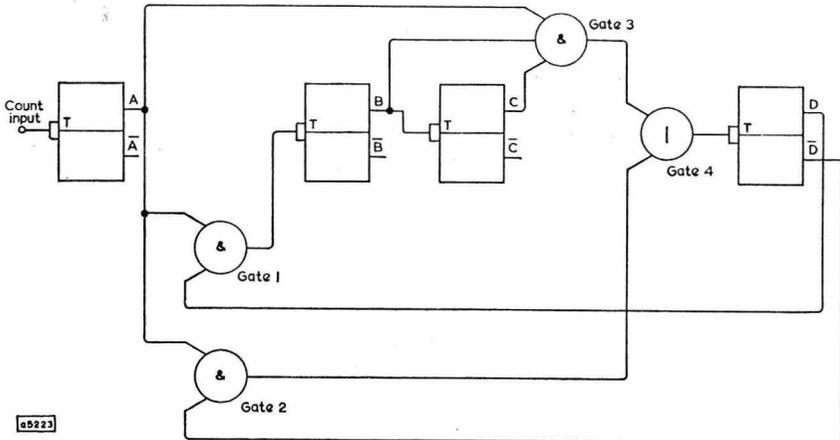
Fig. 103—One form of 1242 BCD counter

TABLE 42
Truth Table of 1242 BCD Counter

Weights	D 2	C 4	B 2	A 1
0	0	0	0	0
1	0	0	0	1
2	1	0	0	0
3	1	0	0	1
4	1	0	1	0
5	1	0	1	1
6	1	1	0	0
7	1	1	0	1
8	1	1	1	0
9	1	1	1	1

in Fig. 104 has speed limitations, largely due to the transient state which exists in the B and C bistable stages during the transition from 7 to 8. For the same types of device, this counter is about 50% slower than a 1248 BCD counter such as that shown in Fig. 97.

Yet another version of the 1242 code is known as the symmetrical, or Aiken code. This code is discussed later in this chapter.

TABLE 43
Alternative Truth Table for 1242 BCD Counter

Weight	D 2	C 4	B 2	A 1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	1	1	0
9	1	1	1	1

H
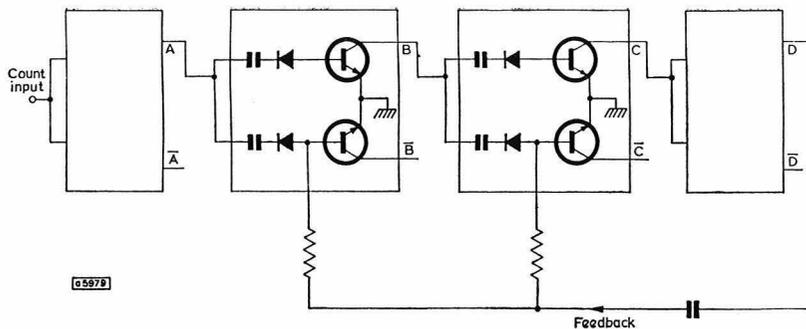
Fig. 104—Asynchronous 1242 BCD counter with feedback

1248 BCD Down Counter

With normal steered bistable elements, a change of input from a logical '1' to a logical '0' is required to produce trigger action. In a down counter, the truth table of which is given in Table 44, the reverse is required, and this is achieved by using the inverted outputs of the counting bistable elements. From the truth table the following deductions can be made.

(1) A changes state at each input pulse.
(2) B changes state when A changes from '0' to '1' except when B, C and D are all absent.

TABLE 44
Truth Table for 1248 BCD Down Counter

Weights	D 8	C 4	B 2	A 1
0	0	0	0	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1

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(3) C changes state when B changes from '0' to '1'.

(4) D sets after the 0000 state and resets when A next changes from '0' to '1'.

The circuit of a 1248 BCD down counter is shown in Fig. 105.
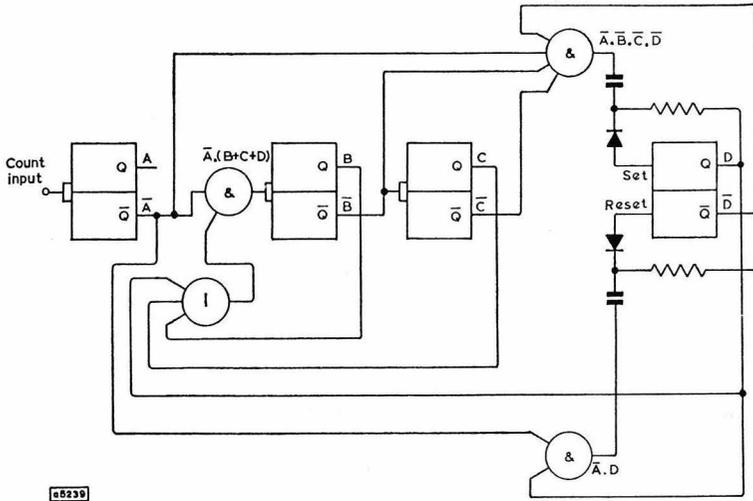
Fig. 105—Asynchronous 1248 BCD down counter

INTEGRATED CIRCUIT COUNTERS

As has been explained earlier in this book, the advent of integrated circuits has made possible the production of complex circuits such as the J-K bistable element. The use of these elements greatly simplifies the design of counting circuits. J-K bistable elements are included in most ranges of integrated circuits such as the OMY, FC and FJ ranges. The differences between these ranges are in the encapsulation, and in the number of J and K inputs. The OMY range is supplied in TO-5 envelopes while the FC and FJ ranges are supplied in flat-packs and dual-in-line packs.

The J-K bistable circuit in the OMY range has only one J and one K input, whereas that in the FC range has three J and three K inputs. Each of the groups of three inputs performs an AND function. The FJ range contains single J-K bistable elements with multiple inputs as well as a dual J-K element with single inputs.

The truth table for a J-K bistable element has been given in Chapter 3, but it is repeated in Table 45 for convenience. This table shows the states after the action of a clock pulse.

111

TABLE 45
Truth Table for J-K Bistable Element

J	K	Q_{n+1} (pin 10)	$\bar{Q}_{n+1}$ (pin 5)
0	0	Q_n	$\bar{Q}_n$
0	1	0	1
1	0	1	0
1	1	$\bar{Q}_n$	Q_n

The pin numbers given refer to the FCJ101 and FCJ102.

From the truth table it can be seen that, if a logical '0' exists at and K inputs, the clock pulse cannot affect the state of the bis element.

Asynchronous 1248 BCD Counter using J-K Bistable Elements

The circuit for an asynchronous 1248 BCD counter using J-K bis elements is shown in Fig. 106. The operating characteristics of this c when circuits of the FC range are used are given in Table 46, an waveforms in Fig. 107. This type of circuit can be built using J-K bis elements with single J and K inputs and replacing the AND gate by a 1 gate plus an inverter.
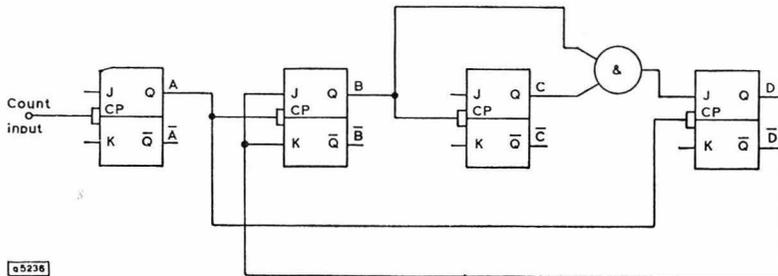
Fig. 106—Asynchronous up counter using J-K bistable elements in 1248 code with feed-forward

TABLE 46
Operating Conditions for Circuit shown in Fig. 106
Bistable elements of the FC range

Maximum operating frequency	$\geqslant$ 10MHz
Supply voltage	$= +6V$
Drive pulse amplitude:	
minimum	$= +2 \cdot 2V$
nominal	$= +4V$
maximum	$= +7V$
Maximum drive pulse fall time ($V_{in} = 4V$, $f = 1MHz$)	$= 100ns$

112

Fig. 107—Waveforms for 1248 BCD asynchronous counter

The FCJ101 and FCJ102 J-K bistable elements have a three-input AND facility on both the J and the K inputs. It is possible to use this unit in a synchronous BCD decade counter, thereby making use of its speed capability without introducing ambiguous states during transitions.

Synchronous 1248 BCD Counter using J-K Bistable Elements
The requirements for the J and K inputs to provide set and reset signals in accordance with the 1248 truth table (Table 40) are deduced in a similar way to the synchronous clocked R-S bistable circuit counter. A synchronous 1248 BCD counter using J-K bistable elements is shown in Fig. 108, and its operating conditions when circuits of the FC range are used are given in Table 47.
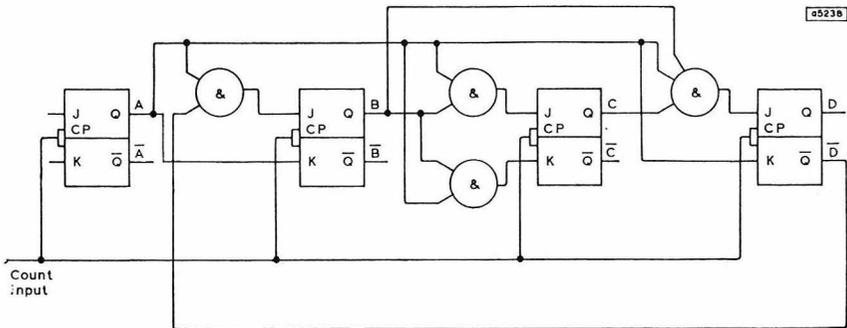
Fig. 108—Synchronous 1248 BCD counter using J-K bistable elements

113

TABLE 47
Operating Conditions for Circuit shown in Fig. 108
Bistable elements of the FC range

Maximum operating frequency	$\geqslant$ 10MHz
Supply voltage	= +6V
Drive pulse amplitude:	
minimum	= +2·2V
nominal	= +4V
maximum	= +7V
Maximum drive pulse fall time (V_{in} = 4V, f = 1MHz)	= 100ns

Synchronous 1242 BCD Counter using J-K Bistable Elements

The truth table of a possible 1242 BCD code is given in Table 48.

TABLE 48
Truth Table of a 1242 BCD Code

	D	C	B	A
Weights	2	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	1	1	0
9	1	1	1	1

Examination of this table enables the following deductions to be made.

(1) A changes state at each input pulse.

(2) B sets to '1' following condition A.$\bar{B}$.$\bar{C}$.$\bar{D}$ and following condition A.$\bar{B}$.C.$\bar{D}$. The J input therefore requires to be fed with A.$\bar{D}$ because $\bar{B}$ is connected to J internally and the condition of C is immaterial.

(3) B resets to '0' following condition A.B.$\bar{C}$.$\bar{D}$ or A.B.C.D. The K input therefore requires to be fed with A.$\bar{C}$.$\bar{D}$+A.C.D.

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(4) C sets to '1' following condition A.B. This is true in states 4 and 8.

(5) The J input may be fed with A.B, setting C after states 3 and 7, and if K is fed with A.B.D, both J and K are '1' in state 9 and the stage changes to the '0' state.

(6) D sets to '1' and resets to '0' following condition A.B.C. The J and K inputs therefore both require to be fed with A.B.C.

A schematic diagram of a synchronous 1242 BCD counter using the FC range of integrated circuits is shown in Fig. 109.

Synchronous Symmetrical 1242 BCD Counter

A symmetrical, or Aiken, code is one in which, if every '1' is replaced by '0' and every '0' by '1', in any state, the nines complement is obtained. The nines complement of a number, n, is $9-n$. For example, the nines complement of 7 is 2. The truth table for a symmetrical 1242 code is given in Table 49, and from this table it can be seen that 7 is represented by 1101, the complement of which is 0010 which represents 2, the nines complement of 7. This type of code is useful for subtraction since, in a counter using this code, the nines complement is always available from the $\bar{Q}$ outputs. It is called symmetrical because it is symmetrical by complements about the line shown in Table 49. A counter operating in this code is shown in Fig. 110.

TABLE 49
Truth Table for a Symmetrical 1242 BCD Code

	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	1	0	1	1
6	1	1	0	0
7	1	1	0	1
8	1	1	1	0
9	1	1	1	1

115
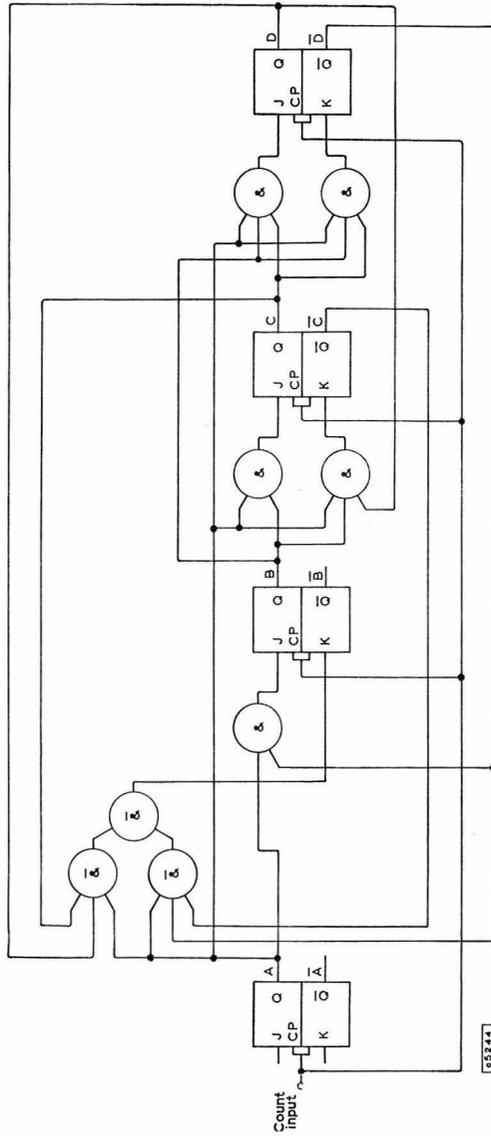
Fig. 109—Synchronous 1242 BCD counter

116
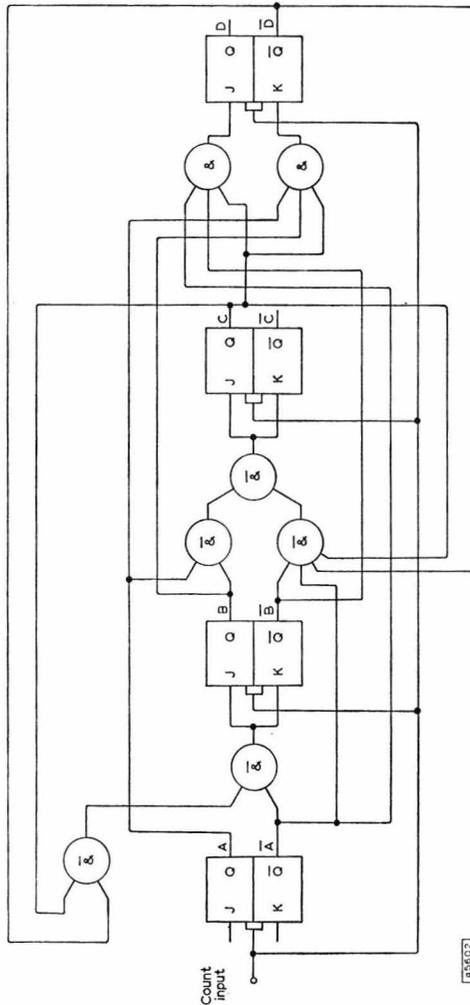
Fig. 110—Synchronous symmetrical 1242 code counter

Count
input

a5602

117

Integrated Circuit BCD Down Counter

A circuit similar to that shown in Fig. 105 can be made using J-K bistable elements, but the advantages of these elements are best realised in synchronous counters. Examination in more detail of the setting and resetting requirements of the four stages in Table 44 allows the following deductions to be made.

(1) A changes state at each input pulse.

(2) B sets to '1' following conditions $\bar{A}.\bar{B}.\bar{C}.D$ or $\bar{A}.\bar{B}.C.\bar{D}$. The J input therefore requires to be fed with $\bar{A}.\bar{C}.D$ or $\bar{A}.C.\bar{D}$ because $\bar{B}$ is connected to J internally.

(3) B resets to '0' following condition $\bar{A}.B.C.\bar{D}$ or $\bar{A}.B.\bar{C}.\bar{D}$. This can be achieved by feeding the K terminal with $\bar{A}.\bar{D}$, since in the state 0100 (4) both J and K inputs have a logical '1' input. As B is already in the '0' state, it will change to the opposite state as required to produce 0011 (3). This argument can be extended to provide a further simplification by feeding K with $\bar{A}$ and J with $\bar{A}.D+\bar{A}.C$.

(4) C sets to '1' following condition $\bar{A}.\bar{B}.\bar{C}.D$. The J input therefore requires to be fed with $\bar{A}.\bar{B}.D$ because $\bar{C}$ is connected to J internally

(5) C resets to '0' following condition $\bar{A}.\bar{B}.C.\bar{D}$. The K input therefore requires to be fed with $\bar{A}.\bar{B}$. The reasoning here is similar to that in (3) above.

(6) D changes state following condition $\bar{A}.\bar{B}.\bar{C}$. If both J and K inputs are fed with this function, the required operation is achieved.

A schematic diagram of a BCD down counter is shown in Fig. 111. If bistable elements of the FC range are used, the counter operates at a frequency of 10MHz. In this counter, the required function for setting B is achieved by using one NAND gate in conjunction with the internal AND gate of the J-K bistable element.

Reversible Asynchronous BCD Counter

A reversible BCD counter is made by combining the counters of Figs. 97 and 105.

All the transfer signal paths must be fed between stages via gates controlled by up or down command signals. Fig. 112 shows a possible method of achieving a reversible counter of the ripple-through type. When the up control line is positive and the down line is zero, the counter counts up. With the down line positive or open-circuit, and the up line at zero potential, all up gates are closed and the counter counts down.

This type of counter has restrictions on the rate of change of voltage applied to the up and down control lines if capacitively steered bistable
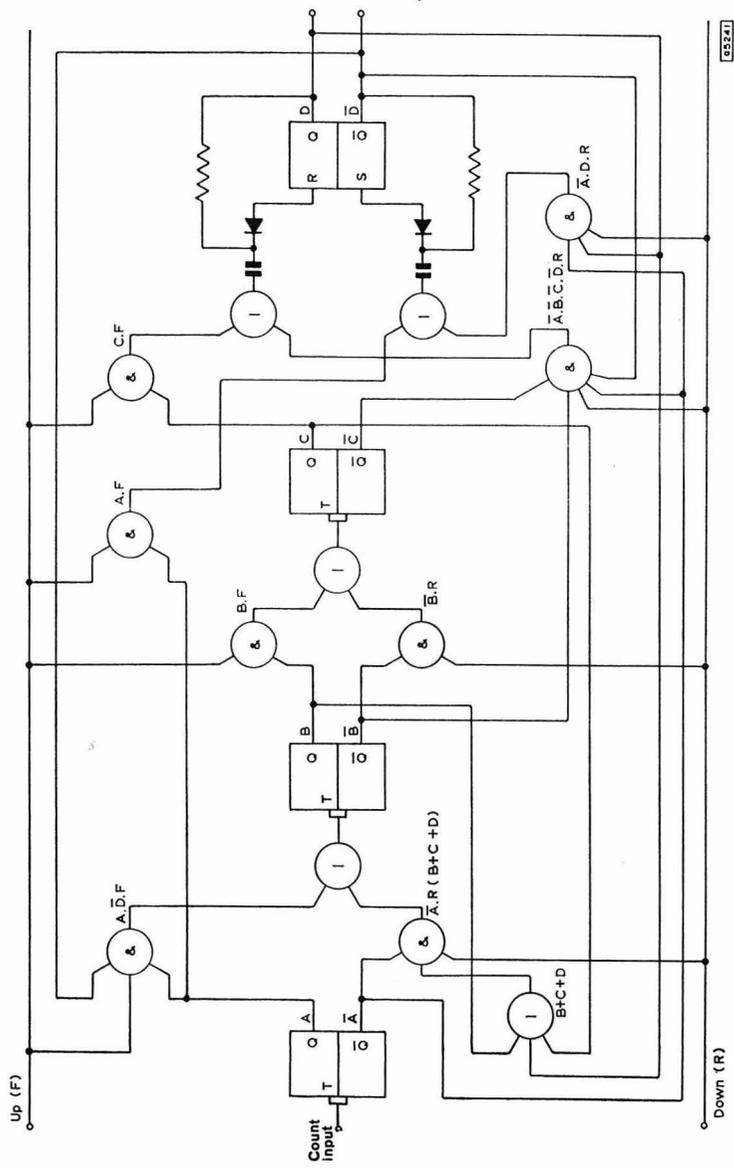
Fig. 111—Synchronous 1248 BCD down counter

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Fig. 112—Reversible asynchronous 1248 BCD counter

120

Fig. 113—Practical reversible asynchronous BCD counter
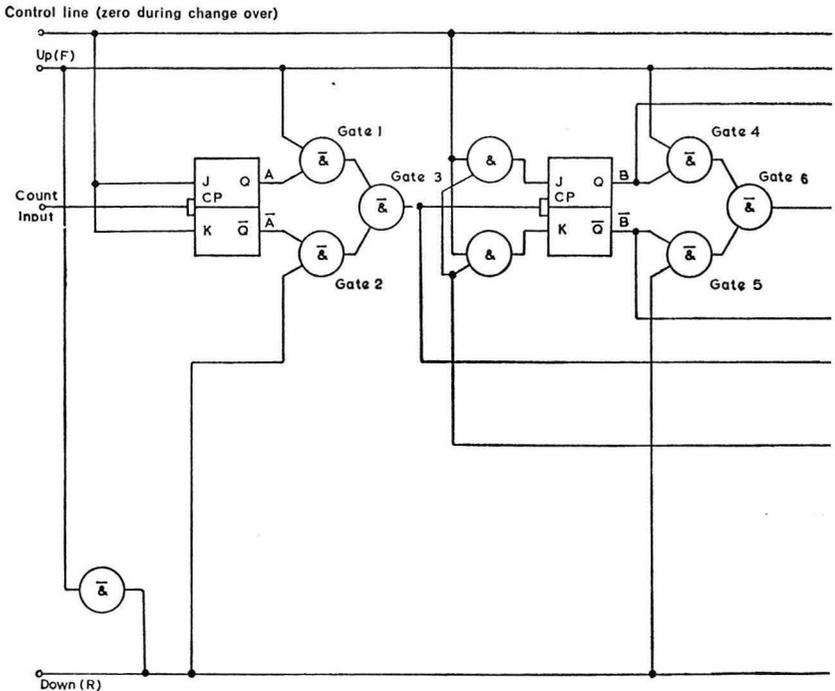
F = Forward
R = Reverse

121

Fig. 114—Asynchronous reversible 1248 BCD

circuits are used. Before changing from up to down, the counter should be stationary, and the rate of change of voltage on the control lines must be low enough not to produce a triggering effect in any of the counting stages. If this is not done, count information will be lost.

A practical realisation of the counter shown in Fig. 112, is shown in Fig. 113. In this circuit, stages A, B and C are triggered bistable circuits and stage D is an R-S bistable circuit which is triggered by a negative-going edge via capacitive inputs.

Asynchronous BCD Reversible Counters using J-K Bistable Elements

A similar arrangement to Fig. 112 can be made with J-K bistable elements but by adding an extra control line to the J and K inputs, the restrictions on reversing the counter are eliminated. During the change of state from up to down or vice-versa, the J and K inputs connected to the control line are held at zero, thereby preventing a change of state in

122
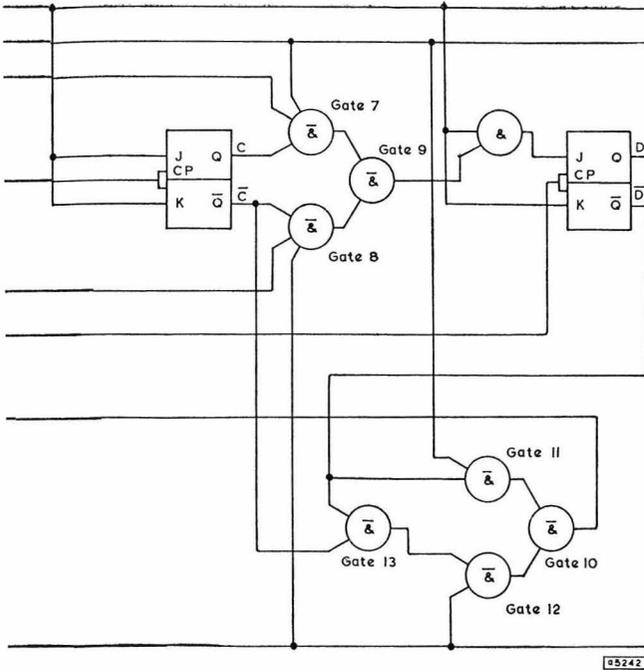
decade counter using J-K bistable elements

any of the bistable elements until the next count pulse arrives. Changes from up to down or vice-versa should not be made during the existence of a count pulse, but only between count pulses. An asynchronous BCD reversible counter is shown in Fig. 114. The counting rate when bistable elements of the FC range are used is in excess of 10MHz.

The operation of the counter is as follows. If the counter is in the 0000 state and the up and down lines are positive and zero respectively, gates 2, 5, 8 and 12 are closed and the clock terminals of all four bistable elements are at zero potential. The first clock pulse changes A only (0001). Gate 1 is now open (two positive inputs and therefore zero output) and the output of gate 3 is positive. The next clock pulse resets A. The clock input to B is restored to zero and B changes state (0010). At the same time, the clock input to D is restored to zero, but since the output of gate 9 is zero, stage D remains in the '0' state. Gates 4 and 6 now make the clock input of stage C positive. The third clock pulse sets A (0011), opening gate 3

123
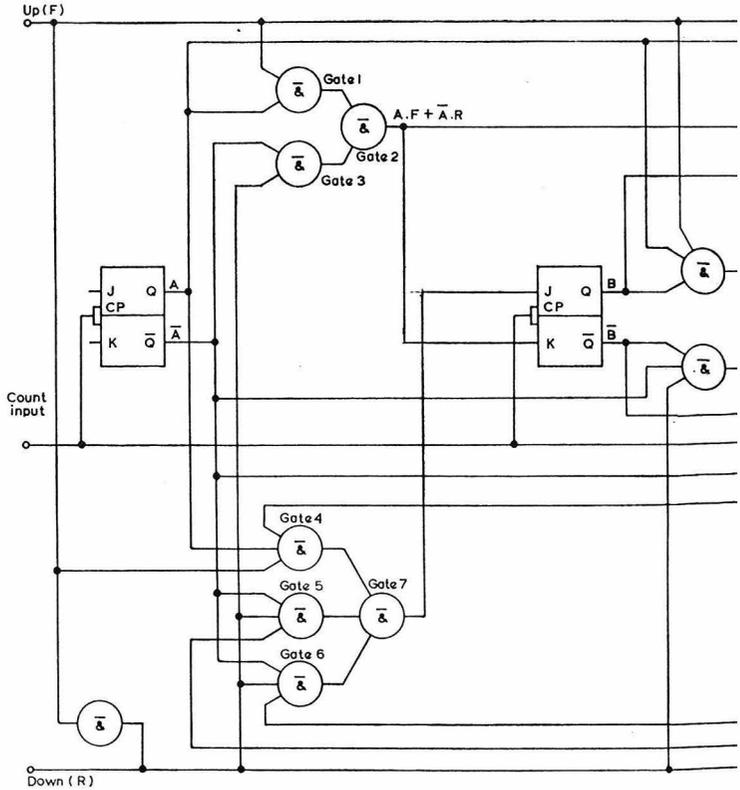
Fig. 115—Synchronous reversible 1248 BCD

again but having no effect on the other stages. The fourth pulse resets A, thereby resetting B. Gate 4 is now closed and the clock input to C is restored to zero, changing C from '0' to '1' (0100).

This process continues until the state 0110 is reached. The next count pulse sets A, making the state of the counter 0111. The clock inputs of B and C are now positive as is the J terminal of D. The output of gate 10 is positive because both inputs to gate 11 are positive, and therefore the J and K inputs of B are positive.

The J and K terminals of D are also positive, and this means that all the stages are primed. The eighth input pulse resets A, causing the clock input to be restored to zero, thereby resetting B. This, in turn, resets C. At the same time, the fall in the output of gate 3 sets D. The counter state is now 1000. The ninth pulse sets A only, making the counter state 1001.

124
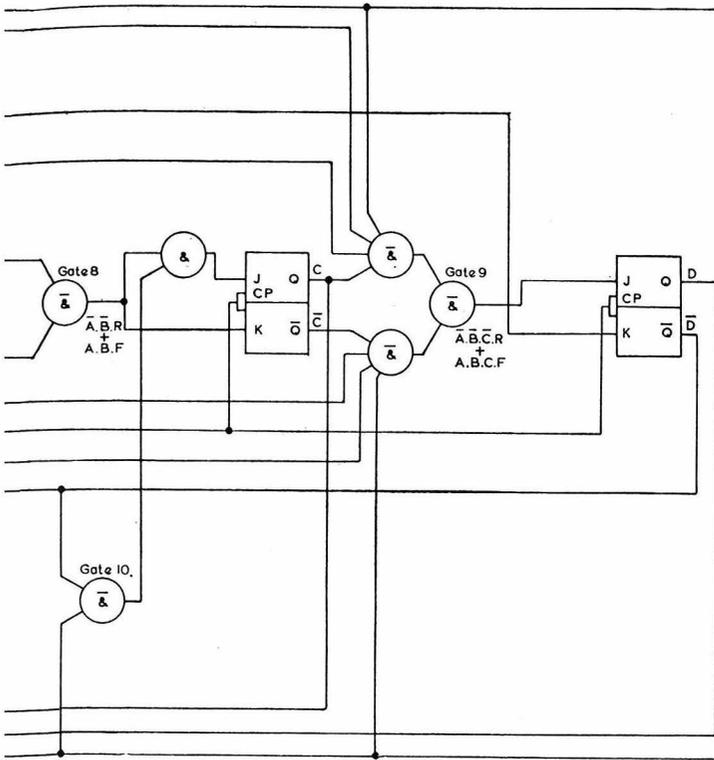
counter using J-K bistable elements

Gate 9 maintains the J terminal of D at zero potential, and the next input pulse, which causes A to reset and therefore to pass a negative edge to the clock input of D, resets D to '0'. The counter is thus reset to 0000.

The sequence of counting in reverse is governed by gates 2, 3, 5, 6, 8, 9, 10, 12 and 13. If the counter is in the 0000 state and the up and down lines are zero and positive respectively, the clock inputs of the B, C and D stages are positive. The J and K terminals of B are, however, kept at zero by gates 10, 11 and 12. The first input pulse therefore sets the A stage. The Ā output therefore becomes '0' and this sets D. The output of gate 13 is now positive, and therefore the J and K inputs of B are both positive. The next input pulse sets the A stage causing the Ā output to become '0', and to trigger B via gate 3. The B̂ output is restored to '0' and triggers the C stage. The counter state is now 0111. Gate 9 is now closed and the

125

I

counter operates as a normal binary down counter until the state 0000 is reached again. The counting rate of this type of counter, when FCJ101 or FCJ102 devices are used, is in excess of 10MHz.

Synchronous Reversible Counter

The synchronous counter shown in Fig. 115 makes full use of the counting speed of J-K bistable elements. It is only slightly more complex than the asynchronous reversible counter, in that it requires two extra gates. The counter is a combination of the synchronous up counter and the synchronous down counter previously described. When devices of the FC range are used, the spare J and K terminals may be connected in pairs to a common control line (not shown) which is at zero when a change from forward to reverse or vice-versa is made. That is, pins 4 and 13 of each element may be connected together to such a common control line. This ensures that the information held in the counter cannot be changed as a result of a change in the direction of count.

Coupling between Decades

Coupling between successive decades may be synchronous or asynchronous. Asynchronous coupling is illustrated in Fig. 116. In a ripple-through 1248 BCD counter of, say, six decades, a maximum ripple-through delay of 14 stage delays can occur (the change from 799 999 to 800 000). If the contents of the counter are sampled during the counting process, ambiguities can occur in the output.
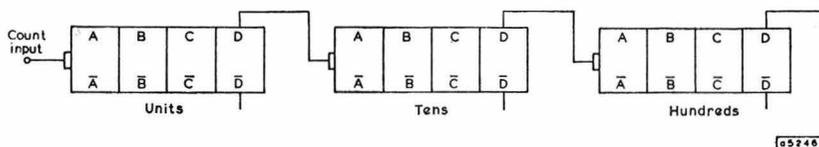
Fig. 116—Asynchronous coupling between decades

If, for example, a single asynchronous decade is to change from 7 to 8, the following sequence occurs.

(a) 0111
(b) 0110
(c) 0100
(d) 1000

Thus, if the counter were sampled at time (c), the contents would appear to be 4, not 7 nor 8.

Similarly, with decades cascaded in series, if ripple-through carry is

126
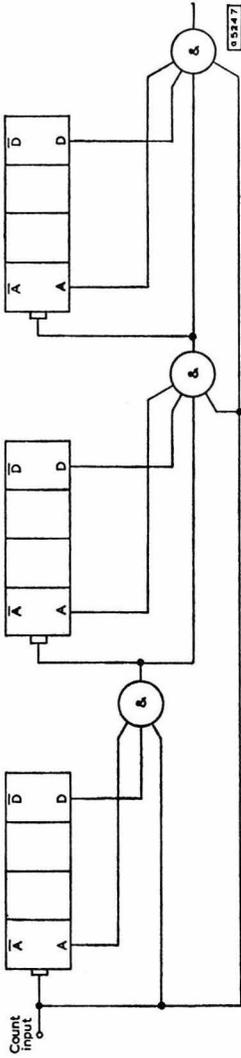
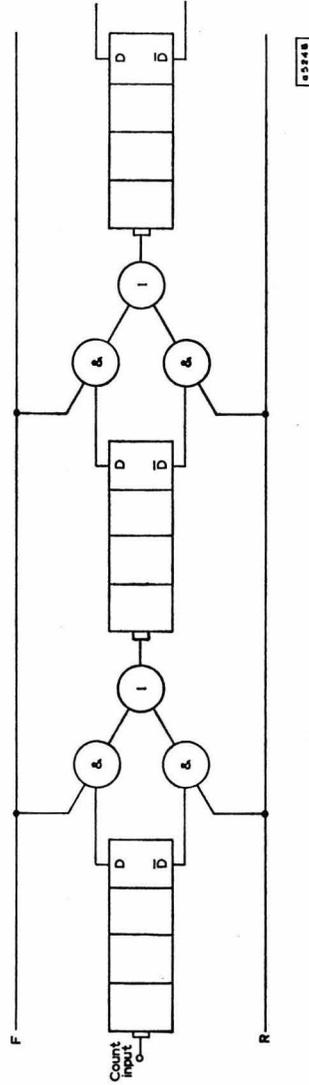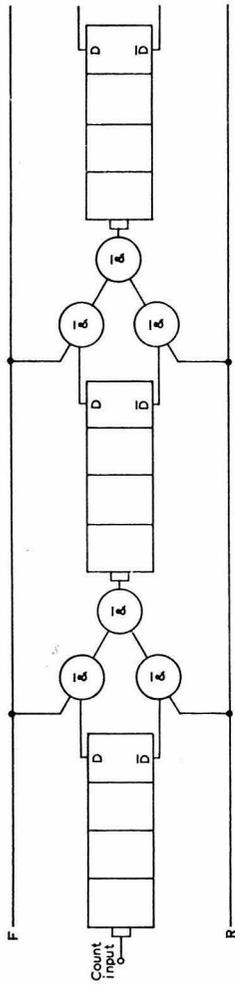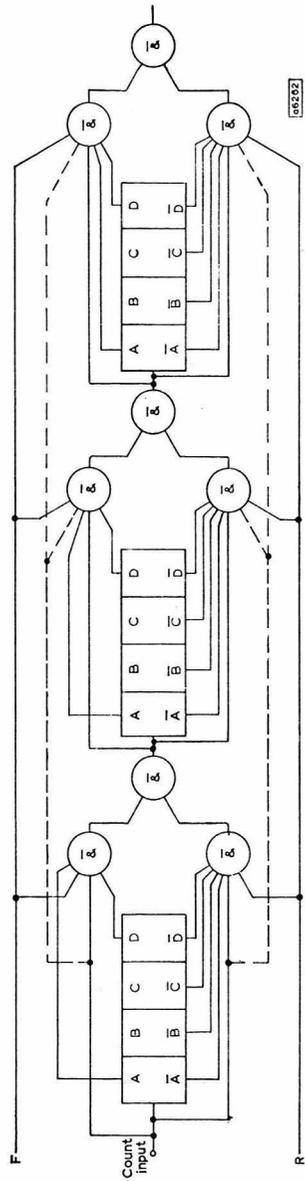Fig. 117—Synchronous coupling between decades operating in 1248 BCD

Fig. 118—Asynchronous coupling between reversible decades

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Fig. 119—Alternative asynchronous coupling between reversible decades

Fig. 120—Coupling between reversible synchronous decades operating in 1248 BCD

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used, ambiguities can occur. For example, in a four-decade counter changing from 0999 to 1000 the sequence is:

(a) 0999
(b) 0990
(c) 0900
(d) 1000

In some applications, this effect is of no importance, particularly if the counter is stationary when a readout is taken. However, in other cases, these ambiguities cannot be tolerated and a synchronous carry between decades is necessary. This is achieved by means of AND gates as shown in Fig. 117. For reversible counters, the asynchronous carry is achieved as shown in Fig. 118. The rate of change of voltage applied to the forward and reverse lines must be low enough to ensure that the trigger inputs of the bistable elements do not respond to them. Alternatively, in counters using integrated circuits, a coupling using NAND gates as shown in Fig. 119 is useful, giving the same logical functions as shown in Fig. 118. Precautions must be taken to ensure that when this form of coupling is used, the counter cannot respond to input pulses which appear as a result of a change in the direction of count. One method of achieving this is to connect the spare J and K terminals to a common control line as described earlier in this chapter under the heading "Synchronous Reversible Counter". Synchronous coupling between synchronous decades is shown in Fig. 120. If the connections shown with broken lines in Fig. 120 are omitted, the coupling still operates, but a delay of two gate delays per decade is introduced into the carry.

COUNTERS USING LESS COMMON CODES

The counting codes discussed in previous chapters, although suitable for most applications, are not suitable for all. Some practical problems demand solution by the use of less common codes. In this chapter several counters using less common codes are considered.

EXAMPLES OF LESS-COMMON WEIGHTED CODES

Sometimes, system economies can be effected by the use of an unconventional code. Two examples of such codes are 1245 BCD and $148-2$ code. A synchronous 1245 BCD counter is shown in Fig. 121 and its truth table is shown in Table 50. An asynchronous $148-2$ code counter is shown in Fig. 122 and its truth table is shown in Table 51. This is interesting because it illustrates the use of a negative weight.
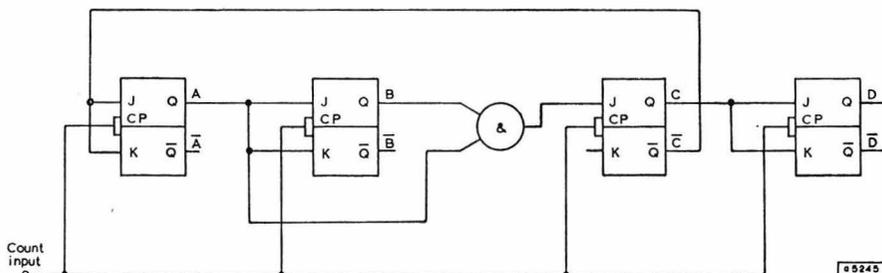
Fig. 121—Synchronous 1245 BCD counter
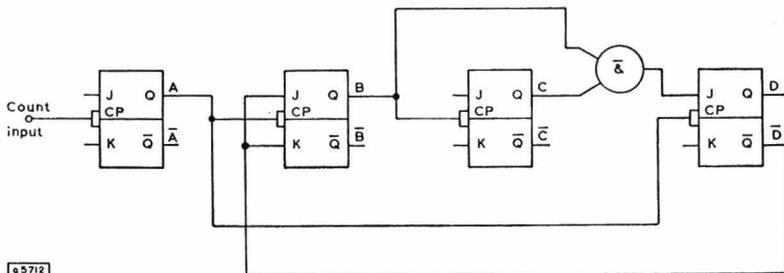
Fig. 122—Counter with weights of 1, 4, 8 and −2

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TABLE 50
Truth Table for 1245 BCD Counter

Weights	D 5	C 4	B 2	A 1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	1	0	0	0
6	1	0	0	1
7	1	0	1	0
8	1	0	1	1
9	1	1	0	0

TABLE 51
Truth Table for 148−2 Code Counter

Weights	D −2	C 8	B 4	A 1
0	0	0	0	0
1	0	0	0	1
2	1	0	1	0
3	1	0	1	1
4	0	0	1	0
5	0	0	1	1
6	1	1	0	0
7	1	1	0	1
8	0	1	0	0
9	0	1	0	1
10	1	1	1	0
11	1	1	1	1

TWISTED-RING COUNTERS

A twisted-ring, or Johnson, counter is similar to a ring counter, such as those discussed in Chapter 6, except that one interstage coupling is reversed, as shown in Fig. 123. A twisted-ring counter has the advantage of needing fewer elements than a ring counter but has the disadvantage that the output requires decoding. The truth table for such a counter is given in Table 52. The truth table is for a counter using five elements, because this gives a cycle length of ten and may therefore be used as a decade counter.

Twisted-ring counters constructed from discrete components and from integrated circuits are shown in Figs. 123 and 124 respectively. The performances of both versions are given in Tables 53 and 54. One unit of the twisted-ring counter, giving details of the R-S bistable element, is shown in Fig. 125 and the performance is given in Table 54. If a somewhat lower counting speed is acceptable, a more economic solution ie obtained by omitting the speed-up diodes D_3 and D_4. The performancs remains identical except that the maximum frequency is limited to 4MHz
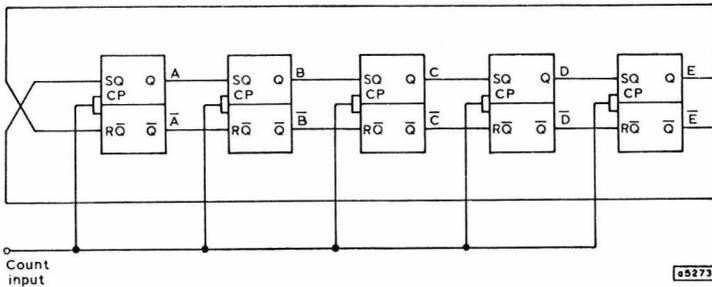
Fig. 123—Schematic diagram of a twisted-ring counter
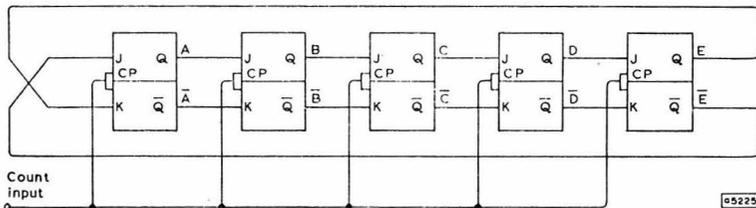
Fig. 124—Twisted-ring counter using J-K bistable elements

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TABLE 52
Truth Table for Twisted-Ring, or Johnson, Counter

	A	B	C	D	E
0	0	0	0	0	0
1	1	0	0	0	0
2	1	1	0	0	0
3	1	1	1	0	0
4	1	1	1	1	0
5	1	1	1	1	1
6	0	1	1	1	1
7	0	0	1	1	1
8	0	0	0	1	1
9	0	0	0	0	1
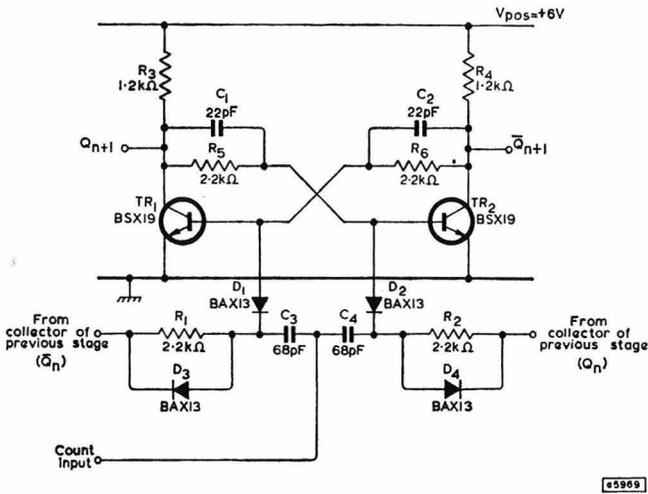
Fig. 125—Clocked R-S bistable element for use in twisted-ring counters

Coupling between Decades

Coupling between decades can be effected by using the output of stage E as the count input to the next decade. If true synchronous coupling is required, however, the function $\bar{D}$ AND E AND Count Pulse must be generated and fed as the count input to the next decade.

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TABLE 53

Performance of Twisted-Ring Counter using Integrated J-K Bistable Circuits of the FC Range

Maximum operating frequency	$\geqslant$ 10MHz
Supply voltage	= 6V
Drive pulse	
amplitude:	
minimum	= 2·2V
nominal	= 4V
maximum	= 7V
maximum rise time at 1MHz	= 100ns
maximum fall time at 1MHz	= 100ns

TABLE 54

Performance of Twisted-Ring Counter using Discrete Components

Maximum operating frequency	= 20MHz
Supply voltage	= 6V
Drive pulse	
amplitude:	
minimum	= 2V
nominal	= 4V
maximum	= 6V
maximum rise time at 1MHz	= 50ns
maximum fall time at 1MHz	= 50ns
duration	> 25ns

CYCLIC PROGRESSIVE (GRAY CODE) COUNTER

One of the disadvantages of the BCD codes discussed in Chapter 7 is that, in changing from one number to the next, it is sometimes necessary to change more than one bit. For example, in changing from 7 to 8 in the 1248BCD code, all four bits change. If all changes do not occur simultaneously, then ambiguities may arise, as explained in Chapter 1. This problem may be overcome by devising a code in which only one bit is required to change between adjacent numbers. Such codes are called cyclic-progressive.

One cyclic-progressive code is known as the Gray code and has the truth table shown in Table 55. From Table 55 it can be seen that, apart from the most significant digit, it is symmetrical about the change from 7 to 8. This makes it a simple matter to extract a code with a cycle length of 10, where changing from the last number in the cycle to the first number in the cycle involves a change of only one digit, as shown in Table 55.

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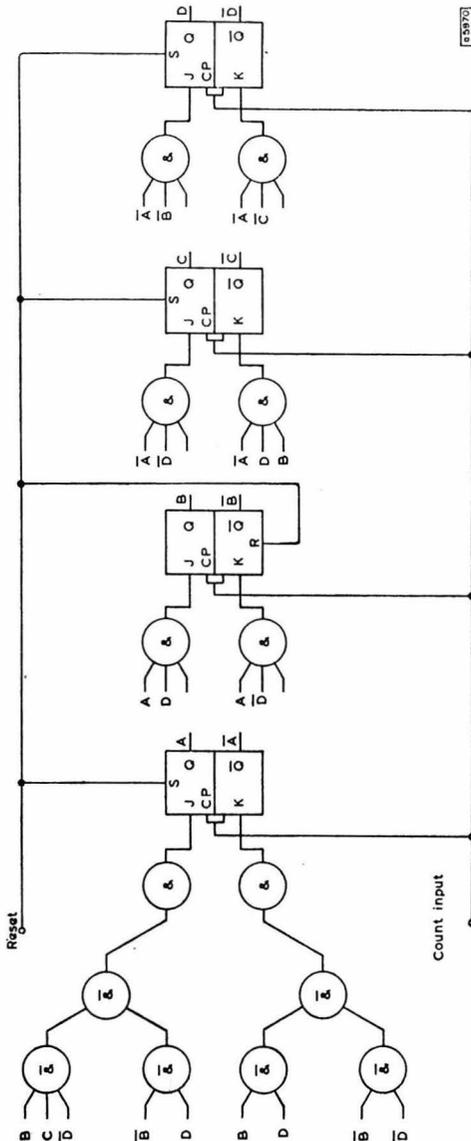
Fig. 126—A Gray code counter with a cycle length of ten made from multiple-input
J-K bistable elements and NAND gates

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A decade counter using this code and made from NAND gates and J-K bistable elements is shown in Fig. 126. Performance details of the counter using integrated circuits of the FC range are given in Table 56.

TABLE 55
The Gray Code

	D	C	B	A	
0	0	0	0	0	
1	0	0	0	1	
2	0	0	1	1	
3	0	0	1	0	
4	0	1	1	0	
5	0	1	1	1	
6	0	1	0	1	
7	0	1	0	0	Gray code with cycle length of 10.
8	1	1	0	0	
9	1	1	0	1	
10	1	1	1	1	
11	1	1	1	0	
12	1	0	1	0	
13	1	0	1	1	
14	1	0	0	1	
15	1	0	0	0	

TABLE 56

Performance of Gray Code Counter using Integrated Circuits of the FC Range

Maximum operating frequency	$= 10\text{MHz}$
Supply voltage	$= 6\text{V}$
Drive pulse	
amplitude:	
minimum	$= 2{\cdot}2\text{V}$
nominal	$= 4\text{V}$
maximum	$= 7\text{V}$
maximum rise time at 1MHz	$= 100\text{ns}$
maximum fall time at 1MHz	$= 100\text{ns}$

"ONE-OUT-OF-FIVE FLOP" COUNTER USING NAND ELEMENTS

Reference was made in Chapter 2 to the fact that a bistable circuit may be constructed with two NAND gates, by connecting the output of each gate to the input of the other gate. This process may be extended to make a circuit with n stable states by using n NAND elements, provided each element has $n-1$ inputs. As an example, the circuit shown in Fig. 127 shows five NAND elements, each with four inputs, connected to make a circuit with five stable states. The circuitry inside the dotted enclosures is the NAND element and that outside is the coupling and steering circuits.

When, for instance, the B NAND gate is saturated, the output of B appears at all inputs except its own, and therefore all the other elements are held off. This, in turn, means that all the inputs to B are high and the circuit is therefore in a stable state. On the arrival of a count pulse, diodes D_1, D_3, D_4 and D_5 are reverse-biased since the collector voltages are fed to the diode cathodes via the steering resistors R_1 to R_5. The collector of stage B is low and, therefore, D_2 is not reverse-biased. On the arrival of a negative count pulse, D_2 conducts and stage B is cut off. The rise in collector voltage of stage B is fed via C_B to stage C, causing it
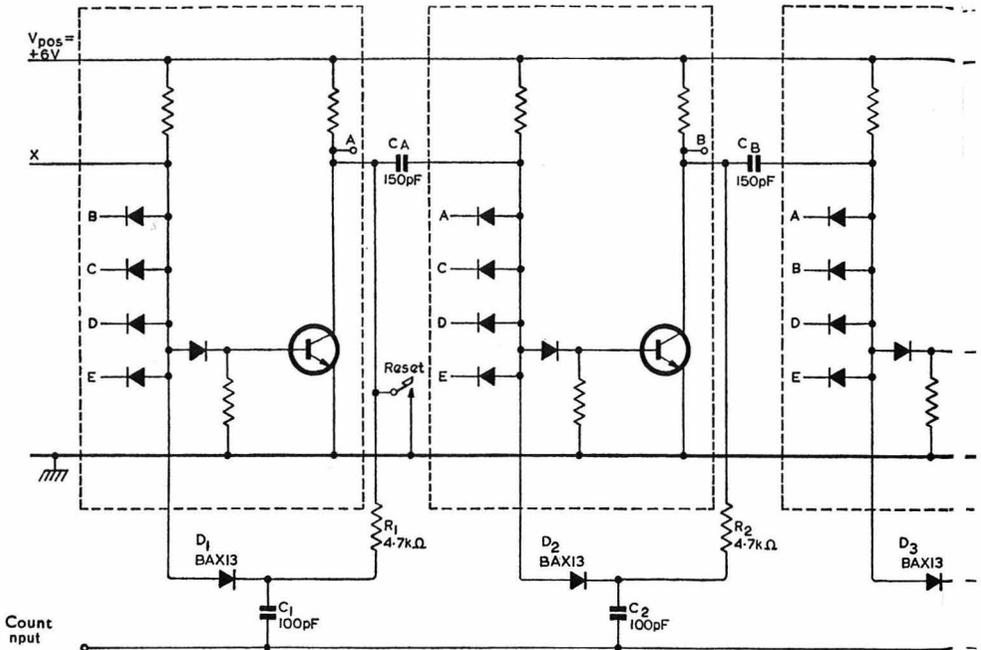
Fig. 127—One-out-of-five flop

to conduct. Once this has happened, the circuit will be in a new stable state in which only gate C is conducting. The performance of this circuit is as shown in Table 57.

By addition of a bistable element, a decade counter is obtained which operates in a one-out-of-five plus one-out-of-two code. One method of doing this is illustrated in Fig. 128. Other methods of interconnection between the bistable stage and the one-out-of-five flop are possible giving different one-out-of-five plus one-out-of-two codes. The truth table obtained by using the method shown in Fig. 128 is shown in Table 58.

TABLE 57

Performance of "One-out-of-five" Flop Counter using Integrated Circuits of the FC Range

Maximum operating frequency	= 1MHz
Supply voltage	= 6V
Drive pulse:	
amplitude	$\geqslant$ 4V
rise time	< 50ns
fall time	< 50ns
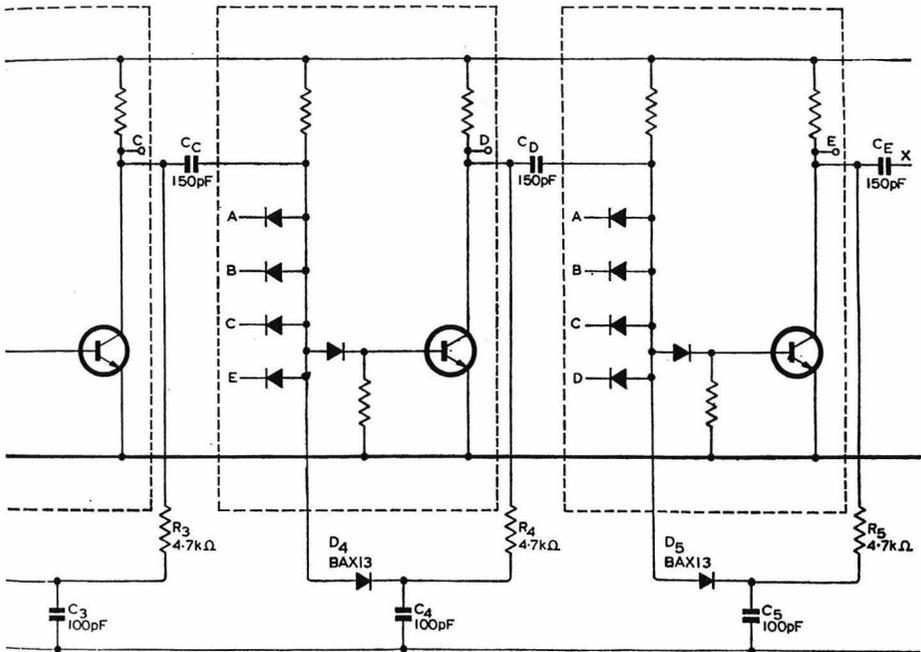
TABLE 58

Truth Table for One-out-of-five plus One-out-of-two Code

	A	B	C	D	E	F
0	0	0	1	1	1	1
1	1	1	0	1	1	1
2	0	1	1	0	1	1
3	1	1	1	1	0	1
4	0	1	1	1	1	0
5	1	0	1	1	1	1
6	0	1	0	1	1	1
7	1	1	1	0	1	1
8	0	1	1	1	0	1
9	1	1	1	1	1	0

1248 WEIGHTED COUNTER WITH A CYCLE LENGTH OF 12

A 1248 counter with a cycle length of twelve counts on the binary scale up to eleven and then reverts to the zero state. This is particularly useful in batch counting where articles are often required in batches of a dozen. A block diagram of the counter is shown in Fig. 129 and performance figures are given in Table 59.

TABLE 59

Performance of 1248 Weighted Counter with Cycle Length of 12 using Bistable elements of the FC range

Maximum operating frequency	= 10MHz
Supply voltage	= 6V
Drive pulse amplitude:	
minimum	= 2·2V
nominal	= 4V
maximum	= 7V
maximum rise time at 1MHz	= 100ns
maximum fall time at 1MHz	= 100ns
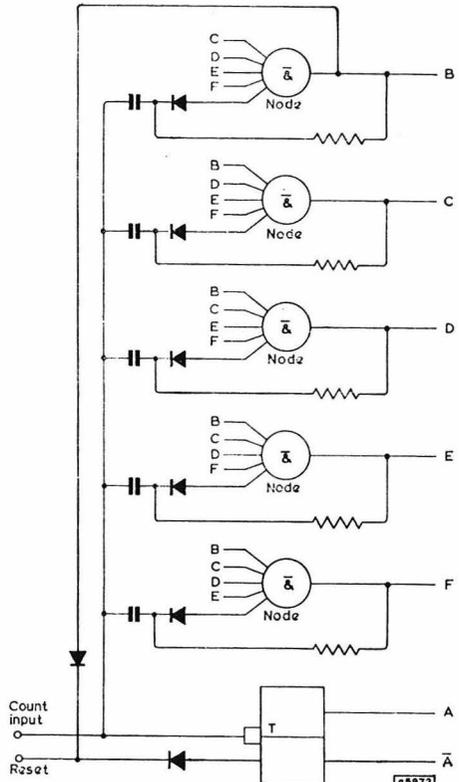
Fig. 128—Decade counter for one-out-of-five plus one-out-of-two code consisting of a one-out-of five flop and one bistable circuit
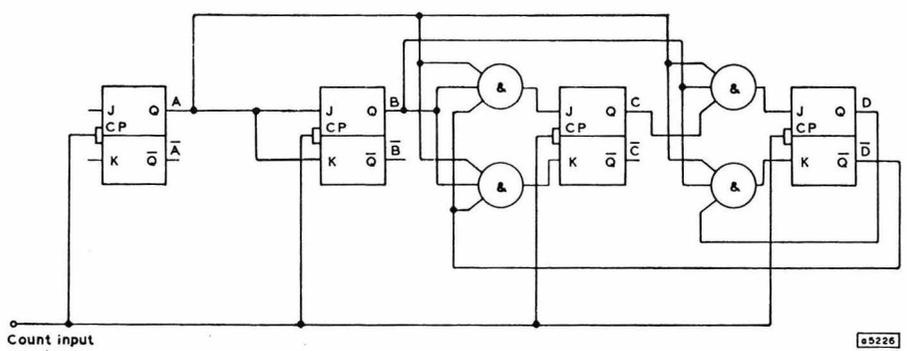
Fig. 129—1248 weighted counter with a cycle length of 12 made from J-K bistable elements

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K

EXCESS-THREE COUNTER

The excess-three code is derived from the 1248 code, starting at three and counting to twelve. The excess-three code has a particular application when arithmetical addition has to be performed. The use of this code simplifies the generation of "carry" signals. Also, since it is a symmetrical code similar to the symmetrical 1242 code described in Chapter 7, the nines complement of the contents of the counter is available from the inverted outputs of the bistable stages.

The truth table for the excess-three code is given in Table 60.

TABLE 60
Truth Table for Excess-three Code

	D	C	B	A
0	0	0	1	1
1	0	1	0	0
2	0	1	0	1
3	0	1	1	0
4	0	1	1	1
5	1	0	0	0
6	1	0	0	1
7	1	0	1	0
8	1	0	1	1
9	1	1	0	0

TABLE 61

Performance of Excess-three Code Counter using Integrated Circuits of the FC Range

Maximum operating frequency	= 10MHz
Supply voltage	= 6V
Drive pulse amplitude:	
minimum	= 2·2V
nominal	= 4V
maximum	= 7V

An excess-three counter is shown in Fig. 130 and the performance of this counter is summarised in Table 61.

Fig. 130—Excess-three counter using J-K bistable elements and NAND gates

CHAIN CODE GENERATORS
The class of counter known as the chain code generator has several other names—among them: M sequence generator, maximal length code generator and pseudo-random generator.

The sequences given by these generators are not governed by the binary

Fig. 131—Chain code generator

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TABLE 62

Truth Table for a Chain Code Generator

	A	B	C	D	E
0	1	0	0	0	0
1	0	1	0	0	0
2	0	0	1	0	0
3	1	0	0	1	0
4	0	1	0	0	1
5	1	0	1	0	0
6	1	1	0	1	0
7	0	1	1	0	1
8	0	0	1	1	0
9	1	0	0	1	1
10	1	1	0	1	1
11	1	1	1	0	0
12	1	1	1	1	0
13	1	1	1	1	1
14	0	1	1	1	1
15	0	0	1	1	1
16	0	0	0	1	1
17	1	0	0	0	1
18	1	1	0	0	0
19	0	1	1	0	0
20	1	0	1	1	0
21	1	1	0	1	1
22	1	1	1	0	1
23	0	1	1	1	0
24	1	0	1	1	1
25	0	1	0	1	1
26	1	0	1	0	1
27	0	1	0	1	0
28	0	0	1	0	1
29	0	0	0	1	0
30	0	0	0	0	1
31	1	0	0	0	0

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code and therefore they are suitable for some applications where the binary code fails to give a simple solution; for instance, counting and division circuits where a base other than two is required.

Essentially, the generator consists of a shift register with feedback; that is, at each shift pulse, a '1' or '0' is fed into the first stage of the register depending on the state of the information contained within the register. In the example shown in Fig. 131, a five-stage synchronous shift register is used and the input is fed with the function $C.\bar{E} + \bar{C}.E$. The result is the sequence shown in Table 62. This is a maximal length code, but it may be shortened to any length by the method shown in the following example.

If the cycle length is to be shortened to 28, the state $\bar{A}.\bar{B}.C.\bar{D}.E$ must be detected and this information must be fed into a five-input NAND gate. The output of this gate is used to set a '1' into A and a '0' into C and E; that is, to set up the number 0 state in place of the number 28 state. The effect is to bypass the unwanted portion of the cycle.

CHAPTER 9

STORAGE

Counters may be divided broadly into two operational classes.

The first of these is the type of counter which is required to count up to a certain number, or count pulses for a given time, and then stop. The information is then held in the counter until it is reset or allowed to count on. Batch counters are an example of this type. In the same class are counters whose contents may be examined directly whilst the count is in progress.

The second type of counter is the type frequently found in instruments such as digital voltmeters, frequency counters and timers. In this class, the counter may be required to count for a given time, or to a given number, and hold the final count in a store for display or use in arithmetical functions. The counter may then be reset and a new count carried out whilst the old count information is still held. Similarly, the contents of a counter may need to be sampled during the count process at discrete time intervals, and the "total so far" held until the next sampling time.

In this second class of counter some form of store, or "staticiser", element is necessary. The store is a bistable element or circuit which, on receipt of a command signal, stores and holds the contents of one element of the counter. Each binary digit, or bit, of information requires one store element or circuit.

NEON STORE FOR PHOTOELECTRIC READOUT

The first circuit, shown in Fig. 132, uses miniature neon tubes, type ZA1004, as the store elements. With the components shown, this circuit is suitable for use at low frequencies (up to 10kHz). No special techniques, such as the use of recovery diodes, are used to make this a fast counter circuit, although the store circuit is quite capable of being used with counters operating at any frequency, provided the necessary output voltage swing is available. The operation of the store circuit depends upon the fact that the ZA1004 has closely controlled triggering, maintaining and extinguishing voltages.

When transistor TR_1 is saturated, with the store control line positive or open-circuited, the cathode of V_1 is held at near zero voltage. Transistor TR_2, however, is in the OFF state and its collector is at about +15V.

The 200V supply fed via R_1 therefore causes V_1 to be triggered, and the common anode line is held at the maintaining voltage of V_1 (about 87V). The anode-cathode voltage of V_2 is therefore 15V less than the maintaining voltage. This value—about 72V—is insufficient to trigger the neon. When the transistor bistable circuit changes state, the situation is eversed, V_2 being in conduction and V_1 being held off. The minimum triggering voltage is 93V.
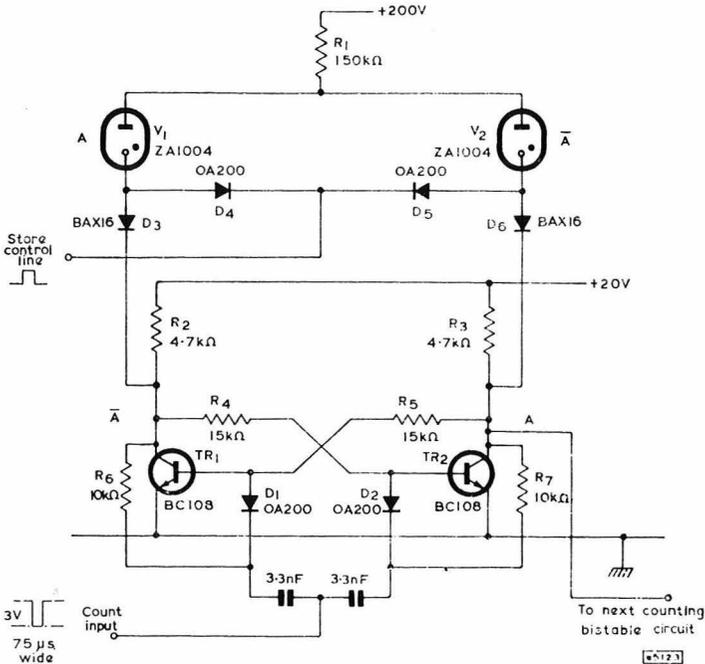
Fig. 132—Transistor bistable circuit using neon storage

At high operating frequencies, the neons do not have time to de-ionize each time the bistable circuit changes state, and both glow continuously. To read out the contents of the counter it is therefore necessary to stop the count first, when the appropriate neon will be ignited. If the store control line is now taken negative or to zero voltage, the conducting neon will remain on but, due to the reverse bias now on diodes D_3 and D_6, the counter bistable stage will have no further effect on the neons. Thus it is possible to display the present count while another count is in progress. This type of store gives a visual binary readout which can be detected by photocells, if required, to drive other indicating devices.

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The circuit has the advantage of complete electrical isolation between the neons and a subsequent readout unit.

The normal sequence of operation with this type of circuit is:

1. Hold store control line at zero.
2. Count.
3. Stop count.
4. Make store control line voltage positive for a short time to transfer information from counter to store.
5. Return store control line to zero and reset counter.
6. Begin new count.
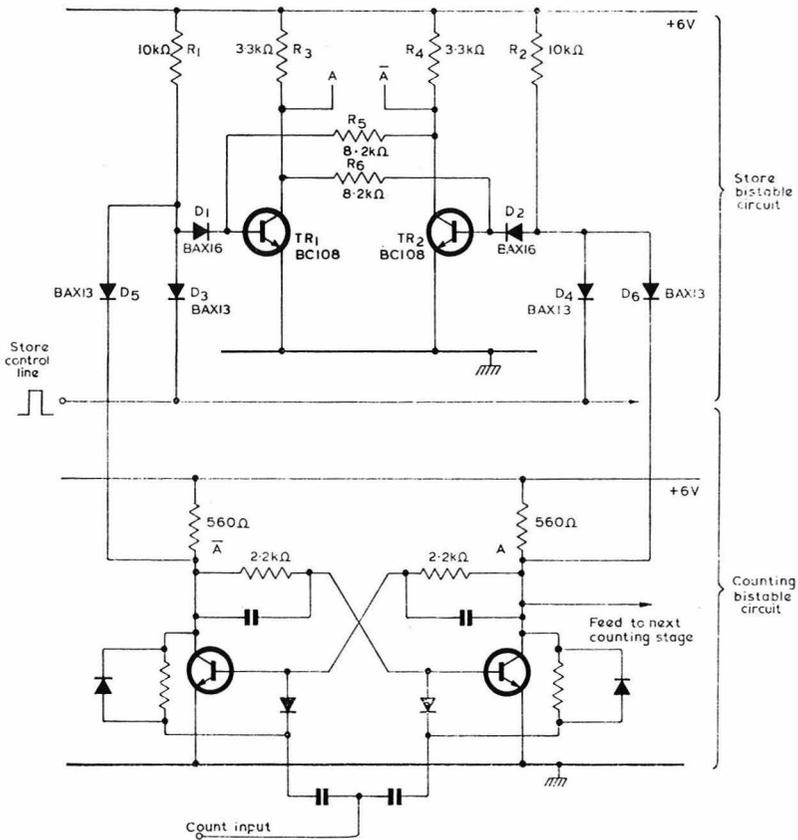
Fig. 133—Transistor bistable store circuit

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TRANSISTOR BISTABLE STORE

A suitable store circuit for use with high- and low-speed transistor counters is that shown in Fig. 133. The store circuit is a Set/Reset bistable element with AND gates on the inputs.

When the store control line potential is low, both the input gates are closed, and the store is effectively disconnected from the counter. A count can therefore proceed without altering the store contents. When the store control line is positive, the input gates are open and the store bistable stage follows the counter bistable stage outputs.

The diodes D_1 and D_2 perform two functions. First they provide isolation between the gate resistor and the bistable cross-coupling, and secondly, they perform a voltage-shifting function between the AND gates (D_5, D_3 and D_4, D_6) and the transistor bases as explained in Chapter 2.

Store circuits such as this are not generally required to operate at very high speeds; a following rate of 10kHz is usually adequate. In such low-speed circuits, OA91 or OA200 diodes could be used for the gating functions. However, if very high following rates are necessary, BAX13 diodes are used for D_5 and D_6 to prevent the capacitances of low-speed diodes having any effect on the counting bistable circuit. If these diodes are used in conjunction with high-speed switching transistors, following rates of several megahertz are possible. The outputs from store bistable circuits may be used directly or may be fed to decoding units for conversion to decimal information, possibly for numerical indicator tube drive.

The circuit shown in Fig. 133 is for 6V operation. Operation at other voltages is, of course, possible by changing the resistor values.

The D bistable element provides a store function with a single information input line. If the Q output of each counting bistable element is connected to the D input of the associated store bistable element, the clock input of the store bistable element controls the tran. fer of information from the counter to the store; that is, the clock input acts as the store control line. J-K bistable elements can also be used as storage elements by connecting the Q output of each counting bistable element to the J input of the associated store bistable element and the $\bar{Q}$ output to the K input. Again, the clock input acts as the store control line.

TRIGGER TUBE STORE

Decimal storage for counters using cold cathode trigger tubes in, for instance, ring counters, may be achieved by the use of a further trigger tube with each stage of the counter. A possible circuit arrangement is shown in Fig. 134.

The store shown in Fig. 134 works on a pulse-plus-bias system similar to that used in the cold cathode tube counters previously discussed. Each trigger electrode is fed via a high resistance from the cathode of one of the counter stages. Thus, the store tube associated with that counter tube which is conducting will have its trigger electrode biased positively by some 90 to 100V. All other triggers will be at zero voltage.
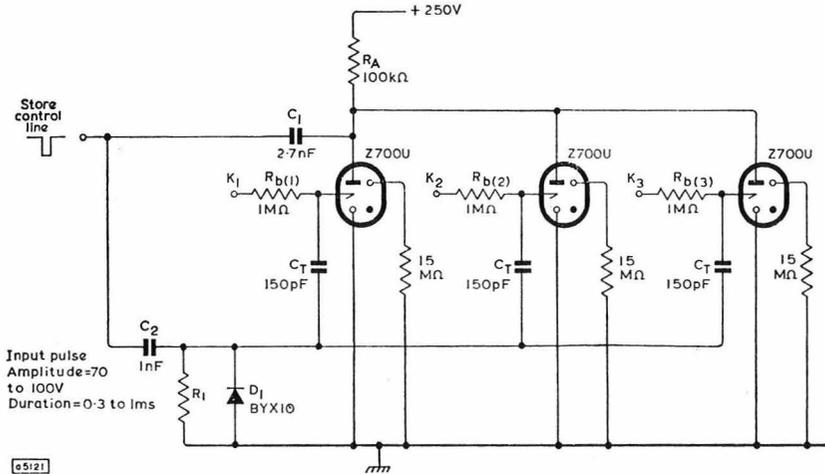
Fig. 134—Cold cathode trigger tube store

A negative-going pulse is applied to the store control line, reducing the anode voltage to a level below the maintaining voltage, and all tubes are extinguished. The anode voltage then begins to recover at a rate determined by the time-constant C_1R_A.

The store pulse is also fed to C_2R_1 where it is differentiated. The negative edge is conducted away by D_1, but the positive edge at the end of the pulse is fed to all trigger electrodes via the trigger capacitors C_T. This pulse, in addition to the bias supplied by the ON counter tube cathode voltage, triggers the appropriate store tube, the others remaining off. This tube remains in conduction until the next store control pulse is received.

SILICON CONTROLLED SWITCH STORE

The circuit of a silicon controlled switch store and numerical indicator tube driver is shown in Fig. 135. The operation of this circuit is as follows.

A positive turn-off pulse saturates transistor TR_1 which switches off all the silicon controlled switches. A positive pulse of at least $5\mu s$ duration, applied to one of the store input lines, turns the appropriate silicon

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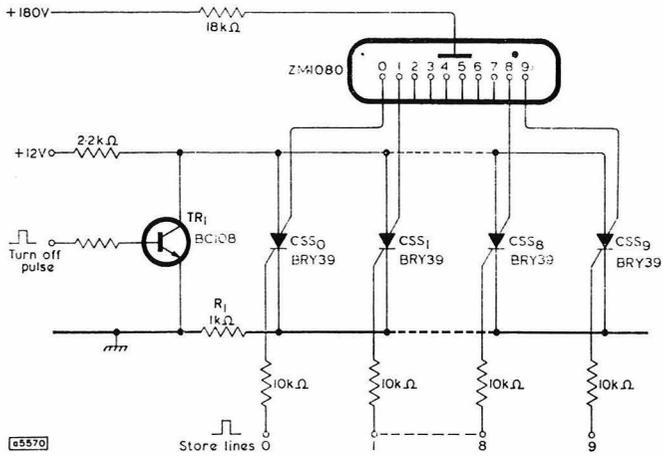
Fig. 135—Numerical indicator tube drive and store circuit using silicon controlle
switches

controlled switch on. None of the other silicon controlled switches can turn on because the bias developed across resistor R_1 maintains them in the OFF state. Because of this, the amplitude of the input pulse must not be greater than this bias value. A maximum amplitude of 5V is suitable.

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DECODING AND CODE CONVERSION

For the information held in coded counters to be made intelligible to human operators it must be converted from its coded form into direct decimal form. This process is a form of code conversion although it is usually known as decoding.

The process of decoding basically consists of finding the simplest unique logic function which describes each coded combination and passing this information through a gate. A basic decimal decoder therefore requires ten AND gates. The structure of the gates used depends upon the load they are required to drive, the frequency of operation and the voltage levels. Decoders are frequently required to operate only at very low speeds; therefore inexpensive, low-speed diodes may be used. However, when diode decoders are used in conjunction with high-speed counters, the capacitive loading imposed by the diode gates may be important, in which case low-capacitance, high-speed diodes must be used. Other forms of gating may be used in decoders; for example, it is sometimes convenient to use NAND gates where integrated circuits are used.

Several AND gate circuits suitable for use in decoders are shown in Fig. 136. The numbers of inputs are not limited to those shown in the figure; in practice two, three or four inputs may be required.

The gate circuit shown in Fig. 136a is suitable for use in low- and medium-speed applications and where high ambient temperatures are not encountered. The gate is capable of supplying a current of about $500\mu A$ to the base of a transistor connected to the output.

The gate shown in Fig. 136b is suitable for use with high-speed counting circuits, and supplies a current of about $450\mu A$ to the output when loaded with the base of a transistor such as a numerical indicator tube driver. The purpose of diode D_4 is to ensure that the transistor remains cut off when the gate input is low, even under worst-case conditions of input and temperature.

A more complex circuit is shown in Fig. 136c. The output of this circuit is slightly negative in the '0' state giving high d.c. noise immunity. The gate gives an output current of about $170\mu A$. The capacitor shown dotted is used where maximum speed is required.

Another simple form of decoding circuit is the resistive AND gate as
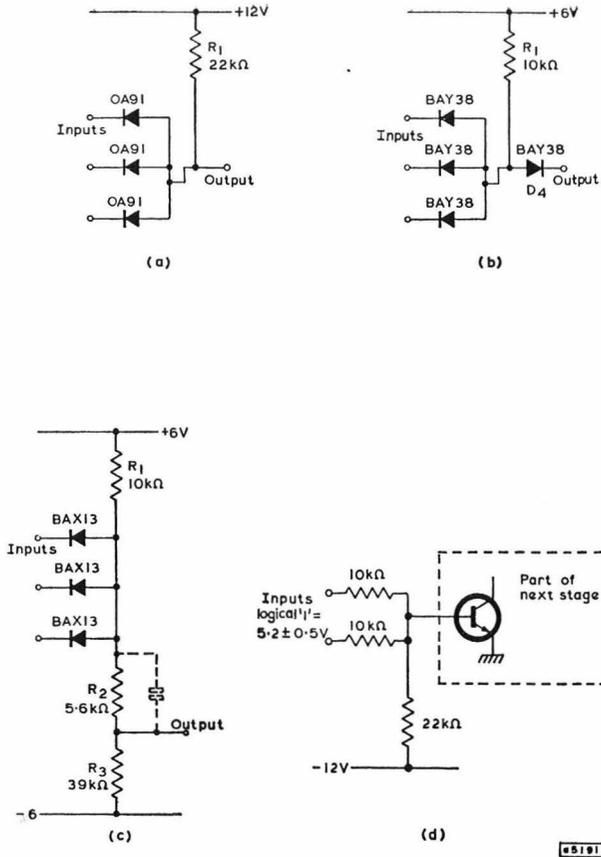
Fig. 136—Decoding AND gates

shown in Fig. 136d. This is particularly useful when only a small number of inputs are to be handled by each gate. When multi-input gates are required, the problems of applying tolerances to the circuits become severe.

Other gates which are useful in decoding circuits are NAND gates which may be coupled to numerical indicator tube drivers. These are discussed in more detail in Chapter 11. The circuit used is shown in Fig. 137. The NAND gates are normally intergated circuits, but a NAND gate can be made from discrete components, if required, as shown in Fig. 138. For circuits

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operating at frequencies higher than about 1MHz, the BAX16 input diodes should be replaced by BAX13 diodes.

The output current of all the gates shown in Fig. 136 may be varied by altering resistance values, but consideration should always be given to the fact that the current in resistor R_1 must be absorbed by the counter or drive circuit when the input voltage to the gate is low.
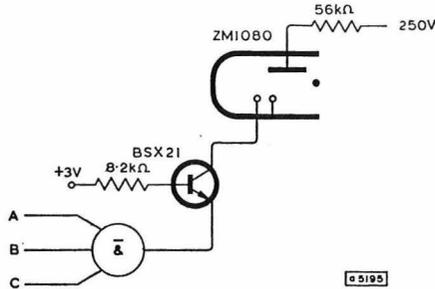
Fig. 137—Decoder and numerical indicator tube driver using NAND gates
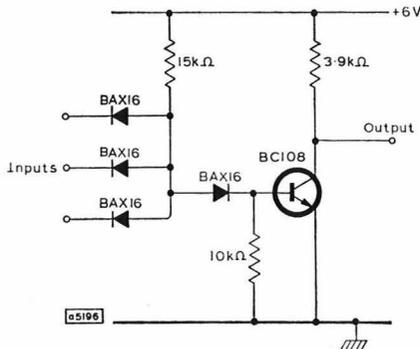
Fig. 138—Practical NAND gate

SIMPLIFICATION BY MEANS OF VEITCH DIAGRAMS
The truth table for a 1248 BCD code is given in Table 63. A possible method of decoding this truth table would be by the use of ten four-input AND gates fed with the functions shown on the right of the table. This method is, however, wasteful of components because it needs 40 diodes when, in fact, the decoding can be achieved with far fewer.

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TABLE 63
1248 BCD Code with Decoding

	D	C	B	A	
0	0	0	0	$0 = \bar{A}.\bar{B}.\bar{C}.\bar{D}$
1	0	0	0	$1 = A.\bar{B}.\bar{C}.\bar{D}$
2	0	0	1	$0 = \bar{A}.B.\bar{C}.\bar{D}$
3	0	0	1	$1 = A.B.\bar{C}.\bar{D}$
4	0	1	0	$0 = \bar{A}.\bar{B}.C.\bar{D}$
5	0	1	0	$1 = A.\bar{B}.C.\bar{D}$
6	0	1	1	$0 = \bar{A}.B.C.\bar{D}$
7	0	1	1	$1 = A.B.C.\bar{D}$
8	1	0	0	$0 = \bar{A}.\bar{B}.\bar{C}.D$
9	1	0	0	$1 = A.\bar{B}.\bar{C}.D$

Fig. 139—Veitch diagram for two variables

TABLE 64
Truth Table for Two Stage Counter

	B	A	Full Decoding
0	0	0	$\bar{A}.\bar{B}$
1	0	1	$A.\bar{B}$
2	1	0	$\bar{A}.B$

The most economical decoding arrangement can be found by using what is known as a Veitch diagram (Ref. 4). This is an extension of the Venn diagram explained in Chapter 2. A Veitch diagram for two variables is

shown in Fig. 139. It can be seen that the diagram is divided into four equal areas, one for each of the possible combinations of variables. In a practical application, some of the combinations are almost certain to be redundant; that is, they will never occur. These redundant terms may be combined with useful terms, thereby reducing the total number of terms necessary. A simple example of the use of Veitch diagrams is provided by a counter consisting of two bistable circuits and capable of counting up to two. The truth table of such a counter is given in Table 64.

The Veitch diagram for the counter is shown in Fig. 140. The combination A.B does not appear in the truth table and is therefore redundant. This is signified on the Veitch diagram by shading the A.B square. The interesting property of the diagrams is that redundant terms may be combined with used terms provided they are symmetrical about a vertical or horizontal line. In Fig. 140, therefore, square 3 can be combined with square 2 and square 1, giving $A.B+\bar{A}.B = B$ and $A.B+A.\bar{B} = A$ respectively. The decoding required is therefore as shown in Table 65.
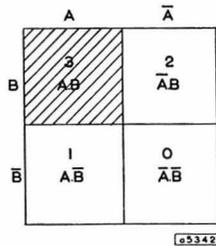
Fig. 140—Veitch diagram for modulo-3 counter

TABLE 65
Simplified Decoding for Two Stage Counter

Number	Decoding
0	$\bar{A}.\bar{B}$
1	A
2	B

From this simplification it is apparent that the decoding requires only one two-input AND gate and two direct connections instead of the three two-input gates which might have appeared to be necessary from the original truth table.

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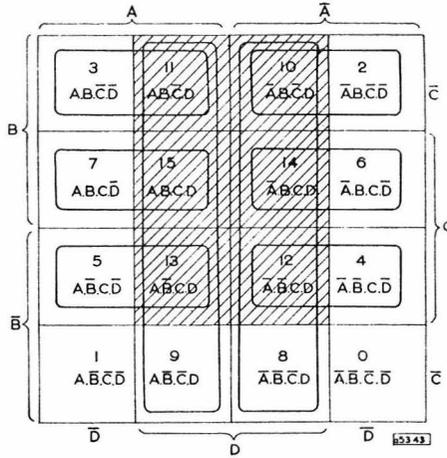
Fig. 141—Veitch diagram for four variables

TABLE 66
Simplified Decoding for BCD Counter

0 may not be combined with any redundant term;
   hence 0 $= \bar{A}.\bar{B}.\bar{C}.\bar{D}$

1 may not be combined with any redundant term;
   hence 1 $= A.\bar{B}.\bar{C}.\bar{D}$

2 may be combined with 10;
   hence $2 = \bar{A}.B.\bar{C}.\bar{D} + \bar{A}.B.\bar{C}.D$ $= \bar{A}.B.\bar{C}$

3 may be combined with 11;
   hence $3 = A.B.\bar{C}.\bar{D} + A.B.\bar{C}.D$ $= A.B.\bar{C}$

4 may be combined with 12;
   hence $4 = \bar{A}.\bar{B}.C.\bar{D} + \bar{A}.\bar{B}.C.D$ $= \bar{A}.\bar{B}.C$

5 may be combined with 13;
   hence $5 = A.\bar{B}.C.\bar{D} + A.\bar{B}.C.D$ $= A.\bar{B}.C$

6 may be combined with 14;
   hence $6 = \bar{A}.B.C.\bar{D} + \bar{A}.B.C.D$ $= \bar{A}.B.C$

7 may be combined with 15;
   hence $7 = A.B.C.\bar{D} + A.B.C.D$ $= A.B.C$

8 may be combined with 12, 10 and 14;
   hence $8 = \bar{A}.\bar{B}.\bar{C}.D + \bar{A}.\bar{B}.C.D + \bar{A}.B.\bar{C}.D + \bar{A}.B.C.D$ $= \bar{A}.D$

9 may be combined with 13, 11 and 15;
   hence $9 = A.\bar{B}.\bar{C}.D + A.\bar{B}.C.D + A.B.\bar{C}.D + A.B.C.D$ $= A.D$

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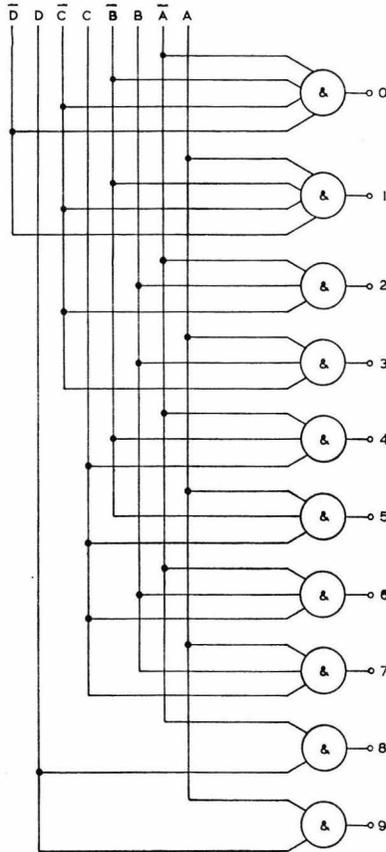
Fig. 142—1248 BCD decoder

Decoding from BCD

For a BCD counter, a four-variable Veitch diagram is necessary, as shown in Fig. 141. The numbers plotted on this diagram are for a 1248 BCD code. Examination of Fig. 141 shows that out of a total of sixteen combinations, only ten are used. There are therefore six redundant combinations. By combining these redundant terms with used terms in the manner described above, the decoding shown in Table 66 is obtained. It is permissible to combine terms or blocks when they are symmetrically

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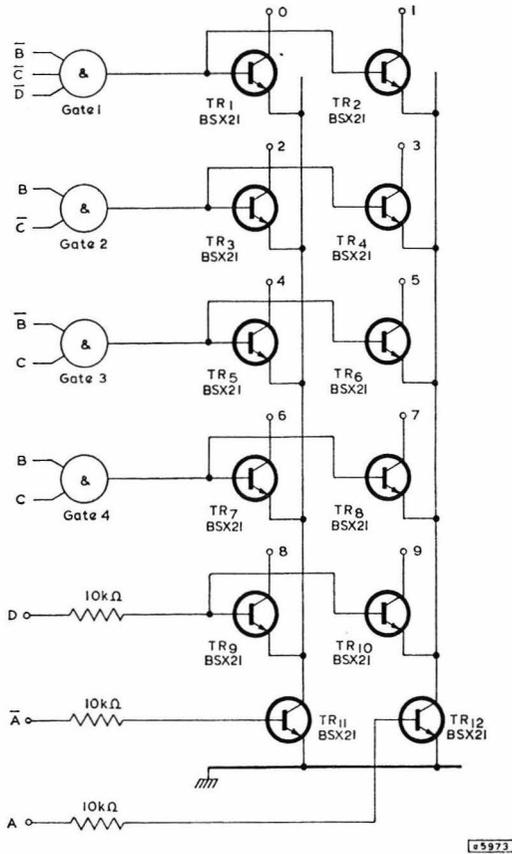
Fig. 143—Transistor decoder and numerical indicator tube driver

disposed about a line. In Fig. 141, for example, the number 9 square may be combined with the number 13 square and this pair may be combined with the symmetrical redundant pair 11 and 15. However, 2 may not be combined with 11. The logic diagram of the decoder resulting from the above simplification is shown in Fig. 142.

The Veitch diagram in Fig. 141 also shows that if the table is split vertically down the centre line, the difference between a used combination in the left half and its symmetrical counterpart on the right lies only in the A term. This is useful because it makes decoding the 1248 code

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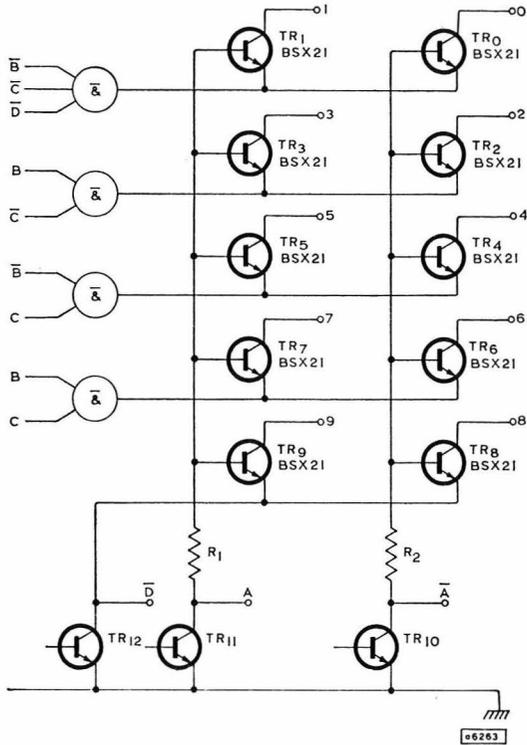
Fig. 144—Odd/even decoder using NAND gates

possible by generating only five functions and switching them with A or Ā as appropriate. A decoder operating on this principle is shown in Fig. 143. This decoder is an economical method of decoding and driving numerical indicator tubes directly. The four gates numbered 1 to 4 generate four of the required functions, the fifth being simply the term D. An alternative method of achieving the same function by the use of NAND gates is shown in Fig. 144. Transistors TR_{10}, TR_{11} and TR_{12} are parts of the counting bistable circuits and resistors R_1 and R_2 limit the base current of the BSX21 numerical indicator tube driver.

Decoding for other codes can be derived using the Veitch diagram and the terms necessary to decode the counters discussed in earlier chapters are given on the succeeding pages.

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Asymmetrical 1242 Code

The truth table for an asymmetrical. 1242 code is shown in Table 67 and the Veitch diagram is given in Fig. 145. The combining of terms is indicated on the diagram and the resulting decoding is given in Table 68.

TABLE 67

Asymmetrical 1242 Code

Weights	D 2	C 4	B 2	A 1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	1	1	0
9	1	1	1	1
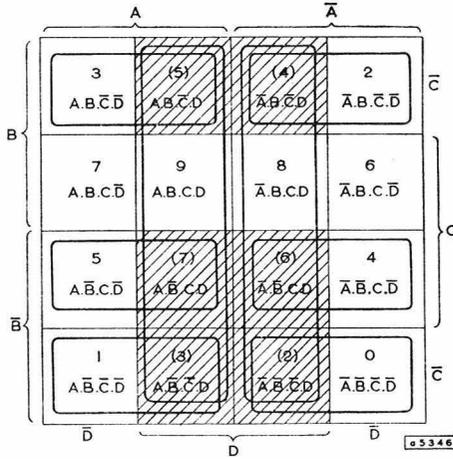
Fig. 145—Veitch diagram for asymmetrical 1242 BCD

TABLE 68
Decoding for Asymmetrical 1242 BCD

Number		Decoding
0	$\bar{A}.\bar{B}.\bar{C}.\bar{D}+\bar{A}.\bar{B}.\bar{C}.D$	$= \bar{A}.\bar{B}.\bar{C}$
1	$A.\bar{B}.\bar{C}.\bar{D}+A.\bar{B}.\bar{C}.D$	$= A.\bar{B}.\bar{C}$
2	$\bar{A}.B.\bar{C}.\bar{D}.+\bar{A}.B.\bar{C}.D$	$= \bar{A}.B.\bar{C}$
3	$A.B.\bar{C}.\bar{D}+A.B.\bar{C}.D$	$= A.B.\bar{C}$
4	$\bar{A}.\bar{B}.C.\bar{D}+\bar{A}.\bar{B}.C.D$	$= \bar{A}.\bar{B}.C$
5	$A.\bar{B}.C.\bar{D}+A.\bar{B}.C.D$	$= A.\bar{B}.C$
6	$\bar{A}.B.C.\bar{D}$	$= \bar{A}.B.C.\bar{D}$
7	$A.B.C.\bar{D}$	$= A.B.C.\bar{D}$
8	$\bar{A}.B.C.D+\bar{A}.\bar{B}.C.D+\bar{A}.B.\bar{C}.D+\bar{A}.\bar{B}.\bar{C}.D$	$= \bar{A}.D$
9	$A.B.C.D+A.B.\bar{C}.D+A.\bar{B}.C.D+A.\bar{B}.\bar{C}.D$	$= A.D$

Alternative Asymmetrical 1242 Code

An alternative truth table for a 1242 code is given in Table 69. The Veitch diagram is given in Fig. 146 and the decoding table in Table 70.

TABLE 69
Truth Table for Alternative 1242 Code

Weight	D 2	C 4	B 2	A 1
0	0	0	0	0
1	0	0	0	1
2	1	0	0	0
3	1	0	0	1
4	1	0	1	0
5	1	0	1	1
6	1	1	0	0
7	1	1	0	1
8	1	1	1	0
9	1	1	1	1
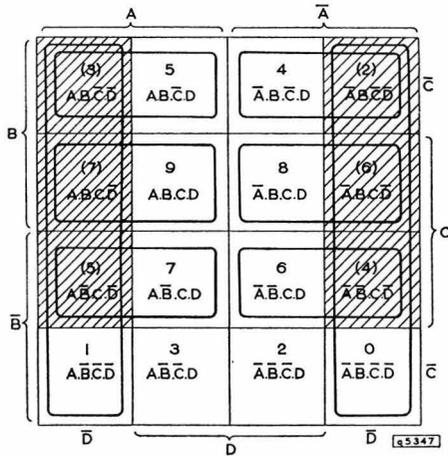
Fig. 146—Veitch diagram for alternative 1242 BCD

TABLE 70
Decoding for Alternative 1242 BCD

Number		Decoding
0	$\bar{A}.\bar{B}.\bar{C}.\bar{D}+\bar{A}.\bar{B}.C.\bar{D}+\bar{A}.B.\bar{C}.\bar{D}+\bar{A}.B.C.\bar{D}$	$=\bar{A}.\bar{D}$
1	$A.\bar{B}.\bar{C}.\bar{D}+A.\bar{B}.C.\bar{D}+A.B.\bar{C}.\bar{D}+A.B.C.\bar{D}$	$=A.\bar{D}$
2	$\bar{A}.\bar{B}.\bar{C}.D$	$=\bar{A}.\bar{B}.\bar{C}.D$
3	$A.\bar{B}.\bar{C}.D$	$=A.\bar{B}.\bar{C}.D$
4	$\bar{A}.B.\bar{C}.D+\bar{A}.B.\bar{C}.\bar{D}$	$=\bar{A}.B.\bar{C}$
5	$A.B.\bar{C}.D+A.B.\bar{C}.\bar{D}$	$=A.B.\bar{C}$
6	$\bar{A}.\bar{B}.C.D+\bar{A}.\bar{B}.C.\bar{D}$	$=\bar{A}.\bar{B}.C$
7	$A.\bar{B}.C.D+A.\bar{B}.C.\bar{D}$	$=A.\bar{B}.C$
8	$\bar{A}.B.C.D+\bar{A}.B.C.\bar{D}$	$=\bar{A}.B.C$
9	$A.B.C.D+A.B.C.\bar{D}$	$=A.B.C$

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Symmterical 1242, or Aiken, Code

The truth table for a symmetrical 1242 code is given in Table 71 and the decoding is given in Table 72. The Veitch diagram is given in Fig. 147. It can be seen from Table 72 that four of the numbers have alternative simplifications. This is useful because it allows a decoder to be designed in which the loading is spread more evenly over the stages.

TABLE 71
Truth Table for Symmetrical 1242 Code

Weight	D 2	C 4	B 2	A 1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	1	0	1	1
6	1	1	0	0
7	1	1	0	1
8	1	1	1	0
9	1	1	1	1
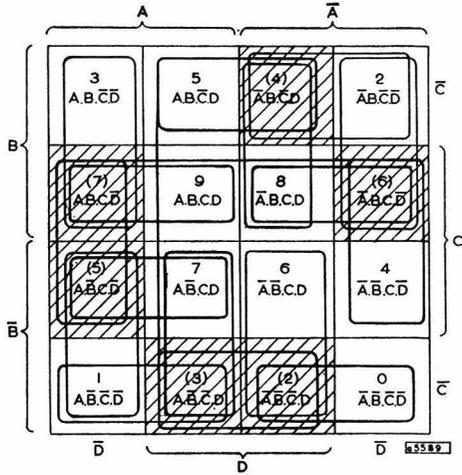
Fig. 147—Veitch diagram for symmetrical 1242 code

TABLE 72
Decoding for Symmetrical 1242 Code

Number		Decoding
0	$\bar{A}.\bar{B}.\bar{C}.\bar{D}+\bar{A}.\bar{B}.\bar{C}.D$	$=\bar{A}.\bar{B}.\bar{C}$
1	$A.\bar{B}.\bar{C}.\bar{D}+A.\bar{B}.C.\bar{D}$	$=A.\bar{B}.\bar{D}$
	or $A.\bar{B}.\bar{C}.\bar{D}+A.\bar{B}.\bar{C}.D$	$=A.\bar{B}.\bar{C}$
2	$\bar{A}.B.\bar{C}.\bar{D}+\bar{A}.B.\bar{C}.D$	$=\bar{A}.B.\bar{C}$
	or $\bar{A}.B.\bar{C}.\bar{D}+\bar{A}.B.C.\bar{D}$	$=\bar{A}.B.\bar{D}$
3	$A.B.\bar{C}.\bar{D}+A.B.C.\bar{D}$	$=A.B.\bar{D}$
4	$\bar{A}.\bar{B}.C.\bar{D}+A.\bar{B}.C.\bar{D}+\bar{A}.B.C.\bar{D}+A.B.C.\bar{D}$	$=C.\bar{D}$
5	$A.B.\bar{C}.D+\bar{A}.B.\bar{C}.D+A.\bar{B}.\bar{C}.D+\bar{A}.B.\bar{C}.D$	$=\bar{C}.D$
6	$\bar{A}.\bar{B}.C.D+\bar{A}.\bar{B}.\bar{C}.D$	$=\bar{A}.\bar{B}.D$
7	$A.\bar{B}.C.D+A.\bar{B}.C.\bar{D}$	$=A.\bar{B}.C$
	or $A.\bar{B}.C.D+A.\bar{B}.\bar{C}.D$	$=A.\bar{B}.D$
8	$\bar{A}.B.C.D+\bar{A}.B.C.\bar{D}$	$=\bar{A}.B.C$
	or $\bar{A}.B.C.D+\bar{A}.B.\bar{C}.D$	$=\bar{A}.B.D$
9	$A.B.C.D+A.B.C.\bar{D}$	$=A.B.C$

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Excess-Three Code
The truth table for the excess-three code is given in Table 73, the Veitch diagram in Fig. 148 and the decoding requirements in Table 74.

TABLE 73
Truth Table for Excess-Three Code

	D	C	B	A
0	0	0	1	1
1	0	1	0	0
2	0	1	0	1
3	0	1	1	0
4	0	1	1	1
5	1	0	0	0
6	1	0	0	1
7	1	0	1	0
8	1	0	1	1
9	1	1	0	0

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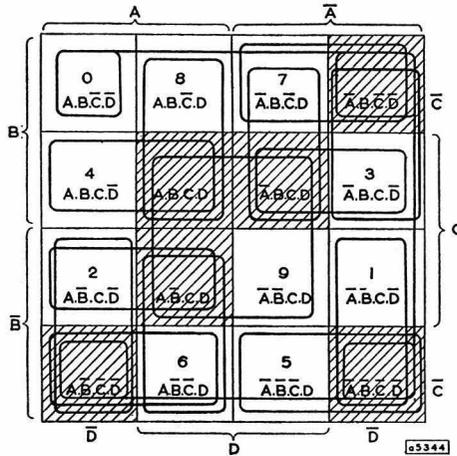
Fig 148—Veitch diagram for excess-three code

TABLE 74
Decoding for Excess-Three Code

Number		Decoding
0	$A.B.\bar{C}.\bar{D}+\bar{A}.B.\bar{C}.\bar{D}+A.\bar{B}.\bar{C}.\bar{D}+\bar{A}.\bar{B}.\bar{C}.\bar{D}$	$= \bar{C}.\bar{D}$
1	$\bar{A}.\bar{B}.C.\bar{D}+\bar{A}.\bar{B}.\bar{C}.\bar{D}$	$= \bar{A}.\bar{B}.\bar{D}$
2	$A.\bar{B}.C.\bar{D}+A.\bar{B}.C.D$	$= A.\bar{B}.C$
	or $A.\bar{B}.\bar{C}.\bar{D}+A.\bar{B}.C.\bar{D}$	$= A.\bar{B}.\bar{D}$
3	$\bar{A}.B.C.\bar{D}+\bar{A}.B.C.D$	$= \bar{A}.B.C$
	or $\bar{A}.B.\bar{C}.\bar{D}+\bar{A}.B.C.\bar{D}$	$= \bar{A}.B.\bar{D}$
4	$A.B.C.\bar{D}+A.B.C.D$	$= A.B.C$
5	$\bar{A}.\bar{B}.\bar{C}.D+\bar{A}.\bar{B}.\bar{C}.\bar{D}$	$= \bar{A}.\bar{B}.\bar{C}$
6	$A.\bar{B}.\bar{C}.D+A.\bar{B}.\bar{C}.\bar{D}$	$= A.\bar{B}.\bar{C}$
	or $A.\bar{B}.C.D+A.\bar{B}.\bar{C}.D$	$= A.\bar{B}.D$
7	$\bar{A}.B.\bar{C}.D+\bar{A}.B.\bar{C}.\bar{D}$	$= \bar{A}.B.\bar{C}$
	or $\bar{A}.B.C.D+\bar{A}.B.\bar{C}.D$	$= \bar{A}.B.D$
8	$A.B.\bar{C}.D+A.B.C.D$	$= A.B.D$
9	$\bar{A}.\bar{B}.C.D+\bar{A}.B.C.D+A.\bar{B}.C.D+A.B.C.D$	$= C.D$

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Gray Code

A counter using a Gray code with a.cycle length of ten is discussed in Chapter 8. The truth table for the Gray code is given in Table 75, the Veitch diagram in Fig. 149 and the decoding requirements in Table 76.

TABLE 75
Truth Table for Gray Code

	D	C	B	A
0	0	0	1	0
1	0	1	1	0
2	0	1	1	1
3	0	1	0	1
4	0	1	0	0
5	1	1	0	0
6	1	1	0	1
7	1	1	1	1
8	1	1	1	0
9	1	0	1	0

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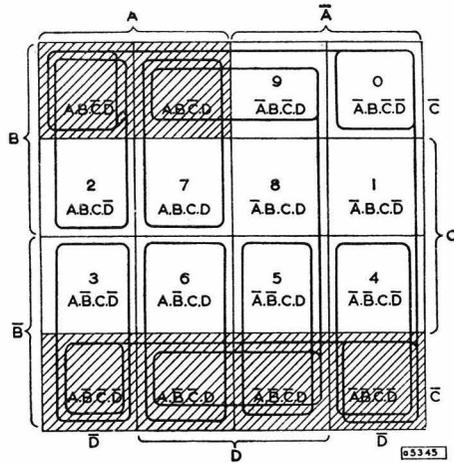
Fig. 149—Veitch diagram for Gray code

TABLE 76
Decoding for Gray Code

Number		Decoding
0	$\bar{A}.B.\bar{C}.\bar{D}+A.B.\bar{C}.\bar{D}+\bar{A}.\bar{B}.\bar{C}.\bar{D}+A.\bar{B}.\bar{C}.\bar{D}$	$= \bar{C}.\bar{D}$
1	$\bar{A}.B.C.\bar{D}$	$= \bar{A}.B.C.\bar{D}$
2	$A.B.C.\bar{D}+A.B.\bar{C}.\bar{D}$	$= A.B.\bar{D}$
3	$A.\bar{B}.C.\bar{D}+A.\bar{B}.\bar{C}.\bar{D}$	$= A.\bar{B}.\bar{D}$
4	$\bar{A}.\bar{B}.C.\bar{D}+\bar{A}.\bar{B}.\bar{C}.\bar{D}$	$= \bar{A}.\bar{B}.\bar{D}$
5	$\bar{A}.\bar{B}.C.D+\bar{A}.\bar{B}.\bar{C}.D$	$= \bar{A}.\bar{B}.D$
6	$A.\bar{B}.C.D+A.\bar{B}.\bar{C}.D$	$= A.\bar{B}.D$
7	$A.B.C.D+A.B.\bar{C}.D$	$= A.B.D$
8	$\bar{A}.B.C.D$	$= \bar{A}.B.C.D$
9	$\bar{A}.B.\bar{C}.D+\bar{A}.\bar{B}.\bar{C}.D+A.B.\bar{C}.D+A.\bar{B}.\bar{C}.D$	$= \bar{C}.D$

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Twisted-Ring Code

The principle of the Veitch diagram may be extended to five or more variables, and to illustrate this, a Veitch diagram for a twisted-ring code is given in Fig. 150. Because, on a diagram of this size, the method used so far to indicate combined variables becomes confusing, the redundant states for each of the ten numbers are shown separately in Fig. 151. The truth table for the twisted ring code, together with the decoding, is given in Table 77.

TABLE 77

Truth Table and Decoding for Twisted-Ring, or Johnson, Code

	A	B	C	D	E	Decoding
0	0	0	0	0	0	$\bar{A}.\bar{E}$
1	1	0	0	0	0	$A.\bar{B}$
2	1	1	0	0	0	$B.\bar{C}$
3	1	1	1	0	0	$C.\bar{D}$
4	1	1	1	1	0	$D.\bar{E}$
5	1	1	1	1	1	$A.E$
6	0	1	1	1	1	$\bar{A}.B$
7	0	0	1	1	1	$\bar{B}.C$
8	0	0	0	1	1	$\bar{C}.D$
9	0	0	0	0	1	$\bar{D}.E$
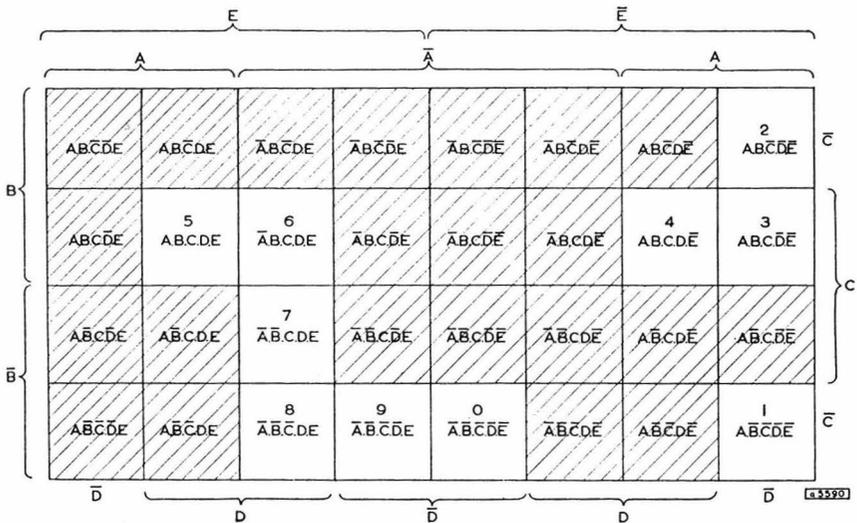
Fig. 150—Veitch diagram for five variables

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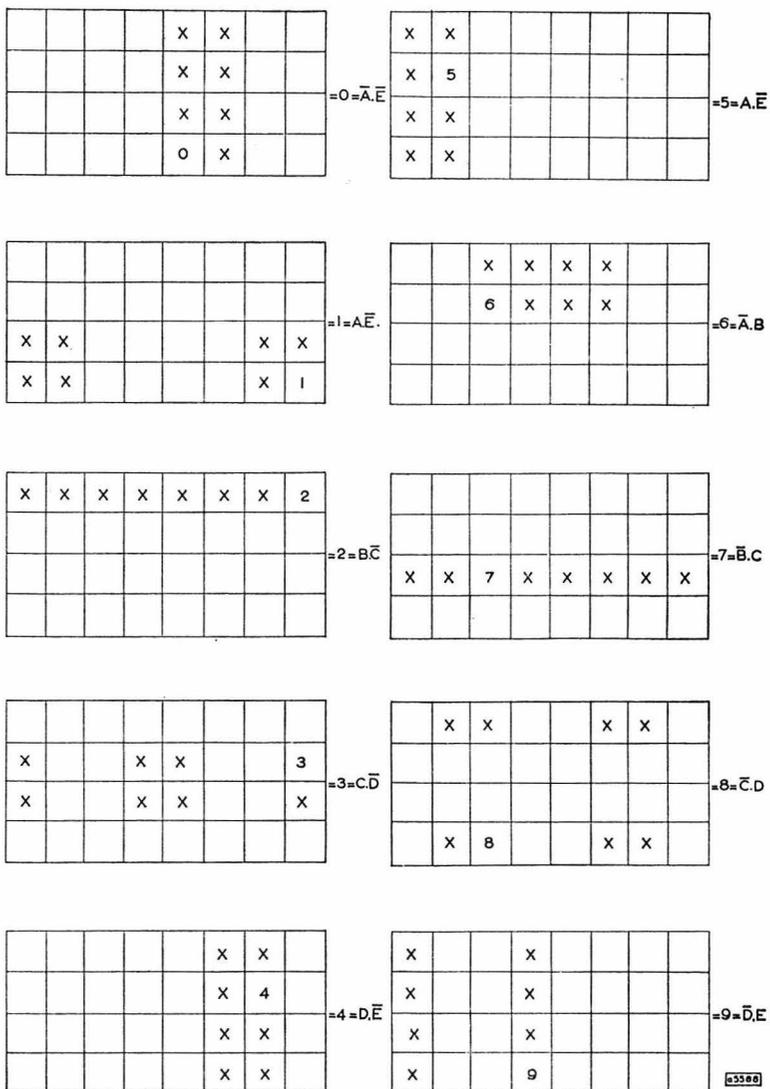
Fig. 151—Simplification of twisted-ring Veitch diagram

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One-out-of-five plus One-out-of-two Code

The truth table and decoding for a one-out-of-five plus one-out-of-two code, which is obtained similarly to the twisted-ring code, are shown in Table 78.

TABLE 78

Truth Table and Decoding for One-out-of-five plus One-out-of-two Code

	A	B	C	D	E	F	Decoding
0	0	1	0	0	0	0	$\bar{A}.B$
1	1	0	1	0	0	0	$A.C$
2	0	0	0	1	0	0	$\bar{A}.D$
3	1	0	0	0	1	0	$A.E$
4	0	0	0	0	0	1	$\bar{A}.F$
5	1	1	0	0	0	0	$A.B$
6	0	0	1	0	0	0	$\bar{A}.C$
7	1	0	0	1	0	0	$A.D$
8	0	0	0	0	1	0	$\bar{A}.E$
9	1	0	0	0	0	1	$A.F$
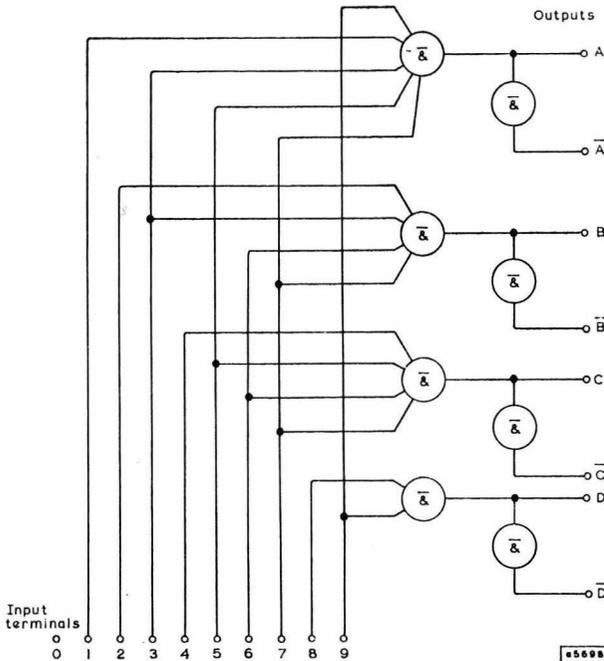
Fig. 152—Decimal to 1248 BCD code converter

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ENCODING

It is sometimes necessary to convert decimal information into an equivalent coded form. This type of problem arises, for example, in keyboard instruments where information is fed in in decimal form but is processed internally in a coded binary form. An example of a code converter from decimal to 1248 BCD is shown in Fig. 152. In operation the required decimal number is fed in by holding its associated input terminal at zero, leaving all others open-circuit or positive.

It is possible to convert from any one code to any other by suitable gates. An example of such a converter is given in Fig. 153 which converts from Johnson code to 1248 BCD.
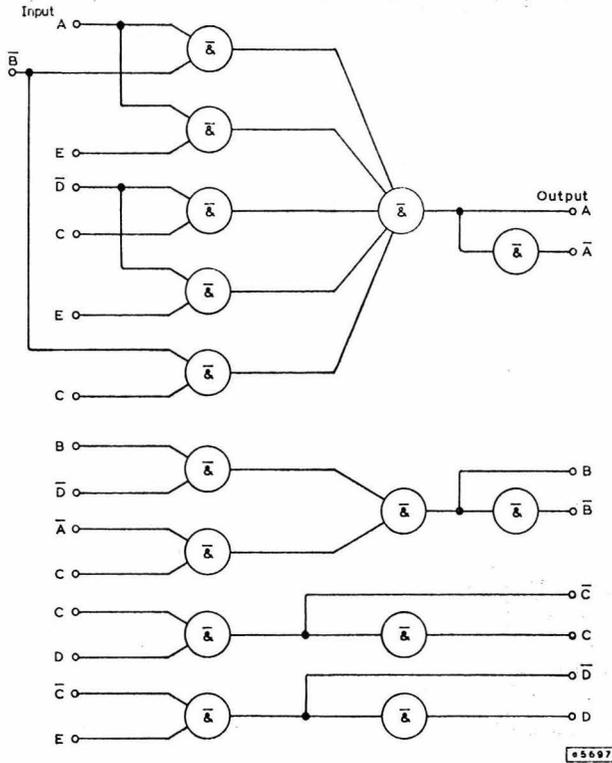
Fig. 153—Johnson to 1248 BCD code converter

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CHAPTER 11

NUMERICAL INDICATOR TUBES

Numerical indicator tubes are cold-cathode gasfilled devices which enable numbers or symbols to be displayed clearly and concisely. They have many advantages over other display systems—among them; reliability, long life, low cost and simplicity of driving requirements. Most of the numerical indicator tubes in use today contain the digits 0 to 9 in one envelope although the principle applies equally well to letters or symbols.

A basic indicator tube consists of a single anode and several cathodes, the cathodes being shaped to form the required characters. The cathodes are stacked, one behind the other, in an order which allows a simple pin numbering system as well as giving a minimum of visual interference between cathodes and an optimum electrical performance.

PRINCIPLES OF A GLOW DISCHARGE

The cold-cathode gasfilled numerical indicator tube operates on the same principle as the familiar gasfilled diode or stabiliser and reference tube. Ionisation caused by external radiation produces electrons which are attracted to the anode and positive ions which are attracted to the cathode. As the anode voltage is increased, the ionisation also increases, producing two threshold effects. First, the electrons remove other electrons from adjacent gas atoms by collision and second, positive ions flowing towards the cathode reach an energy level sufficiently high to remove additional electrons from the cathode surface by bombardment. In this region of the characteristic curve, the discharge is still dependent upon the primary source of electrons, and if this were removed, the discharge would eventually cease.

If the anode voltage is raised still further, a condition is reached where, on average, one electron released from the cathode results in collision with a gas atom whose corresponding positive ion, when striking the cathode, emits another electron. The discharge can now be sustained without the primary source of electrons. This value of anode voltage is known as the ignition, or striking, voltage.

After ignition, the voltage across the tube falls towards its maintaining voltage because slow-moving positive ions form a space charge which is a virtual anode near the cathode. Electrons liberated from the cathode

enter a strong local field and obtain sufficient energy to cause ionisation despite a fall in the voltage across the tube. The tube is now operating in the glow discharge region and the discharge covers a small portion of the cathode. The current density at the cathode is constant, and if the current in the tube increases, the discharge covers a greater proportion of the cathode although this has little effect on the maintaining voltage.

When the discharge completely covers the cathode surface, further increases in current raise the cathode current density and the abnormal glow region is entered. In this region, the maintaining voltage and tube dissipation increase. The numerical indicator tube operates in the abnormal glow region because, in this region, the whole of the cathode is covered by the discharge.

The voltage-current characteristic showing the four regions, is given in Fig. 154. The ignition and maintaining voltages depend on the characteristics of the gas, the cathode material and the electrode geometry. The ignition, and to a lesser extent, the maintaining voltages, also depend on the gas pressure and electrode spacing.
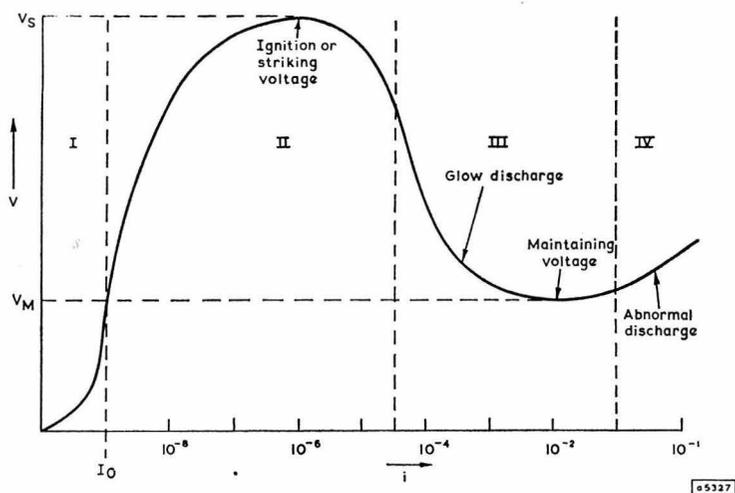
Fig. 154—Voltage-current characteristic of a gasfilled diode

The voltage distribution between the anode and cathode of a gasfilled diode, and its relation to the glow discharge is shown in Fig. 155. Adjacent to the cathode, in the region of greatest change of potential, is a dark region known as the "cathode dark space". At the edge of the dark space, where the curve flattens out, there appears a bright glow usually

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called the "negative glow" whose colour is characteristic of the particular gas filling used. This region completely surrounds the cathode and usually extends about 0·5 to 1mm away from it, this distance being dependent on the gas pressure. This bright "sheath" is the glow normally associated with the tube. Next to the sheath is a dark region known as the "Faraday dark space", then the curve rises and a glow called the "positive column" appears, extending to the anode. The positive column is the glow seen in neon signs, but it is usually eliminated in numerical indicator tubes by suitably arranging the electrodes.
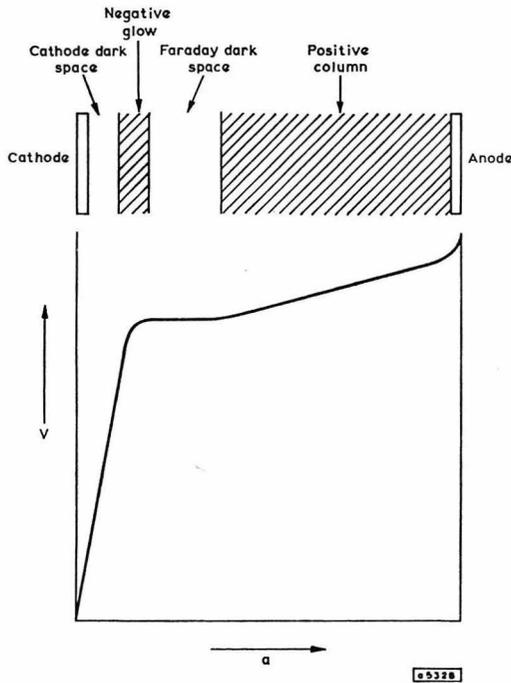
Fig. 155—Voltage distribution between anode and cathode of a gasfilled diode, showing relation to the glow discharge

NUMERICAL INDICATOR TUBE CONSTRUCTION
The construction of typical numerical indicator tubes is shown in Fig. 156.

Ten individual metal cathodes, shaped to form the characters 0 to 9, are mounted one behind the other on supporting rods, and are located by small loops at the top and bottom of each character. The characters are

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spaced away from each other by small insulating beads which are also mounted on the supporting rods. This whole assembly is mounted in a metal cylinder (which forms the anode), part of which is cut away and covered by a hexagonal metal mesh or wire grid through which the characters are viewed. Electrical connections are made to each electrode and these are connected to the base pins. A glass envelope is then sealed to the base and the normal gas filling process is carried out. The material used for the cathodes is of small cross-section and the glow from the cathode during operation is several times the volume of the material. This means that the glowing character is not unduly obscured by the non-glowing cathodes; in fact, the eye has difficulty in resolving the small dark areas of unlit cathodes from the bright glow of the glowing cathode. The light output is almost directly proportional to the cathode current, but current variations within the limits specified in published data result in almost imperceptible variations in brightness.
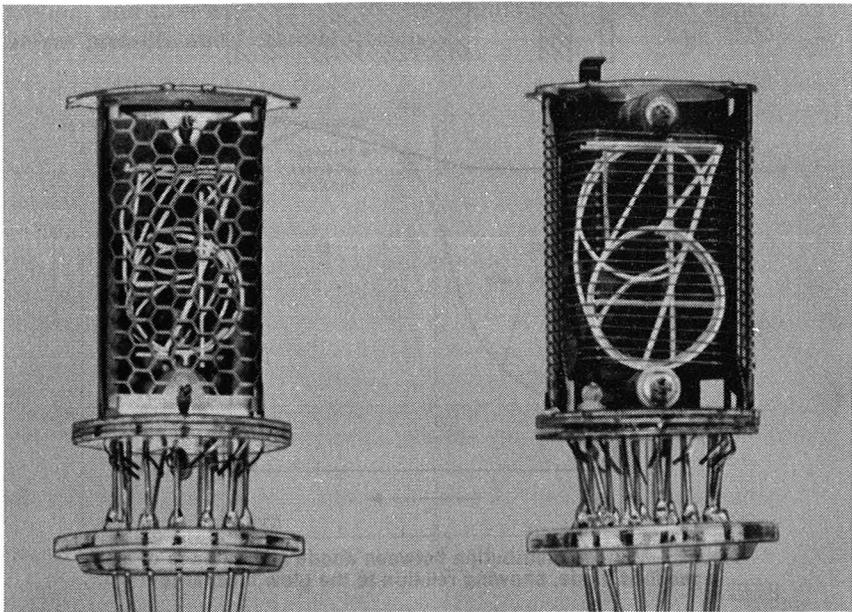
Fig. 156—Electrode structures of typical numerical indicator tubes

Many types of numerical indicator tube use envelopes similar to those of conventional valves, but, more recently, rectangular envelopes have been made which allow closer spacing between tubes and a more aesthetic presentation of display than that possible with the round envelope types.

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ELECTRICAL CHARACTERISTICS OF A NUMERICAL INDICATOR TUBE

Although a numerical indicator tube contains a number of cathodes and one anode, once the required cathode has been selected for display, the corresponding anode-cathode gap can be considered as a single gasfilled diode. The equivalent circuit of a gasfilled diode is shown in Fig. 157.
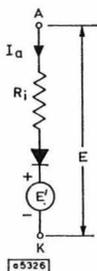
Fig. 157—Equivalent circuit of a gasfilled diode

At terminals A and K, the device presents a constant voltage source, E', in series with an internal resistance R_i and a diode which represents the unidirectional characteristic of the tube. If E is the maintaining voltage of a discharge gap under given current conditions,

$$E' = E - I_a R_i .$$

Because of inconsistencies in materials and processing, the value of E' is not the same for each gap and therefore slight differences exist in the maintaining voltage and in the value of I_k for different gaps. In a typical tube, E' is about 140V and R_i is about 8kΩ. Therefore,

$$E \simeq 140 + 8I_a ,$$

where I_a is in mA.

The numerical indicator tube is more complex than a simple diode in that the non-glowing cathodes act as probes in the discharge. These probes modify the current characteristics of the tube, usually taking a share of the anode current. Typical probe characteristics of these cathodes are shown in Fig. 158.

The probe characteristics of a typical numerical indicator tube, such as the ZM1080 or the ZM1162, are shown for a d.c. anode current range of 1·5 to 2·5mA, in Fig. 158. Only the maximum and individual limits are shown, all the cathode probe characteristics lying between these two limits. The ordinate is the probe current (I_{kk}) and the abscissa is the probe or pre-bias voltage (V_{kk}). The zero point is the ON cathode voltage. It can be seen that, as the value of V_{kk} increases, the value of I_{kk} decreases until the current reverses at a potential of about 115V. This is where the OFF cathodes have begun to function as anodes, and the

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tube should not be operated in this region. As V_{kk} is decreased, the OFF cathodes begin to accept an increasing amount of ion current resulting in a background haze which eventually becomes so bad that it makes the display illegible.
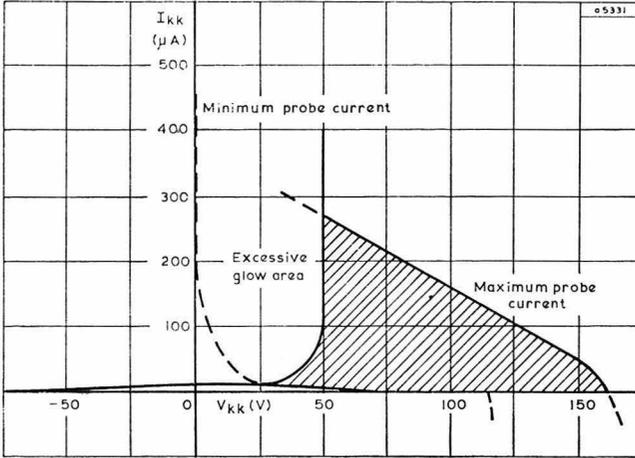
Fig. 158—Probe currents to individual cathodes. D.C. anode current range 1·5 to 2·5mA

OPERATION OF NUMERICAL INDICATOR TUBES
There are various methods of driving numerical indicator tubes and several of them are discussed here.

Switched D.C. Operation
The simplest method of driving a numerical indicator tube is switched d.c. operation. With this method, a voltage in excess of the ignition requirement is applied between the anode and the selected cathode. A series resistor must be used to limit the tube current. A typical circuit using mechanical switching is shown in Fig. 159. The value of resistance is calculated from the equation

$$R_a = \frac{V_{pos} - V_m}{I_a},$$

where V_{pos} is the supply voltage, V_m is the maintaining voltage and I_a is the tube current.

The graph shown in Fig. 160 shows the spread in maintaining voltage of the ZM1080 through its permitted current limits. Projected on these curves are the worst-case load lines for two values of supply voltage and series resistor, with suitable allowances made for tolerances. The area

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bounded by the continuous lines represents the worst-case tolerance for a supply voltage of 250V±10% and a series resistor of 47kΩ±5%. The area bounded by the broken lines is for a supply voltage of 200V±10% and a series resistor of 33kΩ±5%.
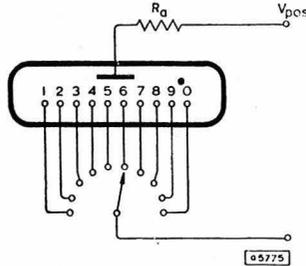
Fig. 159—Mechanical switching of a numerical indicator tube
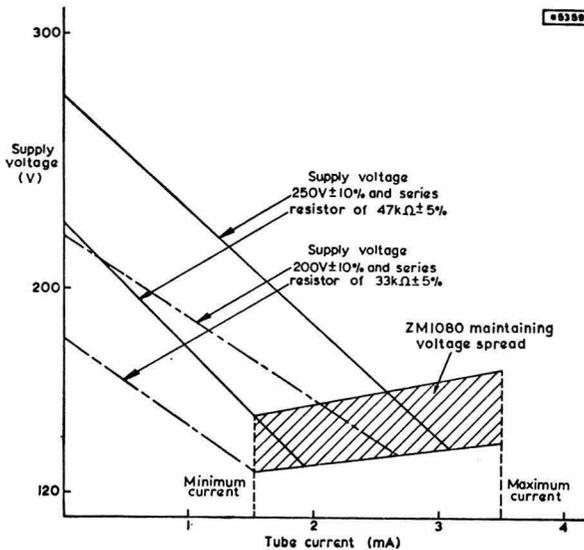
Fig. 160—Graphs of supply voltage against tube current

It can be seen from the graph that, as the supply voltage gets higher, the load line becomes steeper and a constant-current condition is approached. This situation is desirable if the maximum life is to be obtained from the tube. From the lower supply voltage it is seen that, with the quoted value of series resistor, the tube could be operating below its lower current limit. While, with a new tube, this may give results

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which appear satisfactory to the eye, the tube will reach its end-of-life condition more quickly than is indicated in the published data.

The above calculation has been based on the anode current. If the non-glowing cathodes are completely isolated (as they could be in mechanical switching) this has no importance because the cathode current is substantially the same as the anode current. However, if the cathode is not isolated, some of the anode current may be lost to the non-glowing cathodes. This assumes greater importance when electronic switching is used.

Electronic Switching or Pre-bias Operation

With electronic switching, or pre-bias operation, the requirements for establishing a glow and limiting the cathode current are similar to those of mechanical switching. However, when a numerical indicator tube is used in conjunction with electronic switching, it is desirable to use a lower switching voltage to be compatible with semiconductor devices.

A drive circuit containing ideal switches is shown in Fig. 161. In this circuit all the cathodes are connected to the positive line of a pre-bias voltage, and the desired cathode is switched to the negative line when required. The pre-bias voltage can therefore be defined as the voltage difference between "on" and "off" cathodes.
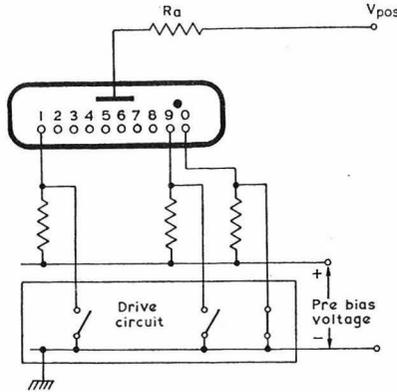
Fig. 161—Electronic switching of a numerical indicator tube

It can be seen from Fig. 158 that the pre-bias voltage is limited in its maximum excursion by the "off" cathodes acting as anodes and in its minimum excursion by the visual appearance of the display.

There are two ways in which these conditions may be satisfied. A

low-impedance voltage source with limits of 50 and 115V may be connected to the non-conducting cathodes or a separate high impedance may be connected to each non-conducting cathode and returned to a voltage source of less than 115V. When the latter method is used, the load line must not enter the excessive-glow region.

Similar effects are seen in all gas-discharge numerical indicator tubes, but values of V_{kk} and I_{kk} differ for various types of tube because the probe characteristics are determined by the electrode layout, cathode cross-sectional area, stacking order and gas pressure.

Transistor Drive Operation
With the introduction of low-cost n-p-n transistors, with high reverse-voltage breakdown, the transistor method of driving numerical indicator tubes has become the most popular. N-P-N devices are of the correct polarity for numerical indicator tube driving because they can be directly connected between the tube cathodes and the negative supply without any additional voltage lines. The power consumed is also low since the transistors operate normally in the reverse breakdown condition, only the required transistor drawing the tube current. If p-n-p devices were used, another voltage line would be required and nine transistors would be turned on, with the one "off" transistor corresponding to the "on" cathode.
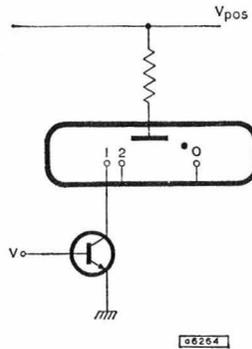
Fig. 162—Transistor driving of a numerical indicator tube

Silicon devices are essential since these can be switched off merely by lowering the base-emitter potential and also because of the sharp break-down characteristics that are not present in germanium transistors.

The probe characteristics of a numerical indicator tube are very important in this mode of operation since they help to determine the operating point of the transistor in the reverse condition. The breakdown

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voltage of the transistor should be high enough to ensure that only the minimum probe current, consistent with a good display, is allowed to flow from the "off" cathodes.
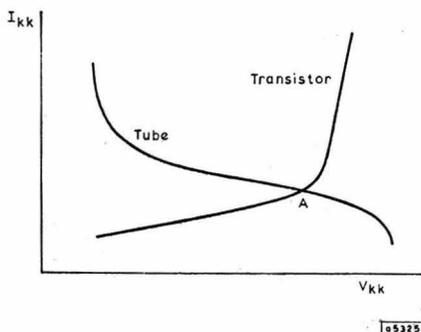
Fig. 163—Graph showing a combination of numerical indicator tube probe and transistor reverse breakdown characteristics

The basic transistor driving circuit is shown in Fig. 162. A combination of numerical indicator tube probe and transistor reverse breakdown characteristics is shown in Fig. 163. The intersection of these characteristics (point A) is the operating condition and care should be taken to ensure that the transistor is capable of handling the power dissipation in these conditions. The avalanche breakdown of a driving transistor must not occur at less than 60V, and the transistor must be able to absorb the probe current at this voltage. Practical circuits using silicon controlled switches and transistors are given in Chapter 10.

Half-wave A.C. Operation
Numerical indicator tubes may be operated with a half-wave rectified a.c. supply in which a pulse of current is applied to the tube on each positive-going half cycle. This enables a supply voltage to be arranged directly from the a.c. mains supply and presents less of a problem than generating a high-voltage d.c. supply when using low-voltage equipment. Provided that the values of peak current given in published data are not exceeded, a life comparable with that of d.c. operation can be achieved. However, the light output is proportional to the mean current and therefore some reduction in intensity can be expected under these conditions.

Use of Silicon Controlled Switch as Numerical Indicator Tube Driver and Store Circuit
By using the latching facility of the silicon controlled switch, the functions

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of numerical indicator tube driving and storage may be combined in one circuit. An example of such a circuit is shown in Fig. 164.

In this circuit, the store control line Y is held at zero. When a positive pulse is applied to the base of TR_1, the collector voltage falls to zero. This causes the anode voltage of all the silicon controlled switches to fall to zero and the switches are therefore turned off. When the base voltage of TR_1 is removed, all the anodes of the silicon controlled switches return to $+12V$ but the switches remain off.

Diodes D_{10} to D_{14} in conjunction with R_{22} form a decoding AND gate fed from a BCD counter. Diodes D_0, D_1, D_2, D_3 etc., are voltage-shifting diodes ensuring that the cathode gate potential of the silicon controlled switches is at zero when the AND gates are closed.

Initially, since the control line Y is at zero, all the decoding AND gates are closed. If now, for example, the number 2 is assumed to be present in the 1248 BCD counter, $\bar{A}.B.\bar{C}$ will be present. Thus, when the store control line Y is taken positive momentarily, gate 2 opens, applying a positive gate pulse to CSS_2, turning it on. None of the input conditions to the other decoding gates is satisfied, and therefore only this one stage switches on, causing the number 2 to be displayed in the numerical indicator tube. When the store control line Y is returned to zero potential, CSS_2 remains on, and the count can proceed without altering the display until the next time arrives when the count is to be sampled.

In this circuit BAX13 diodes are used so that the capacitive loading of the counter, due to the decoding gates, is as small as possible. This is a necessary precaution when decoding from high-speed counters since highly capacitive loading reduces the maximum counting speed.

LIFE PERFORMANCE
The expected life performance of a numerical indicator tube depends to a great extent on the length of time the discharge is investing any particular cathode. With any gas-discharge device, the cathode is subjected to constant ion bombardment which removes material from the cathode and deposits it elsewhere in the tube. This "sputtering" process, as it is known, is, in fact, put to good use in many cold cathode gasfilled tubes during processing. The cathode surfaces are cleaned in this manner and any sputter material thrown on the glass walls of the envelope effectively seals in any foreign matter that may affect the performance of the tube during its life. In a numerical indicator tube, however, although a clean cathode is desirable, sputter material on the envelope would impair the visibility of the display. Some sputtering is unavoidable, but since the rate of sputter is proportional to the peak current of the tube, it can be contained within limits.

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Fig. 164—Decoder, store and numerical indicator tube driver using silicon controlled switches

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If one cathode is continually glowing, sputter material from that cathode is deposited on other cathode surfaces in close proximity. Although the legibility of the glowing cathode is not affected to a great extent, the cathodes on which the sputter is deposited are affected. In fact, the work function of the metal of the adjacent cathodes alters in such a way that it requires a higher current to completely cover the cathode and if this current is not available, the cathode appears patchy. This imposes a minimum permitted current level on the tube. It is possible that complete erosion of the cathode may result from bombardment, but this is unusual.

If the discharge is cycled between characters fairly regularly, this gives a very much improved life figure since each cathode, although receiving some sputter material, is subjected to the cleansing action of bombardment. In this case, the higher the current, the more effective the cleansing. The viewing area of the envelope is protected from sputter material by the use of a shield, or mesh, which is usually connected to the anode.

From the foregoing it is evident that the end of life of a numerical indicator tube is not abrupt, but takes the form of a gradual deterioration of a character. This is convenient, because it enables a tube which is showing signs of deterioration to be replaced before it fails completely.

The normal figures quoted in published data for the life of a numerical indicator tube are 5000 hours with a continuous display of one character, and 30 000 hours when sequentially changing the display from one digit to the next every 100 hours or less. The end of life for the above figures is taken to be the time when any character is unable to be covered completely, although several more thousand hours would probably have to elapse before the character became completely indecipherable. If a tube is operated with a bulb temperature below 0°C, the mercury inside the tube condenses, resulting in a slight increase in the sputter rate. However, if the consequent shortening of life can be tolerated, an operating temperature range of -50 to $+70$°C can be achieved.

N

APPENDIXES
DESIGN PROCEDURES FOR GATES AND BISTABLE CIRCUITS

APPENDIX 1

DESIGN PROCEDURE FOR A DTL NAND GATE

The required operation of a DTL NAND gate is that if any input is held at a logical '0' voltage level, the transistor should be cut off and the output voltage (V_{out}) should be a logical '1'. When all inputs are at a logical '1' voltage level, the transistor should conduct and the output voltage should be a logical '0'. The output current must be sufficient to supply the inputs of several similar gates. The number of gates which one output can feed is known as the "fan-out" (N).
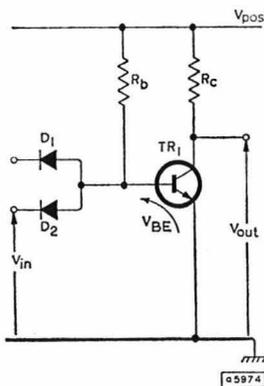
Fig. 165—Basic NAND gate

A basic NAND gate circuit is shown in Fig. 165. In this circuit, when the input voltage is zero, the base voltage of the transistor is equal to the forward voltage drop of one input diode. If silicon diodes are used, this voltage is about 0·7V, which may be sufficient to cause the transistor to conduct. Some other precautions are therefore necessary to ensure that the transistor remains in the OFF condition.

If germanium diodes are used in conjunction with silicon transistors, the simple circuit shown in Fig. 165 may be adequate for some applications but,

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in practice, silicon diodes are normally used. Further, the logical '0' voltage will not be zero but will be the saturation voltage of a transistor when one gate input is fed from the output of a previous similar gate. The difference between the maximum low output voltage of a gate in the '0' state and the maximum low input voltage to maintain a logical '1' is known as the low-state noise immunity.
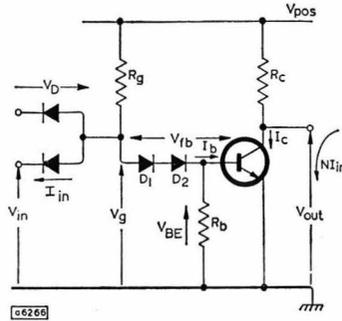
Fig. 166—Practical gate circuit
(Typical component values given on p. 197)

By using a diode or diodes in series with the base of the transistor, as shown in Fig. 166, the input voltage required for the transistor to conduct is increased. In the circuit shown in Fig. 166, two diodes are used to provide the noise immunity required. Before the transistor can conduct, V_g must be equal to $V_{fb}+V_{BE}$ and the input voltage must be $V_{fb}+V_{BE}-V_D$ at least, where V_D is the forward conduction voltage of the input diodes and V_{BE} is the minimum base voltage required to cause the transistor to conduct. The voltage V_{fb} may be provided by one or more diodes, a reference diode or a resistive potential divider in conjunction with a negative bias voltage line.

D.C. CONDITIONS
D.C. conditions are considered for the OFF state and for the ON state.

OFF State
The required condition for the OFF state is given by:

$$V_{in(max)} \leqslant V_{fb(min)}+V_{BE(min)}-V_{D(max)}.$$

The diode gate input current is given by:

$$I_{in(max)} = \frac{V_{pos}-V_{D(min)}}{R_g}.$$

ON State
In the ON state with all inputs high,

$$I_c = N.I_{in(max)} + \frac{V_{pos}}{R_c}$$

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where N is the required fan-out. Therefore,

$$I_c = \frac{V_{pos}}{R_c} + \frac{N(V_{pos} - V_{D(min)})}{R_g} . \qquad \ldots(8)$$

If R_g is equal to PR_c , Eq. 8 can be rewritten in terms of R_c thus:

$$R_c = \frac{N(V_{pos} - V_{D(min)}) + PV_{pos}}{PI_c} \qquad \ldots(9)$$

The transistor base current supplied by R_g is given by:

$$I_b = \frac{V_{pos} - V_{BE} - V_{fb}}{R_g} - \frac{V_{BE}}{R_b} . \qquad \ldots(10)$$

Now

$$I_c = h_{FE} I_b . \qquad \ldots(11)$$

Therefore, by substituting Eqs. 8 and 10 in Eq. 11 and rearranging,

$$N = \frac{h_{FE}(V_{pos} - V_{BE} - V_{fb})}{V_{pos} - V_{D(min)}} - \frac{R_g}{V_{pos} - V_{D(min)}} \left(\frac{h_{FE} V_{BE}}{R_b} + \frac{V_{pos}}{R_c} \right) .$$

Now since $\frac{V_{BE}}{R_b}$ is usually small compared with I_b , and since $V_{D(min)}$ is approximately equal to V_{BE} , the expression can be simplified to

$$N \simeq h_{FE} \left(1 - \frac{V_{fb}}{V_{pos} - V_{D(min)}} \right) - \frac{R_g}{R_c} \left(\frac{V_{pos}}{V_{pos} - V_{D(min)}} \right) ;$$

or,

$$\frac{R_g}{R_c} \simeq \frac{(h_{FE} - N)(V_{pos} - V_{D(min)}) - h_{FE} V_{fb}}{V_{pos}} \qquad \ldots(12)$$

Fig. 167—One gate feeding several others

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A ratio between collector and base resistors in terms of other circuit parameters has now been obtained.

Fan-out

So far, the fan-out has only been considered for the low state. The condition prevailing when one gate feeds several others is shown in Fig. 167. The output of gate 1 is assumed to be high. If one input of each of gates 2, 3, 4 and 5 is held at zero potential, the node points are also at approximately zero, and leakage current flows in diodes A, B, C and D. This leakage current flows in $R_{c(1)}$ and causes a voltage drop. At maximum fan-out, the sum of the leakage currents flowing in $R_{c(1)}$ must not reduce V_{out} below the permitted logical '1' level.

A.C. Conditions

When both inputs of the circuit shown in Fig. 168 are suddenly made positive, D_1 and D_2 are turned off and D_3, after the diode turn-on delay time, begins to conduct. Current begins to flow into the base of the transistor to turn it on.
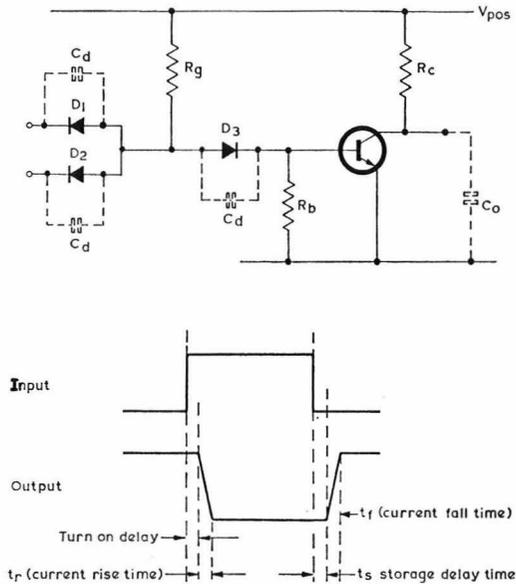
Fig. 168—NAND gate circuit and associated waveforms

During the turn-on delay, a certain charge must be supplied to the base, and so the greater the current which flows into the base, the shorter will be the time taken to supply the required charge. The delay is caused by two factors. One factor is the charge required by the internal emitter capacitance, C_{te}, to bring

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the transistor base voltage to the conduction level. This charging current flows via $r_{bb'}$ and the external base resistance. The other factor is the charge taken up by the collector depletion capacitance.

It can be shown that the delay times are given approximately by the following expressions

$$t_{D(1)} = C_{te}(R_g + r_{bb'})\log_e\frac{V_1 + V_2}{V_2} \qquad \dots(13)$$

where V_1 is the initial voltage below the conduction level, so that $V_1 + V_2$ is the total input voltage swing, and R_b is the base source resistance.

$$t_{D(2)} \simeq \frac{C_{tc}R_c}{1 + C_{tc}R_c\omega_T}, \qquad \dots(14)$$

where C_{tc} is the effective collector depletion capacitance, R_c is the collector load and ω_T is $2\pi \times$ the gain bandwidth product $= 2\pi f_T$.

Current Rise Time t_r (Voltage Fall Time)

The current rise time is determined by collector and circuit capacitances which have to be discharged via the transistor.

The charge which must be supplied is given by
$$Q_r = (C_{tc} + C_0)V_{pos}, \qquad \dots(15)$$
where C_0, is the external circuit capacitance.

The collector current is governed by the base resistor and source voltage and the transistor gain in the linear region. The base source voltage is V_{pos} for the gate being considered. Therefore
$$I_b = \frac{V_{pos}}{R_g},$$
and
$$I_c = h_{FE}I_b = h_{FE}\frac{V_{pos}}{R_g}.$$
The charge which must be supplied to the base is
$$Q_b = \frac{(C_{tc} + C_0)V_{pos}}{h_{FE}}$$
and the time taken to supply this charge via R_b is
$$t_r = \frac{Q_b}{I_b} = \frac{(C_{tc} + C_0)R_g}{h_{FE}} \qquad \dots(16)$$

Thus for t_r to be small, the transistor requires a high value of h_{FE} and at the same time C_{tc}, C_0 and R_g must be small. During the rise time a further current $(V_{pos} - V_{CE(sat)})/R_c$ must also be supplied by the transistor; therefore additional base current is required.

Turn-off Delay t_s

The turn-off delay is the desaturation delay, which depends on the level of base overdrive current applied and the rate at which base charge is removed during turn-off. Ideally, for fast switching, a reverse base current drive should be applied. For the circuit being considered here, however, the base forward current is interrupted and the base is taken to zero voltage via R_b. This has the effect of putting a small negative bias voltage equal to $-V_{BE}$ on the base

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terminal. The amount of reverse base current flowing is therefore very small and best desaturation times are not achieved.

A circuit which applies reverse base drive is shown in Fig. 169.

Some improvement in desaturation delay can be achieved by using a diode with higher capacitances than the input diodes for the coupling (d.c. shifting) diode. An approximation for t_s is then given by

$$t_s \simeq \frac{(I_{bt} - I_c/h_{FE})\tau_s}{I_{br}},$$

where I_{bt} and I_{br} are the forward and reverse base currents, and τ_s is the desaturation time constant. Typical figures for t_s in fast switching transistors in normal operation are 5 to 20ns with reverse base drive such as that shown in Fig. 169, and 20 to 100ns without reverse base drive, depending on the value of the external base resistor R_b of Fig. 168.
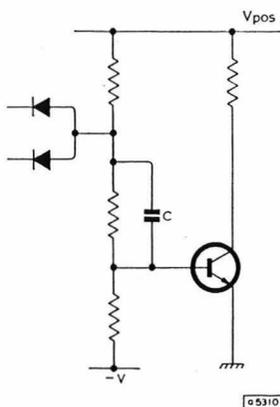
Fig. 169—Circuit with reverse base drive

Current Fall Time t_f (Voltage Rise Time)
When the transistor is cut off, at the end of the desaturation delay the current falls and the collector voltage rises. The rise time of the voltage is determined by R_c, C_{tc} and the load capacitance, C_o, and by the collector time constant $\tau_c(\simeq h_{FE}/\omega_T)$. In practice the time constant is usually determined by R_c in conjunction with the circuit capacitance, and the value of t_f is given by:

$$t_f \simeq 2 \cdot 2 R_c(C_{tc} + C_o). \qquad \ldots(17)$$

If the main consideration in designing a DTL gate of the type in Fig. 166 is speed, and no restrictions are introduced by the need to minimise operating current, the best performance is achieved by choosing the operating point where the transistor has maximum gain.

PRACTICAL DESIGN FOR A DTL GATE
If a gate of the type shown in Fig. 166 is required, with one forward-biased diode, it can be designed using the information given above.

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The BSX20 transistor has maximum value of h_{FE} at a current of about 8mA. To ensure good overdrive, even with minimum h_{FE} samples, a saturated value of h_{FE} of 15 is assumed. This also allows for the small error introduced by neglecting the current in R_b. Other parameters taken for the design are:

$$I_c = 8mA$$
$$V_{pos} = 6V$$
$$\left.\begin{array}{l} V_D = 0{\cdot}6V \\ V_{fb} = 0{\cdot}6V \end{array}\right\} BAX13\ diodes$$
$$fan\ out\ N = 5$$
$$C_{tc} = 4pF;\ C_{te} = 4{\cdot}5pF.$$

From Eq. 12:

$$\frac{R_g}{R_c} = \frac{(15-5)(6-0{\cdot}6)-15\times0{\cdot}6}{6}.$$

Therefore

$$\frac{R_g}{R_c} = 7{\cdot}5 = P. \qquad \ldots(18)$$

Putting this value in Eq. 9 gives

$$R_c = \frac{7{\cdot}5\times6+5(5{\cdot}4)}{7{\cdot}5\times8\times10^{-3}}$$
$$= 1{\cdot}2k\Omega.$$

Therefore from Eq. 18,

$$R_g = 7{\cdot}5\times1{\cdot}2k\Omega = 9k\Omega.$$

The nearest 10% value to this is $8{\cdot}2k\Omega$ and the nearest 5% value is $9{\cdot}1k\Omega$.

The base current which would be supplied in the absence of R_b, assuming the $8{\cdot}2k\Omega$ value, would be

$$\frac{V_{pos}-V_D-V_{BE}}{R_g} = \frac{4{\cdot}8}{8{\cdot}2\times10^3} = 575\mu A.$$

If R_b is also $8{\cdot}2k\Omega$ and a maximum value of V_{BE} of $0{\cdot}75V$ is assumed, at the operating current, R_b will take $92\mu A$, leaving a base current of about $480\mu A$.

The minimum saturated value of h_{FE} which could be tolerated may now be seen to be

$$\frac{I_c}{I_b} = \frac{8}{0{\cdot}48} \simeq 17.$$

The turn-on delay time is determined by $t_{D(1)}$ (Eq. 13) and $t_{D(2)}$ (Eq. 14).

$$t_{D(1)} = 4{\cdot}5\times10^{-12}\times8{\cdot}2\times10^3 log_e\frac{6}{5{\cdot}3}$$
$$= 4{\cdot}4ns$$
$$t_{D(2)} \simeq \frac{4\times10^{-12}\times1{\cdot}2\times10^3}{1+4\times10^{-12}\times10^3\times2\pi\times500\times10^6}$$
$$= 0{\cdot}3ns$$

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Therefore
$$t_d \simeq 4 \cdot 7 \text{ns}.$$
In practice, a slightly longer turn-on delay than this must be expected since no account of the diode performance has been taken.

The rise time as given by Eq. 16 is:
$$t_r = \frac{(4+5) \times 10^{-12} \times 8 \cdot 2 \times 10^3}{20} = 3 \cdot 7 \text{ns}.$$

This is based on stray and load capacitances of 5pF and a minimum value of h_{FE} in the active region of 20.

The turn-off delay is determined more by transistor parameters than by the circuit constants. A desaturation time of some 40ns may be expected.

The fall time, from Eq. 17, is:
$$t_f = 2 \cdot 2 \times 1 \cdot 2 \times 10^3 (4+5) \times 10^{-12} \text{ seconds}$$
$$\simeq 24 \text{ns}.$$

In this expression, the value of C_o, the load capacitance, contributes largely to the fall time.

APPENDIX 2

SIMPLIFIED DESIGN PROCEDURE FOR BISTABLE CIRCUITS

DESIGN OF A BISTABLE CIRCUIT FOR USE AT HIGH FREQUENCIES
The simplified design procedure in this appendix relates to the type of circuit shown in Fig. 170. Speed-up capacitors and recovery diodes are included in this diagram, but their effects on the operation of the circuit will not be discussed until after the basic design procedure.
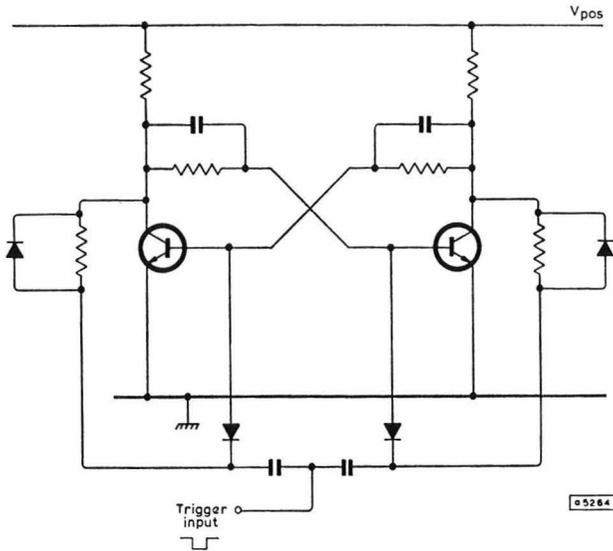
Fig. 170—Bistable circuit

D.C. Conditions
A bistable circuit is shown in Fig. 171. Circuits of this type are normally symmetrical; that is, the two base resistors are equal and the two collector resistors are equal. The value of the collector resistor depends, in practice, upon the external loading. For the purposes of this explanation, R_{cH} will be used to denote the maximum value of R_c—normally the value which is effective in the OFF state—and R_{cL} will be used to denote the effective collector load in the ON state; that is, when current is being supplied to external loads. If TR_2 is

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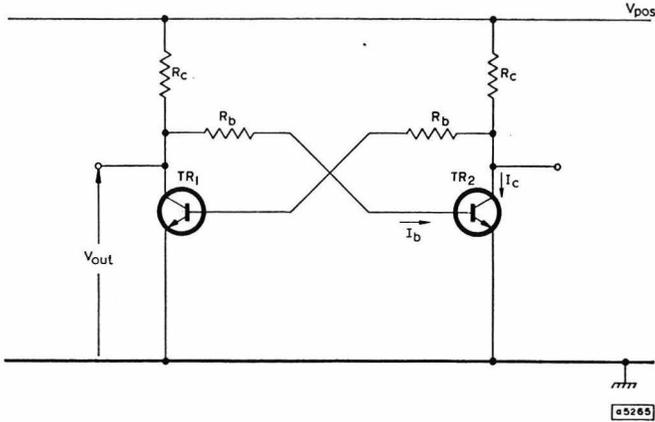
Fig. 171—Bistable circuit showing d.c. conditions

assumed to be conducting, the output voltage at the collector of TR_1 is given by

$$V_{out(high)} = \frac{(V_{pos} - V_{BE})R_b}{R_b + R_{cH}} + V_{BE}$$

or

$$V_{out(high)} = V_{pos} - \frac{(V_{pos} - V_{BE})R_{cH}}{R_{cH} + R_b}. \qquad \ldots(19)$$

For TR_2 to remain in saturation, the value of the collector current is given by:

$$I_c = \frac{V_{pos} - V_{CE\,(sat)}}{R_{cL}}, \qquad \ldots(20)$$

and the base current is given by,

$$I_b = \frac{V_{pos} - V_{BE}}{R_{cH} + R_b}. \qquad \ldots(21$$

The minimum gain that can be tolerated is given by:

$$h_{FE(sat)} = \frac{I_c}{I_b}, \qquad \ldots(22)$$

and therefore, by substituting Eqs. 20 and 21 in Eq. 22;

$$h_{FE(sat)} = \frac{(V_{pos} - V_{CE(sat)})(R_{cH} + R_b)}{(V_{pos} - V_{BE})R_{cL}}. \qquad \ldots(23)$$

The value of $h_{FE(sat)}$ obtained from Eq. 23 is the minimum value required to keep the transistor in saturation. In practice, however, to obtain maximum speed of operation, base overdrive is normally used. The base overdrive factor is usually between 2 and 5, but if the overdrive factor is γ, the minimum value of $h_{FE(sat)}$ is given by:

$$h_{FE(sat)} = \frac{\gamma(V_{pos} - V_{CE(sat)})(R_{cH} + R_b)}{(V_{pos} - V_{BE})R_{cL}}. \qquad \ldots(24)$$

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The choice of suitable values for operating current and load resistors depends upon several factors.

(1) The transistor should be in a high gain region of its characteristic over the whole range of operating current—from no load to full fan-out.

(2) The value of R_c affects the speed of operation because the collector voltage rise time is partly determined by this resistance.

(3) The operating current may need to be kept low to limit the power consumption and dissipation.

In the example considered here, it is assumed that the design is for a fast counting bistable circuit using BSX20 transistors, or BSX19 transistors when a lower fan-out is required. The supply voltage is assumed to be +6V. The BSX19 and BSX20 transistors have maximum gain at currents between 7 and 15mA. In this example, it is assumed that the bistable circuit is required to drive gates which could require a total current of 15mA and that it is capable of driving further similar bistable circuits.

To obtain a short voltage rise time at the collector, the value of R_c should be low. Too low a value, however, would cause the transistor to operate at a high current where the gain is reduced, particularly with full fan-out loading. Operation at too low a current—for example, 1mA—increases the collector voltage rise time and therefore limits the speed of operation, in spite of the fact that the transistor has sufficient gain at 1mA. For this condition, the collector load would be a maximum of 6kΩ and, if C_{tc} has a value of 4·5pF and the stray capacitances a further 5pF, the collector time-constant is 57ns which is too long for operation at frequencies of 5 to 10MHz. To maintain the operating speed, therefore, a compromise must be found.

In this example, a no-load collector current of 5mA is assumed, giving a value of 1·2kΩ for R_c and a collector time-constant of about 12ns. The total operating range of collector current is then from 5 to 20mA over which range the transistor has a high gain. The minimum output voltage from the stage is required to be 4V. The outline specification of the bistable circuit is summarised in Table 79.

TABLE 79

Outline Specification of Bistable Circuit

V_{pos}	=	+6V
$V_{CE(sat)}$	=	0·1V
I_c (unloaded)	=	5mA
Fan-out current (min)	=	15mA
Output voltage (min)	=	4V
Base-emitter voltage	=	0·7V
Counting speed (min)	=	10MHz
Resistor tolerances	=	±10%

The specification given in Table 79 enables values to be substituted in the equations obtained earlier in this appendix.

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Calculation of R_{cH}

The value of R_{cH} is given by

$$R_{cH} = \frac{V_{pos} - V_{CE(sat)}}{I_{C(no\ load)}},$$

therefore

$$R_{cH} = \frac{5 \cdot 9}{5} \simeq 1 \cdot 2k\Omega.$$

Calculation of R_{cL}

From Eq. 20

$$R_{cL} = \frac{V_{pos} - V_{CE(sat)}}{I_{c(max)}},$$

therefore

$$R_{cL} = 0 \cdot 3k\Omega.$$

Calculation of R_b

Rearrangement of Eq. 19 gives

$$R_b = R_{cH}\left[\frac{V_{pos} - V_{BE}}{V_{pos} - V_{out(high)}} - 1\right]. \qquad \qquad \ldots(25)$$

Therefore, by substituting in Eq. 25 with R_{cH} at its highest value within the specified tolerance

$$R_{b(min)} = 1 \cdot 32\left[\frac{6 - 0 \cdot 7}{6 - 4} - 1\right]$$
$$= 2 \cdot 17k\Omega$$

The minimum preferred value that can be used is $2 \cdot 7k\Omega$, with a range of $2 \cdot 43$ to $2 \cdot 97k\Omega$.
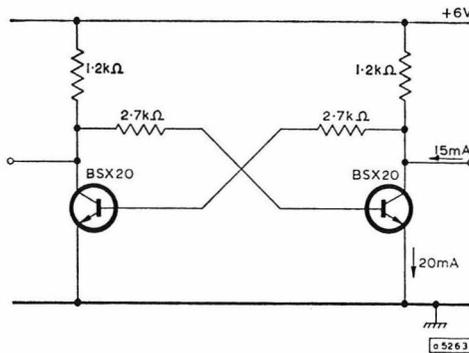
Fig. 172—D.C. circuit of bistable example

Calculation of Overdrive Factor

From Eq. 24

$$\gamma = \frac{h_{FE(sat)}(V_{pos}-V_{BE})R_{cL}}{(V_{pos}-V_{CE(sat)})(R_{cH}+R_b)}$$

The maximum values of R_{cH} and R_b are $1.32k\Omega$ and $2.97k\Omega$ respectively, and the minimum value of h_{FE} for a BSX20 transistor is 40. Therefore the minimum value of γ is given by

$$\gamma = \frac{40(6-0.7)0.3}{5.9(1.32+297)}$$
$$= 2.49$$

The maximum overdrive factor with a value of h_{FE} of 120 is 7.35.

The basic d.c. circuit of the bistable element is shown in Fig. 172.

A.C. Conditions

The basic d.c. circuit, with the addition of triggering and steering elements, is shown in Fig. 173. BAX13 diodes are used because of their high operating speed.
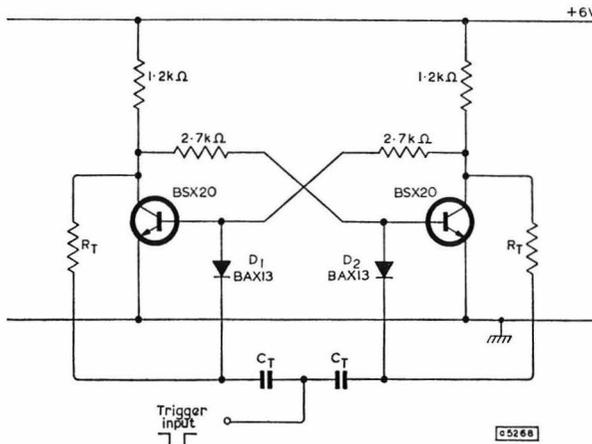
Fig. 173—Basic triggered bistable circuit

For the bistable element to be used as part of a counting circuit, it must be capable of being triggered from the output of a similar stage; that is, by a minimum voltage of 4V. However, in counting circuits using feedback or feedforward, the trigger input may be fed via gating circuits across which a voltage drop occurs. For the purpose of this example, a minimum triggering voltage of 2.5V is assumed.

If the input pulse has a very fast negative-going edge, C_T need only be sufficiently large to turn the conducting transistor off with a 2.5V input, and to hold it off for at least the desaturation time of the transistor. From the published

data for the BSX20, the total turn-off time is 18ns when I_c is 10mA, I_b (on) is 3mA and I_b (off) is -1.5mA. In the circuit derived so far, the maximum forward base current is 1.5mA and the worst case for speed consideration is when this base current is used with the minimum collector current of 4.5mA; that is, with the device heavily in saturation. In this case the effective value of h_{FE} is 3. Provided that C_T supplies sufficient reverse base current, the turn-off time may be expected to be less than 18ns.

When the input voltage falls, either D_1 or D_2 conducts. Thus, with a negative pulse of 2.5V on the input terminal, the transistor base potential falls from $+0.7$ to -1.8V. Capacitor C_T must now absorb the 1.5mA base current from the coupling resistors and must provide a reverse base current of at least 1.5mA. The current flowing through C_T during turn-off is therefore about 3mA. The voltage on C_T must not rise by more than 30% during the turn-off time, because if it did, the turn-off current would not be maintained and the turn-off time would be increased. The value of the charge, Q, is given by:

$$Q = I \times t,$$

therefore
$$Q = 3 \times 10^{-3} \times 18 \times 10^{-9} \text{ coulombs}$$
$$= 54\text{pC}$$

The change in voltage on C_T has been assumed to be less than 0.66V.

Now the value of C is given by

$$C_T = \frac{Q}{V},$$

therefore
$$C_T = \frac{54 \times 10^{-12}}{0.66} \text{farads}$$
$$= 82\text{pF}.$$
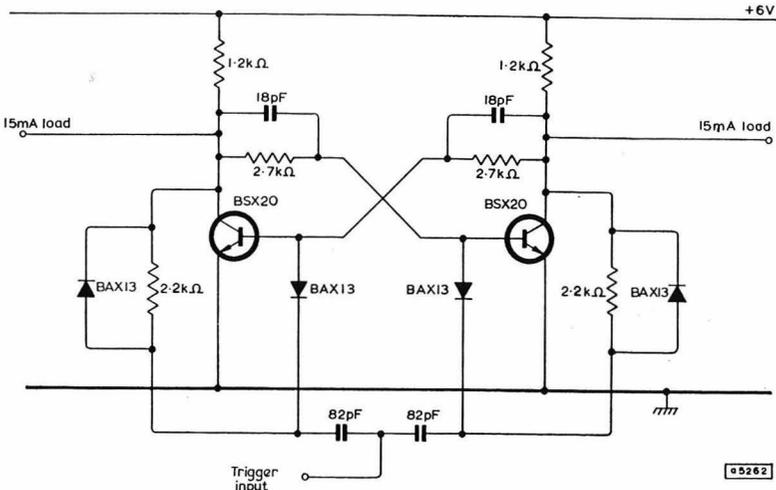
Fig. 174—Complete bistable circuit

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Capacitor C_T must be able to discharge through R_s in two count periods. Therefore, for an operating frequency of 10MHz, the time-constant $C_T R_T$ should be less than 200ns if maximum trigger sensitivity is to be maintained. Therefore;

$$R_T = \frac{200 \times 10^{-9}}{82 \times 10^{-12}} \, \Omega$$
$$= 2 \cdot 43 k\Omega$$
$$\simeq 2 \cdot 7 k\Omega.$$

To conduct the positive edges of the trigger pulses away, diodes are connected across R_T. The value of speed-up capacitance is usually between 10 and 20% of the triggering capacitance. Speed-up capacitors of 18pF provide rapid turn-on, and add little to the triggering voltage requirements. The complete circuit is shown in Fig. 174 and the measured performance is given in Table 80.

TABLE 80
Measured Performance of Bistable Circuit

Maximum counting frequency (no load)	=	25MHz
Maximum counting frequency (resistive load, $I_{load} = 15mA$; triggering voltage = 4V)	=	30MHz
Minimum trigger input (capacitive load, load capacitance $\leqslant 100pF$, $I_{load} = 15mA$, f = 1MHz)	=	1·7V
Maximum input fall time (amplitude = 2·5V, f = 1MHz)	=	50ns
Output fall time	=	15ns
Maximum counting frequency as a binary counter	=	15MHz
Maximum counting frequency as a one-gate decade	=	13MHz

The circuit components may be altered to suit different operating requirements. For example, if the bistable circuit is not required to supply a d.c. load the collector resistors may be reduced to maintain good performance when driving capacitive loads and thereby to obtain a better performance as a binary counter and decade counter. If a lower operating speed is acceptable, the recovery diodes and the speed-up capacitors may be omitted.

In the example given above, the effect of omitting these components were as follows.

Omitting the recovery diodes reduced the operating frequency at the nominal input voltage of 4V to 6MHz and reducing the input voltage to 2·5V reduced the maximum operating frequency to 3MHz. These frequencies applied for a 15mA resistive load. When a 100pF load was added, the operating frequency was reduced to 4MHz with a 4V input.

Omitting the speed-up capacitors whilst retaining the recovery diodes reduced the operating frequency from 30MHz to 14MHz under full load conditions with an input between 2·5 and 4V. The waveform at the output was, however, very poor at this frequency, particularly with capacitive loading.

Omitting the speed-up capacitors and the recovery diodes reduced the operating frequency to 1·2MHz with a 5V input and 3MHz with a 7V input. The nominal input voltage of 4V failed to trigger the bistable circuit. Raising the

voltage to 5V gave an operating frequency of 1·2MHz and raising the voltage to 7V gave a frequency of 3MHz.

BISTABLE STAGE FOR MEDIUM AND LOW FREQUENCY OPERATION USING THE BC108 TRANSISTOR

The elements of a bistable stage operating from a 12V supply at medium or low frequencies are shown in Fig. 176. For this example, the required output voltage is assumed to be 8V and the required operating frequency is assumed to be 1MHz.

The value of C_{tc} for the BC108 transistor is 4·5pF, and 10pF is added for wiring capacitances because of the less critical layout of low-speed circuits. The maximum load resistor is chosen to give a collector time-constant, of about 50ns. The values of the collector resistors is, therefore, 3·3kΩ. The value of V_{BE} is again assumed to be 0·7V. These values may now be substituted in Eq. 7 to obtain the minimum value of R_b.

$$R_{b(min)} = 3·63\left(\frac{12-0·7}{12-8} - 1\right)k\Omega$$

$$= 6·65k\Omega.$$

The minimum resistance of an 8·2kΩ±10% resistor is 7·38kΩ, but the minimum value of a 6·8kΩ resistor is only 6·12kΩ which is too low. If the fan-out
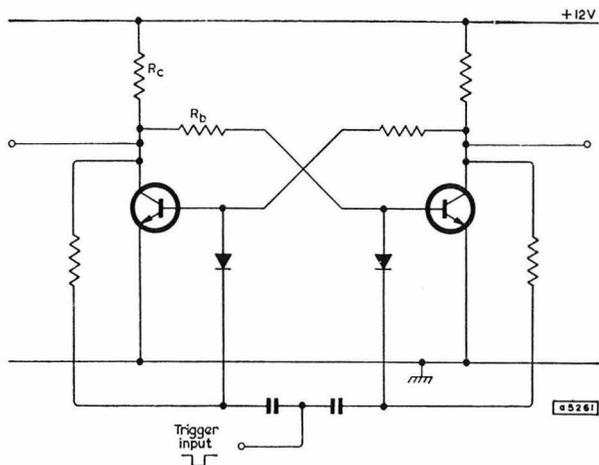
Fig. 175—Elements of a 12V bistable circuit

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d.c. current is 10mA, the total effective value of R_{cL} is given by:

$$R_{cL} = \frac{V_{pos}}{\dfrac{V_{pos}}{R_c} + I_{load}}$$

$$= \frac{12}{\dfrac{12}{3\cdot3} + 10} \, k\Omega$$

$$= 0\cdot87k\Omega$$

Therefore, from Eq. 24

$$\frac{h_{FE}}{\gamma} = \frac{(12-0\cdot1)\times(8\cdot2+3\cdot3)}{0\cdot87(12-0\cdot7)}.$$

$$= 14$$

The minimum value of h_{FE} for the BC108 is about 100 at 10mA in saturation. This gives a minimum value of γ of 7·1, which is a high overdrive factor. The resistor values are shown on the circuit given in Fig. 176, and from these values the maximum value of I_b can be calculated.
From Eq. 3

$$I_{b(max)} = \frac{V_{pos}-V_{BE}}{R_{c(min)}+R_{b(min)}} = \frac{12-0\cdot7}{7\cdot38+2\cdot97}mA$$

$$= 1\cdot1mA$$
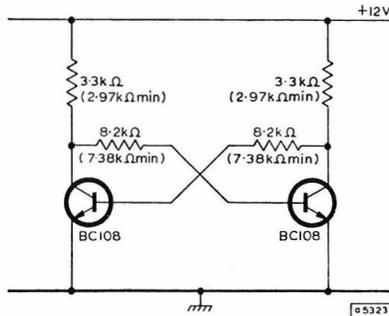
Fig. 176—Bistable circuit showing minimum values

The steering capacitors must remove this current during the desaturation time, which has a maximum value of 500ns. They must also remove a stored charge from the base of the transistor which can have a value of up to 500pC. The total charge to be removed therefore is given by

$$Q_{tot} = Q_S+I_b t_s$$
$$= 500+1\cdot1\times10^{-3}\times500\times10^{-9} \text{ coulombs}$$
$$= 1050pC$$

The output voltage level of this bistable circuit is approximately 8V and it is this voltage which is available to drive subsequent stages. Because of this high

output voltage, it is reasonable to design the stage to operate with a minimum input voltage of 5V, giving a negative base voltage of 4·3V. If the base voltage is allowed to change by 30% as a result of absorbing the total charge calculated above, the value of the capacitor may be calculated as follows. The value of C is given by

$$C = \frac{Q}{V},$$

therefore

$$C = \frac{1050 \times 10^{-32}}{1·3}$$
$$= 800pF.$$
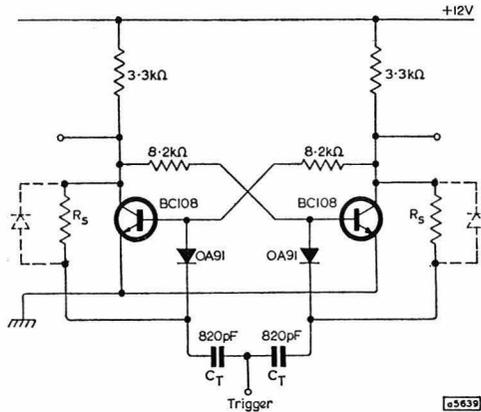
Fig. 177—Bistable circuit using a BC108 transistor
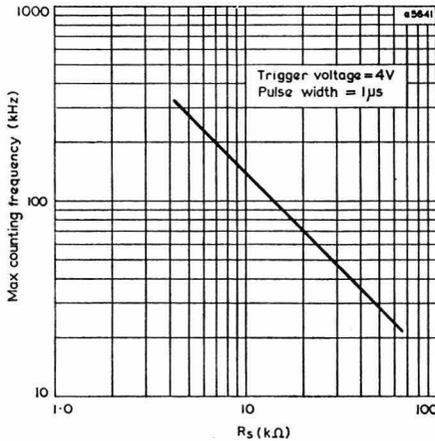
Fig. 178—Measured performance of a bistable circuit using a BC108 transistor, showing how the counting frequency depends upon the value of R_S

The steering resistors should completely discharge the trigger capacitors in two pulse periods. The use of too low a value of steering resistance causes distortion of the output waveform because R_S and R_C form a potential divider to the trigger voltage, and part of the trigger waveform appears at the collector. For this reason, it is not always practicable to use as low a value of resistor as might at first seem desirable, but better speed performance can be obtained by using a higher value of resistance together with recovery diodes.

Steering capacitances should not be reduced below about 390pF, since to do so would require excessively high input voltages in some cases.
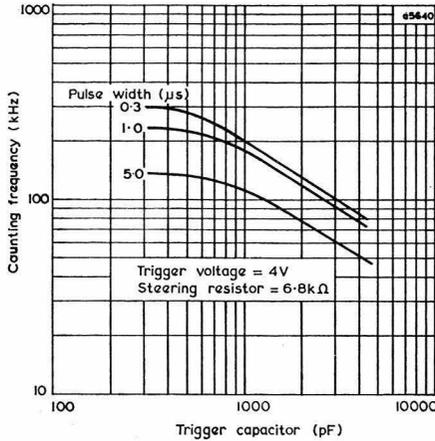
Fig. 179—Measured performance of a bistable circuit using a BC108 transistor, showing how the counting frequency depends upon the value of the trigger capacitor

A counting stage using a BC108 transistor is shown in Fig. 177. The following performance details were obtained by measurement on a prototype counting stage made to the circuit shown in Fig. 177. These performance details are included here chiefly to illustrate the effect of adding speed-up capacitors and recovery diodes and varying other values.

With the basic circuit the output voltage rise time and fall time had values of 100ns and 65ns respectively. By adding 39pF speed-up capacitors, the rise time was increased to 280ns and the fall time was reduced to 30ns. By adding recovery diodes, the maximum operating frequency is increased from 135kHz to 1·3MHz. The effect of varying R_S is shown in Fig. 178 and the effect of varying C_T with one bistable circuit feeding a second similar stage, is shown in Fig. 179.

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