mble

APPLICATION BOOK

M.B.L.E ELECTRONICS
80 Rue des Deux-Gares, Bruxelles 7

MEASUREMENT AND CONTROL
USING 40-SERIES MODULES

OPERATIONAL AMPLIFIERS
DIFFERENTIAL ZERO DETECTOR
PHASE SHIFT MODULE

ERRATUM

Application Book "Measurement and Control using 40-Series Modules".

In the circuit diagram on page 133 a few connections are missing.
The correct diagram is given below.

Fig. 10.1(a). Tachometer circuit.

Measurement and Control using 40-Series Modules

Measurement and Control using 40-Series Modules

Operational Amplifiers
Differential Zero Detector
Phase Shift Module

Edited by **W. R. Easey**

Contents

Foreword

The next decade will show a continued penetration of electronics in the field of instrumentation and control. There are two main reasons to support this forecast: firstly, as industrial processes become more complex, the use of electronic control is almost mandatory; secondly, the existence of more and more electronic circuits, particularly as simple modules, itself suggests control applications which may otherwise remain unthought of. These two mutually stimulating influences lead us to expect not only a continued, but an increased rate of penetration.

In the digital field, standard series of modules from which systems could be built up, were introduced some time ago and have been very successful.

To realize the same basic facility in analogue systems, the 40-Series, presented to you in this publication, has been introduced. Each of the four component modules is a versatile electronic tool which can be used to perform many functions. We hope that the practical applications, backed by a little theory, presented herein will stimulate the imagination of the reader, and lead to the same acceptance of the 40-Series as that derived for the digital series by earlier books.

Dr. W. K. Westmijze

Acknowledgement

1 Introduction

Modern industrial processes rely heavily on automatic control; this has led to a renewed interest in the use, and an improvement in the design, of operational amplifiers and other devices associated with analogue and hybrid analogue/digital systems. The main requirements for these devices are reliability, serviceability, small size and minimum cost. The production of this type of device as modules enables all of these requirements to be met and also creates a new flexibility in system design.

The four 40-Series modules which form the subject of this publication are the DOA40 and DOA42 operational amplifiers; the DZD40 differential zero detector, and the PSM40 phase shift module. These modules lend themselves to an extremely wide range of applications, and the principal sections of this publication deal with building various combinations of the modules into systems.

The systems described include a selection of open- and closed-loop designs which have been built and used by various sections of industry. However, it is not the intention to give the impression that these are rigid designs; rather that they are solutions to everyday problems related to control and monitoring systems.

It is possible that one of these applications exactly fits a particular requirement, although it is more probable that whereas the concept is suitable, the practical values require modification. Therefore some sections of the publication give information which will enable an engineer to adapt the systems presented and to design his own systems from first principles. Our team of application engineers is always available to give advice and assistance on your particular problem.

The last section is intended for the engineer who has not had the opportunity to become fully acquainted with the underlying principles and techniques related to the design and use of operational amplifiers.

1

2 Description of the DOA40 and DOA42 Modules

The DOA40 and DOA42 modules are both high gain, wide band d.c. differential amplifiers which feature low drift characteristics. They are designed to operate from power supplies of $+15$ V and -15 V, but supplies of $+12$ V and -12 V can be used if reduced output characteristics are acceptable. Full technical data is given in Section 11. Each of the two modules comprises a circuit which is potted inside a metal casing; connections are made to the DOA40 by 19 wire terminals and to the DOA42 by 12 pin terminals. Dimensional drawings and terminal locations are given in Figs. 2.1 (DOA40) and 2.2 (DOA42).

Fig. 2.1. DOA40: dimensional drawing and terminal location.

5.1
min
14.1
□ 30.7
0.8

7258797

● C
● k_2
● E_2
● -in
● +in
● E_1
● k_1

+V ●
0V ●
-V ●
out ●
tr ●

7258798

$+V$	$=$	positive supply voltage
$-V$	$=$	negative supply voltage
$0\ V$	$=$	earth and housing
$+In$	$=$	non-inverting input
$-In$	$=$	inverting input
k_1 k_2	$=$	terminals for external freq. compensation

Trim	$=$	for external offset correction
Out	$=$	amplifier output terminal
E_1	$=$	emitter 1
E_2	$=$	emitter 2
C	$=$	collector

Fig. 2.2. DOA42: dimensional drawing and terminal location.

2.1. Circuit Description of the DOA40 Module

The DOA40 operational amplifier incorporates a 6 dB/octave roll-off network to ensure stable operation with all types of feedback. The internal network can be left disconnected and replaced by an external frequency compensation network to increase response times in, e.g. open-loop applications. Also, the input offset voltage can be corrected to zero by an externally connected potentiometer.

3

Fig. 2.3. DOA40: circuit diagram.

The circuit, shown in Fig. 2.3, comprises three stages. Two differential amplifier stages, TR_1 and TR_4 with an associated current sink circuit, TR_2 and TR_3, are used to obtain low drift performance. The third stage is formed by common emitter output amplifier TR_5; TR_6, in the collector circuit of TR_5, is a current sink and limits the dissipation of the output stage. High common mode rejection is ensured by negative feedback to the base of TR_3, via the potential divider R_1, R_2 in the emitter of TR_4. The internal frequency compensation network comprises R_3, C_1 and is connected between the two collectors of TR_1 by short-circuiting terminals 2 and 12. Alternatively, an external network can be connected between terminals 2 and 4. Initial offset voltage can be compensated by an external 15 kΩ potentiometer connected between terminals 6 and 19.

2.2 Circuit Description of the DOA42 Module

The DOA42 operational amplifier incorporates a frequency compensation

circuit which is effective at closed-loop gains equal to, or in excess of, 40 dB ($\times 100$). For stable operation at lower values there is provision to connect an external RC frequency compensating network. Details of this network are given in Section 11. Also, the input offset voltage can be corrected to zero by an externally connected potentiometer.

Features which distinguish this module from the DOA40 are:
– low input current (< 20 nA)
– high input impedance (> 5 MΩ)
– lower common mode voltage ($+5$ V and -5 V)
– the unique facility of allowing a very high differential input impedance *for both inputs* when used as a difference amplifier with feedback.
The circuit of the DOA42 module is shown in Fig. 2.4. Input signals are fed to two Darlington pairs which are connected as a long-tailed pair input stage (TR_1, TR_2 for $+$in, TR_3, TR_4 for $-$in) which feed a long-tailed pair difference amplifier, TR_5, TR_6. Transistor TR_6 is the current

Fig. 2.4. DOA42: circuit diagram.

5

source for the Darlington input circuit. The difference signal from the long-tailed pair TR_5, TR_6 is fed via emitter-follower TR_8 to voltage amplifier TR_9 which forms part of the output stage. Complementary emitter-followers TR_{10} and TR_{11} complete the output stage and provide a high current gain/low impedance output. Diodes D_3 and D_4 protect the output transistors in the event of a short-circuited output.

The frequency compensation network is formed by RC network C_1R_1 and C_2R_2; terminals k_1 and k_2 allow the connection of external networks for gains below 40 dB. Offset voltage may be adjusted to zero by a 25 kΩ potentiometer connected between the terminals *Trim* and $+V$.

2.3 Some Basic Feedback Configurations using DOA40 and DOA42 Modules

This section presents an analysis of some of the more commonly encountered basic operational amplifier circuits. The circuits are dealt with both theoretically and from a practical aspect with regard to the use of DOA40 and DOA42 modules.

Most of the practical circuits described in subsequent sections of this book can be reduced to one of these basic circuits.

2.3.1 INVERTING AMPLIFIER

The principal feature of the inverting amplifier is the capacity for reducing the gain below unity. The basic circuit is shown in Fig. 2.5(a), the input and feedback impedances R_i and R_f being purely resistive. High accuracy

Fig. 2.5(a). Inverting amplifier.

Fig. 2.5(b). DOA42 as an inverting amplifier.

6

and a gain which is directly proportional to R_1/R_f (transfer function $V_0/V_i = -R_f/R_1$) facilitates the provision of gain adjustment by steps. In general the inverting amplifier cannot be regarded as a high input impedance circuit and should not, therefore, be chosen for use in conjunction with high impedance signal sources. However, the DOA42 does not suffer this limitation and can be used as an inverting amplifier with high input impedance (Fig. 2.5(b))

As stated above, the transfer function is $V_0/V_i = -R_f/R_1$, however, this expression assumes that the open-loop gain A_{ol} and differential input impedance Z_{id} are infinite, and that the open-loop output impedance Z_o is zero. In a practical circuit these conditions cannot be realized and the transfer function becomes:

$$\frac{V_0}{V_i} = -\frac{R_f}{R_1} \cdot \frac{X}{Y}$$

where

$$X = 1 + \frac{Z_0}{A_{ol}R_f}$$

and

$$Y = 1 - \frac{1}{A_{ol}}\left\{1 + \frac{Z_0}{R_1} + \frac{Z_0}{Z_{id}} + \frac{R_f}{R_1} + \frac{R_f}{Z_{id}} + \frac{Z_0}{Z_l}\left(1 + \frac{R_f}{R_1} + \frac{R_f}{Z_{id}}\right)\right\}$$

where Z_l is the load impedance.

From the foregoing expression the cumulative error D can be derived as a percentage of the ideal transfer functions; this error is given approximately by:

$$D = \frac{A_{ol}}{100}\left(1 + \frac{R_f}{R_1} + \frac{R_f}{Z_{id}}\right)\left(1 + \frac{Z_0}{Z_l} + \frac{Z_0}{R_f}\right) \%.$$

Substitution of the data given in Section 11 enables the value of D to be calculated for any feedback and input impedance.

For a quick check of input and output impedances to be made, the following approximate expressions may be used. These are: input impedance $= R_1$, and output impedance $= Z_0/A_{ol}(1 + R_f/R_1)$.

Details of the gain-frequency characteristics are given in Section 12.8, and output voltages due to voltage and current offset, and drift, are explained in Section 12.7. An example of drift compensation is given overleaf.

With $R_1 = 2.5$ kΩ, $R_f = 25$ kΩ, and drift compensated for one temperature, application of the DOA40 yields an output voltage drift according to:

$$v_o = v_d \left(1 + \frac{R_f}{R_1} \right) + i_d R_f$$

where $v_d =$ offset voltage drift and $i_d =$ bias current drift. Substituting maximum values the worst possible case is given by:

$$v_0 = 5 \times 10^{-6} (1 + 10) + 7 \times 10^{-9} \times 25 \times 10^3 = 230 \ \mu\text{V/degC}.$$

By connecting a resistance R_c between the positive terminal and ground, the bias current drift in the foregoing expression is replaced by the offset current drift, i_{dd}.

$$R_c = \frac{R_1 R_f}{R_1 + R_f} = 2.275 \text{ k}\Omega;$$

hence the maximum total drift is reduced to 80 μV/degC.

It was stated previously that the inverting amplifier cannot be regarded as a high input impedance circuit; the reason for this is that the value of R_1 is limited. From the expression for D (percentage error) it is apparent that a high value of R_1 leads to a deterioration of loop gain. Also, as the value of R_1 is increased, for a stated gain the value of R_f becomes very high; this results in a high output voltage due to offset and drift ($i_d R_f$). In general this can be overcome by using the DOA42 module; the input current drawn is very low, and the offset and drift are reduced accordingly.

Increased Effective Value of Feedback Resistance

Another difficulty encountered when applying high values of R_1 and R_f is that resistors in the normal range of types suffer a lack of stability. This problem can be overcome by applying a voltage divider circuit at the output as depicted in Fig. 2.6. The voltage gain of the circuit is:

$$\frac{V_0}{V_1} = -\frac{R_f}{R_1} \frac{R_3 // R_f + R_2}{R_3 // R_f} \approx -\frac{R_f}{R_1} \cdot \frac{R_2}{R_3} = -1000$$

($R_3 // R_f =$ the impedance of R_3 in parallel with R_f).

This method of increasing the effective value of the resistance can be applied in several configurations and is also applicable to R_1. However, it should be noted that the effective value of R_f must be substituted in

the expressions for offset voltage and current. Note that for drift calculation (v_o) the *effective* value of R_f (i.e. 1 MΩ) must be used.

Fig. 2.6. Output voltage divider.

Signal Source with Varying Source Impedance

If the source impedance (R_s) of the input signal source is subject to large variations or spreads, the voltage gain A_{cl} will also vary. The possibility of choosing a value of R_1 which is much greater than R_s suggests an apparent solution, but the problems encountered with high values of R_1 and R_f will then arise. A method of coping with such a source impedance is given by the circuit of Fig. 2.7; while $R_s \ll Z_{id}$, variations of R_s have no influence on the closed-loop gain, while for values of R_s approaching Z_{id}, only the accuracy is impaired. Another way of overcoming this problem is to use the circuit shown in Fig. 2.5(b).

Fig. 2.7. Input from varying source impedance.

Inverting A.C. Amplifier

A useful application of the operational amplifier is its use as an a.c. amplifier, where low frequency signals below the range of conventional amplifiers are used. An advantage of this amplifier is that the d.c. output voltage, and hence d.c. shift, is heavily suppressed.

The basic circuit of the inverting a.c. amplifier is shown in Fig. 2.8 (a non-inverting a.c. amplifier is discussed in Section 2.3.2).

The closed-loop gain is given by:

$$A_{cl} = \frac{-R_f}{R_1 + \dfrac{1}{j\omega C_i}} = \frac{-R_f}{R_1} \cdot \frac{1}{1 + \dfrac{1}{j\omega C_i R_1}}.$$

Thus voltage gain is:

$$\frac{V_0}{V_i} = \frac{R_f}{R_1} = -10 \quad \text{if} \quad j\omega C_i R_1 \gg 1,$$

and the lower frequency at which the 3 dB down point occurs is given by:

$$j\omega C_i R_1 = 1,$$

hence:

$$f = \frac{1}{2\pi C_i R_1} = 0.5 \text{ Hz.}$$

The d.c. shift of the output voltage is mainly due to offset current drift with temperature change, i.e. $v_o = i_{dd} R_f$.

For the DOA40 this is 1 mV/degC.

Fig. 2.8. Inverting a.c. amplifier.

Current Driven Load

The circuit in Fig. 2.9 shows the method of connection for a load which requires a current drive. The current in the feedback loop, and hence in the load, follows the relationship $I_L = V_i/R_1$.

10

Fig. 2.9. Current driven load.

2.3.2 NON-INVERTING AMPLIFIER

The principles involved in the non-inverting amplifier are explained in Section 12.4; its main features are:
- the closed-loop gain is independent of source impedance. Thus low values of R_1 can be chosen for high gain circuits.
- a very high input impedance makes it possible to use input signals from high impedance sources. The input impedance Z_{in} is the parallel impedance of the Z_{cm} (common mode impedance) and the effective differential input impedance $Z_{id} \cdot A_{ol}/A_{cl}$ $(= A_{ol}Z_{id} \cdot R_1/(R_1 + R_f)$ (see Section 12.4).

The transfer function of the circuit shown in Fig. 2.10 is:

$$\frac{V_0}{V_i} = 1 + \frac{R_f}{R_1},$$

and the percentage error due to the non-ideal behaviour of the amplifier is given approximately by:

$$D = \frac{100}{A_{ol}} \left\{ \left(1 + \frac{Z_0}{Z_L} \right) \left(1 + \frac{R_f}{R_1} + \frac{R_f}{Z_{id}} \right) + \frac{Z_0}{R_1} \right\}.$$

Fig. 2.10. Non-inverting amplifier.

11

Also, closed-loop gain is affected by the voltage divider formed by R_s and Z_{in}; as Z_{in} is for the most part determined by Z_{cm}, for a first approximation the transfer function can be multiplied by the factor $Z_{cm}/(Z_{cm} + R_s)$ to obtain the effect of a finite Z_{in}.

Because both inputs of the non-inverting amplifier vary with V_1, and a finite CMRR (F) exists, an error voltage is fed to the output. As a percentage of the output voltage, the error voltage is $100/F\%$.

As stated previously, the non-inverting amplifier is especially useful in conjunction with high source impedances. However, the bias current which exists at the positive input can cause a considerable offset voltage. This can be reduced by choosing resistor values so that the parallel resistance of R_f and R_1 is equal to R_s. Full compensation at one temperature can be achieved according to the method outlined in Section 12.7. If bias current flow through the input sources is tolerable, and the output offset voltage is zero, a compensating current can be drawn through R_1 and R_f (see Fig. 12.12a). An advantage of this method is that the input impedance Z_{in} is not reduced by the bias current circuit.

Voltage and current offset, frequency response, and output impedance considerations are identical to those for the inverting amplifier, Section 2.3.1.

Non-inverting A.C. Amplifier

The non-inverting a.c. amplifier exhibits similar properties to those of the inverting a.c. amplifier discussed in Section 2.3.1, but has the advantage of a lower cut-off frequency. If a coupling capacitor is connected to the positive input (as shown in Fig. 2.11) a d.c. path for bias current must be provided. This path is provided by R_c and can be either directly to earth, or to an adjustable voltage (set by R_p). The latter method also offers a means to compensate the voltage drop due to the bias current. As the

Fig. 2.11. Non-inverting a.c. amplifier.

12

resistor R_c is effectively in parallel with Z_{cm}, the transfer function can be approximated to:

$$\frac{V_0}{V_i} = \frac{pR_cC}{1 + pR_cC} \cdot \frac{R_1 + R_f}{R_1},$$

provided that $R_c \ll Z_{cm}$.

The 3 dB-down frequency is thus given by $pR_cC = 1$ (where $p = j\omega$) whence $f_c = 1/2\pi R_c C$.

As the value of R_c can be high, the value of f_c is correspondingly lower than in the inverting a.c. amplifier.

2.3.3 ADDER CIRCUIT

A number of signals can be added together using the circuit shown in Fig. 2.12. With n inputs the output voltage is given by:

$$V_0 = \frac{R_f}{R_1}(V_1 + V_2 + \ldots + V_n).$$

Weighting factors can be added by choosing different values of R_1. If summation without amplication is required, then R_f and R_1 should be of the same value. The adder can be regarded as an inverting amplifier with additional inputs; hence the error D in the output voltage can be calculated using the same equation as for the inverting amplifier (Section 2.3.1), but substituting the term

$$\left(\frac{1}{Z_{id}} + \frac{n-1}{R_1}\right) \quad \text{for} \quad \frac{1}{Z_{id}}.$$

The input impedance, and the gain-frequency relationship, are identical to those for the inverting amplifier.

Fig. 2.12. Adder.

13

The output impedance is given by:

$$\frac{Z_0}{A_{ol}}\left(1 + \frac{nR_f}{R_1}\right).$$

The output voltage caused by offset drift with temperature, and bias current, is given by:

$$v_o = i_d R_f + v_d\left(1 + \frac{nR_f}{R_1}\right).$$

This can be partially compensated by a resistor of value $R_f R_1/(nR_f + R_1)$ (i.e. $R_f//R_1/n$) connected in series with the positive input. The bias current drift i_d is then replaced by the offset current drift i_{dd}. For the DOA40, with $R_f = R_1 = 20$ kΩ, and $n = 3$,

$$v_o = 10^{-9} \times 20 \times 10^3 + 5 \times 10^{-6}\,(1 + 3)$$

$$= 40\ \mu\text{V/degC (maximum value)}.$$

2.3.4 IMPEDANCE TRANSFORMER (FOLLOWER)

A commonly used application of the non-inverting amplifier is the impedance transformer, shown in Fig. 2.13. This circuit gives:
– a transfer ratio approaching unity
– a very high input impedance
– a very low output impedance.

Fig. 2.13. Impedance transformer.

Using a DOA42 operational amplifier in this configuration gives an input impedance of 1000 MΩ (typical value of Z_{cm}), an output impedance of

$$\frac{Z_0}{A_{ol}} = \frac{150}{2.10^5} = 7 \cdot 5 \times 10^{-4}\ \Omega,$$

and a transfer function which is unity but for errors introduced by virtue of the finite values of A_{ol} and F. These errors are:

$$\frac{100}{A_{ol}} = \frac{100}{2.10^5} = 0.0005\%$$

and

$$\frac{100}{F} = \frac{100}{10^5} = 0.001\%.$$

To ensure stable operation an RC-network ($R = 45$ Ω, $C = 68$ nF) should be connected between terminals k_1 and k_2 (DOA42). If a DOA40 module is used in this application, the resistance in series with the positive input terminal must exceed 10 kΩ. Bandwidths for the DOA42 and DOA40 are 1 MHz and 8 MHz respectively.

2.3.5 INTEGRATOR AND HOLD CIRCUITS

The circuit shown in Fig. 2.14 operates as an integrator and, when switch S is opened, the output voltage is given by:

$$V_0 = -\frac{1}{R_1 C_f} \int_0^T V_1 \, dt,$$

where $T = $ integration time.

Fig. 2.14. Integrator.

15

If the d.c. input voltage V_1 is present for a time equal to T, the output is:

$$V_0 = -T \frac{V_1}{R_1 C_f}.$$

Error, introduced by the non-ideal parameters of the operational amplifier is (expressed as a percentage of output voltage):

$$D = \frac{50T}{A_{ol} R_1 C_f} \left(1 + \frac{Z_0}{Z_L}\right)\left(1 + \frac{R_1}{Z_{id}}\right)\%$$

or

$$D = \frac{50T}{A_{ol}' C_f} \left(\frac{1}{R_1} + \frac{1}{Z_{id}}\right)\%$$

where A_{ol}' is the loaded open-loop gain (see Section 12.5).

This is the static error of the circuit and it can be used to evaluate D for any values of T, C_f and R_1 when using the DOA40 and DOA42 modules.

Fig. 2.15 shows the response of the integrator to a suddenly applied d.c. level; the static error is represented by the difference between the ideal and actual response curves.

Fig. 2.15. Integrator output characteristics.

For application as a hold circuit resistor R_1 is disconnected; the output voltage drop due to static error then becomes:

$$D = \frac{50T}{A_{ol}'C_f Z_{id}}\% \qquad \left(\text{as} \quad \frac{1}{R_1} = \frac{1}{\infty} \right).$$

Another source of error is introduced (in both hold and integrator circuits) by offset voltage, bias current i_d and drift. Considering these the expression for output voltage becomes:

$$V_0 = \frac{T}{R_1 C_f}(i_d R_1 + v_d) + v_d = \frac{T i_d}{C_f} + \frac{T v_d}{R_1 C_f} + v_d.$$

When compensation resistor R_c is connected to the positive input terminal, i_d is replaced by i_{dd} (offset current). Adjustment of v_d and i_d to zero then makes it possible to replace these parameters by the corresponding drift values.

The expression for error output voltage indicates that a high value of C_f is preferable to a high value of R_1, and, when the hold circuit is used ($R_1 = \infty$) the bias current plays a dominant role provided that Z_{id} is high.

From the foregoing the design considerations to be taken into account can be summarized as follows:

- Choose a high value of C_f (1 to 10 μF), taking into account the requirement for low leakage current and optimum temperature range and coefficient.
- The value of R_1 must be as low as possible. However, it must also satisfy the requirement that the maximum current through C_f during the maximum integration time (Tm) does not produce an output which exceeds the output voltage and current ratings of the amplifier. Hence:

$$i_1 T_m \leqslant V_{max} C_f$$

$$\frac{V_1}{R_1} Tm \leqslant V_{max} C_f$$

therefore

$$R_1 \geqslant \frac{V_1 Tm}{V_{max} C_f}.$$

A.C. Integrator

When a continuous a.c. signal is applied to the integrator the build-up across C_f will cause the output voltage to exceed the rating of the amplifier. This can be avoided by connecting resistor R_f in parallel with C_f (Fig. 2.16). For d.c. signals and low frequency a.c., the closed-loop gain is $-R_f/R_1$, while for frequencies exceeding $f = (2\pi R_f C_f)^{-1}$, the circuit operates as an integrator. This is demonstrated by the gain-frequency response curves shown in Fig. 2.17. Offset and offset drift considerations are identical to those for the inverting amplifier (see Section 2.3.1).

Fig. 2.16. A.C. integrator.

a) open-loop gain
b) closed-loop gain without R_f
c) closed-loop gain with R_f

Fig. 2.17. A.C. integrator gain-frequency response.

2.3.6 DIFFERENTIATOR

The circuit shown in Fig. 2.18 operates as a differentiator; i.e. the output voltage is proportional to the rate of change of the input signal. The transfer function is given by:

$$V_0 = -R_f C_1 \frac{dV_1}{dt} \text{, or } i_c = C_1 \frac{dV_1}{dt} = -i_f = -\frac{V_0}{R_f}.$$

Fig. 2.18. Basic differentiator.

Clearly, the output rating (V_{max}) of the amplifier must not be exceeded, even by the fastest rate of change of input signal $(dV_1/dt)_{max}$:

i.e., $\left(\dfrac{dV_1}{dt}\right)_{max} \cdot R_f C_1 < V_{max},$ or $C_1 R_f < \dfrac{V_{max}}{\left(\dfrac{dV_1}{dt}\right)_{max}}.$

Inspection of the gain-frequency characteristics of the differentiator (see Fig. 2.19) shows that problems are liable to be encountered with high frequency signals.

At the frequency $f = (2\pi R_f C_1)^{-1}$ (from $1/\omega C_1 = R_f$), the closed-loop gain is unity (0 dB). The closed-loop gain increases linearly with frequency until the line intersects the open-loop gain characteristic and, as the frequency is increased further, the gain follows the open-loop characteristic. Two main disadvantages are inherent in circuits with this type of frequency response; these are:

– the circuit behaviour in response to high frequency noise,
– as the fall off in gain at high frequencies is 12 dB/octave, the circuit tends towards instability.

Fig. 2.19. Basic differentiator gain-frequency response.

19

These difficulties can be overcome by using the circuit shown in Fig. 2.20; the resistor R_1 connected in the input circuit, and capacitor C_f in the feedback network force the frequency response to drop at high frequencies. The frequency response characteristics are shown in Fig. 2.21: over the range 0 Hz to f_1 (where $f_1 = (2\pi R_1 C_1)^{-1}$ the circuit operates as a differentiator; between f_1 and f_f the response is flat (band-pass filter), and above f_f (where $f_f = (2\pi R_f C_f)^{-1}$ the circuit operates as an integrator. Maximum noise suppression is achieved by making $f_1 = f_f$, i.e. $C_f R_f = C_1 R_1$, and this frequency (rate of change of input signal) must be chosen bearing in mind the conditions governing the value of $R_f C_1$. The response obtained from a practical circuit deviates from the ideal characteristic as shown by the dotted line in Fig. 2.21. This deviation is greatest at the frequencies f_1 and f_f; therefore it is advisable to choose $f_1 (= f_f)$ a number of times higher than the expected maximum input frequency. With a ratio of 1 : 10, for example, the deviation is of the order 1 %.

Fig. 2.20. Practical differentiator.

Fig. 2.21. Practical differentiator gain-frequency response.

20

Output voltage caused by bias current can be reduced by connecting R_c to the positive terminal, and the value of R_c should be as low as possible; as a result the value of C_1 should be as high as possible — but electrolytic capacitors must be avoided.

2.3.7 DIFFERENCE (SUBTRACTING) AMPLIFIER

The circuit shown in Fig. 2.22 is a difference amplifier and can subtract two or more signals. With two inputs V_{i1} and V_{i2}, and arbitrary values for R_1, R_2, R_0 and R_f, the weighting coefficients are as given in the expression for the output voltage:

$$V_0 = \frac{R_0}{R_1} \left(\frac{R_1 + R_f}{R_2 + R_0} \right) V_{i2} - \frac{R_f}{R_1} V_{i1}.$$

Fig. 2.22. Subtracting amplifier.

If

$$\frac{R_f}{R_1} = \frac{R_0}{R_2},$$

then

$$V_0 = \frac{R_f}{R_1} (V_{i2} - V_{i1}).$$

Other applications for the difference amplifier are, for example, its use as a bridge circuit, and as a data amplifier. A common requirement of the foregoing applications is the need for a high input impedance at both inputs; however while the input impedance for the positive input ($= R_2 + R_0$) may be satisfactory, that for the negative input ($= R_1$)

is limited by the need to choose a low value of R_1. This difficulty can be overcome by the circuit shown in Fig. 2.23 where followers (see Section 2.3.4) are used in conjunction with each input.

Fig. 2.23. High impedance subtracting amplifier (using three DOA40 modules).

A less expensive circuit can be built using one DOA42 module which maintains high input impedances at both inputs (see Section 2.2). The circuit in Fig. 2.24 shows the feedback network connected between terminals E_1 and E_2 which are brought out specially for this application.

Fig. 2.24. High impedance subtracting amplifier (using one DOA42 module).

This arrangement has the advantage that the input impedance is equal to the high differential input impedance of the open-loop amplifier (typically 20 MΩ), and is not dependent on the resistor values in the external networks. The transfer function is given by:

$$\frac{V_0}{V_i} = \frac{1}{2}\left(1 + \frac{R_f}{R_0}\right) + \frac{2R_f}{R_1 + R_2} - R_f \frac{(R_1 - R_2)}{R_1 + R_2} \cdot \frac{I}{V_i} +$$

$$+ \left(\frac{R_f}{R_0} - 1\right)\frac{(V_{cm} - 2V_{be})}{V_i}$$

22

where: V_{cm} = common mode input voltage (approx. 0.7 V).

V_{be} = base-emitter junction voltage

I = current of internal current sink (approx. 400 μA).

Note that in practice R_o should exceed 10 kΩ.

When $R_2 = R_1$ and $R_f = R_0$ the expression is reduced to:

$$\frac{V_0}{V_i} = 1 + \frac{R_f}{R_1}$$

With the potentiometer connected as shown, offset voltage due to spread of R_1 and R_2 can be compensated. Using precision resistors (e.g. metal film resistors), or small values (< 100 Ω) for R_1 and R_2, the potentiometer can be omitted and the offset compensated using the trim potentiometer (see Section 12.7).

3 Description of the DZD40 Module

The DZD40 module is a differential zero detector and it is usually applied as a zero detector, voltage comparator, polarity detector, adjustable discriminator or differential amplifier. The symbol for the amplifier is shown in Fig. 3.1. Operation of the circuit is such that whenever the differential input voltage between terminals 1 and 3 exceeds a preset trip voltage, the output at terminal 8 switches from LOW (approx. 0 V) to HIGH (V_p). Versatility is enhanced by the outputs at terminals 7 and 14; these outputs assume the HIGH (7)/LOW (14) states when the input at 1 exceeds that at 3, and reverse their states when the input at 3 exceeds that at 1.

Fig. 3.1. DZD40: symbol.

The facility to adjust the trip voltage level and the input impedance makes the DZD40 module compatible with a wide range of input devices.

The truth table below shows the states of the outputs at terminals 7, 8 and 14 for the four input conditions.

Truth table

input terminals		output terminals		
3	1	7	14	8
HIGH	HIGH	HIGH	HIGH	LOW
HIGH	LOW	LOW	HIGH	HIGH
LOW	LOW	HIGH	HIGH	LOW
LOW	HIGH	HIGH	LOW	HIGH

HIGH-HIGH and LOW-LOW in the input rows indicate that signals applied to the inputs differ less than the trip value. HIGH-LOW and LOW-HIGH in the input rows indicate that the voltage difference applied to the inputs exceeds the trip value. In the output columns, HIGH stands for V_p and LOW for 0 V approximately.

Only one output terminal will be LOW for any input combination. Linear outputs from the DZD40 are available at the output terminals 12 and 13. The voltage gain is adjustable up to a maximum figure of approximately 1000. With the circuit in balance ($V_{12} = V_{13}$) the potential at terminals 12 and 13 is approx. -5 V.

The complete circuit of the DZD40 is potted inside a metal casing, and connections are made via 19 wire terminals. A dimensional drawing and details of the terminal locations are given in Fig. 3.2.

Fig. 3.2. DZD40: dimensional drawing and terminal location.

3.1 Circuit Description of the DZD40 Module

The DZD40 differential zero detector comprises a two-stage, d.c.-coupled, differential amplifier, an OR-gate and three inverting amplifiers; the circuit

25

diagram is shown in Fig. 3.3. Input transistors TR_1 and TR_2 are complementary to TR_3 and TR_4 which are connected as a long-tailed pair and give a differential voltage gain of approximately 1000. Externally connected common emitter resistor R_G provides a feedback path for the first stage and its value determines the gain and input impedance; it also helps to set the trip voltage of the circuit. The trip voltage is also affected by the setting of external potentiometer R_V. External potentiometer R_B is used to set the initial balance of the long-tailed pair (see Section 11.3). The two outputs from the long-tailed pair are fed to the OR-gate, which comprises R_{10}, R_{11} and R_{12}, and to output terminals 12 and 13. The difference between the output voltages V_{12} and V_{13} is given by $K (V_3 - V_1)$, where $K \propto 1/R_G$.

While $V_{13} - V_{12}$ is less than the critical value, TR_5 conducts, and

Fig. 3.3. DZD40: circuit diagram.

TR_6 and TR_7 are cut off. When the difference voltage exceeds the critical value TR_6 or TR_7 conducts (depending on the polarity of $V_{13} - V_{12}$) and TR_5 is cut off by the increased emitter bias voltage developed across R_{14}. The outputs at terminals 7 and 14 are in anti-phase with the inputs at terminals 3 and 1 respectively. The DZD40 uses current mode switching techniques (the transistors are never bottomed) to achieve high switching speeds and to reduce the loading of the amplifier. It is therefore necessary to connect terminals 7 and 14 to 0 V when they are not used, or, when they are terminated, to use diodes (cathodes to Q_1 and Q_2) to clamp the output to 0 V and prevent bottoming.

3.2 Functional Configurations using the DZD40 Module

The DZD40 module is particularly useful where a digital output is required from an analogue input; this aspect of application is dealt with in Section 9. Various other applications are considered in this section and, in general, the technique used is to make one input a fixed reference potential while the second input represents the system variable. In this way the output gives information which denotes whether the variable is higher or lower than the reference, and the exact moment at which a change takes place.

When designing a system using the DZD40, the following points should be noted:

- Avoid a short circuit between the terminals 8 and 9 as diode D_1 (see Fig. 3.3) will be damaged.
- To avoid instabilities due to transient switching voltages arising on supply lead inductance, the supply terminals 9 and 19 should be decoupled directly to terminal 0 V by means of low inductance capacitors.
- For slowly diminishing voltages below the trip level, the dv/dt of the zero-going output at terminal 8 will be approximately 10 000 times that of the input signal.
  If a faster dv/dt is required, the voltage at terminal 8 should be applied to a pulse shaper (e.g. PS10, PS20).
- The terminals 7 and 14 provide signals that in most cases can be used directly to trigger units of the 10- and 20-Series or logic circuits having similar input requirements.
- In circuits where high voltages might be detrimental, it is good practice to protect the inputs by an antiparallel diode circuit, thereby limiting the voltage.

27

- If possible, arrange the circuit so as to avoid common mode voltage presence on inputs.
- With a.c. input signals of over 10 kHz a capacitor of 2200 pF should be connected to the terminals 15 and 10. Then only d.c. common mode voltage is allowed.
- If terminal 17 is left unconnected the resistance load at terminal 8 can be 3.6 kΩ.

3.2.1 HIGH/LOW VOLTAGE DETECTION

Low Voltage Zero Detector giving Zero Output at Zero Input

The low voltage zero detector shown in Fig. 3.4 (a) is intended for use with differential input signals up to 700 mV; above this figure the circuit response times deteriorate, although voltages of up to 5 V can be safely applied.

The input/output relationship is as follows:

differential input $V >$ trip level: V_{Q3} is HIGH ($=$ supply voltage)

differential input $V <$ trip level: V_{Q3} is LOW ($=$ 0 V)

sinusoidal input: V_{Q3} is HIGH except for a few degrees either side of zero crossings when it switches to LOW (see Fig. 3.4b), i.e. the module acts as a bi-directional pulse shaper.

Fig. 3.4(a). Low voltage zero detector.

Fig. 3.4(b). Waveforms.

28

Low Voltage Zero Detector giving Complementary Outputs

The circuit shown in Fig. 3.5 (a) gives complementary outputs at terminals 7 and 14 (linked) and 8, Waveforms for a sinusoidal input are shown in Fig. 3.5 (b). The resistance R_L represents the external load and should be greater than 3.6 kΩ; when using both outputs it is advisable to connect a capacitive load (approx. 200 pF) to terminals 7 and 14.

Fig. 3.5(a). Low voltage zero detector (complementary outputs).

Fig. 3.5(b). Waveforms.

29

High Voltage Zero Detector giving Zero Output at Zero Input

The circuit shown in Fig. 3.6 is designed for input voltages exceeding 700 mV; the input/output relationship is exactly as described for the low voltage circuit (Fig. 3.4). Diodes D_1 and D_2 (preferred type BZX13) limit the input voltage, and the resistor R limits diode current and signal source loading.

Fig. 3.6. High voltage zero detector.

High Voltage Zero Detector giving Complementary Outputs

The circuit shown in Fig. 3.7 gives outputs exactly as described for the low voltage circuit (Fig. 3.5). The resistor/diode input circuit allows a larger differential input to be applied, and limits the signal source loading.

Fig. 3.7. High voltage zero detector (complementary outputs).

3.2.2 HIGH/LOW VOLTAGE COMPARISON

In the following circuits V_x and V_{ref} must be of the same polarity.

Low Voltage Comparator giving Zero Output at Zero Difference Input

The circuit shown in Fig. 3.8 gives a zero output when the difference input voltage $(V_x - V_{ref})$ is below the trip voltage. The maximum value of both V_x and V_{ref} is 1 V.

30

Fig. 3.8. Low voltage comparator (zero output).

Low Voltage Comparator giving High Output at Zero Difference Input

The circuit shown in Fig. 3.9 gives a HIGH (= supply voltage) output when the difference input voltage ($V_x - V_{ref}$) is below the trip voltage. The maximum value of both V_x and V_{ref} is 1 V.

Fig. 3.9. Low voltage comparator (high output).

High Voltage Comparator for D.C. Voltages

The circuit shown in Fig. 3.10 allows the comparison of d.c. voltages exceeding 1 V. This circuit avoids common mode difficulties and diodes

Fig. 3.10. High voltage comparator.

31

D_1 and D_2 prevent the input at the input terminals exceeding 5 V. The values of R_x and R_f are calculated as follows:

The voltage between the 0 V and W_1 (Fig. 3.11) will be zero if

$$\frac{V_x}{V_{ref}} = \frac{R_X}{R_r}$$

R_X and R_r can be selected taking into account the loading of the sources V_{ref} and V_X.

Example

V_x is a potential between $+60$ and $+95$ V with respect to the 0 V line. V_{ref} is a reference source of 5 V. Both sources can be loaded with 1 mA max.

It is desired to produce a positive output signal whenever $V_x = 80$ V. As $V_{xmax} = 95$ V, the maximum voltage across $R_x + R_{ref}$ is 100 V. To stay within loading $R_x + R_{ref}$ must be approx. 100 kΩ.

Furthermore $R_x/R_{ref} = 80/5$ for zero detection at 80 V, so $R_x = 16 \ R_r$.

When $R_r = 6.8$ kΩ a trimming potentiometer of 150 kΩ can be used for R_x. The output can be taken from $(Q_1 + Q_2)$ as in Fig. 3.11.

Fig. 3.11. Input circuit.

3.2.3 POLARITY DETECTOR

The circuit shown in Fig. 3.12 produces outputs at terminals 7 and 14 which indicate the polarity of the input. In addition the output at terminal 8 indicates a zero difference input. The input/output relationship is as follows:

inputs		outputs		
1	3	7	14	8
L	H	L	H	H
H	L	H	L	H
L	L	H	H	L
H	H	H	H	L

Fig. 3.12. Polarity detector.

Where the input voltages do not exceed 1 V, the diode limiters, D_1 and D_2, can be omitted. In any case the input voltages at terminals 1 and 3 should be made lower than 2 V (using a resistive step-down circuit if necessary) to avoid common mode influence.

In application this circuit is particularly useful in servo control, direction determination and tolerance automation systems.

4 Description of the PSM40 Module

The PSM40 phase shift module is designed for use in conjunction with a trigger source for the control of the conduction angle of thyristors. In addition to the linear relationship established between phase angle and input drive voltage by most control circuits, the PSM40 module offers consinusoidal control; i.e., the average output voltage is proportional to the input drive voltage. This means that the average voltage developed across a load is independent of a.c. supply voltage variations. The module can be used in single-phase, half- or full-wave systems with an a.c. supply of 15Hz to 10 kHz, the control range being better than 10 to 170°. Three modules can be synchronized for three-phase, full-wave control.

The complete circuit of the PSM40 is potted inside a metal casing, with 19 wire terminals. A dimensional drawing and details of the terminal locations are given in Fig. 4.1.

Fig. 4.1. PSM40: dimensional drawing and terminal location.

4.1 Circuit Description of the PSM40 Module

The circuit of the PSM40 module (Fig. 4.2) comprises a synchronizing input stage, TR_1, a capacitor charge and discharge stage TR_2 and TR_3, a long-tailed pair, TR_4 and TR_5, and output switching stage TR_6 and TR_7. Synchronizing signals are applied to terminals 11 and 12, and are fed via diodes D_1 and D_2; while the synchronizing signal voltage exceeds the forward voltage drop of the diodes, TR_1 is conducting and TR_2 is biased off. When the synchronizing voltage falls below the forward voltage of the diode (i.e. approaching the zero crossing) TR_1 is cut off and TR_2 conducts, rapidly charging the capacitor C_s. A few electrical degrees after the zero crossing TR_1 again conducts and TR_2 is cut off.

While TR_2 is cut off, C_s is discharged through TR_3. For linear control (terminals 2 and 3 linked for 50 Hz, external capacitor between terminals 2 and 10 for other frequencies) TR_3 produces a linear discharge characteristic, and a saw-tooth waveform is fed to the base of TR_4. For cosinusoidal control TR_3 produces a discharge path according to the function 1-$\cos \alpha$; this is achieved by making the appropriate external connections (see Section 11.4).

Fig. 4.2. PSM40: circuit diagram.

While the voltage fed to the base of TR_4 exceeds that at the base of TR_5, TR_4 conducts and TR_5 is cut off. Therefore base current to drive TR_6 is supplied via R_{14} and TR_6 conducts driving TR_7 into saturation. The output at terminal 6 is thus approximately 0 V. As soon as the base potential of TR_4 falls below that of TR_5, TR_5 conducts cutting off TR_6 and TR_7. The output then becomes high; the actual voltage is that of the load supply, up to a maximum of 15 V.

4.2 Linear and Cosinusoidal Control Modes

A simple thyristor circuit with phase angle control is shown in Fig. 4.3. The a.c. supply for the load can be half- or full-wave, and the phase angle α at which the thyristor is triggered is controlled by control voltage e. Hence the power supplied to the load can be regulated. Fig. 4.4 shows how the power supplied to the load can be varied between full power and zero by shifting α from π to 0 electrical degrees.

Fig. 4.3. Thyristor with control unit.

Fig. 4.4. Output voltage.

The full thyristor amplifier circuit (see Fig. 4.5) comprises three stages; the control unit (CU), trigger unit (TU) and thyristor unit (ThU). Control voltage e varies the phase angle α and so regulates the average value of output voltage V_a. The power input voltage V_s can be half- or full-wave, single phase.

Fig. 4.5. Thyristor amplifier.

If the relationship that exists between α and e is linear it can be stated as $\alpha = K_1 e$. However, when α is varied linearly the relationship between α and average voltage V_a developed across a load is cosinusoidal; i.e.

$$V_a = \frac{V_m}{\pi} \int_{\pi-\alpha}^{\pi} \sin \alpha \, d\alpha = \frac{V_m}{\pi} (1 - \cos \alpha).$$

Hence if the control voltage e is made to follow the cosinusoidal relationship $e = K_2 (1-\cos \alpha)$, then:

$$\frac{V_a}{e} = \frac{V_m}{K_2 \pi},$$

i.e. the relationship between e (and hence α) and V_a is linear.

It should be understood that the terms *linear control* and *cosinusoidal control* refer to the relationship between e and α; Fig. 4.6 shows that for a linear control voltage, V_a varies cosinusoidally, (graph a) and for a cosinusoidal control voltage V_a varies linearly (graph b).

Fig. 4.6. V_a/e_m characteristics.

37

In closed-loop control systems both the static and dynamic gain characteristics must be considered. The dynamic gain G_d largely determines the stability of the system (according to the Nyquist criterion), while the system accuracy is inversely proportional to the static gain C_s.

It has been stated previously that for linear control $\alpha = K_1 e$, and that $V_a = V_m/\pi\,(1-\cos\alpha)$. For a control voltage of e_m, the phase angle $\alpha = \pi$; therefore

$$\pi = K_1 e_m \quad \text{and} \quad K_1 = \frac{\pi}{e_m},$$

which modifies the expression for α to: $\alpha = \pi e/e_m$.

Substituting α in the expression for V_a we get:

$$V_a = \frac{V_m}{\pi}\left(1 - \cos\frac{\pi e}{e_m}\right)$$

The dynamic gain G_d is given by:

$$G_d = \frac{dV_a}{de} = \frac{d}{de}\left\{\frac{V_m}{\pi}(1 - \cos\alpha)\right\} = \frac{V_m}{e_m}\sin\frac{\pi e}{e_m}.$$

The solid line in Fig. 4.7 illustrates the sinusoidal relationship between G_d and e; this can be used (by application of Nyquist criterion) to determine system stability.

Fig. 4.7. G_d/e_m characteristic.

Static gain G_s is given by:

$$G_s = \frac{V_a}{e} = \frac{V_m}{\pi}(1 - \cos\alpha)\frac{\pi}{e_m\alpha} = \frac{V_m}{e_m}\frac{(1 - \cos\alpha)}{\alpha}.$$

As stated previously, the accuracy of the system is proportional to the inverse of G_s; assuming the system to be influenced by only one transfer function, the error ε is given by:

$$\varepsilon = \frac{1}{G_s} = \frac{e_m}{V_m} \cdot \frac{\alpha}{1 - \cos \alpha} \ .$$

The solid line in Fig. 4.8 shows the relationship between ε and e.

Fig. 4.8. Errors vs. e_m curve.

For cosinusoidal control the linear equation $V_a = K_2 e$ holds; also, from the expression

$$V_a = \frac{V_m}{\pi} (1 - \cos \alpha), \text{ when } \alpha = \pi,$$

$$V_{am} = 2V_m/\pi;$$

therefore

$$V_{am} = K_2 e_m = 2V_m/\pi,$$

and

$$K_2 = 2V_m/\pi e_m.$$

Hence, substituting for K_2 in $V_a = K_2 e$, we obtain:

$$V_a = 2\ V_m e/\pi e_m.$$

Dynamic gain G_d is given by:

$$G_d = \frac{dV_a}{de} = \frac{2V_m}{\pi e_m} ;$$

this is shown by the dotted line in Fig. 4.7.

Static gain is given by:

$$G_s = \frac{V_a}{e} = \frac{2V_m e}{\pi e_m} \cdot \frac{1}{e} = \frac{2V_m}{\pi e_m} ,$$

and the error ε is given by

$$\frac{1}{G_s} = \frac{\pi e_m}{2V_m} ;$$

this is shown by the dotted line in Fig. 4.8.

The foregoing contrasts the main properties of linear and cosinusoidal thyristor control systems, and it is apparent that, for closed-loop systems, the cosinusoidal control mode is to be preferred. The main advantages are:
– the error is constant over the whole working range
– the stability of the system is independent of the working point.

Hence, with predictable values for both error and dynamic gain, the system can be designed for optimum performance with regard to accuracy as well as stability. Also, as the error is constant, the possibility exists to compensate for the error.

Another important feature of cosinusoidal control is that variations in the mains supply are compensated, i.e. if V_m increases, α decreases (see Fig. 4.4).

5 Power Supply Units and Mounting Accessories

5.1 Power Supply Units

The power supplies required by the modules are detailed in Section 11. Power supply units from the standard range which are suitable for use with the 40-Series modules are:

PE1509: 0-30 V, 0-400 mA
PE1507: 0-15 V, 0-700 mA
PE1212: 10-30 V, 0-100 mA.

These three units give outputs which can be adjusted to give the exact voltage required (12 or 15 V). In addition, the current outputs are more than adequate and can be used to supply other modules or circuit blocks in a system. The PE1212 is intended to be built into a system.

Details of two units which can be built and incorporated in a system are given below.

5.1.1 STABILIZED POWER SUPPLY UNIT

The power supply unit provides positive and negative d.c. outputs which can be adjusted to 12 V or 15 V, and which are stabilized to within 0.2 % for a $+ 10$ to -15 % change in mains supply at outputs from 0 to 400 mA.

A circuit diagram is shown in Fig. 5.1. Each half of the unit comprises a Darlington series regulator and a long-tailed pair differential amplifier. A reference voltage source is provided by zener diodes D_5 and D_7, and the collector of the regulating transistor is connected to a constant current source. Potentiometers R_{21} and R_{22} allow the positive and negative outputs respectively to be adjusted to 12 V or 15 V.

The three-phase transformer/rectifier input circuit can easily be replaced by a single-phase circuit if required. In this case the output is limited to 225 mA.

The circuit (except transformer) can be mounted on a single printed wiring board as shown in Fig. 5.2. Series regulator transistors TR_3 and TR_8 must be mounted on a heat sink.

The 24 V transformer secondary winding (not shown) is suitable for driving the synchronization inputs S_1 and S_2 of the PSM40.

41

Fig. 5.1. Stabilized P.S.U. circuit diagram.

Component list

Component	Catalogue No.
Printed-wiring board (with extractor) SU	4322 026 38870
Connector: type 0.2″, 23 × 1 contacts	2422 020 52592

Capacitors

C_1 = 250 μF, 40 V, electrolytic		2222 023 17251
C_2 = 250 μF, 40 V, electrolytic		2222 023 17251
C_3 = 250 μF, 40 V, electrolytic		2222 023 17251
C_4 = 100 nF, 250 V, metallized polycarbonate		2222 342 45104
C_5 = 250 μF, 40 V, electrolytic		2222 023 17251
C_6 = 250 μF, 40 V, electrolytic		2222 023 17251
C_7 = 250 μF, 40 V, electrolytic		2222 023 17251
C_8 = 100 nF, 250 V, metallized polycarbonate		2222 342 45104

Resistors

R_1 = 1 Ω, 5%		2322 212 13108
R_2 = 1.8 kΩ, 5%		2322 212 13182
R_3 = 2.2 kΩ, 5%		2322 212 13222
R_4 = 1.2 kΩ, 5%		2322 212 13222
R_5 = 1.2 kΩ, 5%		2322 212 13222

42

Fig. 5.2. Component layout.

43

$R_6 = 4.7$ kΩ, 5%   2322 212 13472
$R_7 = 1.2$ kΩ, 5%   2322 212 13122
$R_8 = 1.2$ kΩ, 5%   2322 212 13122
$R_9 = 2.7$ kΩ, 5%   2322 212 13272
$R_{10} = 2.2$ kΩ, 5%   2322 212 13222
$R_{11} = 1 \ \Omega$, 5%   2322 212 13108
$R_{12} = 1.8$ kΩ, 5%   2322 212 13182
$R_{13} = 2.2$ kΩ, 5%   2322 212 13222
$R_{14} = 1.2$ kΩ, 5%   2322 212 13122
$R_{15} = 1.2$ kΩ, 5%   2322 212 13122
$R_{16} = 4.7$ kΩ, 5%   2322 212 13472
$R_{17} = 1.2$ kΩ, 5%   2322 212 13122
$R_{18} = 1.2$ kΩ, 5%   2322 212 13122
$R_{19} = 2.7$ kΩ, 5%   2322 212 13272
$R_{20} = 2.2$ kΩ, 5%   2322 212 13222
$R_{21} = 2.0$ kΩ, 10%, high-stability wire-wound potentiometer [1])
$R_{22} = 2.0$ kΩ, 10%, high-stability wire-wound potentiometer [1])

Semiconductors

D_4 = Voltage regulator (zener) diode   BZY78
D_5 = Voltage regulator (zener) diode   BZY78
D_6 = Voltage regulator (zener) diode   BZY78
D_7 = Voltage regulator (zener) diode   BZY78

TR_1 = PNP transistor   BCY70
TR_2 = NPN transistor   BC107
TR_3 = NPN power transistor   BDY11
                                                 (on heat sink)
TR_4 = NPN transistor   BC107
TR_5 = NPN transistor   BC107
TR_6 = NPN transistor   BC107
TR_7 = PNP transistor   BCY70
TR_8 = PNP power transistor   AD149
                                                 (on heat sink)
TR_9 = PNP transistor   BCY70
TR_{10} = PNP transistor   BCY70

U_1 = Bridge rectifier   BY122
U_2 = Bridge rectifier   BY122
U_3 = Bridge rectifier   BY122

Heat sink: 1.5 mm aluminium, 45 mm square — bent to U-shape 10 mm $\times$ 25 mm $\times$ 10 mm.

[1]) For example, Bourns Trimpot

5.1.2 Voltage Regulator Stabilized Power Supply

This power supply unit (Fig. 5.3) produces positive and negative, voltage regulator diode stabilized, outputs of 12 or 15 V depending on the choice of diodes (BZY95-C12 for 12 V, BZY95-C15 for 15 V). The current drain can be up to 60 mA or 35 mA for 12 V or 15 V outputs respectively.

The three-phase transformer/rectifier input circuit can easily be replaced by a single-phase circuit if required.

If used in conjunction with a PSM40, the transformer 24 V output can be used for driving the synchronization inputs S_1 and S_2.

The circuit (except transformer) can be mounted on a single printed wiring board as shown in Fig. 5.4.

This is a particularly useful arrangement for a small system as the printed wiring board has provision for mounting one DOA40 module with input and feedback components (see Fig. 5.4). Provision is also made to mount two zener diodes (BZY78) to provide a stable reference voltage which can be used in conjunction with a potentiometer as, e.g. set point in closed-loop control systems.

Fig. 5.3. Voltage regulator stabilized P.S.U. circuit diagram.

Fig. 5.4. Component layout.

Component List

Component	Catalogue No.
Printed-wiring board SCU	4322 026 38860
Connector: type 0.2″, 23 × 1 contacts	2422 020 52592

Capacitors

	Catalogue No.
C_1 = 250 μF, 40 V, electrolytic	2222 023 17251
C_2 = 250 μF, 40 V, electrolytic	2222 023 17251
C_3 = 250 μF, 40 V, electrolytic	2222 023 17251
C_4 = 250 μF, 40 V, electrolytic	2222 023 17251
C_5 = 400 μF, 24 V, electrolytic	2222 121 15121
C_6 = 120 μF, 16 V, electrolytic	2222 121 15121
C_7 = 400 μF, 25 V, electrolytic	2222 023 16401
C_8 = 120 μF, 16 V, electrolytic	2222 121 15121

Resistors

	Catalogue No.
R_1 = 100 Ω, 5.5 W, 10 % (three-phase use)	2322 320 31101
R_2 = 100 Ω, 5.5 W, 10 % (three-phase use)	2322 320 31101
R_1 = 180 Ω, 5.5 W, 10 % (single-phase use)	2322 320 31181
R_2 = 180 Ω, 5.5 W, 10 % (single-phase use)	2322 320 31181

Semiconductors

	Catalogue No.
D_4 = Voltage regulator (zener) diode	BZY95-C12
D_5 = Voltage regulator (zener) diode	BZY95-C12
U_1 = Bridge rectifier	BY122
U_2 = Bridge rectifier	BY122
U_3 = Bridge rectifier	BY122

5.2 Matching with Other Control Modules

5.2.1 60-SERIES NORBITS

All four of the 40-Series modules can be connected directly to the inputs of 60-Series Norbits. However, in the case of the DOA40 and DOA42 operational amplifiers, the response times of the Norbit will be reduced by the application of a negative input. To prevent this, it is recommended that the operational amplifier output is coupled to the Norbit input via a 4.7 k Ω resistor, and is connected to ground via a clipping diode (see Fig. 5.5.).

Fig. 5.5. Coupling to Norbits.

5.2.2 INTEGRATED CIRCUITS, 10- AND 20-SERIES MODULES

When coupling integrated circuits, 10- or 20-Series modules to the outputs of 40-Series modules, care must be taken that the input ratings are not exceeded. Also, that the negative outputs from the two operational amplifiers are suppressed. These requirements are met by using a zener diode, connected as shown in Fig. 5.6, which has a zener rating to match the following circuit.

Fig. 5.6. Coupling to I.C., 10- or 20-Series modules.

48

5.3 Printed Wiring Boards for Mounting 40-Series Modules

- 4322 026 36270 (Fig. 5.7). This is an experimenters board which will accommodate up to 10 modules of type DOA40, DZD40 or PSM40. The board fits the mounting chassis 4322 026 38240.

Material: Phenolic resin-bonded paper
Hole diameter: 1.2 mm, plated through
Contacts: 2 × 23, gold plated, 0.2-inch pitch.

Fig. 5.7. Experimenters printed wiring board 4322 026 36270.

– 4322 026 38600 and 38610 (Fig. 5.8). These are experimenters boards (supplied with extractor) which will accommodate up to 20 modules of type DOA40, DZD40 or PSM40. This board is also suitable for mounting DOA42 modules.

The boards fit the mounting chassis 4322 026 38240.

Material: 38600   Glass epoxy
            38610   Phenolic resin bonded paper
Holes: 1.2 mm, plated through
Contacts: 2 × 23, gold plated, 0.2-inch pitch.

Fig. 5.8. Experimenters printed wiring board 4322 026 38600 & 38610.

50

– 4322 026 39890 (Fig. 5.9). Up to four modules of type DOA40, DZD40 or PSM40 can be mounted on this board (see photograph), together with external components. The board fits the miniature mounting chassis 4322 026 38770.

Fig. 5.9. Printed wiring board 4322 026 39890.

Printed wiring board 4322 026 39890 containing 4 modules and other circuits components

51

– 4332 000 00501 (Fig. 5.10). This is an experimenters printed wiring board suitable for mounting one DOA42 module.

Fig. 5.10. Printed wiring board 4322 000 00501.

– 4322 026 34950. This printed wiring board (Fig. 5.11) mounts up to 8 modules of type DOA40, DZD40 or PSM40. The board fits mounting chassis 4322 026 38240.

Material:	Phenolic resin bonded paper
Hole diameter:	1.2 mm plated through
Contacts:	1 × 23, gold plated, 0.2-inch pitch.

Fig. 5.11. Printed wiring board 4322 026 34950.

– 9390 198 00002. The BB60 breadboard block (Fig. 5.12) provides a plug-in mounting for one DOA42 module. However, the DOA42 terminals E_1, E_2 and C must be connected together close to the case, and the terminal pins cut off. Solder connections can be made to the solder lugs on the underside of the block. Blocks are interlocking and a base to mount several modules can be made up.

Body material: rigid grey plastic
Contacts: 2×17 cup shaped, silver plated.

Fig. 5.12. Breadboard block 9390 198 00002.

– 4322 026 32150. The DOA40, DZD40 and PSM40 modules can be secured on a printed wiring board using the locking cap shown in Fig. 5.13. The cap fits over the top of the module; the flexible wire terminals allow the module to be bent over and lie flat on the board. Two solder tags can be used to secure the cap to the board.

Fig. 5.13. Locking cap 4322 026 32150.

5.4 Stickers

Drawing symbols of the four 40-Series modules are available in sticker form. These symbols are useful when making a diagram (e.g. wall chart) of a system. A set of stickers (catalogue number 12NC 4322 026 71951) is shown in Fig. 5.14.

Fig. 5.14. Stickers.

54

Example of a modular unit containing two DOA40 modules and a PSM40 module.

DOA40 and DZD40 modules secured with locking cap.

55

Plasma welding equipment: the power delivered is regulated by thyristors which are controlled by PSM40 modules.

6 Quality Control

The function of quality control is basically to check that the product meets the design requirements, but it also enables improvements in construction, constructional techniques, performance, etc to be sought. It will be realized, therefore, that quality control is a fairly complex science; a detailed account and analysis could occupy the whole of this publicaton.

However, to give an idea of the sort of procedures carried out, this section gives a summary of the test specifications for DOA40, DZD40 and PSM40 modules. The tests are made on samples taken from production such that they are representative of the whole batch. All tests are in accordance with MIL-STD-202.

- *Vibration test:* Method 201 A.
  Frequency 10-55 Hz, amplitude 0.76 mm.

- *Shock test*: Method 202 A. Acceleration 50 g in 3 mutually perpendicular directions.

- *Temperature-cycling test*: Method 102 A, condition D, 5 cycles from —40 °C to +85 °C.

- *Accelerated humidity test:* Method 106 A, 10 cycles (see Fig. 1, page 2 of method 106 A).

- *Long-term humidity test:* (i) Method 1034. Modules not operating. Duration 56 days at +40 °C, relative humidity 95%. Measurements after 7, 14, 28 and 56 days.
  (ii) As in (i) but with the modules operating under the worst electrical conditions with regard to supply voltages, input and output load characteristics.

- *Long-term high temperature test:* Method 108, test condition E, temperature +55 °C, duration 1500 hours, units operating under most unfavourable electrical conditions. Measurements after 250, 500, 1000 and 1500 hours.

- *Terminal strength test*: Test for mounting, soldering, lacquer and coding.

7 Practical Circuits using DOA40 and DOA42 Modules

7.1 General Considerations

One of the principal attributes of the operational amplifier is its ability to handle very small signals, often as low as a few microvolts. In such applications, extraneous or interference signals can quite easily be of the same order as the input signal; however, they are usually introduced via inductive or capacitive coupling and are at a relatively high frequency. Thus, when the wanted signal is d.c., or low frequency, any interference signal can be suppressed simply by limiting the bandwidth of the amplifier.

Where the frequency of the unwanted signal is comparable with that of the input signal, other methods must be employed. The most effective remedy is to avoid the introduction of such signals; this can be achieved by efficient shielding such as a metal box housing. The box should form a complete envelope with no apertures, and all connections to the module should be made via feedthrough capacitors, or co-axial connectors for h.f. signals. Ripple voltages on the supply lines should be suppressed by the use of conventional RC filters.

Earthing

When handling small signals errors are often introduced as a result of earth leakage currents; interference from this source may give rise to d.c. as well as high frequency signals. It is, therefore, a mistake to connect the signal earth line to the 0 V line of the power supplies or the load. One way of avoiding the risk of interference from this source is to use separate earth leads for the supplies, inputs and load, and to connect these leads to a common earth point. The leads should be as short as possible to avoid pick-up.

7.2 Sensor Amplifiers

7.2.1 LEVEL DETECTOR FOR THE MEASUREMENT OF DIODE LEAKAGE-CURRENT DRIFT

The reverse current which flows in a diode is not of constant magnitude,

Fig. 7.1. Circuit diagram of diode leakage-current drift detector.

but varies with time. The circuit shown in Fig. 7.1 provides an output which is proportional to the amount of leakage-current drift beyond the limit imposed.

The leakage current I_R flowing through the diode D under test creates a voltage drop across the series resistor R_1. This potential is used to charge capacitors C_1 and C_2 via relay contacts RA and RB respectively, which are operated by a timing circuit (not shown). When both C_1 and C_2 are charged, RC is closed and current I circulates; the magnitude of I is dependent on the difference in charge of C_1 and C_2, i.e., the drift magnitude, and the direction is dependent on whether I_R is increasing or decreasing (if I_R is decreasing, or the increase is below a certain value, no output signal is required). The charging sequence for C_1 and C_2 is shown in Fig. 7.2.

The current I produces a voltage V_p' at R_2; V_p' is amplified by a gain-of-20, broad-band amplifier to give V_p which is fed via R_6 to input 3 of the DOA40. Reference voltage V_{ref} is also fed to this input and is adjustable by means of R_5 (V_{ref} is adjusted to define the maximum permissible drift). Input terminal 1 of the DOA40 is connected to OV via R_7.

With reference to Fig. 7.3, assume that diode D has a drift greater than that allowable. Initially V_p exceeds V_{ref}, a positive input voltage results at input 3 of the DOA40. Hence, the output voltage at terminal 8 becomes negative, transistor TR_1 is cut off, and the output voltage V_U is $+ 12$ V.

59

Fig. 7.2. Charging sequence of C_1 and C_2. (1) S_1 closes, (2) S_1 opens, (3) S_2 closes, (4) S_2 opens.

Fig. 7.3. Waveforms.

As V_p decays below V_{ref}, the output of the DOA40 becomes 0 V, TR_1 again conducts, and V_U falls to 0 V. The output of the circuit is thus a pulse whose duration is proportional to the amount by which I_R changes during a predetermined period.

Diodes D_1 to D_6 connected across the DOA40 ensure that the output pulse is of constant magnitude. A total minimum forward voltage of

approximately 1.5 V is required before they conduct and no feedback path exists until the DOA40 output V_o becomes large. Consequently the gain is very high for small input signals, but diminishes rapidly above a certain input level. Hence TR_1 is fully driven for the duration of the output and V_U is a pulse of constant magnitude that can be used to trigger a shift register.

7.2.2 Temperature Measurement using a Compensated Cold Junction Thermocouple

Thermocouples have long been used as temperature sensors. However, because the e.m.f. produced is proportional to the *difference* in temperature between hot and cold junctions, thermocouples are inaccurate if no correction is made for variations in cold junction temperature. In the circuit of Fig. 7.4, cold junction temperature compensation is achieved in the following way. The negative input of the DOA40 module U_1 is connected to the thermocouple circuit, whilst the positive input is connect-

Fig. 7.4. Temperature measuring circuit using a compensated cold junction thermocouple.

ed to the correction circuit. The correction circuit comprises a bridge network which has one temperature-sensitive and three temperature-stable arms; at 0 °C the bridge is balanced and the voltage at point A (positive input to U_1) is zero. At temperatures other than 0 °C, unbalance occurs and a correction voltage (either positive or negative) is fed to U_1.

The temperature-sensitive arm of the bridge consists of a 30 Ω copper resistor (type PR7745/00) which is designed to physically accommodate the two cold junctions of the thermocouple, and a 55.6 Ω metal film resistor. This combination is specifically for use with a thermocouple which has a Chromel-Alumel hot junction and gives a useful temperature measuring range from 0° C to 700 °C (12 V module supply) or to 1000 °C (15V module supply). The thermocouple delivers approximately 40 μV/ deg.C, and the gain of U_1 is adjusted so that a temperature of 700 °C (1000 °C) gives an output of 7 V (10 V).

The bridge draws about 1.5 mA from the constant-current supply circuit shown.

With the circuit described, errors in output voltage arising from substantial changes in cold junction temperature are small; e.g., when the ambient temperature is raised to 80 °C, the output error is approximately 6 degC.

Operational amplifier DOA40 (module U_2) is connected as a difference amplifier with a set point circuit, and its purpose is to render the temperature measuring circuit compatible with temperature control systems. It increases the overall gain of the circuit over the required temperature range (proportional band).

The set point voltage is derived from the high stability reference diode (type BZY78) and is fed to the positive input of U_2. The difference between the set point voltage (desired temperature) and the amplified thermocouple output (actual temperature) is amplified by the factor of feedback resistance (500 kΩ potentiometer) to input resistance (10 kΩ). The output signal is used to drive the control system.

The 12-digit catalogue numbers of the special resistors used are listed below:

85.6 Ω, 1 % (three):	2322 123 88569
55.6 Ω, 1 % (one):	2322 123 85569
30 Ω, copper, PR7745/00 (one):	9400 377 45001

NOTE: By changing the bridge resistance, and/or the bridge current, the circuit can be used in conjunction with other types of thermocouple.

7.2.3 MEASUREMENT OF ELECTRICAL NOISE

The circuit of Fig. 7.5 is designed to measure the noise generated in electrical components, and is shown connected to a potentiometer.

Current from the current generator is fed through the potentiometer under test and the voltage developed is fed to the positive input of DOA40 module U_1. To avoid influencing the result, this amplifier employs full negative feedback (to the negative input) and operates as a follower with an input impedance greater than 60 MΩ. The output is a.c. coupled to the positive input of module U_2, which is connected as a gain-of-100 amplifier (ratio of feedback resistance — 500 kΩ — to input impedance — 5 kΩ). The a.c. output from module U_2 is thus a measure of the electrical noise generated in the potentiometer; the gain of the amplifier is constant (100) for signals of frequencies between 1 Hz and 100 kHz. The lower frequency is defined by the RC coupling network between the amplifiers, and the higher frequency is limited by the frequency response of the second operational amplifier.

Fig. 7.5. Circuit for measurement of electrical noise.

7.2.4 SMALL CURRENT DETECTOR

The detection and measurement of small currents demands a device which draws negligible input current; e.g. if a current of the order 10 nA is to be measured to within 1 %, the current drawn by the measuring device must not exceed 0.1 nA. The circuit of Fig. 7.6 uses a DOA40 module with an FET input circuit, which presents a very high impedance, to satisfy this condition.

Fig. 7.6. Small current measuring circuit.

To achieve accurate measurements it is essential that the drain current of the FET is adjusted to a value where the temperature coefficient of V_{gs} is negligible; adjustment is made in the following way:

– adjust potentiometer R_1 to set the output of the DOA40 module to zero,

– heat the FET. If the output of the DOA40 alters significantly from zero, the drain current is either too high (positive output) or too low (negative output) and must be readjusted to zero using potentiometer R_2.

– The procedure should be repeated until the optimum condition is attained.

Reference diodes (BZY78) are included to reduce the influence of supply voltage variations on the offset voltage, and the range of currents that can be measured is selected by using switch S to connect different values of feedback resistors.

7.2.5 COMPENSATION OF TRANSDUCER ZERO ERROR

This circuit provides a means of eliminating or greatly reducing the zero error (caused by drift etc.) in a transducer and the following pre-amplification stages of a measuring circuit. The error compensation is made

automatically without recourse to a meter; time-consuming adjustment of controls before each measurement are not necessary.

The circuit shown in Fig. 7.7 operates in the following way. With switch S_1 closed, switch S_2 open and the transducer unactivated, a possible error signal from the transducer is amplified by U_1 and applied to the hold circuit U_2, the output of which is connected to a differential amplifier U_3. After a time long enough (approx. 1 sec.) to charge C_2, switch S_1 is opened, switch S_2 closed and the transducer is activated.

Fig. 7.7. Compensation circuit. Supplies of $+15$ V and -15 V are required. Resistors R1, 2, 4, 6, 10, 11, 12 and 13 are 1% types.

The resulting signal (including error) is amplified by U_1 and applied to the negative input of U_3. The output of U_3 is then the difference between the error signal applied to termined 1 via R_{11} and the measured value plus error applied to terminal 3 via R_{10}. Thus the measured value without the error signal appears at the output of U_3.

Switches S_1 and S_2 can be either manually operated, or relay-operated reed switches. In the latter case, with the addition of a timer unit, the above process can be carried out automatically.

7.2.6 MEASUREMENT OF LIGHT INTENSITY

A common method of measuring light intensity consists of illuminating a photo-emissive cell, the cell current giving a measure of the light intensity. However, the relationship between current flow and light intensity is linear only if the voltage across the cell is maintained at a low value (a few millivolts).

This requirement is met by connecting the cell to the input of a DOA40 operational amplifier (U_1) shown in Fig. 7.8, the high gain of the amplifier holding the input at almost zero voltage. The output voltage of the amplifier is equal to the product of cell current I_c and feedback resistance R_f, where the latter can be selected in steps with switch S_1.

Fig. 7.8. Light intensity measuring circuit. Supplies of $+15$ V and -15 V are required.

Accurate measurement of low currents is limited by the input current to U_1; when this input current (20 nA max.) becomes significant in relation to the cell current I_c, accuracy falls. Current compensation can be made by adjusting R_1 to give the correct U_1 output for the minimum cell current to be measured. In this case a lower limit to the cell current I_c that can be measured is imposed by the temperature drift (0.5 nA/deg.C max.) of the DOA42.

The circuit can be extended to the measurement of total light energy (e.g. from flash lamps) by integrating the output of the amplifier. This is done by connecting a second DOA42 module (U_2) as an integrator to the output of U_1. Integration is initiated by closing switch S_2 and opening S_3. Current compensation of U_2 can be performed as for U_1 by adjusting R_6.

66

7.3 Input Devices

7.3.1 WIEN BRIDGE OSCILLATOR WITH STABILIZED OUTPUT VOLTAGE SWING

The use of the DOA40 module with a conventional Wien bridge circuit results in an oscillator with a very stable output with regard to frequency and amplitude. With the configuration shown in Fig. 7.9, and a ± 12 V supply, the output is a sine wave of 18 V p-p (approx. 6 V r.m.s.) whose frequency is adjustable between 1 kHz and 15 kHz. The stability achieved using components with a 2 % tolerance was within 0.1 % over an 8-hour period at 2 kHz; i.e. at 2 kHz the output varied by less than $\pm$ 2Hz.

The frequency of the output is adjusted by means of ganged potentiometers R_1 and R_2 in two branches of the bridge, their common point being connected to terminal 1, the positive input of the DOA40. The gain of the circuit is controlled via the potential divider R_6 and R_7 and feedback resistor R_3; the amount of feedback is also influenced by the combined impedance of R_4 and TR_1.

A rise in output voltage is detected and fed to the gate of TR_1 via potentiometer R_5. The gate voltage sets the working point, and hence the drain impedance, of TR_1; the feedback to the negative input of the DOA40 is thus altered to restore the output level to that set by R_6. Because the gate impedance of TR_1 is very high there is negligible current drain from the detection circuit, resulting in a good degree of stability.

Fig. 7.9. Wien bridge oscillator circuit.

7.3.2 Variable Pulse Generators

The pulse generator shown in Fig. 7.10 (a) produces a square wave output voltage whose pulse duration t_p is directly proportional to the capacitance of C_i and the feedback resistance R_f; the pulse duration is given by the expression:

$$t_p = R_f C_i \log_e \left(1 + 2\,\frac{R_1}{R_2} \right).$$

The potentiometer in the feedback loop is variable over a wide range, so enabling the duty cycle to be varied from 0.13 ms to 18.3 ms. The pulse amplitude is 20 V (-10 V to $+10$ V), and the minimum load resistance at the highest p.r.f. (0.13 ms duty cycle) is 10 kΩ. Terminals 2 and 12 of the DOA40 module are left open circuit to avoid limiting the switching speed. With the feedback arrangement shown in Fig. 7.10 (b) the positive and negative parts of the duty cycle can be varied independently. The expression for t_p remains valid, but the value of R_f is different for the positive and negative pulse durations, i.e., for the positive pulse $R_f = R_5 + R_6$, and for the negative pulse $R_f = R_3 + R_4$.

(a)

(b)

Fig. 7.10. (a) Pulse generator (variable duty cycle)
(b) Pulse generator (variable pulse width).

7.3.3 Dual Voltage Reference Unit

The voltage reference unit shown in Fig. 7.11 produces two independently variable output reference voltages of opposite polarities. The two voltages are derived from the same high stability reference diode (BZX48) which has a very low thermal drift characteristic.

The current through the reference diode is adjusted for optimum performance by means of potentiometer R_1, and the diode voltage is fed to the positive input of the DOA40 module U_1. The negative output of this module is further amplified by module U_2 to produce the negative reference voltage. Adjustment of this voltage is by means of potentiometers R_2 and R_3 (coarse and fine respectively).

The output of module U_1 is also fed to the negative input of module U_3 to produce the positive reference voltage. This voltage is adjusted by means of potentiometers R_5 and R_6 (coarse and fine respectively).

The two output voltages can be varied to a maximum value of 5 V, and the maximum permissible current drain from the outputs is 5 mA. Thermal drift of the output voltages was found to be 0.2 mV/degC.

The output voltage range can be extended to 10 V by replacing R_4, R_7 and R_8 (20 kΩ) by resistors of value 10 kΩ, and by using a 15 V supply. All resistors used were metal film, type MR39E, RN60E.

Fig. 7.11. Dual voltage reference unit.

7.3.4 HIGH VOLTAGE STABILIZER

The circuit in Fig. 7.12 operates from a 1000 V d.c. source and produces a stabilized output at 600 V d.c.; it comprises a tube and transistor series regulator which is controlled by a low level circuit employing a DOA40 feedback amplifier.

When the output voltage tends to rise above the level set by potentiometer R_1, the positive input of the DOA40 module becomes more negative. This negative signal is amplified and fed to the base of the series transistor (2N930) so reducing the current flowing in the transistor and the tube (EL34). Therefore the anode to cathode voltage across the tube is increased, and the output voltage is reduced correspondingly, to the original level.

A feature of this circuit is that capacitor C_1 renders the feedback ratio for a.c. signals higher than that for d.c. signals. This has the effect of suppressing ripple voltage, or short-duration transients.

The circuit is protected against short circuits across the output by the zener diode BZY88, and against reverse e.m.f.s. (caused by switching inductive loads) by the diode BYX25.

Hence, the main properties of the circuit are:
- output voltage range 0 to 600 V
- output current 5 mA
- stabilizing factor better than 0.1 %
- output ripple voltage < 0.5 mV$_{p-p}$ for input ripple voltage of 10 V.

Fig. 7.12. Circuit diagram of high voltage stabilizer.

70

This circuit satisfies the requirements of a drive voltage source for a colour TV tube. Increased output voltages and currents can be obtained using the same circuit, the limiting factor being the rating of the EL34 tube. For currents exceeding 100 mA the series transistor (2N930) should be replaced by two transistors connected as a Darlington pair.

7.4 Process and Alarm Control Circuits

7.4.1 TEMPERATURE CONTROL USING THYRISTORS (T.R.C. MODE)

The pulse generator connected to produce independently variable positive and negative pulse widths, described in Section 7.3.2, forms the basis of the temperature control circuit shown in Fig. 7.13. One of the feedback loops contains a PTC resistor, and the second contains an NTC resistor. These resistors are mounted in close proximity to the temperature controlled medium and form the sensors of the system. The ratio of the positive to negative pulse widths at the pulse generator output is thus proportional to the temperature of the medium.

The system operates on the principle of time ratio control (T.R.C.) with zero-crossing triggering, which means that the on-plus-off period of the switched thyristors extends over many cycles of the a.c. supply. Therefore, with zero-crossing triggering, the thyristors conduct over complete half cycles and the advantages of operation at optimum power factor (as sinusoidal current is drawn from the mains supply) and minimum radio interference (thyristor switching occurs at zero crossing of the mains supply cycles) are evident. As the temperature of the controlled medium varies, the duty cycle (ratio of on period of the thyristors to the total on-plus-off period) varies so as to restore the temperature to the set value.

The PA60 power amplifier is connected as a multivibrator and is controlled by the silicon controlled switch SCS_1 which is driven by the output of the DOA40 pulse generators. Trigger pulses at 10 kHz are produced by the multivibrator and are fed to the thyristors via trigger transformer T_1 (TT60). The action of the thyristor trigger circuit for zero voltage crossing is described below.

The a.c. input voltage is rectified by D_1. With SCS_1 turned on, the input circuit is virtually short circuited and the potential applied to input terminal 2 of the PA60 amplifier is held at the LOW level (approx. 1 V); the multivibrator action is thus inhibited, no trigger pulses are produced, and the thyristors are non-conducting.

71

Fig. 7.13. Temperature control circuit.

72

When SCS_1 is turned off (by the output from the DOA40), the rectified voltage is clipped to 12 V by zener diode D_2, and this HIGH level is applied to terminal 2 of the PA60.

Multivibrator action now occurs and trigger pulses are fed via T_1 to the thyristor gates causing them to conduct.

Synchronized thyristor switching is achieved as follows; waveforms are shown in Fig. 7.14. When the cathode-gate drive to SCS_1 is removed (at time t_1), SCS_1 turns off at the end of that half cycle of the rectified supply when the anode current drops below the holding level (at time t_2). Since SCS_1 remains turned off, the PA60 produces a 10 kHz pulse train which is continuous except for the short interval (Δt) between half cycles of the rectified supply voltage, i.e. when the instantaneous voltage across D_2 is too low to keep terminal 2 of the DOA40 at the HIGH level.

Since the gating pulses are applied early in each half cycle, the output thyristors start to conduct almost as soon as their anode voltage becomes positive. The gate drive is maintained over 180°, ensuring reliable thyristor turn-on, even in the case of a highly inductive load.

At time t_3 the cathode-gate drive to SCS_1 is restored, SCS_1 conducts and the PA60 is inhibited; the conducting thyristor remains turned on until that half cycle is completed (t_4).

The repetition rate of the PA60 output is determined by the choice of values of R_7 and C_1. Voltage surges, produced by the primary winding of T_1 during switching, are suppressed by D_5. This diode also prevents transformer saturation by providing rapid decay of current through the

Fig. 7.14. Thyristor switching waveforms.

73

primary winding during cut-off of the output transition of the PA60. Diode D_4 prevents the output of the PA60 becoming short circuited.

Using the circuit described, an oven was controlled at a temperature of 90 °C to within $\pm$ 1 degC. Potentiometer R_1 connected in series with the NTC sensor permits adjustment of the controlled temperature.

7.4.2 TOLERANCE MEASURING CIRCUIT (TOLERANCE SEQUENTIAL COMPARATOR)

A much encountered problem in the field of measurement and control is the comparison of consecutive signals. For example, a signal derived from a standard source may be required to set the upper and lower tolerances for a following signal. If the second signal exceeds these limits a digital output is generated which may be used, say, to readjust a system or reject a faulty product.

The circuit shown in Fig. 7.15 operates as follows. A reference voltage is fed to input terminal 1 and thence to the DOA40 module U_1 which is connected as an impedance transformer. Current compensation is applied to U_1 by the adjustable (0-1 μA) current source formed by TR_1 and TR_2.

With relay switch RA closed (relay coil energized) the output of U_1 charges capacitor C_1 (via 4.7 kΩ resistor); this charge is the reference level (V_1) with which the signal input is to be compared, and is stored by C_1 (RA is now open) by virtue of the high input impedance presented by TR_3 (FET). Potentiometer R_1 is adjusted to produce equal voltages at the gate of TR_3 and the emitter of TR_5 (and hence the emitter of TR_4). The signal is inverted by module U_2 to give $-V_1$.

With switch RA still open, the signal input is fed to input terminal 1 and a signal (V_2) is produced at the output of U_1.

The two signals from U_1 and U_2 are fed to two adders, modules U_3 and U_4 which give similar outputs representing $V_2 - V_1$. The desired limits are preset by potentiometers R_2 (upper limit) and R_3 (lower limit). If the algebraic sum of V_1 and V_2 is too high, V_2 feeds an output to pulse shaper PS10 (U_5) which produces a positive pulse. This pulse is inverted and fed to the OR gate of module U_7 (2GI10). If the algebraic sum is too low, U_4 feeds an output to U_6 which produces a positive pulse. This pulse is also inverted and fed to the OR gate of U_7. In this way the OR gate produces an output whenever the input signal exceeds either the upper or the lower tolerance set by the reference signal.

Fig. 7.15. Sequential comparator.

75

Plant growth sensing equipment: ambient temperature is controlled by PSM40 regulated thyristors.

Plant growth measuring and recording apparatus: small signal inputs are sensed and amplified by DOA40 module amplifier circuits.

7.4.3 SINGLE-LINE MULTITONE TRANSMISSION SYSTEM

In alarm and warning systems where distances between monitoring points and control point are great, or difficult to bridge, a large proportion of the cost is that of transmission lines. This system considerably reduces costs by employing only one double-core transmission line to connect all monitoring points to the control point.

The system is based on the use of different low-frequency signals for each monitor point. These signals are generated by stabilized Wien bridge oscillators as described in Section 7.3.1. Matching receivers at the control panel filter the incoming information and thereby relate it to the monitor point concerned.

The transmission line used is a 600 Ω double-core cable, which has a bandpass of 300-3400 Hz; thus 12 monitoring points may be employed. If more points are required, a wider bandwidth cable may be used, or several systems may be connected in parallel. DOA40 operational amplifiers are used in the transmitters and receivers.

A block diagram of the system is show in Fig. 7.16, and the circuit diagram of a transmitter is given in Fig. 7.17.

Fig. 7.16. Single-line multitone transmission system.

A DOA40 amplifier is used, in conjunction with the series-parallel RC network, to form a Wien bridge oscillator. Output voltage swing is held constant by means of the FET, which is controlled by a detected rendering of the amplifier output signal (FET gate voltage must be set, by adjustment of R_4, to give an output voltage from the DOA40 of 18 V peak-to-peak — see Section 7.3.1).

Fig. 7.17. Circuit diagram of a transmitter.

Parts List for Transmitter Circuit Diagram

All fixed resistors 1/8 W, $\pm 5\%$.

R_1 = 4.7 kΩ
R_2 = 1 kΩ
R_3 = 15 kΩ, potentiometer
R_4 = 100 kΩ, potentiometer
R_5 = 56 kΩ
R_6 = 6.8 kΩ
R_7 = 6.8 kΩ
R_8 = 2.2 kΩ
R_9 = 6.8 kΩ
R_{10} = 330 Ω
R_{11} = 15 kΩ
R_{12} = 4.7 kΩ
R_{13} = 39 kΩ
R_{14} = 68 kΩ
R_{15} = 47 kΩ
R_{16} = 5.6 kΩ
R_{17} = 220 Ω
R_{18} = 1.5 kΩ
R_{19} = 6.8 kΩ

C_1 = 2.7 μF
C_2 = 10 μF, 16 V
C_3 = 0.47 μF
C_4 = 10 μF, 16 V

TR_1 = BFW11 Field Effect Transistor
TR_2 = BC107
TR_3 = BC177
TR_4 = BFW11
T_1 = Transformer type AD9014
D_1 = BAX13

79

If there is no alarm, switch S_1 is closed and holds TR_3 and TR_4 off. Thus the transmitter output signal is not attenuated by the lower part of the system but is fed, via TR_2 and T_1, into the transmission line; the signal fed into the line is approximately 650 mV r.m.s. if the line impedance is 600 Ω (S_1 may be replaced by static switch, e.g. a NORbit).

An alarm signal opens S_1, turning on TR_3 and TR_4 and thus attenuating the signal on the base of TR_2 by a factor of 10.

The output impedance of the line transformer is 7600 Ω so, if 12 transmitter units are connected to one transmission line, the total shunt impedance at the line is 633 Ω. If less than 12 transmitter units are used, 7500 Ω resistors must be substituted so that the total number of units and resistors is always 12.

The receiver unit comprises a single input circuit (Fig. 7.18) and up to twelve selective amplifiers (Fig. 7.19).

Fig. 7.18. Receiver input circuit.

The receiver input circuit is an impedance matching stage between the transmission line and the selective amplifiers, and comprises an input transformer (T_1) feeding an emitter follower. The emitter follower is a.c. coupled to the selective amplifiers. Each amplifier is a DOA40 module with a twin-T network in the feedback loop which gives a Q factor of 10. The resonant frequency is determined by the choice of values of R and C in accordance with the formula $f = (2\pi RC)^{-1}$; thus the same values of R and C are used in a receiver as in the corresponding transmitter (see table - page 82).

80

Fig. 7.19. Circuit diagram of a receiver.

Parts List for Receiver Circuit Diagram

All fixed resistors 1/8 W; $\pm$ 5%.

$$R_1 = 10 \quad k\Omega$$
$$R_2 = 10 \quad k\Omega$$
$$R_3 = 1 \quad k\Omega$$
$$R_4 = 22 \quad k\Omega, \text{ potentiometer}$$
$$R_5 = 2.2 \text{ k}\Omega$$
$$R_6 = 12 \quad k\Omega$$
$$R_7 = 100 \quad k\Omega$$
$$R_8 = 15 \quad k\Omega, \text{ potentiometer}$$
$$R_9 = 2.2 \text{ k}\Omega$$
$$R_E = \text{(see text)}$$
$$C_1 = 100 \quad \mu F \text{ (10 V)}$$
$$C_2 = 0.5 \ \mu F$$
$$D_1 = \text{BAX13}$$
$$D_2 = \text{BZY88/C3V9}$$
$$TR_1 = \text{BC107}$$
$$T_1 = \text{Transformer type AD9014}$$

81

The amplification factor is varied by means of potentiometer R_4; this potentiometer should be adjusted to give an output voltage of 6.5V r.m.s.

The output voltage is detected by diode D_1 and is fed to two 60-series NORBITS which are connected as a Schmitt trigger circuit. Resistor R_E (180 Ω to 470 Ω) is chosen to set the triggering voltage between 3.2 V and 3.8 V with a maximum output voltage of 7 V. The $+12$ V supply voltage for the 60-Series NORbits allows the output to be loaded with four DU drive units.

f (Hz)	R (kΩ)	C (nF)
330	10	47
405	10	39
480	10	33
590	10	27
720	10	22
885	10	18
1060	10	15
1330	10	12
1580	10	10
1930	10	8.2
2330	6.8	10
2850	6.8	8.2

If the working frequencies of the transmitter and receiver are not identical, matching may be effected by connecting suitable resistors across R in either the transmitter or the receiver.

7.4.4 ON/OFF CONTROL SYSTEM FOR TEMPERATURE REGULATION

The on/off temperature regulation system described below is an extremely simple design intended for use with the resistive, or nearly resistive, loads commonly associated with temperature control systems. The load (heater) is switched by means of a single thyristor which is connected across the output of a diode bridge; the load itself is in series with this bridge across the a.c. supply.

Thermistors are used as temperature sensors and the control circuits have a low on/off differential to achieve high control sensitivity, this minimizing temperature overshoot. The control amplifier may be con-

nected either as a simple high-gain amplifier in a system where the amplifier output is directly proportional to the absolute temperature, or as an error amplifier in a system where the amplifier output is proportional to temperature deviation from a set point.

The system shown in Fig. 7.20 uses NTC thermistor R_1 as the temperature sensing element; as the temperature rises, the resistance of R_1 decreases causing the voltage at input terminal 3 of the DOA40 to decrease. When this voltage becomes negative, i.e. when the temperature exceeds the value set by R_2, the DOA40 output swings positive and TR_1 is cut off. Thus the gate drive to thyristor TH_1 is inhibited and the heater (load) is switched off. Conversely, when the temperature becomes too low, the output from the DOA40 swings negative, TR_1 is turned on and TH_1 is triggered; mains current then flows in the heater.

In the control circuit shown in Fig. 7.21 the DOA40 is connected as

Fig. 7.20. Direct temperature control system.

Fig. 7.21. Temperature control by error detection.

83

an error amplifier; the controlled-variable signal (related to controlled temperature) is applied to terminal 3, and the set point signal (desired value) to terminal 1. An error signal (the potential difference between terminals 1 and 3) thus represents the deviation of the actual temperature from the desired temperature. The former is sensed by NTC thermistor R_1, and the latter is set by potentiometer R_2. In all other respects this circuit is identical to that shown in Fig. 7.20.

In the two circuits described, proportional control exists over a narrow band because the control action is not truly on/off. When the actual temperature approaches the set point from a low value (furnace heating up), the output from the DOA40 rises from a negative value towards 0V; thus TR_1 starts to switch off and the collector current (gate drive current) decreases. As this current decreases, the triggering angle of TH_1 moves from a value approaching 180° (maximum current fed to load) towards 90° (minimum current fed to load). As the set point lies within this proportional band, TH_1 will switch off completely only when the furnace temperature is excessively high, e.g. when cooling down to a new set temperature. The principle of proportional control is illustrated in Fig. 7.22 where diagrams (a) and (b) show how the conduction angle decreases

a. Thyristor anode-to-cathode voltage; hatched areas indicate conduction periods (90° to almost 180° conduction angle)
b. Minimum gate current to trigger the thyristor; dotted lines indicate gate drive level; points of intersection, P, denote triggering points.
c. Amplifier output vs. controlled variable (temperature).

Fig. 7.22. Proportional control over a narrow band.

as the gate drive current decreases and the conduction periods reduce gradually to 90° before switch-off occurs.

From the foregoing it will be realized that these circuits combine the simplicity of on/off control with the desirable properties of proportional control. The degree of control accuracy which can be achieved is as good as $\pm$ 0.8 degC for a furnace temperature of 55 °C. Some general recommendations regarding the practical aspects of on/off temperature control are as follows.

- The temperature sensor must be mounted close to the heating element to minimize thermal lag and, consequently, temperature overshoot.

- Air circulation within the furnace is desirable to minimize the process dead time and optimize temperature control. The dead time is the delay between a step change in the process input parameter and the resultant step change in the process output parameter. Processes with a long dead time are difficult to control. Air circulation also helps to establish a uniform temperature throughout the heated space.

- The thermal capacity of the sensor must be as low as possible so that its thermal time constant does not significantly add to that of the process. Bead type thermistors are, therefore, preferred. However, with these thermistors it is necessary to limit the current flowing through them to a low level so as to avoid self-heating effects, and this results in a rather low signal for the control circuit. Hence the selection of a particular thermistor type is a compromise between the characteristics of the thermal process and the control sensitivity.

Selected Components for Maximum Output Power

TH_1	D_1 to D_4 *	R_3 (33 Ω)	C_1 (1000 V d.c.)	$P*$
BTY79-600R	BYX38- 900(R)	1 W	0.1 μF	1.5 kW
BTX68-600R	BYX38- 900(R)	1 W	0.1 μF	1.5 kW
BTY87-600R	BYX48- 900(R)	1 W	0.1 μF	2.9 kW
BTX35-600R	BYX48- 900(R)	1 W	0.1 μF	2.9 kW
BTY91-600R	BYX42- 900(R)	1 W	0.1 μF	3.8 kW
BTX36-600R	BYX42- 900(R)	1 W	0.1 μF	3.8 kW
BTX81-600R	BYX13-1000(R)	2 W	0.15 μF	4.8 kW
BTX82-600R	BYX25-1000(R)	2 W	0.15 μF	6.3 kW

* P = max. output power at 220 V a.c. into a resistance load.

7.4.5 Proportional Plus Integral Action Temperature Controller

The dual mode temperature control circuit described in this Section combines the advantages of; the response of proportional control to transients, and the elimination of offset achieved with integral control. Sudden changes in thermal load, or changes in temperature setting, cause disturbances in controlled temperature to occur that are generally damped out rapidly by proportional action; then, the sustained temperature deviation (offset) inherent in proportional control, is reset to zero by integral action.

Proportional gain and integral action are both adjustable. Thus, adaption to a particular thermal process is possible.

Thyristors are used to control the heater load. To eliminate the non-linear change in output power experienced in phase control, the heater voltage is fed back into the circuit. This feedback also reduces variations of controlled temperature with a.c. voltage fluctuations. A platinum resistance thermometer is used as a temperature sensor. Its advantages are high output, good linearity, and very low drift with time.

This system is suitable for highly demanding applications requiring zero offset and high long-term stability of controlled temperature. With the circuit, as specified, the maximum controllable temperature is 100 °C. Long-term temperature drift is as low as 0.3 deg.C.

Fig. 7.23 shows the circuit diagram of the dual mode control system (proportional plus integral control). A highly stable bridge, consisting of $R_2, R_3, R_4, R_6, R_7, R_8$, is supplied from a stabilized current source $TR_1 \, TR_2$ and forms the input to the control system. Platinum resistance thermometer R_2 has three-wire connection to eliminate the effect on system performance of change in lead resistance with temperature. The controlled temperature is set by adjustment of R_7. The bridge output is about 2 mV/degC.

Differential amplifier DOA42 is supplied at its inputs by the set point signal and the measured variable (input "+in"). The difference between both signals, the error signal, is monitored by meter V; diodes D_2, D_3 provide meter protection.

To allow setting of proportional and integral control, the output of the DOA42 is fed, via a phase shifting network (C_1 and R_{19} to R_{31}) with an adjustable time constant, to TR_3, TR_4, TR_5; a variable part of the collector signal of TR_5 is fed back to the "—in" input. Amplifier TR_3, TR_4, TR_5 is necessary to minimize loading of the phase shifting

network. Since the input resistance at the base of TR_3 is 250 MΩ, the amplifier input resistance is almost entirely determined by the value of biasing resistors R_{37}, R_{38} (amplifier input resistance about 22 MΩ). Provided the bridge resistance at points A and B is low with respect to R_{11} and R_{12}, amplifier performance can be approximately expressed as:

$$G = \frac{\text{DOA42 output}}{\text{error signal}} \approx \frac{R_{14}}{\alpha R_{11}}\left(1 + \frac{1}{j\omega T_j}\right)$$

where α = attenuation of network R_{32}, R_{34} adjusted with R_{34}; reset time T_j = product of C_1 and one of resistors R_{19} to R_{31}.

This expression holds as $R_{11} = R_{12}$ and $R_{14} = R_{16}$.

Potentiometer R_{34} serves to adjust proportional gain; S_1 permits choice of the proper value of integral time (T_j adjustable between about 2 and 750 s).

Transistor TR_7 is driven by the DOA42 output applied to its base through D_4, R_{33} and feedback potentiometer R_{41} (C_3 filters out noise). As the DOA42 output depends on the error signal, the strength of base drive and thus the charge rate of timing capacitor C_4 depends on the deviation of controlled temperature from the set value. The capacitor charge rate determines the thyristor trigger angle, as explained below.

Regenerative transistor pair TR_8 TR_9 saturates as soon as the voltage across C_4 exceeds the zener voltage of D_{10} by a sufficient amount. A pulse is then applied via T_1 to the gates of TH_1 TH_2, triggering one of these thyristors.

Synchronization of the trigger circuit is achieved by discharge of C_4 near the end of each half cycle. Synchronizer operation is evident from Fig. 7.24, in which the difference of the ordinates of curves 1 and 2 represents the base-emitter voltage of TR_6 if emitter junction protection

Fig. 7.24. Synchronizer operation. Curve 1: voltage across R_{49} and R_{51}; Curve 2: voltage across C_6

Fig. 7.23. Circuit diagram of dual mode control system.

Components List to Fig. 7.23

Resistors

R_1 =	560	Ω,	5%, carbon film resistor, style CR25	2322 101 33561
R_2			three-lead Pt resistance thermometer, 100 Ω at 0 °C	
R_3 =	1	kΩ, 0.25%,	precision wire-wound resistor	2322 260 61002
R_4 =	20	Ω,	linear potentiometer	
R_6 =	1	kΩ, 0.25%,	precision wire-wound resistor	2322 260 61002
R_7 =	50	Ω,	ten-turn potentiometer	
R_8 =	100	Ω, 0.25%,	precision wire-wound resistor	2322 260 61001
R_9 =	388	Ω, 0.25%,	precision wire-wound resistor	2322 260 63881
R_{11} =	1	kΩ,	5%, carbon film resistor, style CR25	2322 101 33102
R_{12} =	1	kΩ,	5%, carbon film resistor, style CR25	2322 101 33102
R_{13} =	330	Ω,	linear potentiometer	
R_{14} =	220	kΩ,	5%, carbon film resistor, style CR25	2322 101 33224
R_{16} =	220	kΩ,	5%, carbon film resistor, style CR25	2322 101 33224
R_{17} =	10	Ω, 0.25%,	precision wire-wound resistor	2322 260 61009
R_{18} =	25	kΩ,	linear potentiometer	
R_{19} =	56	kΩ,	5%, carbon film resistor, style CR52	2322 101 63563
R_{21} =	120	kΩ,	5%, carbon film resistor, style CR52	2322 101 63124
R_{22} =	180	kΩ,	5%, carbon film resistor, style CR52	2322 101 63184
R_{23} =	330	kΩ,	5%, carbon film resistor, style CR52	2322 101 63334
R_{24} =	470	kΩ,	5%, carbon film resistor, style CR52	2322 101 63474
R_{26} =	820	kΩ,	5%, carbon film resistor, style CR52	2322 101 63824
R_{27} =	1.5	MΩ,	10%, carbon film resistor, style CR52	2322 101 62155
R_{28} =	2.7	MΩ,	10%, carbon film resistor, style CR52	2322 101 62275
R_{29} =	4.7	MΩ,	10%, carbon film resistor, style CR52	2322 101 62475
R_{31} =	8.2	MΩ,	10%, carbon film resistor, style CR52	2322 101 62825
R_{32} =	220	Ω,	5%, carbon film resistor, style CR25	2322 101 33221
R_{33} =	12	kΩ,	5%, carbon film resistor, style CR25	2322 101 33123
R_{34} =	10	kΩ,	linear carbon potentiometer	2322 350 01007
R_{36} =	15	kΩ,	5%, carbon film resistor, style CR25	2322 101 33153
R_{37} =	2×22	MΩ,	10%, in series, carbon film resistor, style CR52	2322 101 62226
R_{38} =	2×22	MΩ,	10%, in series, carbon film resistor, style CR52	2322 101 62226
R_{39} =	2.2	kΩ,	5%, carbon film resistor, style CR25	2322 101 33222
R_{41} =	500	Ω,	linear potentiometer	
R_{42} =	1	kΩ,	5%, carbon film resistor, style CR25	2322 101 33102
R_{43} =	3.9	kΩ,	5%, carbon film resistor, style CR25	2322 101 33392
R_{44} =	470	Ω,	5%, carbon film resistor, style CR25	2322 101 33471
R_{46} =	1	kΩ,	5%, carbon film resistor, style CR25	2322 101 33102
R_{47} =	330	Ω,	5%, carbon film resistor, style CR25	2322 101 33331
R_{48} =	3.3	kΩ,	5%, carbon film resistor, style CR25	2322 101 33332
R_{49} =	270	Ω,	5%, carbon film resistor, style CR25	2322 101 33271
R_{51} =	2.2	kΩ,	5%, carbon film resistor, style CR25	2322 101 33222
R_{52} =	33	Ω,	10%, carbon film resistor, style CR68	2322 214 12339

Capacitors

$C_1 = 5 \times 6.8$ µF, 10%, in parallel,
metallized polycarbonate capacitor, 100 V
2222 344 21685

$C_2 =$	250 µF, 25 V,	electrolytic capacitor, $-10\%/+50\%$	2222 023 16251
$C_3 =$	40 µF, 16 V,	electrolytic capacitor, $-10\%/+50\%$	2222 001 15409
$C_4 =$	100 nF, 10%,	metallized polycarbonate capacitor, 100 V	

2222 341 29104

$C_6 =$	16 µF, 10 V,	electrolytic capacitor, $-10\%/+50\%$	2222 001 14169
$C_7 =$	100 nF, 10%,	metallized polycarbonate capacitor, 1250 V	

2222 343 79104

TR_1	$=$ BCY32	
TR_2	$=$ BCY10	
TR_3, TR_4	$=$ 2N2484	
TR_5	$=$ BCY32	
TR_6	$=$ 2N1711	
TR_7, TR_8	$=$ BCY39	
TR_9	$=$ BSY10	
D_1	$=$ BZY78	
D_2, D_3	$=$ OA200	$TH_1, TH_2 =$ BTX36-700R
D_4	$=$ BZY63	T_1 $=$ trigger transformer, 3 windings 50 turns
D_5	$=$ OA200	0.22 mm diam. each, P30/19 core
D_6	$=$ BY122	T_2, T_3 $=$ transformer 220/20 V
D_7, D_8, D_9	$=$ OA200	V $=$ Deviation meter
D_{10}	$=$ BZY56	S_1 $=$ Reset time adjust switch
D_{11}, D_{12}	$=$ OA200	S_2 $=$ Mains switch
D_{13}	$=$ BY122	

diode D_5 were not present. It is seen that, almost at the end of the half cycle, the transistor is made to conduct, thus discharging the timing capacitor. Consequently, the capacitor is charged afresh each half cycle (thyristors conducting in turn).

Non-linear elements are highly undesirable in process control. Thyristors function as non-linear elements when phase-controlled, as the controlled power is not proportional to the conduction angle. To obtain linearization, the heater voltage is rectified by D_6 and the resultant d.c. voltage, produced across R_{41}, is injected into the base circuit of TR_7 to obtain negative feedback. The variation in heater power with the measured variable is approximately linear when the heater resistance increases linearly with heater temperature.

Temperature control is as follows. When the temperature tends to rise, thermometer R_2 increases its resistance. This causes the voltages at the "+in" and output terminal of the DOA42 to change in positive direction,

so that TR_7 receives less base drive. Timing capacitor C_4 is charged more slowly and the thyristors are triggered later each half cycle. Less power is supplied to the heater, to counteract the rise in temperature.

The following adjustment procedure, according to Ziegler and Nichols, is recommended to obtain good process control. Amplifier gain is adjusted to about half the value at which control becomes unstable. Then integral action is added, the reset time, τ_i, being reduced to $1/1.2$ times the period of oscillations.

Stabilized voltages are advisable for d.c. supply.

7.4.6 PHOTO-ELECTRIC POSITIONING SYSTEM

The detection of displacement of objects by means of photo-electric devices is a widely used technique in the field of industrial control. A disadvantage inherent to many types of photo-electric devices is the change of parameters with time and temperature, and the natural spread in parameters. These effects are minimized by the circuit shown in Fig. 7.25.

The circuit is designed to ascertain that two plates are exactly situated in pre-defined relative positions. Two silicon photovoltaic sensor cells are mounted at one side of the two plates, and a single lamp is mounted at the opposite side. Holes in the two plates allow equal amounts of light to fall on the two sensors when the plates are correctly positioned.

Fig. 7.25. Photo-electric positioning system.

With correct positioning the outputs of the two sensors completely cancel each other and there is no input to the amplifier circuit. Initial balance between the cell currents is achieved by adjustment of potentiometer R_1.

Displacement of one plate relative to the other gives rise to unequal illumination of the sensors and, therefore, unbalanced cell currents. A voltage input is thus applied to the negative input of the DOA40 amplifier, and the polarity of the signal is an indication of direction in which the plate must be moved to achieve alignment. The amplifier output is used to drive an electro-mechanical transmission system which re-positions the displaced plate. The relative positions of the two plates can be controlled to within 10^{-6} m; at this setting the amplifier output voltage is between -1 V and $+1$ V.

It will be noted that, in this configuration, the DOA40 offers a very high gain (12×10^3), and, even with a source resistance of 10 kΩ, the feedback resistors are of moderate value.

In the foregoing material, positioning in only one direction has been described. It is, of course, quite easy to position the plates in two directions at right angles to each other in the same plane (X and Y directions). To do this it is only necessary to connect a similar but independent system to the plates with the additional photocells in the same plane as the first two (parallel to the plates) and to arrange the second electromechanical transmission system accordingly.

7.4.7 PROCESS ADJUSTMENT BY A DIFFERENTIATOR CIRCUIT

There are a variety of situations, especially in developmental work on a process, in which a number of variables so interact that the only practical method of achieving a desired result is by a trial and error approach. This method can usually be carried out fairly quickly if the response to an adjustment is immediate.

However in other processes (mainly chemical), adjustment of a variable produces a progressive change in the relative percentages of the constituents, giving a response which is time dependent. In this case, to obtain a desired result by simple response measurement can be very time-consuming, as the operator has little indication as to whether the effectiveness of an adjustment is decreasing (in which case we should adjust another variable) or increasing (in which case, despite an existing low rate of rise,

it may be advantageous to leave the settings unchanged). Curve A in Fig. 7.26 shows a hypothetical process in which a desired level L_D must be reached by adjusting three variables, using only an indicator of the value of L as a guide. Curve B in Fig. 7.26 shows the path followed in reaching level L_D when full information is known about the behaviour of the response following an adjustment. The circuit described here is designed to give such information; it provides an accurate indication of the rate of rise or fall in the function, and also indicates the rate at which this change is increasing or decreasing. Thus through the ability to predict to a certain extent the behaviour of the adjusted function, the time required to reach a desired result can be greatly shortened. Furthermore the process lends itself to automatic control as the meters may be replaced by a logic system giving a direct control of the input variables.

Fig. 7.26. Graphs of time against level L for a hypothetical process in which a desired level L_D must be reached by adjusting three variables.

The circuit shown in Fig. 7.27 consists of three operational amplifiers type DOA42, of which the first (U_1) acts as a 100 x inverting amplifier to which is applied a voltage directly proportional to the function to be adjusted. U_2 and U_3 are configured as differentiators, U_2 giving the first derivative of the function, while U_3 differentiates this result, yielding

93

Fig. 7.27. Differentiator circuit. Supplies of $+15$ V and -15 V are required.

the second derivative. Positive or negative values are read from centre-zero meters ME_2 and ME_3 connected to the outputs of the units. In thisl way the following information is obtained:

- meter ME_1 reads the value of the function output;
- if the function increases, decreases or reaches an optimum, meter ME_2 reads positive, negative or zero respectively, and indicates the rate of rise or fall;
- the rate of change of the function is measured by meter ME_3, increasing and decreasing rates being indicated by positive and negative readings respectively. Thus the meter indicates whether an optimum point is a maximum or minimum.

In Fig. 7.26 the first and second derivations L' and L'' indicated by the meters are shown at various points on curve A.

Units U_2 and U_3 of Fig. 7.27 are provided with offset current compensation networks to adjust the meter zero points. Diode limiting networks are used to prevent the DOA42 output voltage ratings from being exceeded. Compensation is applied between terminals K_1 and K_2 of U_2 and U_3 to obtain high stability and a low noise performance. For the same reason capacitors C_3 and C_7, and series resistors R_7 and R_{19} are added to the circuit.

94

The voltage gain of U_1 should be adjusted according to the magnitude of the input signal. The component values shown refer to a voltage gain of 100 which is suitable for input voltages between 1 and 100 mV, with $R_1 = 10$ kΩ. The input signal magnitude to U_2 and U_3 can be adjusted with potentiometers R_6 and R_{18}, while R_5, R_{17} and R_{28} adjust the respective meter sensitivities.

8 Closed-loop Power Control Systems using Operational Amplifier and Phase Shift Modules

8.1 General Considerations

There are two basic methods of operation of closed-loop electronic control systems which use thyristors, these are on/off control and proportional control. On/off control, as the name implies, causes the power supplied to the load to be either full on or full off, i.e., the thyristors are either non-conducting, or fully conducting. This mode of operation cannot eliminate overshoot and, therefore, cycling occurs.

With proportional control, power is supplied continuously to the process at a level determined by the phase angle at which the thyristors are triggered, and this is varied according to the immediate power demand of the load. In general, the degree of control accuracy that can be achieved using proportional control is higher than that using on/off control, and may be further improved by the use of, for example, integral or differential techniques.

8.1.1 PROPORTIONAL BAND

Any thyristor system connected for closed-loop proportional control can be reduced to the block diagram shown in Fig. 8.1.

Fig. 8.1. Block diagram of proportional control, closed-loop system.

The way in which the system operates is as follows. The process is monitored by a sensor whose output (output parameter) is fed to a transducer amplifier which produces a voltage output (measured variable). This voltage is fed to one input of a difference amplifier. A reference voltage, representing the desired state of the process (set point), is fed

from the reference generator to the second input of the difference amplifier. The output of the reference generator can be adjusted to alter the setting of the output parameter.

The difference amplifier output voltage is proportional to the difference between the measured variable and set point. This output voltage controls the control and trigger unit which in turn regulates the phase angle at which the thyristors are triggered and, therefore, the a.c. power supplied to the process via the thyristor unit.

Typical characteristics of a proportional control system are shown in Fig. 8.2; the vertical scale reads a.c. power supplied (expressed as a percentage of maximum power), and the horizontal scale is the measured variable. The scale of 0 to 100% represents the total range over which the system is capable of effecting control. The proportional band is the slope of the characteristic; this represents the range of the measured variable over which the a.c. power supplied varies between the maximum and minimum values.

The range of the proportional band is inversely proportional to the gain of the differential amplifier. Thus, if the gain is doubled the range of the proportional band is halved. In Fig. 8.2 proportional bands of 40% (C-D) and 10% (A-B) are illustrated.

Fig. 8.2. Typical characteristics of a proportional control system.

8.1.2 Offset

At initial switch-on the value of the output parameter is, say, much lower than that of the set point. A large difference input exists at the amplifier inputs and the thyristors are full on (maximum a.c. power). As the output

parameter approaches the set point the proportional band is entered and the phase angle at which the thyristors are triggered is reduced, thus reducing the a.c. power fed to the load.

As the set point is more closely approached the a.c. power is further reduced until the system stabilizes at a state where just enough power is supplied to compensate for losses; this point must be just below the set point. The difference between the set point and the point at which the measured variable stabilizes is termed "offset", and is necessary to maintain an output from the amplifier. With *no* difference input (i.e. when the measured variable equals the set point) the amplifier output would be zero and the thyristors would be turned off. Hence, when the system is set up an allowance must be made in the value of the set point to compensate for offset.

The value of offset can be minimized by increasing the amplifier gain and thus narrowing the proportional band. However, the amplifier gain cannot be increased beyond a certain value as the control system and process form a closed loop involving different time constants. These time constants cause phase shifts to occur in the control loop which lead to oscillations (hunting) when the loop gain is excessive.

To achieve optimum control performance, the amplifier gain is adjusted to half the value at which hunting occurs. The proportional band then covers twice the value of the critical range at which instability just rises.

8.1.3 Use of Operational Amplifier and Phase Shift Modules

In proportional control closed-loop systems of the type broadly described in this section, DOA40 or DOA42 modules may be used to perform the functions of the transducer and difference amplifiers, and PSM modules may be used as part of the control and thyristor trigger unit.

A circuit using a DOA40 module suitable for use as the transducer amplifier is described in Section 7.2.2. It may be possible to use one DOA40 module as a combined transducer amplifier and difference amplifier; such a circuit is described in Section 8.2.

The use of the PSM40 as part of the control and thyristor trigger unit following the difference amplifier produces a mains synchronized pulse output whose pulse width is proportional to the difference between the two analogue inputs, i.e. the difference between the measured variable and the set point.

The control accuracy of a system is dependent on a number of factors.

These are the stability of the measured variable and set point, the behaviour of the process to be controlled, and the properties of the control system itself. Accuracy can be improved by certain circuit refinements which can be incorporated; the exact nature of any refinement is largely dependent on the specific requirements and nature of the process or load to be driven. In the following sections some practical circuits are described. These circuits illustrate some of the possible applications of the DOA40 and PSM40 modules in proportional control closed-loop systems.

8.2 Proportional Control Closed-Loop Temperature Regulation Circuit

In this application one DOA40 module functions as a combined transducer and difference amplifier, and a PSM40 module forms part of the control and thyristor trigger circuit. A difference input is provided from across a temperature sensitive bridge network, and the trigger output circuit is formed by a PA60 power amplifier which is connected to operate as a multivibrator.

8.2.1 FUNCTIONAL DESCRIPTION (Fig. 8.3)

In operation the system functions as follows. A rise in the controlled temperature causes the resistance of R_2 to increase, and the voltage input to terminal 1 changes in the negative direction. Consequently the output from the DOA40 becomes less positive; this lessens the width of the output pulse from the PSM40, and therefore the period during which the PA60 oscillates, and the thyristor phase angle is reduced accordingly. Hence the power fed to the heating element is reduced and the rise in temperature is counteracted.

A similar action occurs when the set point is altered to establish a new (lower) controlled temperature. When the effective value of R_4 is decreased, the voltage input to terminal 3 becomes more positive. This reduces the difference input voltage to the DOA40, and the output becomes less positive. When the set point is increased, or when the controlled temperature falls, the difference input increases, the DOA40 output becomes more positive, and the pulse output of the PSM40 is lengthened. Thus the conduction angle is increased and more power is supplied to the heating element.

Fig. 8.3. Proportional control closed-loop temperature regulation circuit.

*R2 is located in close
proximity to the heater

100

Optimum system performance for a particular heater is obtained by choice of the values of R_1, R_2, R_3 and R_{11}, whilst fulfilling the condition $R_7 = R_8$ and $R_9 = R_{11}$. This ensures that the gains for the two inputs to the difference amplifier are equal, i.e., gain $R_9/R_8 = R_{11}/R_7$. The gain for optimum performance is usually approximately half the value at which the system becomes unstable; a closed-loop gain of approximately 130 for the DOA40 was found satisfactory for the circuit in Fig. 8.3. This circuit was used to control the temperature of an oven, and the control accuracy was within $\pm$ 1 degC; fluctuations in the a.c. supply voltage had no noticeable effect on the controlled temperature. Care is necessary in siting the resistance thermometer (R_2) as this type of sensor has a relatively large thermal lag. However, the consequent temperature overshoot during heating up is reduced by mounting R_2 close to the heater; this results in a minimum value of the overall thermal time constant. The output power that can be delivered to the heater is dependent only on the choice of thyristors and their associated RC network; table 8.1 gives details of output power, thyristor types, etc.

8.2.2 Circuit Description (Fig. 8.3)

The temperature sensitive bridge is formed by R_2, R_3, R_4, R_6; R_3 and R_6 are high-stability resistors, and are chosen to maintain long-term system accuracy. Temperature is sensed by R_2 which is a platinum resistance thermometer capable of a high degree of measuring accuracy for a wide temperature range (up to 800 °C) with negligible drift over a long period, and the required temperature is set by R_4 which is a 10-turn helipot. To avoid reducing the control accuracy it is preferable that a stabilized d.c. source (12 V) is available to supply the bridge.

The bridge output is applied as a differential input signal to terminals 1 (measured variable) and 3 (set point) of the DOA40 module. As the bridge output is fairly high (3.85 mV/degC), drift in amplifier parameters has an insignificant effect on overall performance. The input voltage offset of the DOA40 module is trimmed to zero by means of R_{12} with the bridge output short-circuited to earth.

The output from the DOA40 is fed from terminal 8 to the control input (terminal 7) of the PSM40 phase shift module. An input of between 0 V and $+5$ V d.c. is sufficient to vary the phase angle from $0°$ to $180°$; diode D_1 protects the control input against negative voltages. Anti-phase 50 Hz synchronizing signals (24 V r.m.s.) are fed from the centre-tapped

secondary winding of the mains fed transformer T_1 to terminals 11 and 12 of the phase shift module.

The PA60 amplifier is connected to function as a free-running multivibrator which is inhibited or enabled by the output from the PSM40. With the PSM40 output at the LOW level, the multivibrator is inhibited; when the PSM40 output switches to the HIGH level the PA60 oscillates and a 10 kHz trigger signal is produced. The frequency of the output pulses is determined by the values of R_{16} and C_2. This output is fed via trigger transformer T_2 (type TT60) to the gate electrodes of TH_1 and TH_2. The amplitude of the 10 kHz trigger pulses is approximately one-third of the positive supply voltage to the PA60 (8 V at $+24$ V supply). Voltage regulator diode D_4 prevents reverse voltage surges, generated in the primary winding of T_2 during switch-off, from appearing across the output of the PA60 amplifier; diode D_3 prevents the output of the PA60 amplifier from being completely short-circuited.

Table 8.1

thyristor type**	R_{21}	C_3	max. output (resistive load) at 220 V a.c.
BTY79-600R	33 Ω, 1 W	0.1 μF, 1 kVd.c.	3 kW
BTY68-600R*	33 Ω, 1 W	0.1 μF, 1 kVd.c.	3 kW
BTY87-600R	33 Ω, 1 W	0.1 μF, 1 kVd.c.	5.8 kW
BTX35-600R*	33 Ω, 1 W	0.1 μF, 1 kVd.c.	5.8 kW
BTY91-600R	33 Ω, 1 W	0.1 μF, 1 kVd.c.	7.7 kW
BTX36-600R*	33 Ω, 1 W	0.1 μF, 1 kVd.c.	7.7 kW
BTX81-600R	33 Ω, 2 W	0.15 μF, 1 kVd.c.	9.6 kW
BTX82-600R	33 Ω, 2 W	0.15 μF, 1 kVd.c.	12.5 kW

*   Controlled avalanche device
** The thyristors must be mounted on a heatsink to ensure that the maximum rated junction temperature is not exceeded.

Components List to Fig. 8.3

Capacitors

C_1 = 100 μF (electrolytic), 40 V,
$$+50\%\text{-}10\%$$
C_2 = 12 nF

Diodes

D_1 = OA85
D_2 = BAX16
D_3 = BAX16
D_4 = BYZ88-C9V1

Resistors (fixed)

R_1 = 560 Ω,	1%,	0.5	W
*R_3 = 100 Ω,	1%,	0.25	W
*R_6 = 100 Ω,	1%,	0.25	W
R_7 = 750 Ω,	1%,	0.25	W
R_8 = 750 Ω,	1%,	0.25	W
R_9 = 100 kΩ,	1%,	0.25	W
R_{11} = 100 kΩ,	1%,	0.25	W
R_{13} = 10 kΩ,	10%,	0.25	W
R_{16} = 7.5 kΩ,	10%,	0.25	W
R_{17} = 39 Ω,	10%,	0.25	W
R_{18} = 12 Ω,	10%,	0.25	W
R_{19} = 12 Ω,	10%,	0.25	W

* metal film resistor

Resistors (variable)

R_4 = 500 Ω, 10-turn helipot
R_{12} = 22 kΩ, potentiometer
R_{14} = 50 kΩ, potentiometer

Sensor

R_2 = 100 Ω at 0 °C; platinum resistance
thermometer, type TSL103

Transformers

T_1 = mains transformer, 220 V/24 V
T_2 = trigger transformer, TT60

An example of printed wiring board mounted modules built into a modular control system for 1.25 kW shunt motors.

Static regenerative, 4-quadrantal d.c. motor control system: 3-phase input; 80 kW, 400 V output. A full description is given in our Application Information No. 453 entitled "Modular Power Control, Full-Control Systems".

8.3 D.C. Motor Control with Current Limiting

In many control systems using thyristors the load current is subject to large fluctuations and, under certain circumstances, may rise to a value in excess of the circuit capability. This is particularly the case where a process is run-up from an initial condition far removed from the desired operating point, e.g., heating an oven from cold, starting a motor from rest. In these cases it is necessary to equip the system with a means of current limiting which enables the controlled region to be reached without running the risk of overloading circuit components at any time.

The block diagram in Fig. 8.4 shows a thyristor controlled d.c. motor; the system uses advanced and average current limiting techniques to contend with conditions of high current demand. These techniques are described briefly in the following text; a thorough explanation is given in our Application Information No. 449, Section 3.4.

Fig. 8.4. Block diagram of closed-loop control system for a d.c. motor.

8.3.1 Functional Description

The system (Fig. 8.5) has three separate feedback loops, two of which limit current flow through the thyristors when full power is demanded, and one to maintain stable conditions once the control region is reached. Only one loop is effective at any instant, and this is selected by the dual inverting amplifier 2IA60 which functions as a logical limiter. The output of the 2IA60 is fed to the PSM40 phase shift module which, in turn, controls the PA60 (connected as a multivibrator) and hence the phase angle of the thyristors. The action of this part of the system is exactly the same as that described in Section 8.2. Note that the reference and sensor voltages are of opposite polarity and are fed to the same input terminal.

106

When the set point is altered to accelerate the motor, V_{ref} is much larger than the tachometer output and the output from the DOA40(U_1) operational amplifier is sufficiently positive to reverse bias diode D_1. The least positive input to the logical limiter is the voltage supplied via feedback loop I; part of this voltage (ΔV) is determined by potentiometers R_X and R_Y (Fig. 8.5) and potential V_o, and is a constant value for a particular setting of the potentiometer. Hence the advance current limiting feedback voltage is $V_a + \Delta V$, where V_a is the armature voltage. As the motor accelerates the armature current increases from I_a to I_a' whilst the back e.m.f. of the armature remains instantaneously at the original value E. Hence we have,

$V_a + \Delta V = E + I_a' R_a$ (where R_a is armature resistance)

But for stable running conditions

$V_a = E + I_a R_a$;

substituting in the previous equation,

$E + I_a R_a + \Delta V = E + I_a' R_a$;

therefore:

$I_a' = I_a + \Delta V / R_a.$

However, because the feedback is positive, the armature current will increase at a rate determined by the feedback time constant (α). Taking this into account, the above formula becomes:

$$I_a' = I_a + \frac{\Delta V}{R_a}\left(1 + \frac{t}{\alpha}\right),$$

where t is the time after switching on.

Since the permitted value of I_a is dictated by the armature rating, the degree of overload current which can be tolerated is set by

$$\frac{\Delta V}{R_a}\left(1 + \frac{t}{\alpha}\right).$$

Note that when starting from rest, the values of I_a and t in the above equation are zero. Hence:

$$I_a' = \frac{\Delta V}{R_a}.$$

This means that the permissible starting current is equal to the amount by which I_a can be tolerably exceeded, but is less than the permissible peak armature (and thyristor) current.

Fig. 8.5. Circuit diagram of closed-loop control system for a d.c. motor.

The effect of the advance current limiting feedback loop (loop I) is to control the rate at which the armature current builds up, but it does not limit the final value of this current. The final value is controlled by the average current limiting feedback loop (loop II) which assumes control after the first few cycles of the applied supply. The changeover from loop I to loop II is assisted by the inclusion of a delay network in loop I, so that loop II takes effect when the armature current has increased to a value sufficient to produce a feedback voltage across R_s which, after amplification by the DOA40 (U_2), exceeds the sum of the zener voltages of D_2 and D_3; thereafter the voltage at terminal 14 of the 2IA60 is blocked.

8.3.2 CIRCUIT DESCRIPTION (Fig. 8.5)

The set point voltage is derived from a voltage regulator diode, resistor network connected across the —24 V supply and is fed to terminal 3 of the module U_1. This terminal also receives the fed back tachometer output (via loop III). Two RC filter networks suppress initial overshoot and ripple voltages.

The module 2IA60 is a dual inverting amplifier but is used in conjunction with the preceding diode as a logical limiter. Three inputs are fed to the module, at terminals 4 and 14, and the least positive of these is automatically selected; the input voltages are normally positive, but under certain circumstances they can have a negative polarity.

Module PSM40 converts the analogue input signal into mains synchronized output pulses, and amplifier PA60 produces 10 kHz trigger pulses which are fed to the thyristors via the TT60 trigger transformer. An RC network delays the application of the +24 V supply to this part of the circuit to ensure that the thyristors remain untriggered until the control circuits are stabilized.

Average current limiting feedback is fed via loop II and is tapped from a resistive network connected across R_5 which carries the motor armature current. Module U_2 amplifies the fed back voltage and when the amplifier output exceeds the zener voltages of D_2 and D_3 it is fed to the 2IA60 module. Diode D_4 provides protection against reverse polarity voltages.

The advance current limiting feedback voltage (via loop I) is determined by potentiometers R_x and R_y An RC time constant is introduced into the loop by C_1.

The motor is supplied from a single-phase mains source which is switched by S_1; transients are suppressed by the L and RC input networks.

Motors with a power rating of 1 to 5 h.p. can be controlled to within
0.5% of full speed, and a set current stability of better than 5%. For
motors rated above 5 h.p. it is recommended that a three-phase system
is used; this requires two more PSM40 modules and thyristor trigger units.
A detailed circuit is given in Application Information 449, Section 4.2.

8.4 Supply for Reversible Two-speed D.C. Motor

The circuit described below controls a d.c. motor in both directions at
two preset speeds. The phase and voltage components of a resolver signal
are used to operate the circuit. Changing from high to low speed occurs
when the resolver signal level drops below a certain value. At a still lower
signal level the motor is stopped, and on reversing the signal phase the

Fig. 8.6. Variation of motor speed and direction with control signal amplitude E. With
E "positive" or in phase with the synchronizing voltage V_{syn} (in anti-phase with V_{syn}'),
the motor will rotate in a certain direction, say clockwise. With E negative, the motor
will rotate counter-clockwise. Time relationships of E with V_{syn} and V_{syn}' are shown
under the graph. Motor direction can be reversed only if E is made less then $\pm$ 50 mV.

110

motor runs in the opposite direction. Two speeds are again available by increasing the signal level. Fig. 8.6 illustrates the way in which motor speed is controlled by resolver output.

The control unit consists basically of the following circuits; input amplifier, motor speed control, stop circuit, motor direction control and thyristor trigger circuit. With the aid of the block diagram (Fig. 8.7) and the circuit diagram (Fig. 8.8), the operation of these circuits is described below.

Fig. 8.7. Block diagram of supply for reversible two-speed d.c. motor.

8.4.1 Input Amplifier Circuits (modules U_1 and U_2)

The circuit input is provided by a resolver signal, variable in phase voltage level. As a reference, the resolver is connected to a 6.3 V 50-60 Hz supply. The negative halves only of the input sine-wave are fed to an operational amplifier DOA40 (U_1), the positive halves being short-circuited by a diode.

The DOA40 module inverts and amplifies the input signal, amplification being adjustable with R_6. The output of U_1 is fed to the positive input of a second DOA40 (U_2) which amplifies the signal about 10 times.

111

Fig. 8.8. Part (a)-logic.

112

Fig. 8.8.(b) Circuit diagram of the system. Part (a) is concerned with logic, and part (b) with the thyristor triggering. Note that a special printed wiring board (TTU) is available for mounting units U_8, U_9 and U_{10}. The supply for U_3, U_5, U_6 and U_7 is $+12$ V; U_1, U_2, and U_4 require $+12$ V and -12 V.

8.4.2 MOTOR SPEED CONTROL (MODULES U_3 AND U_4)

Signals from the output of U_1 are fed via a ripple filter to dual inverting amplifier 2IA60 (U_3) connected as a Schmitt-trigger. When the output of DOA40 (U_1) decreases below a certain level, the first stage of U_3 goes to the off state, resulting in a low-level voltage output. This low-level voltage is fed to the phase-shift circuit PSM40 (U_4) and triggers the motor-supply thyristors so that they conduct over a small angle. This gives a low average motor voltage and thus a low motor speed.

With a high-level resolver signal, the output of the 2IA60 (U_3) goes high triggering the thyristors via U_4 so that they conduct over a wide angle. This gives a high average motor voltage and thus a high motor speed.

High and low speeds are adjustable with potentiometers R_{30} and R_{31} respectively.

The PSM40 is synchronized with a symmetrical 24 V, 50 Hz reference signal. For 60 Hz mains supply, the 10 kΩ resistor between pins 1 and 4 should be replaced by a resistor of lower value.

113

8.4.3 Stop Circuit (module U_5)

The output of DOA40 (U_2) is fed to a second Schmitt-trigger circuit 21A60 (U_5) similar to module U_3. At a resolver signal level about 10 times lower than that necessary for switching U_3, the output of U_5 switches to zero, thus turning off the thyristor trigger circuit and stopping the motor.

8.4.4 Motor Direction Control (modules U_6, U_7 and U_8)

Signals from the output of U_2 are fed to a bi-stable multivibrator (flip-flop) formed by 2NOR60 (U_6). The half sine-wave output of U_2 is compared with the 24 V reference signal V_{ref} from the transformer T_1, and depending on the phase relationship with the resolver signal, the flip-flop switches to one of its positions. The input switching level is about a factor of 3 below the input switch-off level of U_5, protecting the motor against a direction reversal command at operating speed. The outputs of U_6 are connected to a second flip-flop U_7 (via an RC delay network). In this way the outputs of U_1 are delayed about 30 ms after the first flip-flop U_1 switches over.

The two pairs of outputs CCW', CCW (counter-clockwise) and CW', CW (clockwise) are each fed to one half of the 2NOR60 (U_8). The outputs 14 and 5 from either half can be high only when both input signals of a pair are low and the PSM40 (U_4) output to pins 7 and 16 of U_8 is high. Thus, depending on the phase of the resolver signal, one of the U_8 outputs goes high, triggering one of the thyristor pairs for the desired motor direction. Both outputs of U_8 are zero (and thus none of the thyristors are triggered) only for a low resolver signal or during a short delay time (30 ms) after switching over of U_6, when the output pairs from U_6 and U_7 are out of phase.

8.4.5 Thyristor Trigger Circuit (modules U_9 and U_{10})

Outputs 14 and 5 of U_8 are connected to the self-oscillating trigger circuits U_9 and U_{10}. When the input signal to pin 2 is high, feedback from pin 2 via a diode causes the PA60 to oscillate at a frequency of about 10 kHz. The output pin 13 is connected via a series resistance of 39 Ω to a trigger transformer type TT60 giving two output trigger signals. A diode and voltage regulator diode are connected between pin 13 and the 24 V supply to suppress transformer switch-off transients.

114

Thyristors TH_1 and TH_2 are triggered by unit PA60 (U_9) and thyristors TH_3 and TH_4 by unit PA60 (U_{10}) to give positive and negative motor supply respectively.

Fig. 8.9. A simple arrangement for circuit and motor supplies

8.5. Illustrated Power Control systems.

The power control systems shown in the following illustrations use standard printed wiring boards and modules. Details of any system, or printed wiring board used therein, are given in our Application Information books relating to Modular Power Control, Half and Full Control Systems (Nos. 449 and 453 resp.)

Fig. 8.10. Single-phase, open-loop, half control system using a phase shift trigger and supply unit (PSU). One module, a PSM40, from the 40-Series is used.

115

Fig. 8.11. Three-phase, open-loop, half control system using a phase shift trigger and supply unit (PSU). One module, a PSM40, from the 40-Series is used.

Fig. 8.12. Single-phase, closed-loop, half control system using a supply and current measuring unit (SCU), and a phase shift trigger and control unit (PCU). One PSM40 and two DOA40 modules are used.

117

Fig. 8.13. Three-phase, closed-loop, half control system using a supply and current measuring unit (SCU), a phase shift and control unit (PCU), and a twin-phase shift trigger unit (TPU). Windings a_1/a_2, b_1/b_2, c_1/c_2 are trigger transformers: diodes that are connected in antiparallel with the thyristors are not shown. Three PSM40 modules and two DOA40 modules are used.

Supply and
voltage sta-
bilization unit
(SU)

| three—phase bridge rectifier assembly (I) | M — T | three—phase bridge rectifier assembly (II) |

Fig. 8.14. Three-phase, closed-loop, full control system. Full control is achieved using a double bridge configuration; one bridge controls forward rotation and regenerative braking of reverse rotation, while the second bridge controls reverse rotation and regenerative braking of forward rotation.
Close speed control is effected using advance and average current limiting techniques. The system uses six types of unit: the illustration shows one of the three pairs of PTU and TTU units necessary for a three-phase system.

119

9 Digital-to-Analogue/Analogue-to-Digital Conversion

9.1 Introduction

Information relating to the measurement or control of a process may be presented electrically in either digital or analogue form, the choice being determined largely by the nature of the process. However, the form dictated by the process is often at variance with that most suitable for application to associated control or measuring equipment and, therefore, it is both desirable and economic to translate from one form to the other. The relative simplicity and economy with which the following analogue-to-digital and digital-to-analogue converters can be built is largely attributable to the use of DOA40 and DZD40 modules in conjunction with 10-series circuit blocks.

9.2 Simple Analogue-to-Digital Converter

The analogue-to-digital converter described here was developed primarily for driving stepping motors, and ensures a gradual approach to the final (zero) position of a motor. However, the simplicity of design makes the converter suitable for a very wide range of applications.

The block diagram of the converter is shown in Fig. 9.1. A gate input allows the pulse generator to produce a negative-going pulse whenever the integrator output voltage rises above a certain level. Thus, when a negative analogue signal is applied at the integrator input, a steadily increasing level is produced which, when it exceeds the gate threshold, triggers the pulse generator. An output pulse is thus produced and the lagging (positive-going) edge of this pulse is fed back to the integrator input, reducing the integrator output below the gate threshold voltage and cutting off the gate. The magnitude of the analogue input voltage thus determines frequency of the output pulses and analogue-to-digital conversion is achieved.

Fig. 9.1. System block diagram.

A detailed circuit diagram is given in Fig. 9.2 and is supplemented by waveform diagrams in Fig. 9.3. A negative analogue voltage, V_{in}, is applied to the input. The DOA40 output rises linearly at a rate proportional to the magnitude of V_{in}, until it reaches the gate threshold; V_{out} then drops to zero and no further current flows through R_{16} and R_{17}. Capacitor C_5 discharges, keeping V_{out} low for a short period, but when this discharge is no longer effective V_{out} returns to a positive value — thus

Fig. 9.2. Circuit diagram.

Fig. 9.3. Analogue-to-digital conversion waveforms. 1) Width determined by C_5, 2) Width determined by V_{in}.

121

a negative pulse is generated of duration dependent on the value of C_5. The lagging edge of this negative pulse is fed back through TR_1 to the input of the DOA40, reducing the output of the DOA40 to zero. The DOA40 once again starts to integrate V_{in} and the cycle is repeated. Hence, whilst the negative pulses are of fixed width, the frequency of the pulses is a function of the input signal magnitude.

Figure 9.4 shows how the transfer function of the converter can be varied horizontally by V_r and how steepness of transfer function can be varied by choice of C_2. It can also be seen that the maximum frequency is reduced as C_5 is increased (as a wide pulse cannot occur as frequently as a narrow one).

An extra input has been provide at the gate circuit and, by means of this input, the pulse generator can be controlled externally.

Fig. 9.4. Transfer characteristic of system.

9.3 Digital-to-Analogue Converter

This general purpose digital-to-analogue converter uses a diode-gated resistance ladder network in conjunction with a DOA40 operational amplifier to convert a digital input into an analogue output voltage. The output voltage range is from 0 to —9.9 V, and the intrinsic error is less then 0.25% of full scale.

The information to be translated into an analogue value is presented in parallel output, binary coded decimal form as derived, for example, from the FF12 blocks (flip-flops) of a DCA10-B circuit board. Other digital codes could, of course, also be dealt with by suitably modifying the ladder network described.

122

Fig. 9.5. Ladder component.

The operation of the ladder network (Fig. 9.6) can best be understood by first considering just one of its component members, as illustrated in Fig. 9.5. In the arrangement shown V_n and V_r are maintained at constant potentials of $+18$ V and $+12$ V respectively, and V_f at $+2$ V. The digital information is fed in via terminal A, which may be at either 0 V, representing binary digit 0, or $+12$ V representing binary digit 1. The information output is the current I, which may be either zero or a finite value proportional to the resistance R, depending on the signal present at terminal A.

The voltage across the resistance R can be calculated from the equation:

$$V_r + V_{D1} - V_R - V_{D2} - V_f = 0,$$

giving:

$$V_R = V_r - V_f + (V_{D1} - V_{D2}).$$

If care is taken to ensure that V_{D1} and V_{D2} are equal (preferably within 5 mV), then

$$V_R = V_r - V_f = 12 - 2 = 10 \text{ V},$$

and the current I is:

$$I = V_R/R = 10/R.$$

This current flows to terminal X, however, only if a 1 signal ($+12$ V) is presented at A; if a zero signal (0 V) is presented, the current is diverted via D_3 and does not appear at terminal X. The function performed by the circuit of Fig. 9.5 can thus be expressed:

if A is 1: $I = 10/R$,
if A is 0: $I = 0$.

A number of such circuits can be connected in parallel to form a ladder network for translating a signal encoded in a corresponding number of parallel binary digits. If the resistors are graded in binary progression, as in the ladder network of Fig. 9.6, the total output current is then an analogue of the quantity represented by the binary input signal. Thus the output current can be expressed by the equation:

$$I = (V_r - V_f)\,(A/R + 2B/R + 4C/R + 8D/R)$$

$$= (10/R)\,(A + 2B + 4C + 8D),$$

in which A, B, C and D are the parallel binary input digits and may be either 0 or 1. For an ordinary 8-4-2-1 binary coded decimal input, therefore, the analogue output current of the circuit of Fig. 9.6 is as given in the table below.

Fig. 9.6. *Diode-gated resistance ladder network.*

| binary output | | | | | analogue output |
A	B	C	D		
0	0	0	0	$I = (10/R)\,(0)$	$= 0$
1	0	0	0	$I = (10/R)\,(1)$	$= 10/R$
0	1	0	0	$I = (10/R)\,(2)$	$= 20/R$
1	1	0	0	$I = (10/R)\,(1 + 2)$	$= 30/R$
0	0	1	0	$I = (10/R)\,(4)$	$= 40/R$
1	0	1	0	$I = (10/R)\,(1 + 4)$	$= 50/R$
0	1	1	0	$I = (10/R)\,(2 + 4)$	$= 60/R$
1	1	1	0	$I = (10/R)\,(1 + 2 + 4)$	$= 70/R$
0	0	0	1	$I = (10/R)\,(8)$	$= 80/R$
1	0	0	1	$I = (10/R)\,(1 + 8)$	$= 90/R$
0	0	0	0	$I = (10/R)\,(0)$	$= 0$

The ladder network translates only the units decade; a similar network for the tens decade can be constructed using resistances equal to $R/10$, $R/20$, $R/40$ and $R/80$. The current output of both decades will then be:

$$I = (10/R)\,(A + 2B + 4C + 8D + 10E + 20F + 40G + 80H),$$

and if R is given a value of 100 kΩ the current will vary in increments of 0.1 mA ($= 10$ V/100 kΩ) between 0 and 9.9 mA.

Fig. 9.7. Analogue current-to-voltage converter.

A more useful analogue can be provided by converting the current into a corresponding voltage. The conversion is carried out by means of the circuit of Fig. 9.7, in which the balanced input operational amplifier shown is a DOA40 circuit block with transistor TR added to obtain an output current in excess of 10 mA. The open-loop gain of the DOA40 is high ($\simeq 10^5$), so when feedback is applied the closed-loop gain is determined solely by the ratio of the input and feedback network impedances. No current flows into or out of the input terminals 1 and 3; therefore, $I_1 = I_o$ and $I_2 = I_3$ and the potential V_f of both terminals is determined by the network R_2, R_3;

$$V_f = V_r R_3/(R_2 + R_3) = 2 \text{ V}.$$

Moreover,

$$I_1 = (V_r - V_f)/R_1' = (V_f - V_o)/R_o,$$

in which R_1' is the resistance due to R_1 in parallel with those resistors of the ladder network through which the current I is flowing.

125

From this it is apparent that the value of the output voltage V_o can be expressed:

$$V_o = V_f - I_1 R_o,$$

in which $I_1 = I + I_{R1}$; therefore;

$$V_o = V_f - IR_o - I_{R1}R_o.$$

Also, from the known voltage drop across R_1, the value of I_{R1} can be found to be:

$$I_{R1} = (V_r - V_f)/R_1 = (12 - 2)/5 \times 10^3 = 2 \text{ mA}.$$

Therefore, since R_o is 1 kΩ:

$$V_o = 2 - IR_o - (2 \times 10^{-3})(1 \times 10^3) = -IR_o.$$

Thus, since I varies between 0 and 9.9 mA in increments of 0.1 mA, V_o varies between 0 and -9.9 V in corresponding increments of 100 mV. The circuit diagram of a complete, two-decade converter is given in Fig. 9.8.

Fig. 9.8. Two-decade, digital-to-analogue converter.

9.4 Analogue-to-Digital Converter

The digital-to-analogue converter described in Section 9.3 can also be adapted to the opposite purpose: to translate an analogue voltage into a corresponding digital signal. To do this, it is operated in conjunction

126

with a pulse generator, a digital counter and a voltage comparator to carry out the following sequence:

(1) With the analogue voltage V_x presented to one pair of input terminals of the DZD40 comparator, the conversion cycle is started by triggering the pulse generator (PS10) via FF10, the output of which starts the counter.

(2) The coded output of the counter (a running indication of the number of pulses originated by the pulse generator) is translated by the digital-to-analogue converter into a corresponding series of stepwise changes in voltage (V_o) for presentation to the second pair of comparator input terminals.

(3) When the voltages at both pairs of comparator input terminals coincide, the comparator inhibits the pulse generator, thereby stopping the counter at a digital count corresponding to the analogue value of the comparator input voltages. The output of the counter is then available for use whenever a digital representation of the voltage may be required.

The circuit arrangement for carrying out this sequence is shown in Fig. 9.9, in which the logic functions are carried out by 10-Series circuit blocks.

Fig. 9.9 Analogue-to-digital converter.

The comparator is a DZD40 zero detector, a two-stage differential amplifier followed by a current mode OR-gate and an inverting amplifier. In response to a null voltage at the input it originates a negative-going 12 V output step.

The comparator output step changes the state of an FF10 bistable multivibrator which in turn governs the operation of the pulse generator (a PS10 pulse shaper externally reconnected as a free-running relaxation oscillator). Thereafter no further pulses are delivered to the counter, so the digital count registered at that instant remains available until a new conversion cycle is started.

To restart the cycle a pulse is applied to the second input terminal of the FF10 bistable multivibrator, restoring it to its initial condition. The positive-going voltage at one output terminal then restores the PS10 pulse generator to operation, and the negative-going voltage from the other, reshaped by a PS10 pulse shaper, clears and resets the digital counter.

The critical element for carrying out the conversion is the comparator, in which the analogue voltage is compared with a stepwise declining voltage to detect a null; a simplified diagram of the circuit arrangement used is shown in Fig. 9.10. The analogue voltage V_x is taken to be positive, and the stepped reference voltage V_o negative, with respect to earth. A null therefore occurs at point A when $V_o = -\alpha V_x$, in which the factor α is the ratio of the two resistors R_1 and R_2.

The sensitivity of the DZD40 is such that it provides an output indication (a negative-going step from $+12$ V to 0 V) when the potential at point A is within 3 mV of zero. If R_1 and R_2 are equal, therefore, α is unity and the output voltage V_{out} will drop to zero only when the absolute values of V_o and V_x are within 3 mV of each other.

So as not to exceed the maximum common mode voltage or the maximum differential input voltage of the DZD40, the two OA200 diodes

Fig. 9.10. Comparator.

shown at input terminal 12 in Fig. 9.10 are actually connected in anti-parallel across both input terminals, as shown in Fig. 9.9.

The minimum input impedance of the comparator, as seen by the digital-to-analogue converter, is:

$$Z_{i\ min} = R_1 + R_2//R_{i\ min},$$

in which R_1 and R_2 are both 100 kΩ, and $R_{i\ min}$, the minimum input impedance of the DZD40, is 50 kΩ; therefore,

$$Z_{i\ min} = 133\ k\Omega.$$

9.5 Accuracy and Inherent Errors

Since it is common to both of the circuit arrangements described in Sections 9.3 and 9.4, it is appropriate to consider the accuracy of the analogue-to-digital converter first. The potential sources of error are the ladder network, the current-to-voltage conversion circuit, and the reference voltage V_r.

In each branch of the ladder network the critical components are the numerically graduated resistor R and the diodes, particularly D_1 and D_2 (see Fig. 9.5).

The resistors used are of the metal film type with a tolerance of 0.1% and a temperature coefficient of 25×10^{-6}/deg.C. The diodes D_1 and D_2 are matched with respect to forward voltage drop and in each branch of the network the value of R_h is selected so that the difference between V_{D1} and V_{D2} does not exceed 5 mV.

Any spread in the values of the graduated resistors of the ladder network will be reflected in the total current I delivered to the current-to-voltage converter, the effect being worst when all resistors are at the same extreme of their tolerance limits and the count presented to the network is highest (that is, 99 in a two-decade counter). In that case, the discrepancy in the current due to the resistor tolerances will be:

$$\Delta I_R = 0.001\ (I_{max}) = 9.9\ \mu A.$$

Similarly, spreads in the diode voltages within the 5 mV tolerance will also account for a change in the current, this effect too being worst when

all deviations are at the limit and the count is highest; then the discrepancy will be:

$$\Delta I_D = \Delta V_D (10/R + 80/R + 1/R + 8/R) = 5 \times 10^{-3}(99/10^5) = 4.95 \ \mu A.$$

The maximum possible deviation of the ladder current due to resistor and diode voltage tolerances is therefore:

$$\Delta I = \Delta I_R + \Delta I_D = 9.9 + 4.95 = 14.85 \ \mu A.$$

The effect of this deviation on the output of the current-to-voltage converter can be determined from the relation $V_o = V_f - I_o R_o$ (see Fig. 9.7). If only small changes are to be dealt with, the following expression is valid:

$$\Delta V_o = \Delta V_f - \Delta I_o (R_o + \Delta R_o),$$

in which $\Delta I_o = \Delta I + \Delta I_1$. Disregarding possible variations in V_r for the time being, ΔI_1 depends on the tolerance applicable to R_1. As in the case of the ladder resistors, this is 0.1%; so, since $I_1 = 2$ mA, $\Delta I_1 = 0.001 \ (2) = 2 \ \mu A$. The total variation in I_o is therefore: $4I_o = 14.85 + 2 = 16.85 \ \mu A \approx 17 \ \mu A$.

Since $V_f = V_r R_3/(R_2 + R_3)$ the variation due to resistor tolerance is:

$$\Delta V_f = V_r \left\{ \frac{R_3 + \Delta R_3}{R_2 + \Delta R_2 + R_3 + \Delta R_3} - \frac{R_3}{R_2 + R_3} \right\}$$

in which the worst combination of conditions occurs when ΔR_3 is positive and ΔR_2 negative, giving:

$$\Delta V_f = 3.4 \ \text{mV}.$$

The maximum possible change in output voltage due to spreads in I_o and V_f is therefore:

$$\Delta V_o = \Delta I_o (R_o + \Delta R_o) + \Delta V_f$$
$$= 17 \times 10^{-6} (10^3 + 1) + 3.4 \times 10^{-3} = 20.4 \ \text{mV}.$$

This value pertains to a two-decade converter registering its maximum output voltage (that is, 9.9 V, corresponding to a numerical input of 99). Expressed in per cent the error is thus:

$$\Delta V_o/V_o = (20.4 \times 10^{-3}/9.9)100 \approx 0.2\%,$$

in which the effect of variation in the reference voltage V_r is not taken into account. If it is desired to keep the total error within 1%, for example, the tolerance on V_r must not exceed 0.8%.

130

By way of comparison, it is of interest to consider the results of a similar error analysis applied to a converter operating in conjunction with a three-instead of a two-decade input signal source. The maximum output voltage will be taken to be 9.9 V, as before, but to accommodate the additional decade a minimum voltage of 10 mV instead of 100 mV, will be used. In that case, the maximum ladder current error due to the resistor and diode voltage tolerances is:

$$\Delta I = 14.85 + 0.9 + 0.9 = 16.65 \ \mu A,$$

and the resulting variation in I_o is:

$$\Delta I_o = 16.65 + 2 = 18.65 \ \mu A.$$

The spread in V_f is unaffected by the addition of a decade, so the new output voltage error due to component tolerances becomes:

$$\Delta V_o = 18.65 + 3.4 \approx 22 \ \text{mV}$$

or, expressed in per cent:

$$\Delta V_o/V_o = 0.22\%.$$

Some saving can be made in component costs, without greatly sacrificing accuracy, by using resistors with a 5% instead of a 0.1% tolerance in the units part of the latter network. In a three-decade network, the possible error in the current I is then:

$$\Delta I = 14.85 + 4.5 + 0.9 = 20.25 \ \mu A,$$

and the resulting output voltage error is:

$$\Delta V_o = 20.25 + 3.4 = 23.65 \ \text{mV}.$$

The error of the analogue-to-digital converter depends not only on that of the digital-to-analogue converter, but also on that of the comparator; the total error can be found by adding the errors due to both elements.

To minimize the effect of noise and interference the differential sensitivity of the DZD40 can be adjusted to 3 mV; since the full scale input voltage to the comparator is 9.9 V, the resulting error is: $\Delta V_i/V_i = (0.003/9.9) \ 100 = 0.03\%$.

To this must be added the potential error $\Delta(R_1/R_2)$ due to the tolerances of the two resistors comprising the input network:

$$\Delta\left(\frac{R_1}{R_2}\right) = \left\{\frac{R_1}{R_2} - \frac{R_1 + \Delta R_1}{R_2 + \Delta R_2}\right\} 100\%,$$

in which, for the circuit under consideration $R_1 = R_2$. Assuming that metal film resistors with a tolerance of 0.1 % are used, one being at the upper and the other at the lower limit of tolerance, this gives:

$$\Delta\left(\frac{R_1}{R_2}\right) = \left\{1 - \frac{R + \Delta R}{R - \Delta R}\right\} 100 = 0.2\%.$$

The total comparator error is therefore:

$$\Delta V_i / V_i + \Delta(R_1/R_2) = 0.23\%.$$

Combined with the previously calculated error of the two-decade digital-to-analogue converter, the maximum potential error of the analogue-to-digital converter is thus:

$$\Delta V_o / V + \Delta V_i / V_i + \Delta(R_1/R_2) = 0.22 + 0.03 + 0.20 = 0.45\%.$$

The foregoing calculations are based on an assumed ambient temperature of 25 °C. Taking the temperature coefficients of the resistors and diodes into consideration, it can be shown by similar means that for operation over a temperature range from 0 °C to 50 °C, the maximum error of the digital-to-analogue converter increases to 0.34%, and of the analogue-to-digital converter to 0.66%. The influence of possible variations in the reference voltage V_r has not been taken into account.

10 Miscellaneous Applications using DOA and DZD Modules

10.1 Control Circuit for Motor Speed Equalization

The circuit (Fig. 10.1 a & b) is intended to equalize the rotational speed of two motors, and allows very fast speed equalization without overshoot. This is achieved by using two speed bands, both being adjustable for slope and turn-over point. The circuitry from the VSO's to the inputs of DOA40 modules U_5 and U_6 is designed to provide an accurate measurement of motor speed over a wide range.

Information concerning the speed of the motors is obtained using VSO's. When the vane mounted on the shaft of the motor bridges the gap of its VSO, a pulse is fed to the NOR unit. In the case recommended for low speeds, where a disc on the shaft is used, two NOR units in

all diodes type BAX13

Fig. 10.1(a). Tachometer circuit

Fig. 10.1(b). Level detection circuit.

series must replace the single NOR unit between the VSO and the memory (2 NOR units B and C) in order to give a pulse of the correct polarity. When the output of the VSO goes LOW, the output of NOR(C) goes HIGH causing the output of U_1 to increase linearly from a negative value. When this voltage has risen to a certain level it resets the memory. Potentiometers R_1 and R_2 are used to adjust the pulse widths of the outputs of U_1 and U_2 to equal values. The output signal is fed to U_3 which is connected as an active low-pass filter, and the resulting final output is a d.c. voltage proportional to the speed of the motor.

The outputs of U_3 and U_4 are connected in parallel to two DOA40 modules U_5 and U_6 connected as differential amplifiers, having a gain of 50 and 10 respectively. Two level detectors with adjustable trip level (to $\pm$ 5 V) are connected to the output of each differential amplifier, one trip level being negative while the other is positive. The output levels of the detectors provide information, detailed below, concerning the speed of the motors.

– If the speed of both motors is approximately equal all outputs are low (zero volts).

– If the speed of motor M_1 is higher than that of motor M_2, A is high and A_1 zero. For M_2 higher than M_1, A_1 is high and A is zero.

– If the difference in the motor speeds is within certain limits (covered by outputs A and A_1), the outputs B and B_1 are zero. However, exceeding these limits results in a high level at B_1 and zero at B (or vice versa) depending on whether M_1 is slower or faster than M_2 (or vice versa).

The levels A, A_1, B and B_1 are used to drive the logic system shown in Fig. 10.2. While the difference in speed between M_1 and M_2 remains high the output of U_{16} is high, making the output of U_{18} low. Thus the output of U_{23} or U_{24} is high, depending on whether A or A_1 is high. In this way information is supplied to speed up or slow down the appropriate motor.

Fig. 10.2. Logic circuit.

135

If the motor speeds have approached each other within a certain value, the output of U_{16} becomes low. This sets free the operation of the pulse generator (consisting of the units U_{17}, U_{18}, U_{19}, U_{20}, U_{25}, U_{26}) making the output of U_{18} alternatively high and low. The high and low durations at this output depend on the delay time of U_{26} and U_{25} respectively. Thus the motor synchronizing power is applied in two steps, the second adjustable, in order to prevent overshoot.

As soon as the speeds are approximately equal, A_2 and A_1 become zero, making the outputs of U_{23} and U_{24} zero via U_{11} and thus removing synchronizing power to the motors.

As mentioned above, the two proportional bands are adjustable for slope and turn-over point, the latter by means of the 10 kΩ potentiometer in the level detectors and the former by changing the gain of the DOA40 modules U_5 and U_6. Thus the difference in motor speeds at which the steps take place may be adjusted. Fig. 10.3 shows the relationship of the differential amplifier outputs to motor speed, points A, A_1, B, B_1 being the turn-over levels of the corresponding outputs. The sections over which a step takes place are shown as heavy lines. A graph of equalizing power vs. motor speed is given in Fig. 10.4, points 1, 2, 3 and 4 on both graphs being the speeds at which a step change occurs.

10.2 General Two-way Process Control System

The circuit shown in Fig. 10.5 depicts a simple method of obtaining two-way process control (i.e. positive or negative action) suitable for many industrial applications. Although the scheme described here is intended for use as an automatic *pH* (ionization level) control equipment, the circuit is obviously easily adaptable to any other testing process requiring positive and negative control. Only a few components are needed, and the low cost of the system should give it a wide field of application.

A voltage corresponding to the *pH*-level of the substance under test is amplified 100 times by the DOA40. A reference voltage pH_{ref}, which will normally be of the same order of magnitude, is compared with this amplified test voltage pH_x, and if the difference at terminals 3 and 1 of the DZD40 is greater than the preset tolerance a LOW level will appear at 7 or 14. Thus the appropriate burette tap is opened by its RD10/ 2.G110/FF12 circuit. If the pH_x and pH_{ref} are within 1 mV, DZD40 output 8 will be LOW, so inhibiting the 2.G110 and keeping both burette taps closed.

Fig. 10.3. Output voltage of differential amplifiers U_7, U_8, U_9, U_{10} plotted against relative motor speed.

Fig. 10.4. Equalizing power plotted against relative motor speed.

Fig. 10.5. pH-level control circuit.

137

The pH measuring indicator is a 50 mV, 50 Ω milliammeter. The signal is amplified 100 times by the DOA40 connected as a stable amplifier, and appears at input 3 of the DZD40 across the potential divider R_1 R_2.

Reference pH is obtained with the aid of a 2N930 transistor acting as a current generator, which develops a voltage across the potential divider R_3 R_4. Resistors R_5, R_6 provide coarse and fine control, so that the pH reference level, read on the milliammeter (same type as pH measuring instrument) can be set at any value. A reference voltage thus appears at 1 of the DZD40. The two input terminals of the DZD40 are bridged by diodes to bypass excessive input voltage swings.

Polarity detection is possible with the DZD40; 7 LOW indicates more base should be added, 14 LOW indicates that extra acid is required. In addition, a positive indication that neither base nor acid is required is provided by 8 being LOW. If this happens, FF10a output 6 turns LOW, so holding both 2.G110 outputs at HIGH. The FF10 output may also be used to drive an RD10/lamp circuit indicating when the pH level is correct.

Before this state is reached, one DZD40 input will usually be more than 1 mV higher than the other. If 1 is higher, 7 and 8 will be HIGH and 14 LOW. Thus FF12 output 6 will be HIGH on application of a negative-going trigger pulse at 7, and 2.G110 output 16 LOW; the RD10 will conduct causing some acid to be added to the substance under test. The trigger pulses may originate from a manually-controlled push-button (in which case contact bounce elimination must be done via FF10b). This is the "start" push-button in the diagram.

The pH of the substance requires a certain interval to attain its final value after adding some base or acid. Thus the rate at which acid or base is added must be restricted, so that the pH of the substance at the instant 8 becomes LOW is within required limits.

10.3 Fluxmeter with Digital Read-out

A magnetic flux Φ that induces a potential e across a moving coil of N turns can be expressed by the integral:

$$\Phi = (1/N) \int e \, dt.$$

The fluxmeter described evaluates this integral and presents the result in digital form.

Compared with other flux measuring instruments in which a ballistic

counteract any deviation of the output voltage from zero. In fact, therefore, the DOA40 operates as a null-seeking sum and difference integrator. Counting the number of pulses applied to one of the terminals as positive and of those applied to the other as negative, their algebraic sum is proportional to the integral $(1/N) \int e \, dt$ and, hence, to the measured flux Φ.

To derive the required pulses, the output of the DOA40 is applied to the DZD40 zero detector which, in turn, furnishes gating signals for the two OS11 multivibrators via a pair of GI10 gate inverters. The multivibrators are synchronously triggered by a PS10 pulse shaper connected to operate as a free-running relaxation oscillator.

In response to any deviation of the integrator output potential by 1 mV or more, and depending on the polarity of such deviation, a potential of 12 V appears at one output terminal of the DZD40, and of 0 V at the other. Owing to the intervention of the gate inverters, the multivibrator governed by the terminal which is at 12 V is inhibited. As a result, pulses are delivered only to that terminal of the DOA40 at which their effect is to counteract the original deviation.

For example, if the output of the integrator is more than 1 mV *above* zero, a potential of 12 V appears at terminal 7 of the DZD40, and of 0 V at terminal 14. The gate inverter connected to the latter thereupon gates the multivibrator connected to the negative input (terminal 3) of the DOA40, causing the output of the integrating network to *fall* until it is again within 1 mV of zero. Conversely, if the output of the integrator *falls* more than 1 mV below zero, the multivibrator that is governed by terminal 7 of the DZD40 is gated, applying pulses to the positive input of the DOA40 (terminal 1) and causing the output to *rise* until it is within the 1 mV margin. (When the output of the integrator is between $+1$ mV and -1 mV, the differential sensitivity limits of the DZD40, terminals 7 and 14 are both at 12 V, so in that event both multivibrators are inhibited and no corrective pulses are applied to the integrator.)

It is important that the pulses applied to both input terminals of the DOA40 have equal and opposite effects on its output. To compensate for tolerances in the two integrating networks and the two multivibrators, therefore, one of the latter is provided with a variable trimming resistor.

By adjusting the resistance the duration of the respective multivibrator pulses can be varied until the desired equality is obtained.

Pulses for application to the input terminals of the DOA40 are taken from the Q_2 output terminals of the multivibrators; digital read-out is obtained by applying the conjugate pulses from the Q_1 terminals, to-

galvanometer is used, its accuracy is less dependent on the speed of the measuring coil relative to the field and there is less likelihood that the output indication will overrun the limit of the read-out scale. Moreover, the output persists after relative movement has ceased and is available in a form that is directly usable for control purposes. Provided the measuring coil and integrating network are suitably dimensioned, a field of any strength can be measured.

As shown in Fig. 10.6, the instrument employs a DOA40 operational amplifier, a DZD40 zero detector, and supplementary circuit blocks of the 10-series; namely, two OS11 monostable multivibrators, two G110 gate inverters, and a PS10 pulse shaper.

The DOA40 is connected as an integrator with the measuring coil L across input terminals 1 and 3. If the potential e induced in the coil by the field to be measured were the only input to these terminals, the output voltage would then be proportional to the desired integral, $(1/N) \int e \, dt$ and could be indicated or recorded with standard instruments. For many purposes, however, a digital read-out is more desirable, and in the circuit shown this is provided with the aid of a feedback loop which can supply uniform pulses either to terminal 1 or terminal 3 in such a way as to

Fig. 10.6. Fluxmeter with digital readout. (The OS10 blocks have been superseded by OS11 type blocks; connections remain as shown.)

139

gether with the output potentials of the two gate inverters, to a pulse counter. A circuit built up of DCA10 panels equipped with ZM1020 numerical indicator tubes and, preferably, arranged as a non-complementary counter with plus and minus indications is suitable.

An advantage of nulling the output of the integrator is that it remains within 1 mV of zero, whether or not a measurement is in progress. Thus the integrator output does not reflect the influence of drift in the operational amplifier (DOA40). This influence does show up, of course, in the output indication of the pulse counter, which must therefore be reset before a measurement is taken.

In the circuit arrangement shown in Fig. 10.6 a measuring coil comprising 330 turns and having an internal resistance of about 10 kΩ is used.

10.4 Electronic Potentiometer

For control purposes it is often necessary to provide a voltage that can be regulated by either an analogue or a digital information signal. A useful low-impedance source for such a voltage can be made using the DOA40 operational amplifier and circuit blocks of the 10-series.

If the available input signal is digital (comprising, for instance, two parallel trains of information pulses), it can be applied to the balanced input terminals of the DOA40 via two OS11 monostable multivibrators. If it is analogue (for instance, a voltage derived from a high impedance source), a DZD40 zero detector and a source of triggering or synchronizing pulses are also needed. The circuit arrangement for digital control is shown in Fig. 10.7, and for analogue control in Fig. 10.8.

Referring first to the arrangement of Fig. 10.7, the DOA40 is externally connected, by means of resistors R_1 and capacitors C_1, as a difference amplifier and integrator. That is, to provide an output voltage V_o proportional to the difference between the signals V_1 and V_3 applied to its two input terminals:

$$V_o = 1/(R_1 C_1) \int_0^t (V_1 - V_3) \, dt.$$

If V_1 and V_3 are pulses of uniform shape (amplitude and duration), then the voltage V_o will be directly proportional to the difference between the number of V_1 and V_3 pulses. Not only that, but its value will persist even

Fig. 10.7. Digital circuit.

Fig. 10.8. Analogue circuit.

142

when no further pulses are delivered. Besides subtracting and integrating, therefore, the DOA40 also fulfils a memory function.

To ensure complete uniformity of the V_1 and V_3 pulses, they are derived from two OS11 monostable multivibrators which are themselves triggered by incoming information pulses applied to the 7 input terminals. (The gate input terminals are not used and are allowed to float.) In the circuit drawing, the pulse input to one multivibrator is designated V_7, and to the other V_7'; pulses applied to the V_7 input cause an increase, and those applied to the V_7' input a decrease, in the output voltage V_o of the DOA40.

The capacitor C_2 connected between the 11 and 17 terminals of each multivibrator determines the length of the output pulses. The higher the capacitance, the longer the output pulse and the greater the corresponding change in V_o. Conversely, the greater the feedback capacitance C_1 associated with the DOA40, the smaller the corresponding change in V_o. The unit increment of output voltage, ΔV_o, is in fact proportional to $2t/R_1C_2$, in which t is the duration of the multivibrator output pulse. The variable resistor R_3 connected to terminal 11 of one of the multivibrators makes it possible to equalise the unit increments of the multivibrators.

For analogue control (Fig. 10.8) the gate input terminals 3 and 4 of the multivibrators are connected to the outputs 7 and 14 of a DZD40 zero detector and the trigger input terminals are connected to a common clock-pulse generator, as shown in Fig. 10.8. Both multivibrators are therefore synchronously driven by the clock-pulse generator, and each is either gated or inhibited according to the output condition of the zero detector. The latter is in turn governed by the relative values of two input terminal potentials, V_{w1} and V_{w2}, either or both of which may reflect a measured variable (i.e., one may be a fixed reference potential). According to the relation between these values, 7 may be at $+12$ V and 14 at 0 V, in which case the right-hand multivibrator is gated, and the left-hand one inhibited; or 7 may be at 0 and 14 at 12 V, in which case the left-hand multivibrator is gated and the right-hand one inhibited.

The differential sensitivity of the DZD40 is 1 mV after balancing (see Section 11.3 – Minimum offset voltage), so if $(V_{w1} - V_{w2}) > 1$ mV, terminal 7 is at 0 V and 14 at 12 V. This means that the right-hand multivibrator (feeding input 1 of the DOA40) is inhibited and the left-hand one (feeding input 3) gated. Therefore, as long as $(V_{w1} - V_{w2})$ remains greater than 1 mV the output voltage V_o of the DOA40 will rise at a rate depend-

143

ing on the values of C_1 and C_2 and the frequency of the clock-pulse generator. Conversely, if $(V_{w2} - V_{w1}) > 1$ mV the condition of the two multivibrators is reversed and the output voltage V_o will fall.

The synchronizing clock-pulses may be supplied from an external source, or from a clock-pulse generator built in to the system. For this purpose a PS10 pulse shaper externally connected as a free-running oscillator is satisfactory. A digital indication of the output voltage V_o can be obtained by connecting a reversible pulse counter to terminals 6 of the two OS11 multivibrators.

In either the digital or the analogue mode of operation, the output voltage can be returned to zero by means of the reset switch S shunting the capacitors C_1.

10.5 Hold (Temporary store) Circuit

The duration or intensity of an operation on a product is often required to be dependent on the value of a property inherent in the product. Usually, however, only a limited time is available to measure the magnitude of the property, after which the information obtained must be stored during the complete operation cycle. If the information can be produced in the form of an electrical signal, the circuit described offers a simple solution to the above problem.

Referring to Fig. 10.9, the signal V_i is applied to the input terminal while the switch S (e.g. a relay) is in position 1. The output voltage V_o is $-V_i$. After a time sufficient to charge the R_2-C_1 network, the switch S is switched to position 2 and the signal V_i can be removed. The output is a low impedance source, and information from it can be obtained over a time "t" during which the output voltage holds its original value ($-V_i$).

Fig. 10.9. Hold circuit.

144

With the circuit values shown, the voltage drop 400 ms after switching S to position 2 is given by:

$$\frac{I \times t}{C_1} = \frac{20 \times 10^{-9} \times 0.4}{0.33 \times 10^{-6}} \approx 25 \text{ mV}_{max}$$

I is the maximum input current to the DOA42 module. The pulse diagram (Fig. 10.10) illustrates the operation of the circuit.

If a longer time or less voltage drop is required, a larger capacitor may be used, provided that a longer input signal pulse duration can be tolerated. The pulse duration must be 5 to 6 times the time-constant of the feedback network R_2-C_1.

The input voltage V_i is limited to $\pm$ 10 V with the values of R_1 and R_2 shown. An input voltage higher than 10 V may be applied if the value of R_1 or R_2 is altered according to the relation $V_i/10 = R_1/R_2$. The output V_o is then $V_i \cdot R_2/R_1$.

Fig. 10.10. Pulse diagram.

10.6 Detector for Small Moving Objects

The circuit shown in Fig. 10.11 presents a simple method for the detection of small moving objects, such as the lateral movement of a wire of thread. This is particularly useful for detecting broken threads when working with textiles. A photo-cell detector provides an input for a DZD40 differential zero detector which produces a pulse output.

The photo-cell is normally illuminated and therefore presents a low resistance. Interruption of the light source by the presence of the wire causes a sudden increase in cell resistance and capacitor C_1 is rapidly charged towards $+12$ V, so providing an input to the DZD40. This module is thus tripped and the output switches to $+12$ V. When full illumination is restored, a negative-going input is applied to the DZD40 and the output switches back to 0 V. The capacitive input network ensures that no response is produced by slow changes in illumination or temperature effects.

Fig. 10.11. Circuit for detection of moving objects.

Setting-up is done by adjustment of potentiometers R_1 and R_2; R_2 is set so that no output results from the maximum variation of ambient lighting and temperature, and R_1 is adjusted to produce an output every time the light source is interrupted.

10.7 A Logarithmic Amplifier

This circuit uses the logarithmic voltage-current relationship in a semi-conductor junction to provide, by means of feedback in an operational amplifier, an output which is the logarithm of the input voltage. An accurate logarithmic output may be obtained for input voltages ranging from 100 μV to 10 V.

The circuit is shown in Fig. 10.12. The relation between collector current I_C and base-emitter voltage V_{BE} is given for transistor TR_1 by the equation:

$$V_{BE(1)} = \frac{kT}{q} \log_e \frac{I_{C(1)}}{I_{EBS(1)}} \tag{1}$$

where I_{EBS} is the emitter cut-off current (collector short-circuited to base). Similarly for transistor TR_2:

$$V_{BE(2)} = \frac{kT}{q} \log_e \frac{I_{C(2)}}{I_{EBS(2)}} \tag{2}$$

The high-gain operational amplifier DOA42 (U_1) ensures that the collector of TR_1 is very nearly at 0 V, so that the assumption that $V_{BE(1)} = V_{CE(1)}$ is accurate. For TR_2 the equality $V_{BE(2)} = V_{CE(2)}$ holds.

146

Fig. 10.12. Logarithmic amplifier. Resistors R_1, R_8, R_9, R_{11} and R_{12} are metal-film types. Supply voltages of $+15$ V and -15 V are required.

Substitution in the eqs (1) and (2) yields for the voltage at point P:

$$V_P = V_{CE(2)} - V_{CE(1)} = \frac{kT}{q} \log_e \frac{I_{C(2)} \, I_{EBS(1)}}{I_{C(1)} \, I_{EBS(2)}} \tag{3}$$

Transistors TR_1 and TR_2 are a matched pair, so $I_{EBS(1)} = I_{EBS(2)}$. Therefore eq. (3) reduces to:

$$V_P = \frac{kT}{q} \log_e \frac{I_{C(2)}}{I_{C(1)}} \tag{4}$$

$I_C(2)$ is supplied from the constant current source consisting of transistors TR_3 and TR_4 and has a constant value of approximately 10 μA. $I_{C(1)}$ is directly proportional to the input voltage V_i, since the current drawn by the input of U_1 is negligible and the collector voltage of TR_1 is almost zero. Thus eq. (4) can be expressed as:

$$V_P = \frac{kT}{q} \log_e \frac{I_{C(2)} \, R_1}{V_i} \tag{5}$$

147

Logarithmic amplifier — view of the constructed unit

Fig. 10.13. Offset voltage adjustment circuit.

from which it appears that the voltage V_P is proportional to the logarithmic value of the input voltage V_i. Expressed in $\log_{10}$ form, eq. (5) becomes:

$$V_P = 2.303 \frac{kT}{q} \log_{10} \frac{I_{C(2)} R_1}{V_i},$$

giving

$$V_P = 59.6 \log_{10} \frac{I_{C(2)} R_1}{V_i} \text{ mV at } 27\,^\circ\text{C}.$$

The zero output voltage point can be adjusted by adjusting the TR_2 collector current $I_{C(2)}$ with R_{10}.

If input signals of less than 10 mV are to be applied, offset voltage and current adjustments of U_1 are required. The circuit for offset voltage adjustment is given in Fig. 10.13, R_8 being used to adjust the output voltage of U_1 to zero. Offset current adjustment may be then be made (for conditions of zero output with 100 mV input) by adjusting R_3 (Fig. 10.12) to give an output voltage V_p of $+180$ mV for an input voltage V_i of 100 μV (the minimum input voltage for which an accurate logarithmic output may be expected).

A second DOA42 (unit U_2) has been added to the circuit for amplification of the logarithmic signal. It also acts as a buffer, making the voltage at point P independent of output loading.

Some practical points should be noted:

– the matched pair of transistors TR_1 and TR_2 used in the test circuit were development types; however, selected examples of the BCY87 transistor having a high h_{FE} at low I_C may be used.
– the circuit is suitable for positive input voltages only.
– in the circuit layout, all 0 V lines should be grounded at a single point and long wires avoided (especially near the inputs of U_1).

149

10.8 Circuit for Measuring Deviation from Standard

The circuit (Fig. 10.14) was originally designed to measure the deviation in current of a lamp under test from that of a standard lamp. It can easily be adapted to a variety of applications requiring testing for deviation from a standard, and with the addition of the level detectors shown, can indicate whether or not an item under test is within tolerance. A feature of the circuit is its high accuracy, since circuit component tolerances or variations produce a proportional output error only in the tolerance reading, and not in the total measured current. Thus if the measuring error is 1% and the current deviation from standard of the item under test is 3%, the error in measurement of total current is only 0.03%.

The basic circuit is a DOA42 inverting amplifier which gives 100 times amplification. Normalization is carried out by inserting a standard lamp LA_s in the test circuit and adjusting either V_{ref} or potentiometer R_3 to give a zero output from the DOA42 (U_1). Lamp testing can now be carried out, the difference between the voltage drop across R_1 and the reference voltage V_{ref} giving an output signal from U_1 which can be read on a meter. The output voltage from U_1 is given by $V_o = \pm X I_s R_1$, where X is the deviation in percent and I_s is the current through the

Fig. 10.14. Deviation measuring circuit. Resistor R_1 is a high-stability type.

standard lamp. Thus if $R_1 = 1 \ \Omega$ and $I_s = 1$ A, the percentage deviation will be shown directly on a voltmeter. Measurements at other currents can be performed by adjusting V_{ref}.

A positive indication (by lamps or other means) of over-tolerance can be provided by the addition of two level detectors, U_2 (negative level) and U_3 (positive level). The tripping levels corresponding to the upper and lower tolerance limits are adjustable with potentiometers R_{15} and R_9 respectively.

Stirling Motor.

Equipment for monitoring Stirling motor running characteristics.

11 Technical Performance

11.1 DOA40 Module

The technical performance figures for the DOA40 module are given below; a circuit diagram and description are given in Section 2.1.

Temperature
Ambient temperature range:
operating	0 to +85 °C
storage	—40 to +85 °C
Max. case temperature	91 °C

Power supply
Supply voltages

$$V_P = +15 \text{ V} \pm 3\%$$
$$V_N = -15 \text{ V} \pm 3\%$$

Supply currents

$$I_P = 10 \text{ mA} + \text{load current}$$
$$I_N = 10 \text{ mA} + \text{load current}$$

Input data (ambient temperature +25 °C unless noted otherwise)

Open-loop gain	minimum	typical
d.c. max. load	25 000	60 000
d.c. 100 kΩ load	100 000	150 000

Input voltage offset
Initial offset can be trimmed to zero by means of an external variable resistor of 15 kΩ between terminals 6 and 19.

	maximum	typical
drift with temperature change (0 °C to +85 °C)	5 μV/degC	3 μV/degC
drift with supply voltage change for +15 V supply	47 μV/V	20 μV/V
for —15 supply	20 μV/V	13 μV/V

Input current

Each input	maximum	typical
bias current	700 nA	300 nA
drift with temperature change (0 °C to +85 °C)	7 nA/degC	3 nA/degC

Differential

initial offset	35 nA	6 nA
drift with temperature change		
(0 °C to +85 °C)	1 nA/degC	0.3 nA/degC

Input impedance	*minimum*	*typical*
between inputs	75 kΩ	200 kΩ
common mode	60 MΩ	100 MΩ

Input voltage

max. voltage between inputs	+5 V and −5 V
max. common mode voltage	+10 V and −10 V
common mode rejection	20 000 (min.)
	60 000 (typ.)

Voltage noise (16 Hz - 16 kHz)   3 μV (r.m.s.)

Output data

Output voltage (at a load current of 6 mA)	+10 V to −10 V (at least)
Load resistance	1.67 kΩ (min.)
Output resistance	< 5 kΩ

Frequency response (Fig. 11.1)	*minimum*	*typical*
Unity gain bandwidth (small signal)	8.5 MHz	9.5 MHz
Full output response (20 V_{p-p})		
with 10 kΩ load	40 kHz	60 kHz
with 1.67 kΩ load	33 kHz	50 kHz
Slewing rate ($R_{load} = 10$ kΩ)	2.5 V/μs	3.7 V/μs

Fig. 11.1. DOA40 gain-frequency characteristic.

Specifications for the DOA40 used with 12 V supply

With a 12 V supply, the data remains the same as given for the 15 V supply, with the following exceptions:

Power supply voltages	$V_P = +12 \text{ V} \pm 5\%$
	$V_N = -12 \text{ V} \pm 5\%$
Power supply currents (load current and	$I_P = 8 \text{ mA}$
feedback current to be added)	$I_N = 8 \text{ mA}$
Input currents	multiply the data given for 15 V supply by 0.8
Common mode voltage	+8 V and −8 V
Output voltage at a load current of 5 mA	+9 V and −9 V
Load resistance	1.8 kΩ (min.)

For special applications certain characteristics can be modified by the use of external circuits. These circuits modify the technical data as follows data not listed here remains unaltered):

11.1.1 MAXIMUM DIFFERENTIAL INPUT VOLTAGE

For non-linear operation the maximum permissible differential input voltage can be increased to +10 V and −10 V by connecting two anti-parallel BAX13 diodes across the inputs, and a 680 Ω resistor in series with each input.

11.1.2 INCREASED OUTPUT POWER

See section 12.6 and Fig. 12.8.

Output current	50 mA at +10 V to −10 V

11.1.3 REDUCED INPUT CURRENT/INCREASED INPUT IMPEDANCE

See section 12.7 and Fig. 12.13.

	maximum	typical
Supply voltage rejection (both supplies)		80 μV/V
Input voltage drift with temperature change (0 °C to +85 °C)	10 μV/degC	5 μV/degC
Input current		
each input		
bias current	60 nA	40 nA
drift with temperature change		0.25 nA/degC

differential		
initial offset	6 nA	4 nA
drift with temperature change		
(0 °C to +85 °C)		0.1 nA/degC

	minimum	*typical*
Input impedance		
between inputs	10 MΩ	15 MΩ
common mode		600 MΩ
Common mode rejection		10,000
Unity gain bandwidth		6.5 MHz
Full output frequency (20 V_{p-p})		40 kHz

11.1.4 Zero Adjustment of Input Current

See Section 12.7 and Fig. 12.14.

11.2 DOA42 Module

The technical performance figures for the DOA42 module are given below; a circuit diagram and description are given in Section 2.2.

Temperature

Ambient temperature range:

operating	−25 °C to +85 °C
storage	−55 °C to +85 °C
Max. case temperature	85 °C

Power supply

Supply voltages $\qquad V_P = +15$ V $\pm 3\%$

$\qquad\qquad\qquad\qquad\qquad\ V_N = -15$ V $\pm 3\%$

Supply currents (load current to be added) $\quad I_P = 3.7$ mA

$\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\ I_N = \ \ 1$ mA

Input data (ambient temperature +25 °C unless stated otherwise)

Open loop gain	*minimum*	*typical*
d.c., max. load		106 dB
d.c., 10 kΩ load	100 dB	106 dB

Input voltage offset

Initial offset can be trimmed to zero by means of an external variable resistor of 25 kΩ between terminals "Trim" and "+V".

	maximum	typical
Drift with temperature change (0 °C to +85 °C)		7 μV/degC
Drift with supply voltage change		
for +15 V supply	± 20 μV/V	± 10 μV/V
for −15 V supply	± 20 μV/V	± 10 μV/V

Input current	maximum	typical
Each input		
bias current	20 nA	5 nA
drift with temperature change (0 °C to +85 °C)	0.5 nA/degC	0.1 nA/degC
Differential		
initial offset	4 nA	1 nA
drift with temperature change (0 °C to +85 °C)	100 pA/degC	30 pA/degC

Input impedance	minimum	typical
between inputs	5 MΩ	20 MΩ
common mode		1000 MΩ

Input voltage	
Max. voltage between inputs	+5 V and −5 V
Max. common mode voltage	+5 V and −5 V
Common mode rejection	min. 80 dB typ. 100 dB

Voltage noise (0-10 kHz)	maximum	typical
	15 μV (r.m.s.)	8 μV (r.m.s.)

Output data
Output voltage (total current 5 mA)   min. +10 V to −10 V
Load resistance   min.   2 kΩ
                              (short-circuit proof)

Output resistance   typ. 150 Ω

Frequency response	typical
Unity gain bandwidth (small signal)	5 MHz
Full output response (20 V_{p-p})	
with 10 kΩ load	45 kHz
with 2 kΩ load	40 kHz
Slewing rate ($R_{load} = 10$ kΩ)	2.5 V/μs

158

Specifications for the DOA42 used with 12 V supply

With a 12 V supply, the data remains the same as given for a 15 V supply with the following exceptions:

Power supply voltages	$V_P = +12$ V $\pm 5\%$
	$V_N = -12$ V $\pm 5\%$
Power supply currents (load current to be	$V_P = 2.9$ mA
added)	$V_N = 0.8$ mA
Input currents	multiply the data given for 15 V supply by 0.8
Max. common mode voltage	$+4$ V and -4
Output voltage at a load current of 4 mA	$+9$ V and -9 V
Load resistance	min. 2.25 kΩ

Fig. 11.2(a) gives the frequency response for various gain levels. When the amplifier is applied with a loop gain of less than 40 dB external compensation, RC series circuits have to be connected between the pins k_1 and k_2. The corresponding external correction networks are given in Fig. 11.2(b).

Use as an operational amplifier

For use as an operational amplifier the terminals E_1, E_2 and C should be strapped together.

Fig. 11.2 (a) DOA42 gain frequency characteristic.

feedback = 40 dB
gain = 60 dB

feedback = 60 dB
gain = 40 dB

feedback = 80 dB
gain ≈ 20 dB

feedback = 100 dB
gain = 0 dB

Fig. 11.2 (b) External correction networks.

Pitch grinding machine for metal film and carbon resistors.

11.3 DZD40 Module

The technical performance figures for the DZD40 module are given below; a circuit diagram and description are given in Section 3.1. Component references refer to Fig. 3.3.

Temperature
Ambient temperature range:
operating	0 to 70 °C
storage	—40 to +85 °C

Power supply
Supply voltages

$V_{19} = +12 \text{ V} \pm 5\%$ or $+15 \text{ V} \pm 1\%$
$V_9 = +12 \text{ V} \pm 5\%$ or $+15 \text{ V} \pm 1\%$
$(V_{17} = V_{18} = V_{16} = V_{19}$ approx.)

Supply currents
$I_{19} = 6 \text{ mA}$ ⎰ at nominal values of
$I_9 = 8.3 \text{ mA}$ ⎱ V_{19} and V_9

Input data
Differential offset voltage after balancing (see "Initial adjustments")	0.1 mV
Voltage drift as a result of a change in temperature, measured at a source impedance of 10 kΩ	
typical value	3 μV/degC
maximum value	5 μV/degC
Maximum common mode voltage	± 2 V
Common mode rejection $\lvert V_{13} - V_{12} \rvert$	typ. 80 dB
Differential offset current	< 30 nA
Current drift as a result of a change in temperature (typical value)	1 nA/degC
Differential input resistance (R_i)	see Figs. 11.3 and 11.4
Common mode impedance	typ. 1.2 MΩ
Maximum value of $\lvert V_3 - V_1 \rvert$ to avoid extra delays	700 mV
Maximum voltage between input terminals	5 V
Frequency range	0-200 kHz

From 100 to 200 kHz the differential sensitivity reduces; the input voltage must be multiplied by the factor η (see Fig. 11.5).

Fig. 11.3. Curve a: typical differential input resistance.
        Curve b: typical input resistance between each input and 0 V.
        Curve c: minimum differential input resistance.
        Curve d: minimum input resistance between each input and 0 V.

Fig. 11.4 Temperature coefficient of the differential input resistance.

Fig. 11.5. η is the input requirement factor for frequencies over 100 kHz (1.8 at 200 kHz,
        1 up to 100 kHz).

163

The differential sensitivity ($|V_3 - |V_1||$) is adjusted by means of gain control resistor R_G between 2 and 4; see Fig. 11.6. Curves a and d in this figure are worst case limits at $T_{amb} = 0\,°\text{C}$. Curves a and b apply to the minimum input signal at which TR_5 or TR_6 is conducting (V_7 or V_{14} is LOW and TR_7 is not conducting (V_8 is HIGH). Curves c and d apply to the maximum input signal at which TR_5 or TR_6 is not conducting (V_7 and V_{14} are HIGH) and TR_7 is conducting (V_8 is LOW). Curves b and c give typical values at $T_{amb} = 25\,°\text{C}$.

Fig. 11.6 Differential sensitivity vs R_G curves.

The curves in Fig. 11.7 apply to the minimum input signal at which TR_5 or TR_6 is conducting (V_7 or V_{14} is LOW) and TR_7 is not conducting (V_8 is HIGH).

Fig. 11.7 Minimum differential sensitivity vs R_V curves.

The curves in Fig. 11.8 apply to the maximum input signal at which TR_5 and TR_6 are not conducting (V_7 and V_{14} are HIGH) and TR_7 is conducting (V_8 is LOW).

Output data for outputs A_1 and A_2 (terminals 13 and 12)

Voltage gain   see Fig. 11.9

Maximum undistorted voltage $V_{13} = -V_{12}$ 1 V

Bandwidth at 3 dB   0-150 kHz

Minimum load resistance   100 kΩ

Fig. 11.8 Maximum differential sensitivity vs R_V curves.

Fig. 11.9 Voltage gain vs R_G curves.

165

Output data for outputs Q_1 and Q_2 * (terminals 7 and 14)

Maximum current at $V > 0$ V **	3.5 mA
Load resistance	3.6 kΩ

Output data for output/Q_2 (terminal 8)	*17 and 16 interconnected*	*17 and 16 not interconnected*
Maximum current	2.5 mA	3.5 mA
Load resistance	5 kΩ	3.6 kΩ

INITIAL ADJUSTMENTS

Minimum offset voltage

Connect a 50 kΩ trimming potentiometer (R_B) to the terminals 5 and 6, slider to terminal 16. Set the slider to the centre position. Short circuit the input terminals 1 and 3.

Connect a resistor to the terminals 2 and 4 to obtain the desired gain (see "Sensitivity").

Connect a d.c. millivoltmeter with high input impedance, or an oscilloscope, to the terminals 12 and 13; the meter or the oscilloscope must be floating.

Apply the supply voltages; allow a few minutes for block temperature distribution to reach a stable value before reading the amplified offset voltage on the millivoltmeter.

Correct the offset voltage by turning the slider of the trimming potentiometer in such a way that minimum reading on the meter or the oscilloscope is obtained. When reading comes below 20% of full-scale value, switch to higher meter sensitivity. A correct adjustment shows a final value of a few millivolts, depending upon the actual gain.

Observe the voltmeter or oscilloscope for some time after balance has been achieved; the reading should be stable.

Remove the short circuit across the input terminals and remove the voltmeter or the oscilloscope. Leave the slider of the potentiometer in optimum position.

---

* If the outputs Q_1 and Q_2 are not used terminals 7 and 14 should be connected to terminal 10 (0 V).

** Clamp diodes (e.g. BAX13, BAY38, IN4009) must be externally connected to terminals 7 and 14.

Notes – Where no particular requirement for balance is to be met, the trimming potentiometer can be replaced by resistors having the value found during the balance procedure. Unbalance will give unequal output wave shapes at terminals 7 and 14 as well as an alternation of two forms at terminal 8 with a sinusoidal input voltage.

Sensivitity

Coarse adjustment can be made by connecting a resistor (R_G) to the terminals 2 and 4; if a trimming potentiometer of 500 Ω is used for this purpose the gain can be set over a wide range. The terminals 16 and 18 must be interconnected. For the correct value of R_G, see Fig. 11.3. After the resistor between the terminals 2 and 4 has been adjusted, fine adjustment can be made by disconnecting terminal 16 from terminal 18 and by connecting a variable resistor (R_V) of 150 kΩ to the terminals 15 and 16 (without influencing the input impedance).

11.4 PSM40 Module

The technical performance figures for the PSM40 module are given below; a circuit diagram and description are given in Section 4.1. Component references refer to Fig. 4.2.

Temperature
Ambient temperature range:

operating	—25 to +85 °C
storage	—40 to +85 °C

Power supply

Supply voltage
$$V_{19} = +12 \text{ V} \pm 5\%, \ V_9 = -12 \text{ V} \pm 5\% \quad \text{or}$$
$$V_{19} = +12 \text{ V} +10\%, \ V_9 = -12 \text{ V} +10\% \text{ or}$$
$$V_{19} = +12 \text{ V} -10\%, \ V_9 = -12 \text{ V} -10\%$$

Supply current
$$I_{19} = I_9 = \text{approximately 10 mA (excluding load current)}$$

Note – As the output voltage V_6 is dependent upon switch-on sequence and rise time of the supply voltages, it is recommended that terminal 6 is temporarily short circuited to terminal 0 when switching on.

Input data
Control voltage V_c
   maximum (limiting)   5 V
   minimum (limiting)   0 V
Control current I_c 0.5 to 0.33 mA
Maximum wiring capacitance at the control
input (terminal 7)   200 pF

Output data
Output voltage
   high level (TR_7 non-conducting)   max. 15 V
   low level (TR_7 conducting)   max. 0.5 V
                                      min.   0 V
Output current   max. 25 mA at 0.5 V
                                        ($T_{amb} = -25\ °C$)
Minimum control range of phase angle (α)   10-170°

Synchronization
Synchronization voltage (V_s)   24 V_{rms}, $+15\%$,
                                         -20%

Nominal synchronization current (I_s)
   linear control   approx. 4 mA
   cosinusoidal control   approx. 8 mA
Synchronization frequency range   15 Hz to 10 kHz

The synchronization voltage (Fig. 11.10) can be supplied by a transformer with or without a centre tap and, preferably, provided with an electrostatic screen between the primary and the synchronization winding to avoid capacitive zero shift. When a transformer is used the outputs of the transformer have to be connected to the terminals 11 and 12. When

Fig. 11.10 Synchronization voltage.

a transformer with a centre tap is used, the centre tap is connected to terminal 10. Furthermore two diodes (OA200 or an equivalent type) must be connected with the cathodes to the terminals 11 and 12, and the anodes to terminal 10.

When the terminals 2 and 3 are interconnected the unit can be used at a synchronization frequency of 50 Hz. For frequencies higher or lower than 50 Hz terminals 2 and 3 must be left disconnected and an external capacitor has to be connected between the terminals 2 and 10. The value of the capacitor is given by:

$$C = \frac{11}{f} \ \mu F.$$

Connections and Adjustments

For *linear control* connect terminals 5, 15 and 16 together.

For *cosinusoidal control* connect:
terminal 5 to terminal 14
terminal 17 to terminal 18
terminal 10 to terminal 18 via an electrolytic capacitor (+ve to terminal 10) value 100 μF, rating 40 V.

For *single-phase operation* the phase angle can be adjusted to give one of the three conditions detailed below.

A. For approximately $0°$ at a control voltage of 0 V:

(i)   Connect the module for linear or cosinusoidal control
(ii) Connect a potentiometer (47 kΩ) between terminals 1 and 4, a resistor (1 kΩ) between terminals 6 and 19, and connect terminal 7 to 0 V (terminal 10). Set the potentiometer to maximum resistance.
(iii) Connect a d.c. voltmeter (mV) between output terminal 6 and terminal 10. Apply the d.c. supply and the synchronization voltages.
(iv) Note that the voltage indicated on the voltmeter is approximately 0 V. Decrease the value of resistance presented by the potentiometer until a sharp rise in output voltage occurs.
This value of resistance gives the required phase angle/control voltage relationship.
(v)   Remove the 1 kΩ resistor.

B. For exactly 0° at a control voltage of 0 V.

(i) Connect the module as described above, but omit the connection between terminals 7 and 10.
(ii) Set the potentiometer to maximum resistance.
(iii) Apply the d.c. supply and the synchronization voltages.
(iv) Apply a control voltage of 50 to 100 mV between terminals 7 and 10.
(v) Decrease the value of resistance presented by the potentiometer until a sharp rise in output voltage occurs. This value of resistance gives the required phase angle/control voltage relationship.
(vi) Remove the 1 kΩ resistor.

This method of adjustment ensures that a phase angle of exactly 0° is achieved, but introduces a threshold of 50 to 100 mV before the control region is entered.

C. For 5° to 15° at a control voltage of 0 V.

(i) Connect the module as described in the first procedure, but replace the d.c. voltmeter with an oscilloscope.
(ii) Observe the pulse output and set the phase angle to the required value by adjusting the potentiometer.
(iii) Remove the 1 kΩ resistor.

After the phase angle has been set, the potentiometer can be replaced by a fixed resistor. Typical values are 10 kΩ for linear control, and 33 kΩ for cosinusoidal control. If greater accuracy is required when setting up a system to either of the first two conditions, the d.c. voltmeter can be replaced by an oscilloscope.

For *multi-phase operation* where the phase angles of two or more modules with a common control voltage have to be equal over the whole control range. It is therefore necessary to adjust the phase angle at the top end, and at the low region of the control range as follows:

A. For linear control at maximum control voltage.

(i) Connect the modules for linear control.
(ii) Apply the d.c. supply voltage (but *not* the synchronization voltage).

170

(iii) Measure the voltage at terminal 2 of each module. If there is a difference between these voltages connect a resistor (value approximately 1 Ω/mV) between terminals 17 and 18 of the module having the highest voltage at terminal 2. In this way the voltages can be made equal.

B. For cosinusoidal control at maximum control voltage.

(i) Connect terminals 5 to 15 and terminals 17 to 18.
(ii) Apply the d.c. supply voltages, and also connect a d.c. voltage of $+$ 30 V to terminals 18.
(iii) Measure the voltage at terminal 2 of each module. If there is a difference between these voltages connect a resistor (value approximately 3 Ω/mV) between terminals 17 and 18 of the module having the highest voltage at terminal 2. In this way the voltages can be made equal.

C. For linear and cosinusoidal control at low control voltages.

The previously described procedures ensure that the phase angles are equal at maximum control voltage. To ensure equality over the whole range the following procedure is necessary.

(i) Connect the modules for linear or cosinusoidal control.
(ii) Adjust one module to give 0° phase angle with a control voltage of 0 V (see *single-phase operation*) and leave the 1 kΩ resistor in situ between terminals 1 and 4.
(iii) Connect a d.c. voltmeter between terminal 6 of the module which has been adjusted in (ii), and terminal 6 of the other module. Also, connect a 1 kΩ resistor between terminals 6 and 19 of each module.
(iv) Apply a control voltage of 1 V to each module. Vary the value of the resistor between terminals 1 and 4 of the module to be adjusted until a minimum reading on the voltmeter is obtained. The phase angles of the two modules are now equal over the whole range.

The foregoing adjustments can be made more accurately by using an oscilloscope instead of the d.c. voltmeter. Accuracy may be particularly important in multi-phase systems driving a.c. loads. For adjustment of

the phase angle at maximum control voltage using an oscilloscope connected to the output terminal 6, the following procedure is necessary.

(i) Connect the modules as described previously, but with a potentiometer (500Ω) between terminals 17 and 18.

(ii) Connect a 1 kΩ resistor between terminals 6 and 19.

(iii) Apply the synchronization voltage and compare the pulse output with the mains supply cycle, or with another module synchronized by another phase of the system.

(iv) Adjust the potentiometer between terminals 17 and 18 to give the correct relationship. The final value is typically 330Ω.

(v) Remove the 1 kΩ resistor between terminals 6 and 19.

To adjust the phase angle at low control voltages using an oscilloscope, the procedure described previously can be used, simply substituting an oscilloscope in place of the d.c. voltmeter.

12 Definitions and Parameters of Operational Amplifiers

The operational amplifier is a d.c. amplifier which combines the properties of very high voltage gain and low drift; it is normally used in conjunction with a negative feedback network in which the feedback is so heavy that the input to output voltage relationship is defined in terms of the network, and not by the properties of the amplifier itself. Such a mode of operation demands that a high degree of stability is maintained for many kinds of negative feedback.

Some of the mathematical operations which can be performed using only one amplifier and a suitably connected feedback network are:

- add

- subtract

- invert

- integrate

- differentiate

Other circuits which can be built with the operational amplifier include:

- comparators

- multivibrators

- sensor amplifiers

- logarithmic amplifiers

- converters

The type of operational amplifier which is most widely used is the d.c. differential (difference) amplifier. This is characterized by having two inputs and it amplifies the difference between these two inputs whose absolute values can lie within a wide range of voltages. The explanations given in this section are related mainly to this type of amplifier.

12.1 Voltage Gain and Negative Feedback

The general symbol for an operational amplifier is shown in Fig. 12.1; the apex of the triangle points in the direction of the signal flow, and the two inputs are designated *positive* $(+)$ or *non-inverting* and *negative* $(-)$ or *inverting*. When a potential difference is applied between the input terminals a positive output results when the $+$ terminal is most positive, and a negative output results when the $-$ terminal is most positive. Hence the output is proportional to the *difference* of the two input signals. The gain of the amplifier is defined as being the ratio of the output voltage to the difference of the two input signals; hence,

$$A_{ol} = \frac{V_o}{V_2 - V_1}$$

where A_{ol} is the *open-loop* gain of the amplifier, i.e. without feedback.

Fig. 12.1. General symbol for an operational amplifier.

When negative feedback is applied, part or all of the output signal is fed back to the *negative* input. As the output signal is of opposite polarity to the input, the feedback reduces the effective gain of the amplifier; the gain of the amplifier plus feedback network is A_{cl}, the *closed-loop* gain or *transfer function* (f). By varying the feedback network configuration, the transfer function can be selected to give the desired relationship between the input and output signals.

One of the more common operational amplifier plus feedback configurations is shown in Fig. 12.2. The input and feedback signals are

Fig. 12.2. Operational amplifier with feedback.

174

applied to the *negative* input, and the *positive* input is connected to earth. Feedback is obtained via impedances Z_f and Z_1; Z_f is the *feedback* impedance, and Z_1 is the *input* impedance. A positive input signal V_1 applied to the *negative* input via Z_1 produces a negative output signal V_o. Part of V_o is fed back via Z_f, thereby reducing the input signal to the amplifier. An equilibrium is established for which the following equations are true:

– input signal due to V_1:

$$= V_1 \frac{Z_f}{Z_f + Z_1}$$

– input signal due to V_0:

$$= V_o \frac{Z_1}{Z_f + Z_1}$$

– The effective input signal $e = V_o/A_{ol}$ (N.B. A_{ol} is a negative quantity). Therefore the equation relating the input voltage is:

$$V_1 \frac{Z_f}{Z_f + Z_1} + V_o \frac{Z_1}{Z_f + Z_1} = \frac{V_o}{A_{ol}}. \tag{i}$$

As A_{ol} approaches an infinite value, this becomes:

$$V_1 \frac{Z_f}{Z_f + Z_1} + V_o \frac{Z_1}{Z_f + Z_1} = 0$$

whence:

$$\frac{V_o}{V_1} = -\frac{Z_f}{Z_1}$$

This expression implies that the transfer function (V_o/V_1) is completely independent of the amplifier parameters. However, in practice A_{ol} has a finite value and the transfer function, from equation (i), becomes:

$$\frac{V_o}{V_1} = -\frac{Z_f}{Z_1} \cdot \frac{1}{1 - (1 + Z_f/Z_1)/A_{ol}} \tag{ii}$$

from which it is seen that the significance of A_{ol} decreases as its magnitude

increases and, therefore, in any circuit configuration the following condition must be fulfilled to enable the use of a wide range of feedback configurations:

$$\frac{A_{cl}}{A_{ol}} \ll 1, \quad \text{or} \quad \frac{A_{ol}}{A_{cl}} \gg 1$$

This ratio defines the accuracy of the transfer function and is called the *loop gain*.

The accuracy obtainable with the circuit is calculated by substituting values in equation (ii): if Z_f and Z_1 have values of 20 kΩ and 1 kΩ respectively, and A_{ol} is -10^5, then the transfer function is given by:

$$\frac{V_o}{V_1} = -20 \cdot \frac{1}{1 + 21/10^5} = -19.996$$

Hence the ideal value of 20 is approached to within 0.2 %. A quick method to check the transfer function of an ideal operational amplifier with feedback is described below. While the amplifier operates in the linear region, it can be assumed that the voltage between the input terminals is zero; viz,

$$e = \frac{V_o}{A_{ol}} = \frac{V_o}{\infty} = 0$$

For example, in Fig. 12.2 the *positive* input of the amplifier is grounded, therefore the voltage at the *negative* input is zero. Hence the current flowing in Z_1 is V_1/Z_1, and that in Z_f is V_o/Z_f.

The assumption that no current flows into the *negative* input implies that the sum of the two currents is zero, i.e.,

$$\frac{V_o}{Z_f} + \frac{V_1}{Z_1} = 0$$

or,

$$\frac{V_o}{V_1} = -\frac{Z_f}{Z_1} (= A_{cl})$$

12.2 Input Voltage Ratings

It has already been stated that the output of an operational amplifier is a voltage which increases linearly as the difference between the two input signals increases, and that the absolute values of the inputs are immaterial. However, the latter is only true for a limited voltage range; this is called the *common mode* input voltage range. Nominal inputs outside this range cause a deterioration in common mode rejection ratio (see Section 12.3) and, eventually, non-linear operation of the amplifier.

The difference voltage that is applied between the two inputs is also subject to a limiting range; this is called the *differential* input voltage range. In practice the differential input range is usually much larger than would be applied to the amplifier operating in the linear region. This is because the high open-loop gain would cause the output rating of the amplifier to be exceeded long before the differential input voltage reached its maximum value. For example, the output voltage rating of a DOA40 is $\pm$ 10 V, and the differential input range is $\pm$ 5 V; hence a differential input of 5 V would cause a theoretical output of 5 A_{ol}, i.e. 5×10^5 V, and the amplifier would be saturated. It follows that the maximum practicable differential input is in the region of 100 μV. In situations where it is necessary to limit the differential input voltage, a pair of diodes can be connected in antiparallel as shown in Fig. 12.3 While the amplifier operates in its linear region the diode leakage current is very small due to the low voltage between the inputs. Diodes of the type BAX13 are suitable for this application with the DOA40 and DOA42 amplifiers.

Fi. 12.3. Antiparallel input protection diodes.

12.3 Common Mode Rejection Ratio

When the two inputs to an operational amplifier are exactly equal, the output should be zero volts. In practice this condition is rarely achieved and a small output voltage usually exists even when the inputs are equal.

This voltage is called the *common mode error* voltage and is defined in terms of the *common mode rejection ratio* (CMRR); i.e., the ratio F of the voltage (E_{cm}) that must be applied between the short-circuited inputs and earth, to the differential input voltage (e_d) required to produce the same output voltage E_o (Fig. 12.4). Hence:

$$F = \frac{E_{cm}}{e_d}, \quad \text{but} \quad e_d = \frac{E_o}{A_{ol}}$$

therefore

$$F = A_{ol} \cdot \frac{E_{cm}}{E_o}$$

Typical values of F are 60,000 and 100,000 for DOA40 and DOA42 respectively.

Fig. 12.4. Common mode error voltage.

12.4 Input Impedance

Two types of input impedance have to be considered, these being the differential and common mode input impedances.

12.4.1 DIFFERENTIAL INPUT IMPEDANCE

This is defined as being the impedance between the input terminals of the amplifier, and it should be as high as possible. In Fig. 12.5 the load presented to the voltage source V_1 approximates to Z_1 as e approaches zero; therefore the finite differential input impedance Z_{id} has no effect on the input impedance of the circuit as a whole. However, circuit analysis shows that part of the input signal flows through Z_{id} and, therefore, the input is attenuated. The amount of current which flows in Z_{id} is approximately e/Z_{id}. Therefore, it is also dependent on e, and as $e = V_o/A_{ol}$, on A_{ol}. The effect of a low differential input impedance may be regarded as a reduction of loop gain and a consequent deterioration of transfer

178

Fig. 12.5. Differential input impedance.

function, and is felt only in applications where no feedback is used. A feature of the DOA42 module is the high value of Z_{id}, this being greater than 5 MΩ.

12.4.2 COMMON MODE INPUT IMPEDANCE

The common mode input impedance, Z_{cm}, is defined as the impedance from one input terminal to ground, while the other terminal is not connected. Typical values of Z_{cm} for the DOA40 and DOA42 modules are 100 MΩ and 1000 MΩ respectively. The importance of a high common mode input impedance is illustrated by the non-inverting amplifier shown in Fig. 12.6. An input signal, V_1 is applied between the positive input and ground. For a high gain amplifier the voltage e between the inputs approaches zero (see Section 12.2); this implies that the voltage at the negative input terminal is also V_1. Therefore, regarding Z_f and Z_1 as a voltage divider, the output voltage, V_o, is given by:

$$\frac{V_o}{V_1} = \frac{Z_1 + Z_f}{Z_1} = 1 + \frac{Z_f}{Z_1} \ (= A_{cl})$$

It can be shown that the load presented to V_1 due to Z_{id} is approximately $Z_{id} \cdot A_{ol}/A_{cl}$, which, for a DOA40 with $A_{ol} = 10^5$, $Z_{id} = 200$ kΩ and an A_{cl} of 20, is 10^9 Ω.

Fig. 12.6. Common mode input impedance.

179

This impedance is shunted by Z_{cm} (10^8 Ω) and the total load presented to V_1 is 0.9×10^8 Ω. However, despite this limitation, the input impedance is much higher than that presented by the circuit shown in Fig. 12.2 and, therefore, is preferred where signals from high source impedance circuits are used. Hence the condition that $Z_{cm} \gg Z_S$ is maintained for the voltage divider formed by these two impedances.

12.5 Output Impedance

Although the output impedance Z_o of an operational amplifier should be as small as possible, the value is not critical as the application of feedback reduces the effective value. However, an undesirable effect of a high value of Z_o is the consequent reduction in open-loop gain. In the circuit of Fig. 12.7, Z_o forms a voltage divider with the parallel impedances Z_L and Z_f (as the negative input is at approximately zero volts). This means that the output voltage V_o is *not* equal to eA_{ol} but is given by eA'_{ol} where

$$A_{ol}' = A_{ol} \cdot \frac{Z_L'}{Z_L' + Z_o} :$$

Z_L' is the total external load, i.e.

$$Z_L' = \frac{Z_L \cdot Z_f}{Z_L + Z_f} .$$

Hence the value of A'_{ol} must be related to a specific load; the DOA40 and DOA42 modules have open-loop gains of 25 k and 100 k at total load resistances (Z'_L) of 1.67 kΩ and 100 kΩ respectively.

As stated previously, the application of feedback reduces the effective output impedance; this reduction is governed by the factor

$$\frac{1 + A_{ol}}{A_{ol}'} ,$$

Fig. 12.7. Output impedance.

180

where $A_{cl} = Z_f/Z_L$. The values of Z_o for the DOA40 and DOA42 modules are 5 kΩ and 150 Ω respectively. Thus for the DOA40, with $A_{cl} = 20$ and $A'_{ol} = 25$ k (see above), the effective output impedance (when loaded with 1.67 kΩ) is

$$Z_o' = \frac{1 + A_{ol}}{A_{ol}'} \cdot Z_o = \frac{5.10^3 \cdot 21}{25.10^3} = 4.05 \ \Omega.$$

12.6 Output Limitations

The DOA40 and DOA42 operational amplifiers are guaranteed to pro-
duce output voltages over the range -10 V to $+10$ V at full load current.
These currents are 6 mA and 5 mA respectively. Higher output currents
can be obtained by using an external current booster; the circuit shown
in Fig. 12.8 is capable of delivering 50 mA at -10 V and $+10$ V (the
feedback resistor and load are connected to the booster output, *not* the
amplifier output).

Fig. 12.8. Output current booster.

In some cases the output voltages produced by the operational ampli-
fier exceed the input ratings of the following circuit. Therefore, the output

voltage must be limited. Figure 12.9(a) shows two arrangements of diode limiters, one for limiting the negative output swing (diode plus voltage regulator diode) and one for limiting both positive and negative output swings (two voltage regulator diodes). However, these methods can only be used with feedback networks which have a moderate impedance as the voltage regulator diodes conduct an appreciable leakage current. This current is dependent on factors such as the type of diode, voltage, temperature, etc., but normally represents an equivalent impedance of 1 to 20 MΩ. The value of the equivalent impedance can be raised by using the low leakage current circuit shown in Fig. 12.9(b). In this circuit the diode leakage current is very low .The voltage at point A is given by the product of the voltage regulator diode leakage current and the value of R_p (R_p is normally between 10 kΩ and 100 kΩ). Therefore there is a very small voltage across the anti-parallel diodes. This gives an equivalent impedance of 500 MΩ to 5000 MΩ at a temperature of 25 °C. As a rough guide it can be taken that the impedance will halve for each temperature rise of 10 degC, when silicon semiconductors are used.

Fig. 12.9(a). Voltage limiter.

Fig. 12.9(b). Voltage limiter with low leakage current.

182

12.7 Offset Voltage, Bias and Offset Current

For an ideal amplifier the output voltage is zero when both inputs are connected to ground. However, any practical circuit exhibits a certain output voltage under these conditions and the voltage which must be applied between the inputs to reduce this output voltage to zero is termed the input offset voltage. This voltage may be positive or negative and is a function of temperature, supply voltage and ageing of components.

12.7.1 OFFSET VOLTAGE AND TEMPERATURE

The initial offset voltage in the DOA40 and DOA42 modules can be adjusted to zero by means of an external potentiometer. However, the value of offset voltage is not a constant value but is subject to drift, the most significant factor causing this drift being temperature. For the DOA40 module the drift (maximum) is 5 μV/degC, referred to the input.

Fig. 12.10. Equivalent input offset voltage.

The input offset voltage can be represented by an equivalent voltage source V_d in series with one of the input terminals (see Fig. 12.10) of a drift-free amplifier. The output voltage due to the offset is subjected to the negative feedback: viz. the output voltage due to V_d is, for the feedback configuration of Fig. 12.10, equal to

$$V_o = V_d \left(1 + \frac{Z_f}{Z_1} \right).$$

Transferred to the input of the total circuit the equivalent input signal is

$$V_d \left(1 + \frac{Z_1}{Z_f} \right).$$

12.7.2 BIAS AND OFFSET CURRENT

Another offset source can be formed by the bias (= input) currents of the amplifier. We say "can" because, if the impedance from input terminals to (signal) ground is zero no output voltage due to the bias currents will be exhibited. Unlike offset voltage the effect of offset current depends on the magnitude of the feedback network, and not on the ratio of feedback and input network. The input or bias current drawn can be represented by current sources i_{d1} and i_{d2} as in the circuit diagram shown in Fig. 12.11. The maximum input currents for the DOA42 module are 20 nA. It is interesting to know what output voltages can be expected in the circuit of Fig. 12.11 due to the input currents. As the impedance in series with the positive input is zero, i_{d2} has no effect. In the case of i_{d1}, since any current which flows to the negative input is inherently compensated by an equal and opposite current through the feedback impedance Z_f, an output voltage $V_o = i_{d1}Z_f$ will be exhibited. Reflected to the input as an input voltage source the equivalent voltage is $i_{d1}Z_1$. In the case of the DOA42 for example, if Z_f is 50 kΩ the maximum output voltage due to the input current is $20 \times 10^{-9} \times 50 \times 10^3 = 1$ mV. As long as the reflected offset voltage due to the bias current is lower than a few millivolts, it can be adjusted to zero with the same external potentiometer as is used for adjusting the offset voltage. However, compensation of higher offset voltages in this way may lead to a serious deterioration of the voltage driftperformance.

Fig. 12.11. Equivalent input and bias current.

The influence of the bias current can be reduced by choosing equal impedances in both input terminals. One may imagine that the positive input will change in potential due to the voltage drop across Z_c, caused

184

by i_{d2} (see Fig. 12.11), just as the potential of the negative input changes due to i_{d1}. So for

$$i_{d1} = i_{d2}$$

and

$$Z_c = \frac{Z_1 \cdot Z_f}{Z_1 + Z_f}$$

the voltage between the inputs is kept at zero and no output voltage is exhibited. However, in practice i_{d1} and i_{d2} have different values, and i_{dd} $(i_{dd} = i_{d1} - i_{d2})$ is defined as the differential input current or offset current, being 5 nA max. for the DOA42. The amplifier used in the circuit of Fig. 12.11 with $Z_f = 50$ kΩ and $Z_c = Z_1 Z_f/(Z_1 + Z_f)$ yields an output voltage of $5.10^{-9} \times 50.10^3 = 0.25$ mV max., an improvement by a factor of 4.

The bias current to each terminal can be adjusted to zero by applying a compensating current from an external current source as shown in Fig. 12.12 (Figs. 12a and 12b show the bias currents for the negative and positive input terminals respectively). The potentiometer is adjusted so that the output voltage of the amplifier is zero, i.e. the current through the 15 MΩ resistor is made equal to the bias current. After adjustment the 10 MΩ resistor should be removed. The values given are valid for the compensation of bias currents for the DOA40. For the DOA42 the resistor of 15 MΩ and 10 MΩ should be replaced by 150 MΩ and 100 MΩ respectively.

Fig. 12.12(a). Bias current compensation (−in terminal).

Fig. 12.12(b). Bias current compensation (+in terminal).

One has to take into account that the bias current drift is only compensated for one temperature, so the current drift data is similar to the uncompensated one. The bias current and offset current drifts of the DOA42 are 0.5 nA/degC and 0.1 nA/degC respectively. In Fig. 12.13 a method is given to reduce the bias current as well as the bias current drift for the DOA40. The dual transistor BCY87 is connected as an emitter-follower and reduces the input current to 60 nA max. and the offset current to 6 nA max., with typical drifts of 0.25 nA/degC and 0.1 nA/degC respectively. Another advantage of this circuit is the high differential input impedance (10 MΩ min.).

Though the output voltages due to the voltage and current offset can be of either polarity, during initial design they ought to be added to envisage the worst possible case.

Fig. 12.13. Bias current reduction.

12.8 Frequency Response and Stability

12.8.1 OPEN-LOOP GAIN

For stable operation using all kinds of feedback it is imperative that the phase shift of the amplifier between the negative input and output never becomes zero while the open-loop gain exceeds unity. Therefore, most amplifiers are given one single (forced) frequency roll-off of 6 dB/octave which results in a maximum phase shift of 90° (see Figs. 12.14a and 12.14b). Fig. 12.14(a) shows the gain-frequency characteristic in which the absolute value of the open-loop gain is plotted in dB's against a logarithmic frequency scale (Bode diagram); f_A is called the roll-off frequency and f_1 the unity gain bandwidth. In general, only the latter is published, and is 9.5 MHz (typ.) for the DOA40 module. In contrast to the DOA40, which has a frequency characteristic approaching 6 dB/

Fig. 12.14(a).
Frequency characteristic.

Fig. 12.14(b).
Phase-shift characteristic.

octave between the frequencies f_A and f_1, the DOA42 is provided with a built-in roll-off network which guarantees stable operation for closed-loop gains of 40 dB and higher. For closed-loop gains lower than 40 dB ($100 \times$) frequency compensating networks have to be connected to the circuit externally. Details of this network are given in Section 11.2.

12.8.2 CLOSED-LOOP GAIN

It is interesting to note the frequency response of a closed-loop system. As an example, the circuit of Fig. 12.2 is used, where Z_1 and Z_f are assumed to be purely resistive (R_1 and R_f resp.). The A_{cl}/frequency curve is indicated by the broken line in Fig. 12.14(a), A_{cl} being approx. R_f/R_1. The curve is a straight line up to the frequency f_{cl} where the closed-loop gain curve intercepts the open-loop gain curve and then follows the latter. The value of f_{cl} can be calculated from the equation:

$$\frac{f_{cl}}{f_1} = \frac{A_{cl}}{A_{ol}}$$

from which:

$$f_{cl} = f_1 \frac{A_{cl}}{A_{ol}}$$

187

For the frequency behaviour of closed-loop systems the following observations may be made:

– As the closed-loop and open-loop gain curves approach the point of intersection, the accuracy of the former is substantially reduced due to a reduction in loop gain (see Fig. 12.14a).

– As a general rule, the circuit is stable if the rate of closure between the open-loop and closed-loop gain curve in less than 12 dB/octave. This is important as some feedback networks exhibit a closed-loop gain which increases with the frequency (e.g. a differentiator, see Section 2.3.6).

– For frequencies in the region of f_1 the gain/frequency curve tends to drop faster than 6 dB/octave and the phase margin is narrowed to less than 90°. In these circumstances external time-constants may lead to instability in closed-loop circuits. Therefore, it is advisable to increase the total external resistance to the positive input (including the source resistance) up to 10 kΩ when the DOA40 is used as follower (see Section 2.3.4).

– Though the 6 dB/octave roll-off ensures good overall stability, it limits the response speed of the circuit. However, in open-loop configurations the phase shift is of minor importance while the speed has to be high; in circuits using the DOA40 this can be used to eliminate the forced roll-off by not connecting terminals 12 and 2.

12.8.3 FULL POWER FREQUENCY

The reader should keep in mind that the open-loop gain/frequency curve, as depicted in Fig. 12.14, holds only for small signals, i.e. up to approx. 10 mV. For higher output voltages the full power frequency, f_{fp}, is defined as being the maximum frequency at which the rated output voltage is still valied. For the DOA40 and DOA42 modules the full power frequency is 40 kHz at a rated output voltage of 20 V peak-to-peak.

12.8.4 SLEWING RATE

The way in which an operational amplifier responds to a step function is called the slewing rate; this is defined as the output voltage change per

188

unit time in response to a step function applied to the input. Full power frequency and slewing rate can be related to each other according to the following equation, which is valid for most amplifiers:

$$\frac{\mathrm{d}V_o}{\mathrm{d}t} = V_o 2\pi f_{fp} \text{ volts/second.}$$

where V_o is the output voltage rating (10 V).
The slewing rate of the DOA40 and DOA42 is 2.5 V/μs.

12.9 Noise

With the exceptions of outputs due to offset and temperature drift, any unwanted or spurious output signal not correlated to the input signal is considered as noise.

Though drift might be considered as noise at very low frequencies, the term noise will be reserved for higher frequency signals. Noise can be represented as a voltage and current source at the input of the operational amplifier and can be dealt with according to the methods applicable to the offset voltage and current sources given in Section 12.7.

The noise voltage of the DOA40 is 3 μV r.m.s. for the frequency range from 16 Hz to 16 kHz. In the main this is thermal noise, which is generated in any (semi)-conductor. For this type of noise the equivalent r.m.s. noise voltage source is given by the formula:

$$E_n = \sqrt{4 \cdot F_n \cdot k \cdot T \cdot \Delta f \cdot R_s} \qquad (k = \text{Boltzmanns constant,}$$
$$F_n = \text{noise factor})$$

From this equation one may conclude that for a low value of E_n a small bandwidth Δf and a low source resistance R_s must be chosen. With a feedback network resistance of R_f, the E_n can be kept low by connecting a capacitor C_f between the negative input and output terminals. The 3 dB down frequency of the closed loop circuit is given by:

$$\frac{1}{2\pi R_f C_f} \text{ Hz.}$$

Another source of noise is pick-up, i.e. interference signals of a well-defined frequency or frequencies. The most common pick-up is a 50 or 60 Hz signal originating from the mains supply. Adequate shielding and l.f. decoupling of the d.c. supply lines are the most satisfactory steps to take in minimizing this type of pick-up.

12.10 Performance Measurements (DOA40)

12.10.1 OPEN-LOOP GAIN

The open-loop gain was determined with the aid of the circuit arrangement of Fig. 12.15, in which the feedback impedance ($Z_f = 100$ kΩ) is much larger than the output impedance ($Z_o = 10$ kΩ); the input signal was a sine wave of 1 V amplitude and 2 Hz frequency. The values of v_2 and v_o were measured and the gain was calculated from the ratio v_o/e_d. Since

$$e_d = v_2/101 \approx v_2/100,$$

$$A = 100 \, v_o/v_2.$$

Substituting measured values of v_o and v_2,

$$A = 100(10/3.55 \times 10^{-3}) = 2.8 \times 10^5.$$

Fig. 12.15. Circuit arrangement for determining open-loop gain A_{ol}.

12.10.2 DIFFERENTIAL INPUT IMPEDANCE

The differential input impedance Z_{id} was determined using the circuit shown in Fig. 12.16. The input was a 1 V, 2 Hz signal. Values of v_2 and v_o were measured and were 5.3 mV and 10 V respectively. The voltage across Z_{id} is equal to v_o/A, and e_d' equals $v_2/100$; therefore, knowing the open-loop gain, the value of Z_{id} can be calculated from:

$$Z_{id} = \frac{v_o/A}{v_2/100 - v_o/A} \cdot R_s,$$

Fig. 12.16. Circuit arrangement for determining the differential input impedance Z_{id}.

in which R_s represents the resistance in series with the amplifier input terminals and amounts to 54 kΩ. For the measured values of v_o, v_2 and A, this gives:

$$Z_{id} = 113 \text{ k}\Omega.$$

12.10.3 Common Mode Input Impedance

The common input impedance Z_{cm} was determined by applying a 10 V peak-to-peak, 2 Hz signal to the follower circuit of Fig. 12.17. Initially R_1 was short-circuited and the value of v_o measured; the value of R_1 was then increased until v_o dropped to 90 % of its original value. This occurred at $R_1 = 3.3$ MΩ, giving:

$$Z_{cm} = 9R_1 = 9 \times 3.3 \times 10^6 = 30 \text{ M}\Omega.$$

Fig. 12.17. Follower circuit used for determining the common mode input impedance Z_{cm}.

12.10.4 Output Impedance

The output impedance Z_o was determined with the aid of the circuit used for measuring the open-loop gain (Fig. 12.15); the input was a 1 V, 2 Hz

signal. With an external load Z_L of 10 kΩ connected to the output, the gain A' dropped to 2.1×10^5, giving:

$$Z_o = (A/A' - 1)Z_L$$
$$= (2.8 \times 10^5/2.1 \times 10^5 - 1)10 \times 10^3 = 3.5 \text{ k}\Omega.$$

12.10.5 UNITY-GAIN BANDWIDTH

The frequency at which gain dropped to unity, the unity-gain bandwidth f_1, was measured using the circuit shown in Fig. 12.18. The frequency of a 10 mV input signal was increased until the output signal dropped to the same amplitude as the input; this occurred at:

$$f_1 = 9.6 \text{ MHz}.$$

12.10.6 FULL-POWER FREQUENCY

The circuit shown in Fig. 12.18 was also used to determine the full power frequency f_{opt}. Initially the amplitude of the input voltage was adjusted until the output voltage had reached a peak-to-peak value of 20 V; the frequency of the input signal was then increased until distortion became noticeable; this occurred at:

$$f_{opt} = 50 \text{ kHz}.$$

Repeating the measurement with the output voltage increased to 26 V peak-to-peak, the corresponding full power frequency was reduced to:

$$f_{opt} = 35 \text{ kHz}.$$

Fig. 12.18. Circuit for determining the unity gain bandwidth and full power frequency. The frequency of v_1 is continuously variable.

12.10.7 SLEWING RATE

The slewing rate was measured using the circuit shown in Fig. 12.19. With the output voltage displayed on an oscilloscope, a 10 V step was applied to the input. The duration of the resulting output ramp was found to be $t = 3.3$ μs, indicating a mean slewing rate of:

$$v_o/t = v_1/t = 3 \text{ V/}\mu\text{s}.$$

Fig. 12.19. Circuit for determining the maximum slewing rate: v_1 is a 10 V step.

12.10.8 CURRENT DRIFT AND OFFSET CURRENT

The offset current, temperature-dependent current drift and differential current drift were found using the circuit shown in Fig. 12.20. The output voltage, measured at an ambient temperature T_{amb} of 26 °C with switch S_1 closed, was 3 V, corresponding to an offset current of:

$$I_{off} = v_o/R_f = 3/10^7 = 300 \text{ nA}.$$

With the ambient temperature at 65 °C, the output voltage was found to be 2.3 V, corresponding to a decrease in offset current of 70 nA, indicating the following temperature-dependent current drift:

$$i_d = \Delta I_{off}/\Delta T = 70/(65 - 26) = 1.8 \text{ nA/deg.C.}$$

The differential current drift i_{dd}, measured in the same way but with switch S open, was found to be 0.24 nA/deg.C.

Fig. 12.20. Circuit for measuring the offset current, temperature-dependent current drift (both with S_1 closed) and differential current drift (S_1 open).

12.10.9 OFFSET VOLTAGE DRIFT AND NOISE

The temperature-dependent offset voltage drift was investigated using the circuit shown in Fig. 12.21. At an ambient temperature of about 25 °C the offset voltage V_{off} was first reduced to zero; then the temperature was raised to 65 °C and the change in output voltage measured. This was found to be $\Delta V_o = 78$ mV, indicating an offset voltage

$$V_{off} = \Delta V_o/G = 78 \times 10^{-6} = 78\ \mu V,$$

corresponding to a drift of:

$$v_d = \Delta V_{off}/\Delta T = 78 \times 10^{-6}/(65 - 25) = 1.9\ \mu V/\text{deg.C.}$$

By displaying the output on an oscilloscope, the circuit of Fig. 12.21 was also used to determine the noise voltage V_{noise}. At 90 % of the peak-to-peak value, the output voltage v_o was 10 mV, corresponding to the following noise voltage referred to the input:

$$V_{noise} = v_o R_1/R_f = 10^{-2} \times 10^2/10^5 = 10\ \mu V.$$

Fig. 12.21. Circuit for measuring noise and offset voltage drift, and the dependence of offset voltage on supply voltage.

12.10.10 INFLUENCE OF LOAD CURRENT

The influence of the load current i_L on the output voltage v_o was investigated using the circuit shown in Fig. 12.22. The variable resistor R_L was used to increase the value of i_L until the output voltage showed noticeable distortion. The procedure was repeated for several values of input voltage, the corresponding values of i_L and v_o then being plotted against each other to obtain the graph of Fig. 12.23.

12.10.11 COMMON MODE REJECTION RATIO

The common mode rejection ratio F was determined using the circuit shown in Fig. 12.24. With an input signal of 5 V amplitude at 2 Hz, the amplitude of the output voltage v_o was found to be 11.5 V, the common mode rejection ratio thus being:

$$F = A\, v_1/v_o = 2.8 \times 10^5 \times 5/11.5 = 120\,000.$$

194

Fig. 12.22. Circuit for determining the influence of the load current on the output voltage of the amplifier.

Fig. 12.23. Load current plotted as a function of the output voltage.

Fig. 12.24. Circuit for measuring common mode rejection ratio.

To measure the dependence of the offset voltage V_{off} on the supply voltages the circuit of Fig. 12.21 was used. The output voltage v_o was first adjusted to zero at the nominal supply voltages, then a programme of changes was made in the supply voltage and the corresponding input voltage offsets were measured. The table below gives the absolute and relative values thus determined, the latter being referred to the supply voltage variation.

relative variation of supply voltages		resulting offset voltage variation	
$\pm V_b$	$-V_b$	absolute	relative
0	$+10\%$	$+13\ \mu V$	$8.50\ \mu V/V$
0	-10%	$-16\ \mu V$	$10.50\ \mu V/V$
$+10\%$	0	$-14\ \mu V$	$9.50\ \mu V/V$
-10%	0	$+16\ \mu V$	$10.50\ \mu V/V$
$+10\%$	-10%	$-28\ \mu V$	$18.50\ \mu V/V$
-10%	-10%	$-1\ \mu V$	$0.67\ \mu V/V$
$+10\%$	$+10\%$	$-1\ \mu V$	$0.67\ \mu V/V$
-10%	-10%	$+29\ \mu V$	$19.50\ \mu V/V$

Apparatus for measuring the flatness of semiconductor material surfaces.

Stirling engine with generator to demonstrate its multi-fuel capacity. Power: 10 hp; speed: 3000 rpm; fuels: alcohol; various lead-containing gasolines; diesel, lubricating, olive, salad and crude oils; propane, butane and natural gas.

199

Technology relating to the products described in this publication is shared by the following firms.

Argentina
FAPESA I.y.C.
Melincué 2594
Tel. 50-9941/8155
BUENOS AIRES

Australia
Philips Electrical Pty. Ltd.
Miniwatt Electronics Division
20, Herbert St.
Tel. 43-2171
ARTARMON, N.S.W.

Austria
WIVEG
Prinz Eugenstrasse 32
Tel. 65 16 21
1041 WIEN

Belgium
M.B.L.E.
80, rue des Deux Gares
Tel. 23 00 00
1070 BRUXELLES

Brazil
IBRAPE S.A.
Rua Manoel Ramos Paiva 506
Tel. 93-5141
SAO PAULO

Canada
Philips Electron Devices
116 Vanderhoof Ave.
Tel. 425-5161
TORONTO 17, Ontario

Chile
Philips Chilena S.A.
Av. Santa Maria 0760
Tel. 39 40 01
SANTIAGO

Columbia
SADAPE S.A.
Calle 19, No. 5-51
Tel. 422-175
BOGOTA D.E. 1

Denmark
Miniwatt A/S
Emdrupvej 115
Tel. 69 16 22
KØBENHAVN NV

Finland
Oy Philips A.B.
Elcoma Division
Kaivokatu 8
Tel. 10 915
HELSINKI 10

France
R.T.C.
La Radiotechnique-Compelec
Avenue Ledru Rollin 130
Tel. 797-99-30
PARIS 11

Germany
VALVO G.m.b.H.
Valvo Haus
Burchardstrasse 19
Tel. (0411) 33 91 31
2 HAMBURG 1

Greece
Philips S.A. Hellénique
Elcoma Division
52, Av. Syngrou
ATHENES

Hong Kong
Philips Hong Kong Ltd.
Components Dept.
St. George's Building, 21st Fl.
Tel. K-42 82 05
HONG KONG

India
INBELEC Div. of
Philips India Ltd.
Band Box Building
254-D, Dr. Annie Besant Road
Tel. 45 33 86
Worli, BOMBAY 18 (WB)

Indonesia
P.T. Philips-Ralin Electronics
Elcoma Division
Djalan Gadjah Mada 18
Tel. 44 163
DJAKARTA

Ireland
Philips Electrical (Ireland) Pty.
Newstead, Clonskeagh
Tel. 69 33 55
DUBLIN 6

Italy
Philips S.p.A.
Sezione Elcoma
Piazza IV Novembre 3
Tel. 69.94
MILANO

Japan
I.D.C.C. Ltd.
Kokusai Building, 7th floor
Marunouchi
Tel. (213) 6751.7
TOKYO

Mexico
Electrónica, S.A. de C.V.
Varsovia No. 36
Tel. 5-33-11-80
MEXICO 6, D.F.

Netherlands
Philips Nederland N.V.
Afd. Elonco
Boschdijk, VB
Tel. (040) 43 33 33
EINDHOVEN

New Zealand
EDAC Ltd.
70-72 Kingsford Smith Street
Tel. 873 159
WELLINGTON

Norway
Electronica A/S
Middelthunsgate 27
Tel. 46 39 70
OSLO 3

Peru
CADESA
Av. Abancay 1176
Tel. 7 73 17
LIMA

Portugal
Philips Portuguesa S.A.R.L.
Rua Joaquim Antonio de Aguiar 66
Tel. 68 31 21/9
LISBOA

South Africa
EDAC (Pty) Ltd.
South Park Lane
New Doornfontein
Tel. 24/6701-2
JOHANNESBURG

Spain
COPRESA S.A.
Balmes 22
Tel. 2 32 03 00
BARCELONA 7

Sweden
ELCOMA A.B.
Lidingövägen 50
Tel. 08/67 97 80
10250 STOCKHOLM 27

Switzerland
Philips A.G.
Edenstrasse 20
Tel. 051/44 22 11
CH-8027 ZUERICH

Taiwan
Philips Taiwan Ltd.
Plastic Building, 10th Fl.
No. 1, section 2, Nanking East Rd.
Tel. 55 97 42
TAIPEI

Turkey
Türk Philips Ticaret A.S.
EMET Department
Gümüssuyu Cad. 78-80
Tel. 45.32.50
Beyoglü, ISTANBUL

United Kingdom
Mullard Ltd.
Industrial Electronic Controls Div.
Manor Royal
Tel. 0293-28787
CRAWLEY

202

United States
Mullard, Inc.
100 Finn Court
Tel. (516) 694-8989
FARMINGDALE
Long Island, N.Y. 11735

Uruguay
Luzilectron S.A.
Rondeau 1567, piso 5
Tel. 9 43 21
MONTEVIDEO

Venezuela
C.A. Philips Venezolana
Elcoma Department
Colinas de Belle Monte
Tel. 72.01.51
CARACAS