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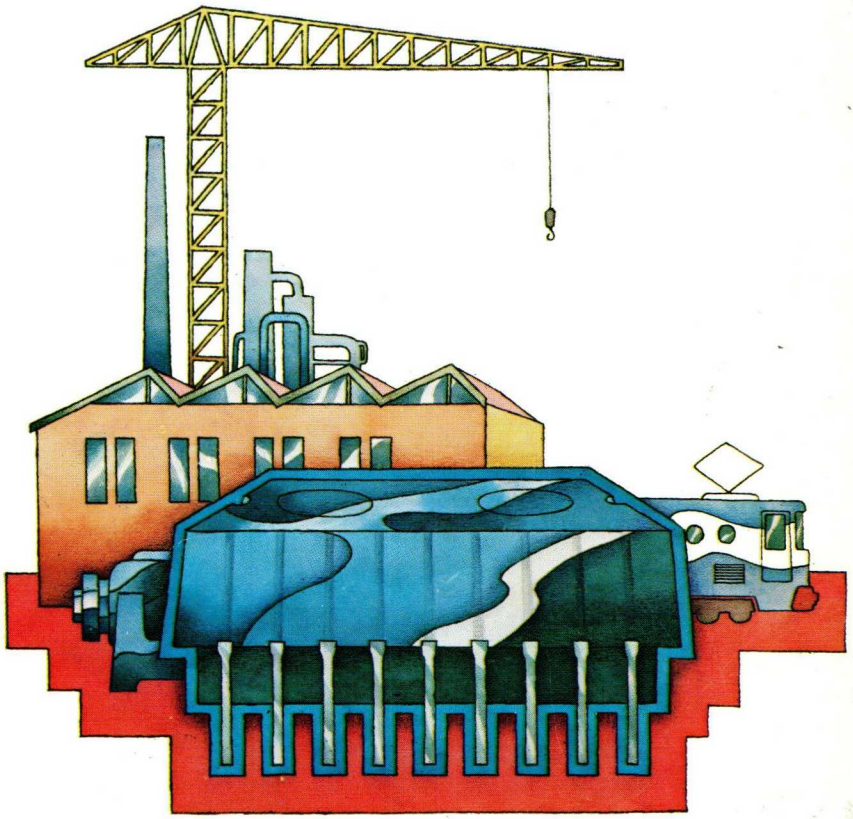
Thyristor and triac power control using 61-series modules



ERRATUM

The formula near the bottom of p. 125 should read:

$$k = \overline{\overline{p} + r + y + b}.$$

Thyristor and Triac Power Control using 61-Series Modules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Thyristor and Triac Power Control using 61-Series Modules

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Elcoma Publications Department Eindhoven

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Contents

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H.K.

Preface

Often mistakenly regarded as mere replacements for mechanical switches or gas-filled tubes, thyristors and triacs have not yet been on the scene long enough for all of their many advantages to be fully appreciated, much less exploited. In that sense they must still be regarded, if not as neglected, at least as under-employed members of the semiconductor family. To help remedy that situation this book attempts to acquaint engineers and potential users with some of the many benefits to be gained from intelligent application of the thyristors and triacs nowadays available – and to prepare them to take similar advantage of the more advanced versions now under development when they too become available.

In pursuit of this aim, the line taken is a concrete and practical one, not abstract or theoretical. Specific circuits are described which span the full range of thyristor and triac applications in present-day industrial control. Some are conventional and may already be well known to many readers; others, such as those taking advantage of specific thyristor properties for a.c. motor control, are more advanced and not yet as widely familiar. In choosing the circuits to be discussed it has been necessary to exercise considerable selectivity. In so small a compass it would be impossible to deal with all applications and all of the proven circuits for carrying them out. The criterion for selection has therefore been that the circuits should not only be illustrative of broad classes of applications and the principles underlying them, but that they should also point the way to further development and adaptation, guiding and – it is to be hoped – stimulating the reader to break new ground.

Notwithstanding the variety of circuits and applications discussed, certain basic functions are common to nearly all of them. Moreover, as circuit designers have gained confidence in the versatility of modern semiconductors they have tended to think more in terms of these functions than of the specific circuit configurations and components needed to perform them. It is in recognition of this tendency that the 61-series of circuit modules has been developed. Incorporating as they do all of the commonly required functions, these modules enable the designer to concentrate on system rather than circuit design. Having been developed with an eye to the specific requirements of thyristor and triac control, they provide him with the unequivocal assurance that if the system logic is correct the constituent circuits will unfailingly carry it out.

The scope of this book is necessarily limited to only a fraction of the many applications in which thyristors and triacs have so far proved their value. Moreover, development continues and new areas of application are steadily being opened up. Besides acquainting the reader at least with the broad outlines of the territory already explored, we hope that this book will also give him the confidence to strike out on his own and still further extend that territory.

1. The purpose of the 61-series circuit modules

1.1 Cost reduction — the modular approach

Industrial power control systems are usually assembled by interconnecting a number of basic functions. Most of these functions are simple logic operations using binary arithmetic, but a few are more specialized. When it is necessary to perform standard circuit operations, there are obvious advantages in using standard circuit elements to do the job. The 61 series circuit modules (NORbits) are such standard elements. They are compatible with the earlier 60 series NORbits, and are housed in the same tough packages. They are inexpensive and readily available and, most important for the systems designer, they are tried and tested, with well defined characteristics.

The 61 series of circuit modules has been specifically developed for incorporation in solid state power control systems. To make them suitable for such a demanding application, their design philosophy includes several major objectives. Firstly, and most obviously, the modules must be reliable because they will be used in a variety of hostile environments: noisy electrical supplies, varying temperatures, high humidity, mechanical shock and vibration. Unless the circuits can withstand such conditions they will not do their job properly. Secondly, to take full advantage of the cost-reducing volume production, the performance of each module must be as flexible as possible, and be achievable with the minimum number of peripheral components.

Having established these design principles, how do the 61 series match up to them? To answer this question, a number of basic control functions will be analyzed and compared with the capabilities of the various modules in the range. Following this introductory survey, the full range of blocks will be listed and their functions described.

1.2 Some simple circuits investigated

The following circuits frequently appear in power control and have therefore been chosen for more thorough discussion:

- phase control
- time-proportional control
- automatic temperature control
- inverter control.

1.2.1 Phase control

Fig. 1-1 gives the block diagram of a simple phase control circuit and waveforms illustrating its principle. D.C. or a.c. power control is provided by varying the trigger angle of the thyristor(s) or triac in series with the load. (The triac can only be used to control a.c. power.)

The basic functions distinguished here are: (1) the "trigger source" for bringing the power device into conduction, (2) "phase control" for controlling the trigger angle and thus the power in the load.

The trigger signal should last long enough for the current through the power device to reach latching level (latching current* larger than holding current); otherwise, conduction will not continue after the trigger signal has ceased. This implies that a wide trigger pulse is needed for a very inductive load the current through which rises slowly.

* also called pick-up current.

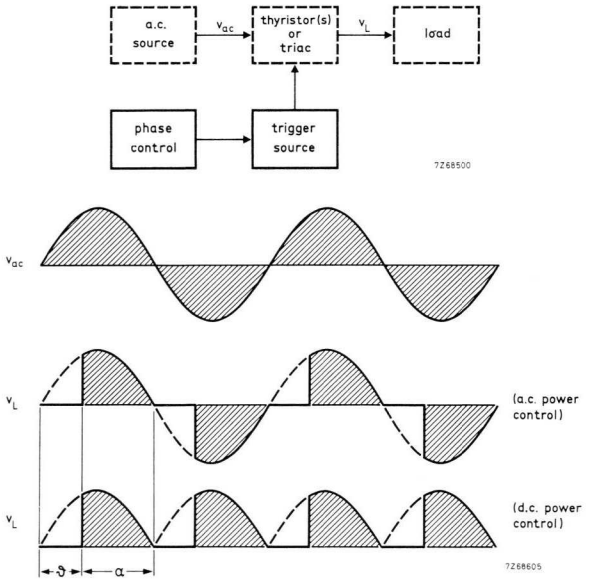


Fig.1-1 Principle of phase control. ϑ = trigger angle; α = conduction angle.

Triggering through a pulse transformer is generally preferred because this isolates the control circuit from the gate input which is live to the mains. However, the necessity for a wide pulse in the case of an inductive load requires the use of a bulky transformer.

The solution is to use trigger pulse bursts rather than single pulses and to connect an RC-series network across the inductive load. During a pulse, a substantial current flows through the power device to charge the capacitor. Between pulses, the capacitor discharges into the inductive load and aids in building up the magnetic field. As a result, turn-on follows after the first few pulses, even if the pulse length is only 20 μs. The time constant of the RC-series network must be of the same order of magnitude as the pulse repetition period, the value of the resistor depending on the holding current of the controlling thyristor. At 10 kHz pulse repetition frequency, 100 Ω in series with 1,5 μF should be satisfactory for most applications.

Thus, one recommended functional element is a *high-frequency trigger transformer*, capable of passing, without significant loss, pulses of 10 μs to 20 μs width. Fig. 1-2 shows the circuit diagram of a transformer triggering two thyristors simultaneously.

Fig.1-2 Trigger transformer circuit.

Fig. 1-3 is one possible trigger pulse generator circuit producing a train of trigger pulses. It consists of charging network R_1C_1, Schmitt trigger ST_1, inverting output amplifier A_1, and regenerative feedback loop D_1R_2. This generator has integrating action, which has the advantage of low susceptibility to interference: a substantial charge must be accumulated on C_1 before the trip-on level of the Schmitt trigger is reached.

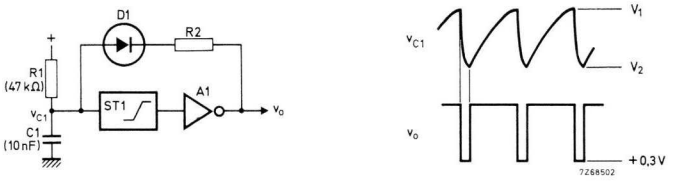


Fig.1-3 Trigger source.

Operation is clear from the waveforms in Fig. 1-3. A continuous charge current is supplied to C_1 via R_1. Each time the voltage on C_1 reaches the trip-on level V_1 of ST_1, the output amplifier is switched into saturation (v_o dropping to about 0,3 V, i.e. saturation level), and the capacitor is abruptly discharged through $D_1 R_2$. As soon as the trip-off level V_2 is reached, the capacitor charges again to repeat the process. Output voltage v_o is applied to the trigger transformer. Pulse width (v_o at +0.3 V) depends on the switching hysteresis $V_1 - V_2$ of ST_1 and on time constant $C_1 R_2$; the pulse interval (v_o high) is determined by the Schmitt trigger hysteresis and $R_1 C_1$.

As seen from Fig. 1-3, the *Schmitt trigger* and the *inverting output amplifier* are the functional elements representing the trigger source. (Components $R_1 D_1 R_2$ are also included in the circuit block.)

The oscillator circuit of Fig. 1-3 produces a continuous pulse train because C_1 is continuously supplied with charge current. This would give uninterrupted conduction of the thyristors. To make phase control possible, synchronization with the mains must be provided, and the complete circuit is shown in Fig. 1-4. Because of the linear sawtooth voltage occurring across C_2, *linear phase control* (by change of V_{contr}) is achieved.

Network $R_3 C_2$ and emitter follower A_2 form a time base generator whose repetition period is made equal to one-half a.c. cycle by synchronization with the full-wave rectified signal v_{sync}. Capacitor C_2 charges via R_3 but is synchronously discharged each half a.c. cycle by v_{sync} through the base-collector diode D_2 of emitter follower A_2. (The emitter follower reduces the load on network $R_3 C_2$.) The time base output of A_2 is applied to capacitor C_1, the latter being synchronously discharged via D_3.

Synchronous discharge of the capacitors causes the trigger pulses to terminate before the 180° point, so that no uncontrolled conduction of the thyristors will ensue.

The thyristor conduction angle increases with the control voltage V_{contr} (Fig. 1-4); this is seen as follows. The control voltage creates a bias voltage on C_1 (voltage step in v_{C1}). With V_{contr} zero, no bias voltage exists and the voltage built up across C_1 each half cycle is below the trip-on level of ST_1. As a result, the thyristors will not conduct. With V_{contr} present, trigger pulses are generated (see v_{C1}- and v_o-waveforms) each time v_{C1} exceeds the trip-on level V_1 (V_2 is the trip-off level). The capacitor bias voltage increases with V_{contr}; this advances the start point of the trigger pulses and causes the thyristors to conduct over a

greater angle. Fig. 1-5 illustrates that linear phase control occurs over a large range of thyristor conduction angles.

The phase control circuit of Fig. 1-4 requires the addition of an *emitter follower* to the range of functional elements. Further, a *synchronization circuit* is needed. See the full-wave rectifier circuit of Fig. 1-6. The synchronization voltage must be fairly large because the capacitors in Fig. 1-4 should be discharged close to the end of the half cycle. Linear phase control will then result down to a small conduction angle (about 15° in Fig. 1-5). At 2×20 V a.c. input, the synchronization signal is about 30 V peak.

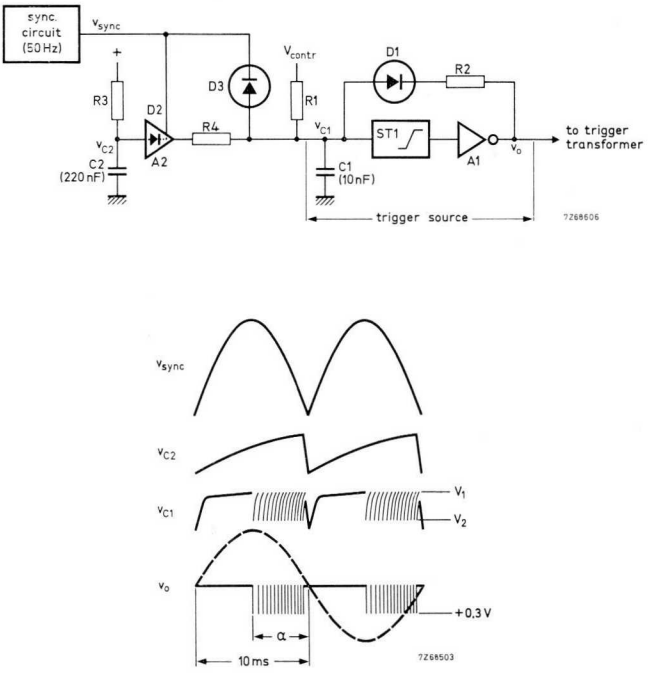


Fig.1-4 Complete circuit giving linear phase control.

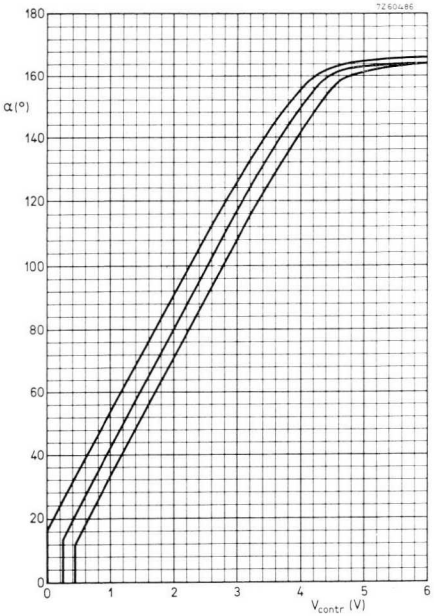


Fig.1-5 Control characteristic of a linear phase control circuit, for three values of the a.c. supply voltage. α = conduction angle.

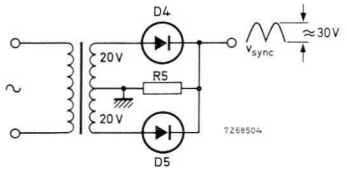


Fig.1-6 Synchronization circuit.

1.2.2 TIME-PROPORTIONAL CONTROL

Fig. 1-7 illustrates the principle of time-proportional control. A triac is shown as the power control element, but a pair of thyristors in anti-parallel could equally well be used. In the graph, t_o is a fixed repetition period, and the triac conduction period t_{on} is equal to a whole number of mains cycles. The average power in the load is proportional to t_{on}/t_o and is varied by changing the length of t_{on}.

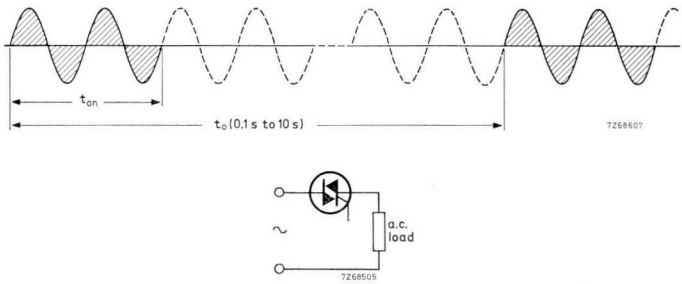


Fig.1-7 Time-proportional control principle.

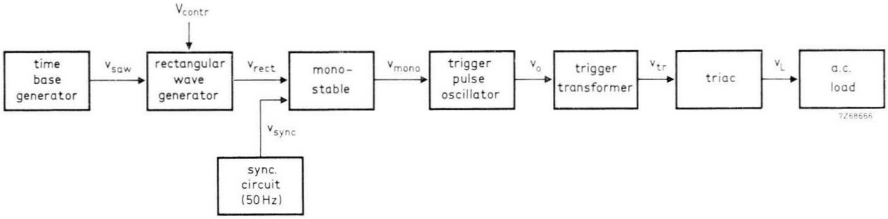
The triac is triggered synchronously with the cross-over points of the mains voltage. This offers the advantages of the highest possible power factor (because a sinusoidal current is drawn from the a.c. input), a low rise rate of thyristor current and absence of radio-frequency interference. A further advantage is that, as distinct from phase control, time-proportional control can be fairly easily linearized.

Time-proportional control is most widely used to control temperature. To avoid temperature fluctuations, t_o must be taken less than one-tenth of the thermal time constant of the controlled process. Time-proportional control combines the simplicity of on/off control and the accuracy of proportional control.

Fig. 1-8 shows one example of a time-proportional control system using a triac. The basic functions are represented by the square blocks. The time base generator produces a sawtooth voltage v_{saw} with a repetition period t_o (see the waveform). The rectangular-wave generator converts this sawtooth into a rectangular

output, whose duty cycle – $(t_o - t_{on})/t_{on}$ – depends on the magnitude of d.c. control voltage V_{contr}. The effect of an increased value of V_{contr} is shown by the dashed portion in the v_{saw}- and v_{rect}-waveshapes.

As seen from the lowermost waveform, which shows load voltage v_L, power is passed to the load (during period t_{on}) as long as v_{rect} is LOW. If δ is the duty cycle of v_{rect}, the average power fed to the load (varied by V_{contr}) is proportional to $1 - \delta$.



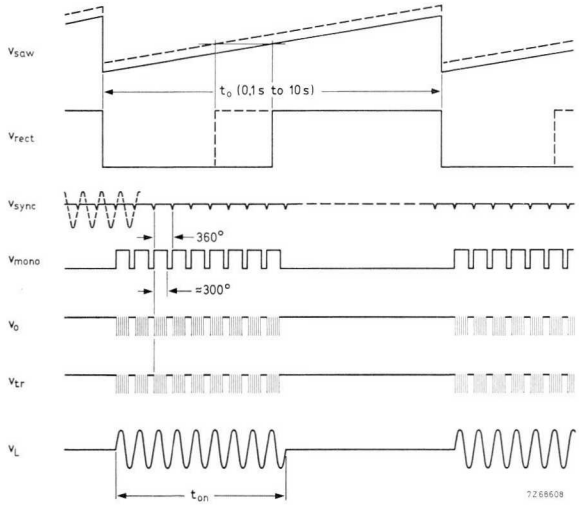


Fig.1-8 Time-proportional control system.

The signal v_{rect} is supplied to a monostable circuit together with v_{sync}, which is a synchronization voltage dropping to zero at the completion of each full a.c. cycle. The monostable can only produce an output pulse (15 ms duration) after a momentary interruption of its total input signal $v_{rect} + v_{sync}$. Consequently, synchronous pulses exciting the trigger pulse oscillator are generated as long as v_{rect} is LOW (see the v_{mono}- waveform).

Circuit operation is further explained by the waveshapes of the trigger pulse oscillator output v_o, the gate signal v_{tr}, and the load voltage v_L. The trigger pulse bursts are made to extend over about 300° for the following reasons: (1) the triac must continue to conduct each second half cycle even with a strongly inductive load; (2) there must be ample margin to prevent triggering of the triac at the beginning of a new mains cycle after v_{rect} has switched to HIGH level. It is thus ensured that *full* load cycles occur.

The basic functions are detailed in Figs 1-9 to 1-15 and will be discussed below.

Fig. 1-9 shows the diagram of the time base generator. Its operation is the same as that of the trigger source in Fig. 1-3 (compare the waveforms in both illustrations). However, the repetition period of this circuit is much longer owing to the larger values of R_1 and C_1. Buffer stage A_1 (high input impedance) is necessary because the value of R_1 is large. The sawtooth period t_o depends on time constant R_1 C_1 and is variable by adjusting R_1.

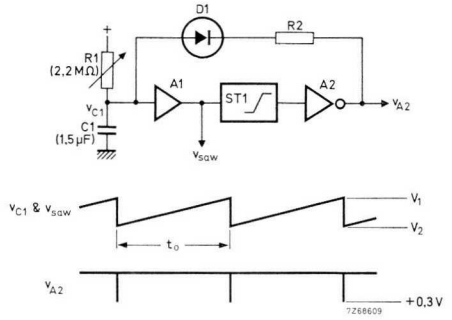


Fig.1-9 Time base generator.

In Fig. 1-10, the time base generator is shown again, but now has the rectangular-wave generator added. The sawtooth voltage v_{saw} is passed through emitter follower A_3 and fed to the input of Schmitt trigger ST_2, together with d.c. control voltage V_{contr}. Since the total input signal v_{in} passes both the trip-on

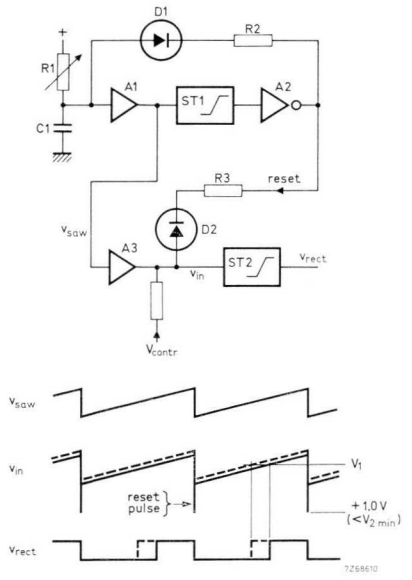


Fig.1-10 Time base generator and rectangular-wave generator.

and trip-off levels V_1 and V_2 of ST_2, a rectangular output v_{rect} occurs. The dotted sections in the waveforms of v_{in} and v_{rect} show the change of these signals due to an increase of V_{contr}.

Because the output of A_2 is LOW (+ 0,3 V saturation level) during the "fly-back" periods of the sawtooth output, this level is used to reset (via D_2R_3) the Schmitt trigger ST_2. The necessity for reset is shown in Fig. 1-11, which gives the time function of v_{in} for the case of V_{contr} gradually increasing. As the illustration shows, the duty cycle of the rectangular output wave v_{rect} increases abruptly to unity (point P) when the minimum value of v_{in} passes the trip-off level V_2 of the Schmitt trigger. This discontinuity in the change of the duty cycle is avoided by reset (see Fig. 1-12). The reset level should, of course, be lower than the expected minimum trip-off level V_{2min} of ST_2.

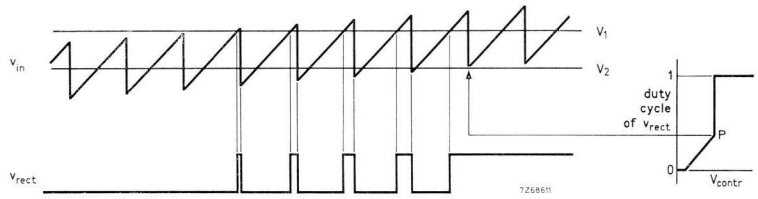


Fig.1-11 Duty-cycle discontinuity.

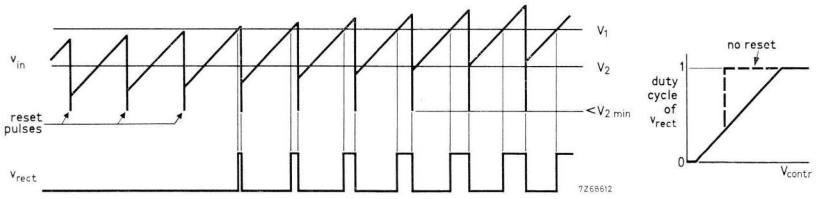


Fig.1-12 Effect of reset.

Fig. 1-13 shows the synchronization circuit and illustrates how the rectangular-wave generator output v_{rect} and the synchronization voltage v_{sync} are mixed. With v_{rect} HIGH, base current is continuously supplied (via D_5) to the input of the monostable. As the left-hand portion of the waveshape $v_{rect} + v_{sync}$ shows, the input signal is at a steady + 0,8 V level. For v_{rect} LOW, the situation becomes as follows.

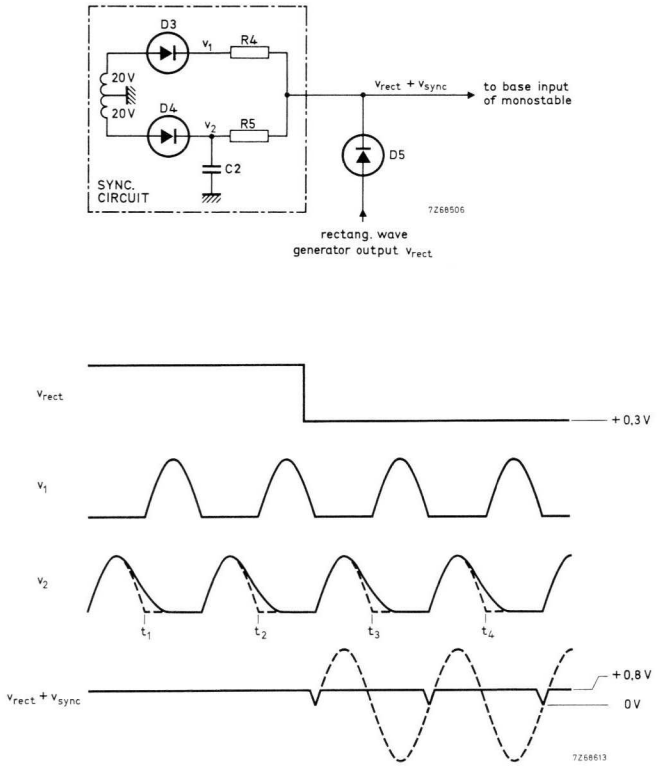


Fig.1-13 Mixing of rectangular and synchronization signals.

A full-wave rectified current is supplied by voltages v_1 and v_2 to the base input of the monostable via R_4 and R_5. However, because the voltage on C_2 has not yet fallen to zero at the end of the half-cycles during which the capacitor is being charged, every alternate zero point in the waveform of rectified current is suppressed (times t_1, t_2, t_3 and t_4). So the zero points are spaced over *full-cycle* intervals, as shown by the right-hand portion of the time function $v_{rect} + v_{sync}$. Diode D_5 prevents the base input from being shorted by the saturated output stage of the rectangular-wave generator. It should be noted that the zero points occur only while v_{rect} is LOW.

Fig. 1-14 shows the circuit of the monostable. With base drive applied (input signal $v_{rect} + v_{sync}$ at + 0,8 V), the output v_{A5} of inverting amplifier A_5 is at saturation level (+ 0,3 V), so C_3 cannot charge. The amplifier is cut off while, at the full-cycle mains zero cross-over points, the base drive is interrupted. Now C_3 charges rapidly through collector resistor R_c and diode D_6.

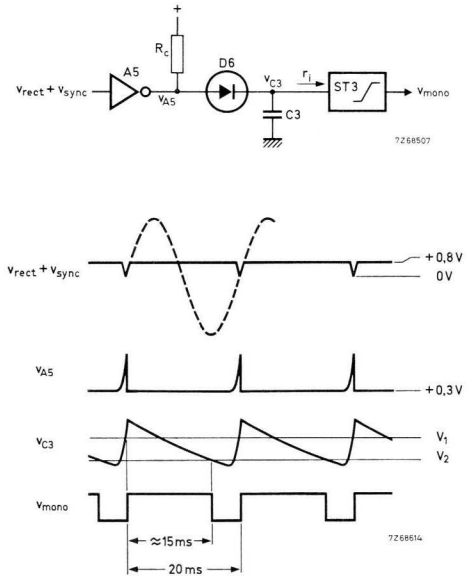


Fig.1-14 Monostable.

During the charging process, the trip-on level V_1 of ST_3 is exceeded (see v_{C3}-waveform) and the monostable output, v_{mono}, is switched HIGH.

When base drive is re-applied, the output of A_5 will collapse. Since the capacitor is prevented (by non-return diode D_6) from discharging into the amplifier output, it will discharge via the input resistance of ST_3. The value of C_3 has been so selected that the trip-off level V_3 is passed about 15 ms after re-application of the base drive. As a result, 15 ms pulses emerge from the monostable output (ref. v_{mono}-waveshape).

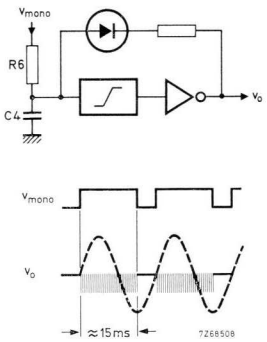


Fig.1-15 Trigger pulse generator.

The monostable output pulses should not extend into the next a.c. cycle. Otherwise the ON-cycles of load voltage would contain an odd number of half mains cycles. This is intolerable for a transformer load because of the d.c. component involved.

The circuit of the trigger pulse generator, given in Fig. 1-15, is the same as that of Fig. 1-3. In this case, however, the charging network R_6C_4 is not supplied from a d.c. voltage but from the monostable output, v_{mono}, which is switched between HIGH and LOW levels. The circuit can only function while C_4 is being charged, that is, with v_{mono} HIGH. Thus, 15 ms pulse bursts are produced starting coincidently with the full-cycle zero cross-over points of the mains input (see the v_o-time function), hence, synchronous triggering occurs.

Summarizing, the application of the functional elements in the circuit, and the number of times each is used, is as follows:

- trigger transformer 1×
- Schmitt trigger 4×
- inverting output amplifier 3×
- emitter follower 2×
- synchronization circuit 1×

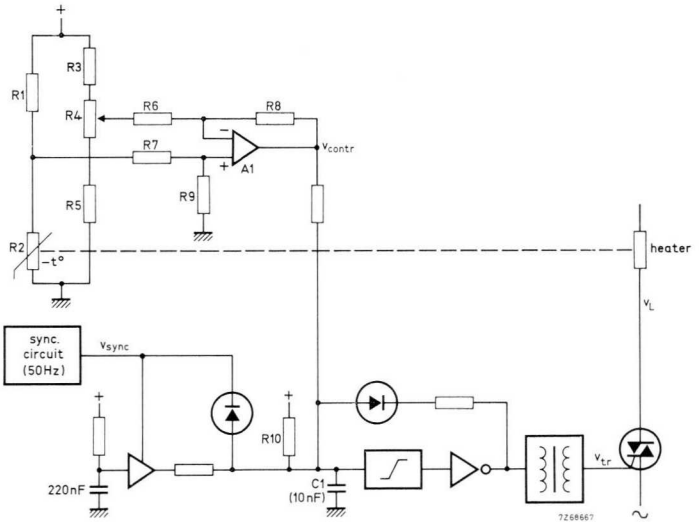
The universality of the functional elements chosen is clearly demonstrated: some element types were used more than once, and no new types had to be added to those proposed in section 1.2.1.

1.2.3 Automatic temperature control

A manually operated control system is made to function automatically by adding a degenerative feedback loop (closed-loop control). In the temperature control system of Fig. 1-16, feedback is introduced by use of NTC thermistor R_2 which senses the controlled temperature. The output of temperature-conscious bridge R_1 to R_5 is fed to error amplifier A_1. The bridge should consist of stable components, so that no drift of controlled temperature occurs.

In Fig. 1-16, the lower part of the diagram represents the phase control and trigger circuit already given in Fig. 1-4. Error amplifier A_1 supplies the control voltage for adjusting the trigger angle of the triac which controls the power to the heater.

The waveforms clarify circuit operation. For a high temperature, NTC thermistor R_2 has a low resistance, therefore, the non-inverting input of error amplifier A_1 is lower in potential than the inverting input. Consequently, the amplifier output v_{contr} is negative, and only a small net current is available so that C_1 charges at a low rate (positive bias current supplied via R_{10}). The triac is triggered late in each half cycle, and its conduction angle is small. There is not enough heater power to maintain the high temperature, and the latter will drop causing the resistance of the NTC thermistor to increase. As a result, the amplifier output v_{contr} increases. Capacitor C_1 receives a higher charging current, the triac is triggered earlier in each half cycle, and more power is delivered to the heater thus reducing the rate at which the temperature drops. A steady



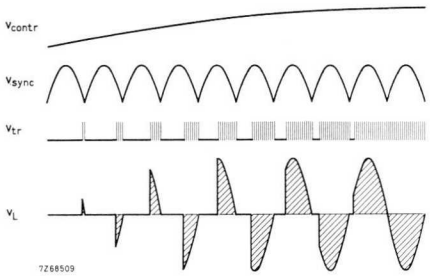


Fig.1-16 Closed-loop temperature control.

working condition is attained for the bridge approaching balance. The value of v_{contr} is then such that the phase angle is maintained at a value for which the heat supplied is equal to the thermal losses (controlled temperature at the desired level).

The differential gain of the error amplifier in Fig. 1-16 is equal to the ratio R_8/R_6 provided that the bridge source resistance is negligible, R_7 is equal to R_6, and R_9 equal to R_8. Owing to the limited gain, a substantial change in input voltage is required for the output voltage to vary between its extreme positive and negative values. The system has, therefore, proportional control properties.

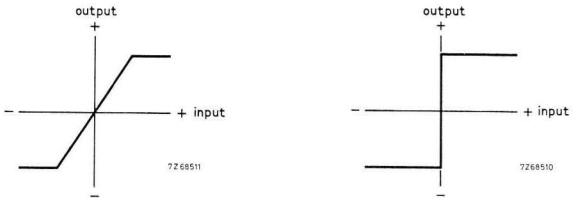


Fig.1-17 Output characteristics of error amplifier (left) and comparator (right).

Removal of feedback resistor R_8 will increase the amplifier gain to the very high open-loop value. The amplifier then functions as a comparator whose output voltage swings between both extreme values for an input voltage change approaching zero, so that the system assumes on/off control properties. Fig. 1-17 illustrates the output characteristics of (a) an error or difference amplifier, (b) a comparator.

It follows that the *operational amplifier* (which can be connected as an error or differential amplifier or as a comparator) is indispensible as a functional element in closed-loop control.

1.2.4 Inverter control

Inverters convert d.c. into a.c. (see Section 4.5). Fig. 1-18 shows a simple inverter control circuit. The variable-frequency pulse oscillator drives the scaler-of-two, which provides voltages v_1 and v_2 as input signals for the trigger pulse oscillators. Each of these oscillators delivers trigger pulses while its input is HIGH.

Owing to the dividing action of the scaler-of-two, the working frequency of the inverter is half that of the variable-frequency pulse oscillator. The trigger outputs v_{tr1} and v_{tr2} are in anti-phase as are v_1 and v_2.

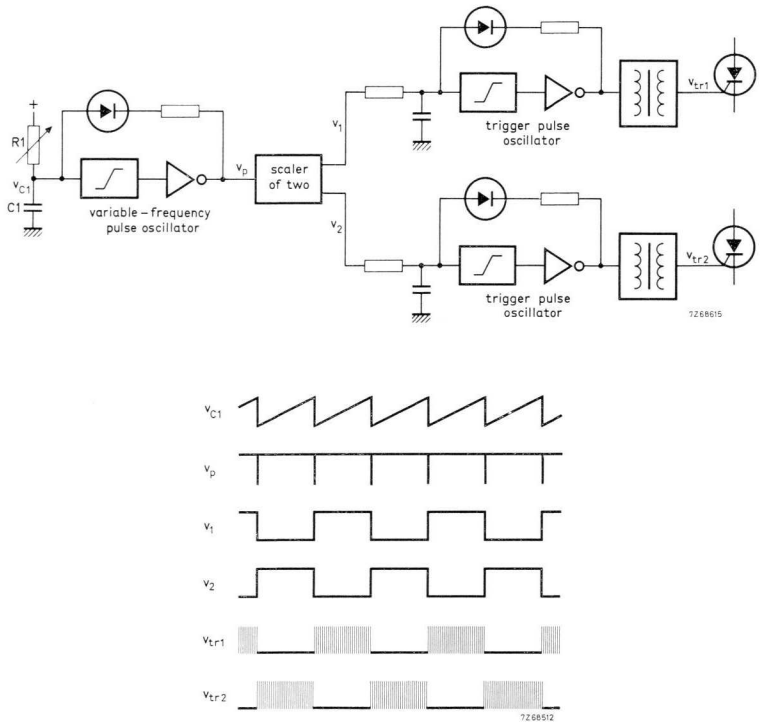


Fig.1-18 Inverter drive.

The d.c. voltage which feeds charging network R_1 C_1 is stabilized to prevent the supply voltage variations from affecting the inverter working frequency.

The new basic function encountered in this circuit is the scaler-of-two. Its operation can be carried out by a bistable circuit which merely consists of two NOR gates connected "head-to-tail". Since many control circuits need *logic functions* (such as welding timers and some motor controls), a circuit block offering these facilities will be useful.

1.3 Properties of the 61-series

We have seen in the foregoing that the functional elements needed for power control are:

- high-frequency trigger transformer
- Schmitt trigger
- inverting output amplifier
- emitter follower
- synchronization circuit
- operational amplifier
- logic functions.

In addition, it is useful to include a *d.c. source* for feeding the circuit modules. Table 1-1 shows how the new 61-series embodies the various functional elements.

Table 1-1. Functions of the new 61-series of circuit modules.

type no.	description	functional elements
RSA61	rectifier and synchronization assembly	D.C. supply, synchronization circuit.
UPA61	universal power amplifier	Schmitt trigger, inverting output amplifier, emitter follower.
DOA61	differential amplifier	operational amplifier.
2.NOR61	dual NOR gate	logic functions.
TT61*	dual trigger transformer	high-frequency trigger transformer.

* Intended for mounting on 0,1-inch pitch p.c. board, or on the UMC60 universal mounting chassis.

The 61-series includes new functions, such as the synchronization circuit and the Schmitt trigger.

As in the case of the 60-series, the modules have a size A transfer-moulded housing containing the components (resistors and semiconductor devices). Fig. 1-19 shows the outline. The pins on both sides of the modules are staggered and their spacing suits mounting on 0,1-inch pitch printed-circuit boards. The end recesses allow nut-and-bolt mounting, for instance, on a UMC60 universal mounting chassis.

Pin numbers are moulded on the top and the bottom of the modules. Probe-guide grooves run down the sides of the blocks to facilitate testing from above. The terminals are suitable for both soldered and wire-wrap connections.

The modules meet the standards laid down in IEC68 and MIT-STD-202C for the following tests: dry heat life, long-term damp heat (not operating and operating), temperature cycling, vibration, shock, robustness of terminations, solderability and solder heat.

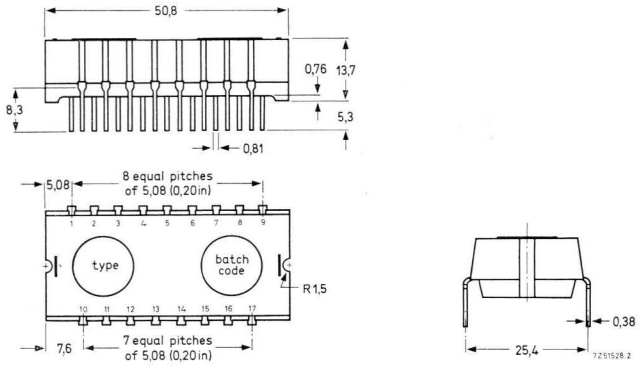
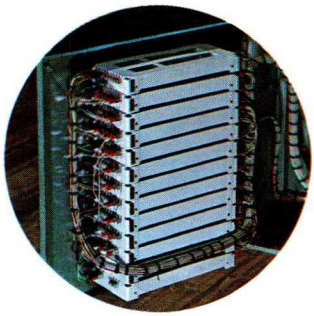
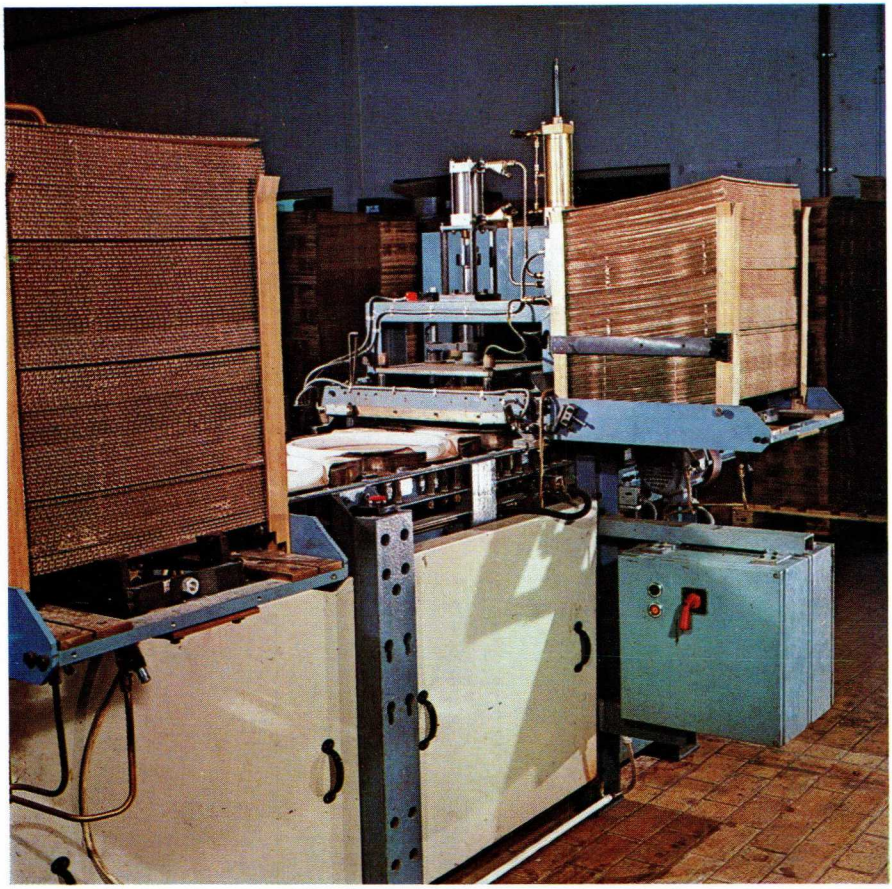


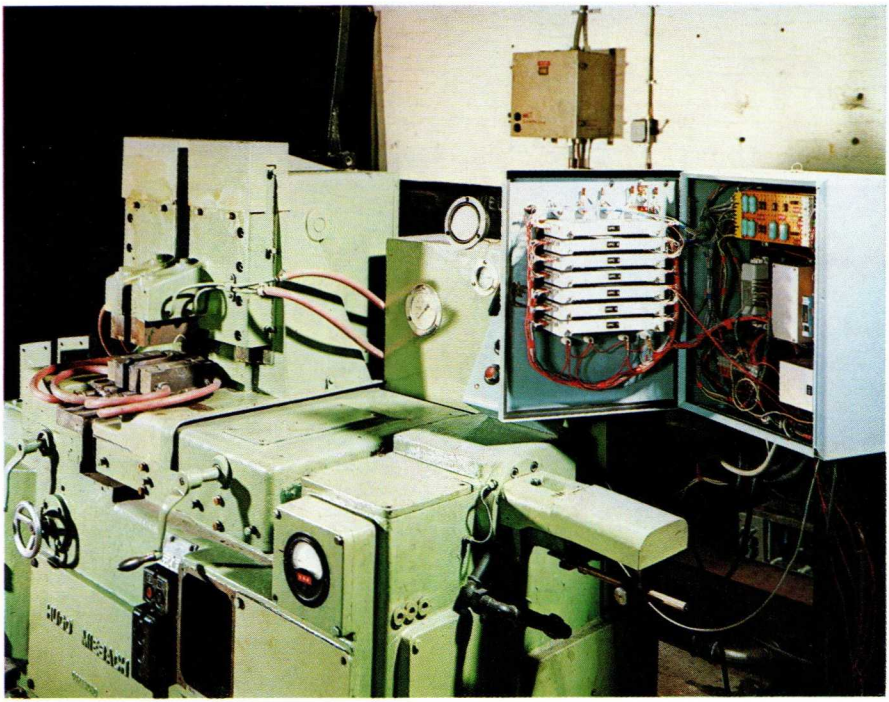
Fig.1-19 Outline of size A circuit module.

Temperature ratings are as follows: storage -40 °C to $+85$ °C, operating -10 °C to $+70$ °C. The modules are intended to work from a supply voltage of 24 V $\pm$ 25%, or 12 V $\pm$ 5%.





Packing machine (lower picture) capable of handling 2100 40-watt fluorescent lamps per hour; defective units are rejected. Control circuit consists of 52 NORbits housed in 13 universal mounting chassis UMC60 (upper picture).



Control desk of automatic chain link welder described in Section 4.8.3. Cabinet (right) houses NORbit control system fitted in seven UMC60 universal mounting chassis.
Courtesy of Kon. Ned. Grofsmederij, Leiden, The Netherlands.

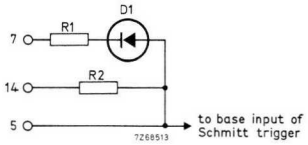


Fig.1-20 Input facilities of Schmitt trigger (UPA61).

The modules have variants of the functions they contain; this leads to increased flexibility and reduces the required number of external components. Figs 1-20 and 1-21 give some examples.

The Schmitt trigger of the UPA61 has a triple input; see Fig. 1-20. There is a diode-and-resistor input (pin 7) providing gating facilities; in the circuits discussed earlier, this input was used as a regenerative feedback path for pulse generation. There is a resistor input (pin 14) providing matching to the output of the circuit blocks. For low-level triggering, input pin 5 should be used.

Fig. 1-21 shows a few variants (with pin numbers) of the UPA61-emitter follower stage; resistors R_3 and R_4 are within the circuit modules. In Fig. 1-21*a*, R_4 is in parallel with R_3, so that more current can be absorbed when the stage acts as a "current sink". Fig. 1-21*b* shows the emitter follower driving subsequent circuitry via a series resistor (R_3); the advantage is that the input resistance of the stage is hardly affected by the load connected to pin 1. In Fig. 1-21*c*, the stage works as an inverting amplifier; feedback (via R_3) has been added in the circuit of Fig. 1-21*d*. Collector resistor R_c is external to the module.

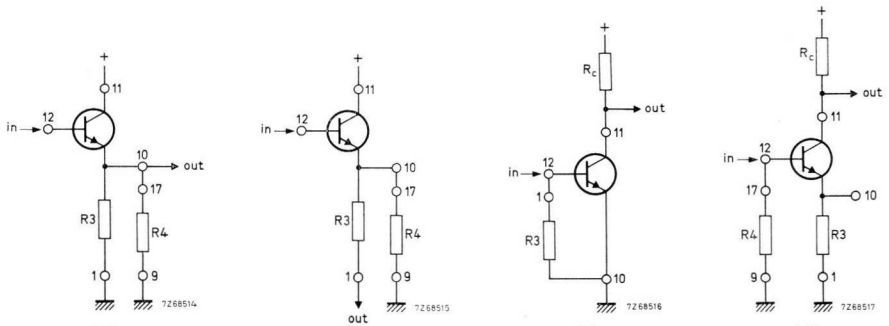


Fig.1-21 Variants of emitter-follower functional element (UPA61).

Likewise, the DOA61 contains resistive networks to form the various circuit configurations associated with operational amplifiers.

To sum up, the benefits of the 61-series are:

- rugged construction and complete sealing of the components, resulting in reliable operation, even in hostile environments
- performance according to the specification ensured under the most diverse operating conditions
- great versatility allowing rapid circuit build-up using a minimum number of peripheral components
- full compatibility with the 60-series of circuit modules and accessories.

2 Detailed description of the circuit modules

2.1 General

This chapter is intended to familiarize the reader with the 61-series NORbits and it gives detailed information as to their properties and discusses their most important applications. Because the TT60 thyristor trigger transformer is an indispensable accessory to the 61-series, its description is also given. Some characteristic data and ratings are included for the purpose of discussion; for full particulars, our Data Handbook System should be consulted and reference made to an earlier publication on the NORbits[1]).

The specified performance of the circuit modules is valid for operation from a d.c. supply voltage of 24 V $\pm$ 25% or 12 V $\pm$ 5%; the DOA61 differential amplifier needs a symmetrical supply and its characteristics are specified for $\pm$ 12 V as well as $\pm$ 15 V.

Under the headings "Functions" appearing in the sections that follow, the purpose of the circuit blocks is outlined.

The 61-series is an extension of the 60-series NORbits, and Table 2-1 gives a survey of the latter.

[1]) Product News, ordering code 9399 263 07601 - 61-series Circuit Modules.

Table 2-1 60-series NORbits.

type no.	description
2.NOR60	dual four-input NOR gate
4.NOR60	quadruple 2 × 2 + 2 × 3 input NOR gate
2.IA60	dual inverter amplifier
2.LPA60	dual low-power amplifier
PA60*	power amplifier
GLD60	grounded load driver
TU60	timer
2.SF60	dual switch filter
HPA60*	high-power amplifier.

* size B circuit module.

2.2 Drive unit

To allow matching between NORbits, the concept of the Drive Unit (D.U.) has been adopted. One D.U. is the drive on one input of a 2.NOR60 or 4.NOR60 stage – with the other input(s) returned to 0 V – which is required to bring the output to LOW level ($\leqslant +0{,}3$ V).

Output capability, also expressed in D.U., denotes the number of 2.NOR60 or 4.NOR60 inputs that can be driven simultaneously from a single output. The fan-out is the ratio of output capability (in D.U.) to the number of D.U. required per input. For instance, the 2.NOR61 has a 10 D.U. output capability at 24 V $\pm$ 25%, and each input needs 2 D.U. Thus, the fan-out is $10/2 = 5$.

Roughly speaking, 100 kΩ input impedance conforms to 1 D.U., 50 kΩ to 2 D.U., 33 kΩ to 3 D.U., etc.

2.3 RSA61 rectifier and synchronization assembly

Functions – +24 V unstabilized supply for NORbits
+12 V and −12 V stabilized supplies for operational amplifiers, e.g. DOA61
−24 V unstabilized supply
mains-synchronization of a zero cross-over switch or a phase control circuit.

Fig. 2-1 is the circuit diagram of the RSA61; the functions of the various diodes are as follows:

D_1 – voltage reference diode; clamping diode
D_2 – clamping diode; gating diode
D_3, D_4 – single-phase half-wave rectifiers; two-phase half-wave rectifier (by joining pins 2 and 3); most common use: synchronization circuit (pins 2 and 3 joined)
D_5 to D_8 – bridge rectifier (input transformer – without centre tap – connected to pins 1 and 10); two-phase half-wave rectifiers (centre-tapped input transformer)
D_9, D_{10} – voltage regulator diodes providing +12 V and −12 V stabilized voltages.

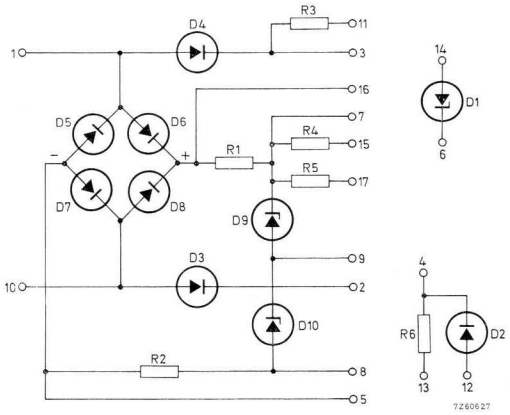


Fig.2-1 RSA61-circuit diagram.

Resistors R_4 and R_5 are used for charging externally connected timing capacitors; one specific application is for time base generation in linear phase control circuits (section 4.4.5).

The RSA61 can be used for delivering positive and negative supply voltages, or only positive supply voltages. These variants will now be discussed.

2.3.1 RSA61 DELIVERING POSITIVE AND NEGATIVE SUPPLY VOLTAGES

In the circuit diagram of Fig. 2-2*a* (Fig. 2-2*b* is the wiring diagram), diodes D_6 D_8 and D_5 D_7 are two-phase half-wave rectifiers giving +24 V and −24 V outputs with respect to pin 9 (transformer centre tap); C_1 and C_2 are smoothing capacitors. Zener stabilized voltages (+12 V and −12 V) are available at pins 7 and 8. To increase the current capability of the −12 V supply, R_6 should be connected in parallel with R_2, as shown dotted in the diagram. The maximum output current available from each output follows from Table 2-2.
Stabilization of the +12 V and −12 V outputs is ensured over the input voltage range of $2\times$ 20 V − 15% to $2\times$20 V + 10%. The rated maximum input voltage is $2\times$22 V. A.C. input current is 375 mA maximum.

An unsmoothed full-wave rectified voltage, commonly used for the synchronization of a phase control circuit or a zero cross-over switch, becomes

available when pins 2 and 3 are interconnected, as shown in Fig. 2-2*a*. The synchronization points are where the voltage drops to zero, which occurs coincidently with the zero cross-over points of the mains voltage. The synchronization voltage can be taken from pin 2 (or 3), using R_3 for termination (pin 11 connected to the 0 V line). Alternatively, the synchronization voltage can be derived from pin 11, using R_3 as the source resistance.

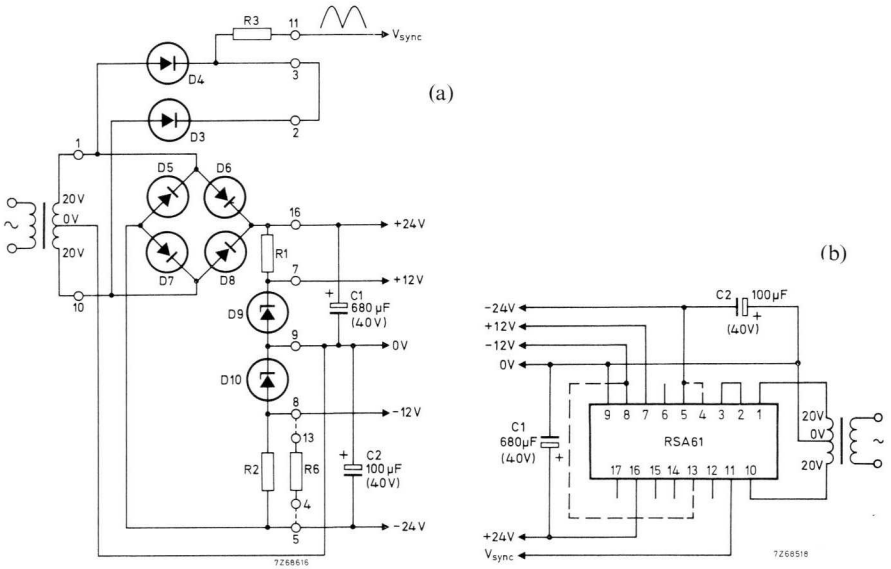


Fig.2-2 RSA61 delivering positive and negative supply voltages: (a) circuit diagram showing essential components only, (b) wiring diagram.

Table 2-2 RSA61-output ratings (Fig. 2-2).

pins	nominal output voltage	max. output current	remarks
16 and 9	+24 V unstabilized	220 mA	—
7 and 9	+12 V stabilized	8 mA	—
8 and 9	—12 V stabilized	4 mA	—
8 and 9	—12 V stabilized	7 mA	pins 8/13 and 4/5 joined
5 and 9	—24 V unstabilized	220 mA	—

2.3.2 RSA61 DELIVERING POSITIVE SUPPLY VOLTAGES ONLY

Fig. 2-3 shows the RSA61-circuit for supplying +24 V (unstabilized) and +12 V (stabilized). The synchronization circuit, not shown here, is the same as that in Fig. 2-2. Table 2-3 gives the output capability.

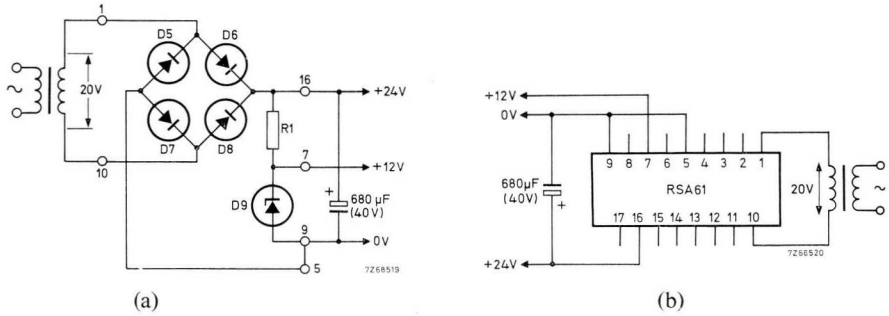


Fig.2-3 RSA61 delivering positive supply voltages only: (a) circuit diagram, (b) wiring diagram.

Table 2-3 RSA61-output ratings (Fig. 2-3).

pins	nominal output voltage	max. output current
16 and 9	+24 V unstabilized	220 mA
7 and 9	+12 V stabilized	8 mA

The nominal a.c. input voltage (betweens pins 1 and 10) must not exceed 20 V; otherwise, if the mains voltage is 10% above nominal, the output voltage at pin 16 will be higher than the permissible maximum supply voltage valid for the NORbits (30 V).

2.4 UPA61 universal power amplifier

Functions – d.c. switching amplifier
pulse generator
phase control circuit
current source.

Fig. 2-4 gives the circuit diagram of the universal power amplifier UPA61. The functions of the circuit sections are given below.

TR_1 – Buffer; driver; inverting stage; current source. Variants of this stage were discussed in section 1.3

TR_2 TR_3 – Schmitt trigger. This circuit has three inputs, and the purpose of each input is described in section 1.3. There are two outputs: a biased output at pin 3, and an unbiased output at pin 13. For logic applications, the low level at pin 3 is too high (about 2,5 V at 12 V d.c. supply and 4,5 V at a 24 V d.c. supply). If the d.c. supply is 24 V $\pm$ 25%, the output at pin 13 can drive:
(a) the UPA61 power stage (TR_4)
(b) up to four stages of a 2.NOR60, 4.NOR60 or 2.NOR61, *two inputs of each stage being connected in parallel.*
NOTE: In case (b), a terminating resistor of say 15 kΩ must be connected between pins 13 and 9. It will then be ensured that the LOW output level does not exceed +0,3 V despite the leakage current of D_2. Alternatively, R_5 can be used (by interconnecting pins 17 and 13)

TR_4 – Inverting power stage. The load is connected in parallel with R_{10} (between pins 8 and 16). Diode D_3 is used as a clamping diode to protect TR_4 against inductive-load surges, for gating, or for level shifting.

The peak output current allowed is 5 A over a 20 ms period, or 2 A over a 20 ms period repeating each second.

Schmitt trigger input sensitivity is according to Table 2-4.

The following sections discuss the various UPA61 arrangements.

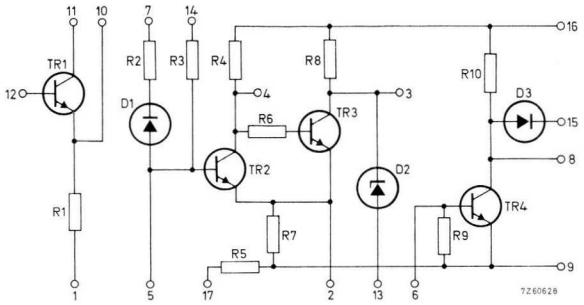


Fig.2-4 UPA61-circuit diagram.

Table 2-4 Schmitt trigger input sensitivity at a 24 V ± 25% d.c. supply.

input drive at pin 14	2 D.U.*
input voltage to switch on load current (trip-on level)	
at pin 5**	$\geqslant$ 8,2 V
at pin 14	$\geqslant$ 11,4 V
input voltage to switch off load current (trip-off level)	
at pin 5*	$\leqslant$ 1,6 V
at pin 14	$\leqslant$ 1,8 V
on/off hysteresis	
at pin 5**	$\leqslant$ 4,8 V
at pin 14	$\leqslant$ 4,9 V

* See section 2.2.

** Drive source resistance $\geqslant$ 2,2 KΩ.

2.4.1 UPA61 SWITCHING A 90Ω LOAD

Fig. 2-5 gives the schematic and wiring diagrams of a circuit in which the UPA61 is used to to switch a load of 90Ω, or more. Because the current gain of the output stage is sufficient, no drive stage is necessary.

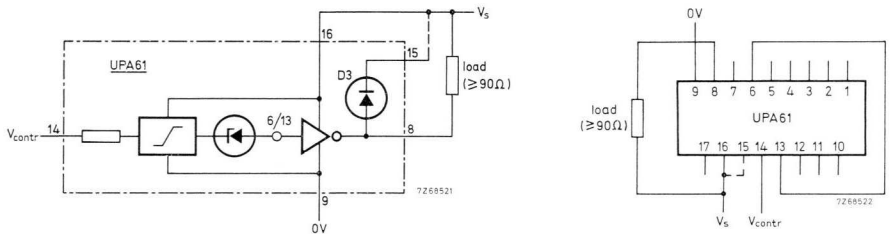
With V_{contr} HIGH (specified to be 11,4 V, or higher), the Schmitt trigger trips on, driving the power stage into saturation (specified output level $\leqslant +0{,}3$ V). When V_{contr} is LOW (specified to be 1,8 V, or lower), the Schmitt trigger trips off, and the power stage is cut off (output level raised to that of the d.c. supply voltage for an unloaded output).

The Schmitt trigger hysteresis (difference between trip-on and trip-off levels) at pin 14 is 4,9 V, or lower, and the prescribed drive is 2 D.U.

In the case of an inductive load, pins 15 and 16 must be interconnected; diode D_3 is then in parallel with the load, thereby protecting the output transistor against voltage surges produced by the load inductance.

At a supply voltage of 24 V $\pm$ 25% d.c., the current consumption is 25 mA plus the d.c. load current.

The inrush current of an incandescent lamp load should be observed. Quiescent current to pre-heat the lamp or current-limiting series resistance must be used if the transistor current rating (5 A during 20 ms) would otherwise be exceeded.



(a) (b)

Fig.2-5 UPA61-circuit switching a load of 90 Ω minimum: (a) circuit diagram, (b) wiring diagram. V_i is the positive supply voltage (24 V $\pm$ 25%).

Fig. 2-6 illustrates the UPA61 output stage driven from a 2.NOR60, 4.NOR60 or 2.NOR61. The 2,7 kΩ collector resistor ensures adequate base-drive at 24 V $\pm$ 25% d.c. supply voltage. Two NOR inputs should be connected in parallel.

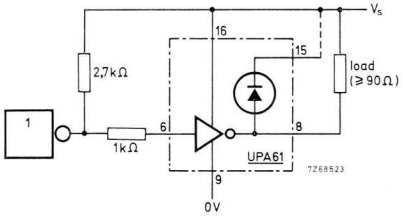


Fig.2-6 2.NOR60, 4.NOR60 or 2.NOR61 driving UPA61 output stage.

2.4.2 UPA61 SWITCHING A 30 Ω LOAD

The circuit illustrated in Fig. 2-7 is for switching a load with a minimum resistance of 30Ω. The drive stage has been added to this circuit so as to increase its overall current gain and thereby provide the necessary increased output

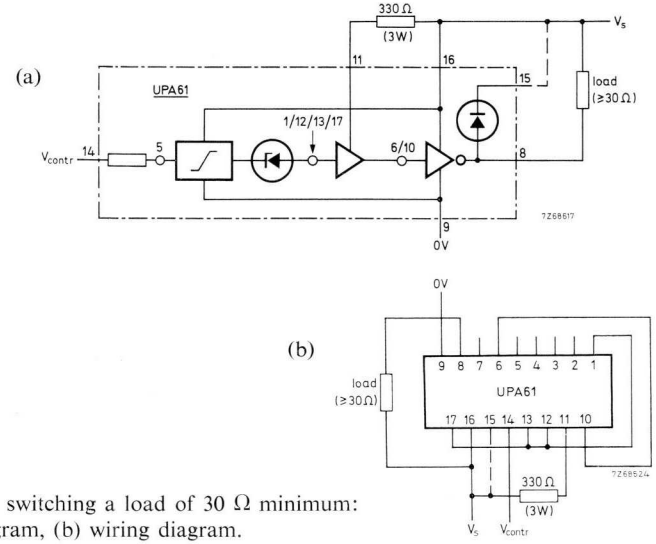


Fig.2-7 UPA61-circuit switching a load of 30 Ω minimum: (a) circuit diagram, (b) wiring diagram.

current capability. As in the circuit discussed previously, the specified output level is equal to +0,3 V (the maximum logic "0" level) or lower.

Pins 15 and 16 must be interconnected if the load is inductive.

With a supply of 24 V d.c. ± 0,25%, the current consumed is 110 mA plus the d.c. load current.

Methods of switching a lamp load are given in the previous section.

2.4.3 UPA61 AS A LOW-POWER PULSE GENERATOR

Where pulses must be delivered to a load (usually a thyristor gate circuit) with a resistance not less than 90Ω, the circuit given in Fig. 2-8 is suitable. The principle of operation of this circuit is discussed in section 1.2.1. The pulse repetition rate is inversely proportional to the value of C_1 and increases with the d.c. control voltage V_{contr}. No pulses occur if V_{contr} is less than the trip-on level of the Schmitt trigger.

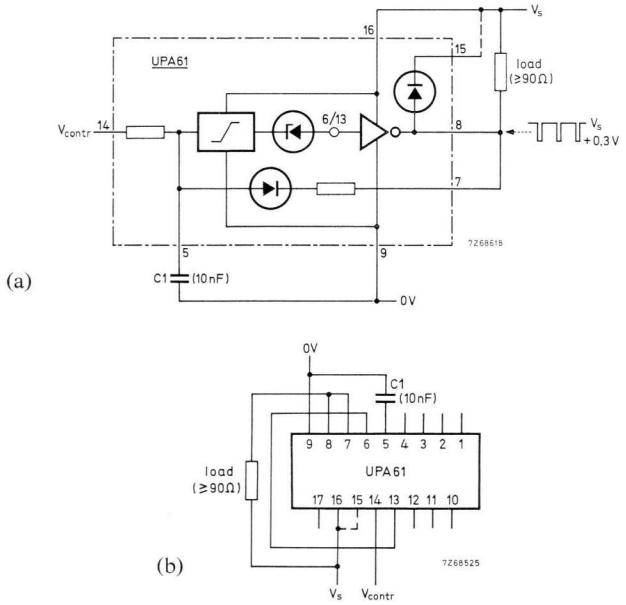


Fig.2-8 UPA61-pulse generator connected to drive a load of minimum 90 Ω: (a) circuit diagram, (b) wiring diagram.

The graphs given in Figs 2-9 and 2-10 show the results of measurements on a a single circuit (24 V d.c. supply voltage). The witdh, Δ, of the negative going output pulses is independent of V_{contr} and, as Fig. 2-10 shows, increases with the value of C_1.

In most cases, C_1 is 10 nF, which, as seen from Fig. 2-10, gives a pulse repetition rate of about 10 kHz and a pulse width of 20 μs.

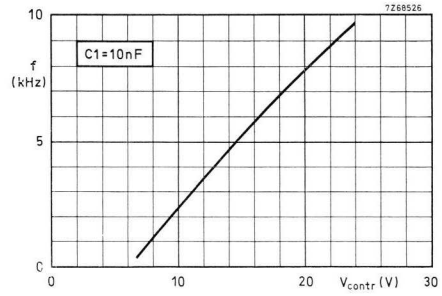


Fig.2-9 Pulse frequency, f, vs. d.c. control voltage, V_{contr}, for 24 V d.c. supply voltage and C_1 equal to 10 nF.

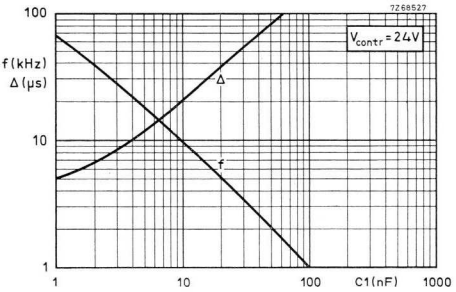


Fig.2-10 Pulse frequency, f, and pulse width, Δ, vs. C_1 for d.c. control voltage V_{contr} and the d.c. supply voltage equal to 24 V.

2.4.4 UPA61 AS A HIGH-POWER PULSE GENERATOR

The UPA61, connected according to Fig. 2-11, functions as a high-power pulse generator capable of supplying a load resistance of not less than 15Ω. This circuit is suitable, for example, for triggering an ignistor*.

Because a high current is drawn by the output transistor, the duty cycle of output current must not exceed 30% (2 A peak output current at 24 V +25%).

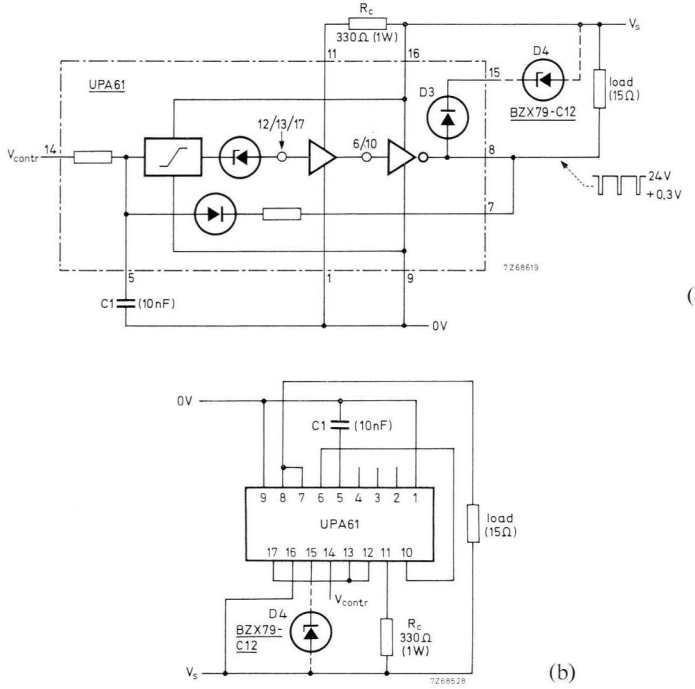


Fig.2-11 UPA61 connected as a 10 kHz pulse generator for driving a 15 Ω load: (a) circuit diagram, (b) wiring diagram.

* An ignistor consists of a pair of high-power, disc-type thyristors connected in anti-parallel and clamped between water-cooled heatsinks. Because of the large wafer area, the power needed for triggering is fairly high.

This duty cycle increases with the control input V_{contr}; also, a low value of C_1 will increase the duty cycle. The duty cycle will not exceed the prescribed maximum at $V_{contr} = 24$ V, when C_1 is 1 nF, or larger, 10 nF being normally used.

Pulse repetition frequency and width are read from the graphs in Figs 2-9 and 2-10.

Because of the high level of switched output current, the load must be shunted by D_3 and D_4 as shown, if it is inductive. During the intervals between pulses, the load inductance will then drive D_4 into breakdown and cause a rapid decay of load current, thereby ensuring that the load current has dropped to zero before the next pulse commences; saturation of the load inductance is thus avoided. Diode D_3 prevents the negative-going output pulses being shorted by D_4.

2.4.5 UPA61 AS AN INVERTED-SAWTOOTH GENERATOR

The UPA61 connected according to Fig. 2-12 functions as an inverted-sawtooth generator operating as follows. Transistor TR_1 receives a constant base drive and, hence, functions as a current source discharging capacitor C_1 at a constant rate. The loss of charge is replenished by repetitive pulses applied to pin 8;

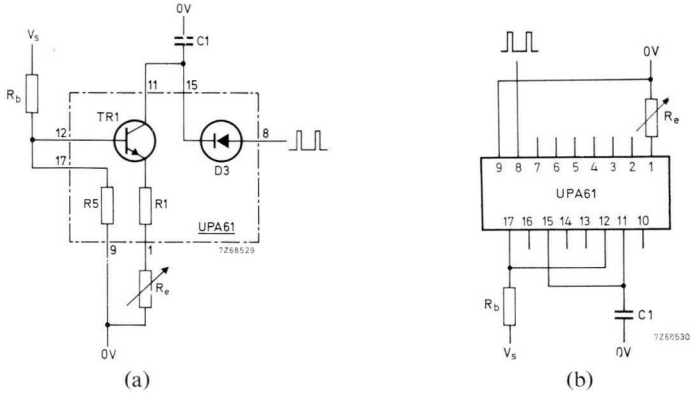


Fig.2-12 UPA61 working as an inverted-sawtooth generator: (a) circuit diagram, (b) wiring diagram.

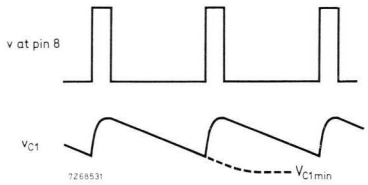


Fig.2-13 Waveforms to Fig.2-12.

diode D_3 prevents the capacitor from discharging into the pulse source. Because of the high charge current, the pulse time required is short. Fig. 2-13 shows the waveforms of the circuit.

Because the capacitor cannot discharge to a lower voltage than approximately that at the base of TR_1, the minimum capacitor voltage:

$$V_{C1\,min} = V_s\, R_5/(R_b + R_5).$$

The discharge rate of the capacitor is determined by the collector current of TR_1. A linear sawtooth is generated provided that C_1 does not discharge to $V_{C1\,min}$; the latter is prevented at any given pulse repetition frequency by adjustment of emitter series resistor R_e.

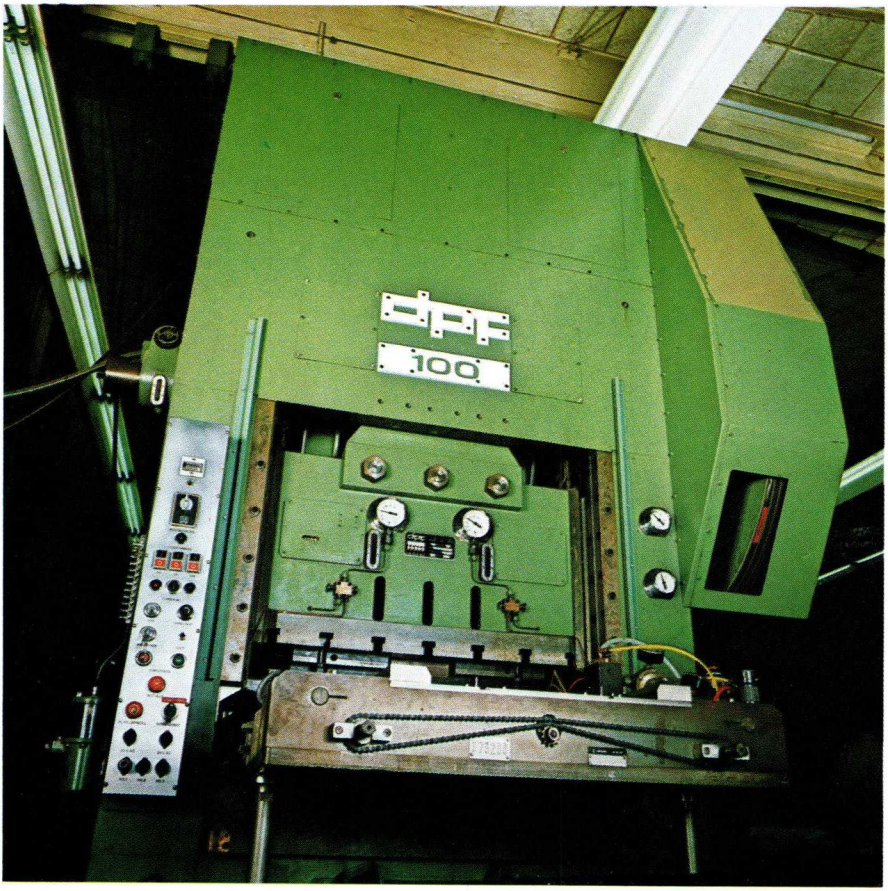
2.5 TT60 and TT61 trigger transformers

The TT60 and TT61 trigger transformers are intended to be driven by a pulse generator (3 kHz to 12 kHz working frequency).

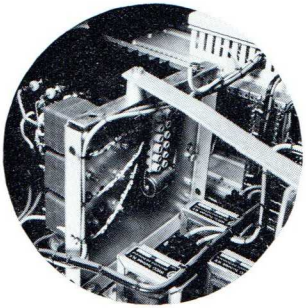
2.5.1 TT60 TRIGGER TRANSFORMER

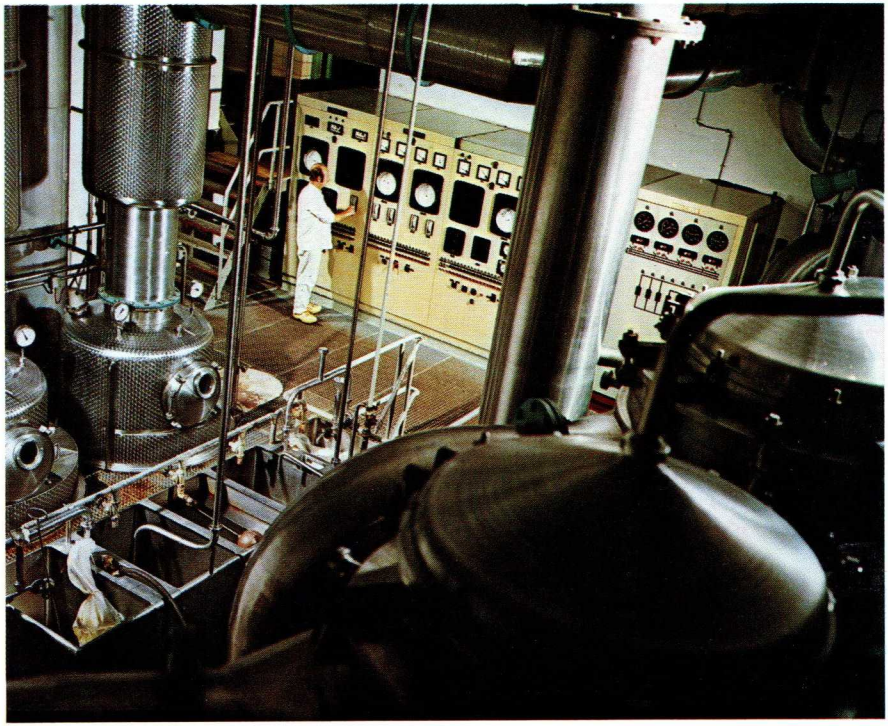
Function – Isolation and matching between pulse generator output and gate circuit.

The TT60 consists of a trigger transformer encapsulated in a mould with a threaded stud for heatsink or stack mounting close to the thyristors; because gate and cathode leads are short, screening is not necessary. A further advantage is that the gate leads, which carry a dangerous voltage, are held outside the low-voltage control section.



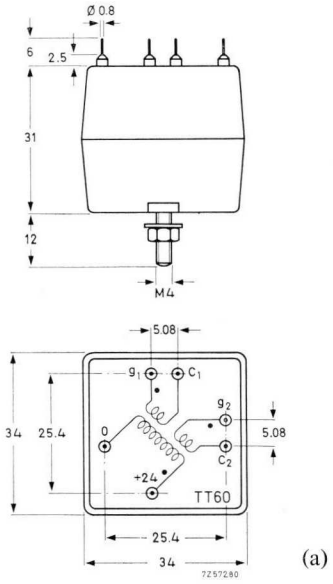
This 100-ton press for p.c. board manufacture is driven by a variable-speed 10 h.p. motor which is supplied from a 12 kVA three-phase inverter of the type described in Section 4.6.3.





This milk powder production plant is controlled by NORbits. Upper picture shows TT60 trigger transformers used for thyristor control.
Courtesy of Messrs. Sasburg, Benningbroek, The Netherlands.

Fig. 2-14 shows the outline and schematic diagram of the TT60; g_1 g_2 are the gate connections and c_1 c_2 are the cathode connections. It is seen that two thyristors can be triggered simultaneously. Turns ratio is 3: (1 + 1), and the secondary windings may be connected in series for powerful triggering. The unit can withstand 5 kV d.c. test voltage (1 minute duration) between any two windings.



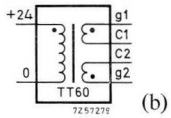


Fig.2-14 TT60 trigger transformer: (a) outline, (b) drawing symbol.

2.5.2 TT61 DUAL TRIGGER TRANSFORMER

Function – Isolation and matching between pulse generator output and gate circuit.

Fig. 2-15 shows the diagram of the TT61 NORbit (outline discussed in section 1.3). The turns ratio of each transformer is 3 : 1. As with the TT60, two thyristors can be triggered simultaneously, or the secondary windings may be connected in series (primaries paralleled) to obtain powerful triggering.

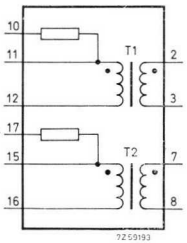


Fig.2-15 Diagram of TT61 NORbit.

The primary windings of the TT61 each incorporate a 82Ω series resistor for current sharing or current limiting. These resistors can withstand 24 V +25% at up to 30% duty cycle. Precautions must be taken to prevent the output transistor of the driving pulse generator from staying in saturation; this would burn out the resistors. If such a condition cannot be avoided, external resistors with adequate power rating must be used.

This trigger transformer can withstand a test voltage of 4 kV d.c. (1 minute duration) between any two windings. It is suitable for mounting either on a p.c. board or on a UMC60 universal mounting chassis.

The following specification applies.

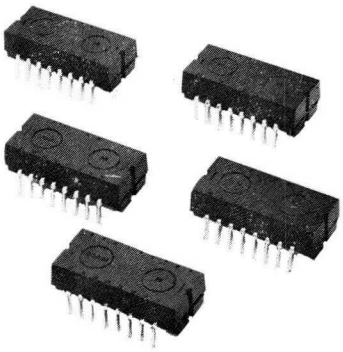
Primary inductance $\geqslant$ 2,2 mH. Primary resistance $\leqslant$ 4Ω. Secondary resistance $\leqslant$ 0,6 Ω. Current rating of primary winding 0,8 A at 1 : 3 duty cycle. Volt-second capability 600 V μs at pins 11,12 or 15,16.

2.6 Trigger source using UPA61, TT60 and TT61

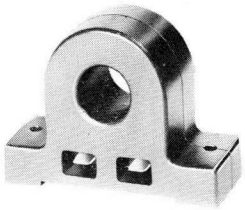
Figs 2-16 and 2-17 illustrate trigger sources using the UPA61 as a pulse source and the TT60 or TT61 for coupling its output to the thyristor or triac gate. Gating (I_G/V_G) characteristics, valid for the specified *minimum* supply voltage (24 V − 25%), are included to show the capabilities of the circuits, which are briefly discussed below.

Fig. 2-16 – This pulse oscillator circuit is the one discussed in Section 2.4.3. The 82Ω resistor is included for current limiting; in the case of the TT61, the internal resistor is used. This circuit can trigger all thyristors except the least sensitive types.

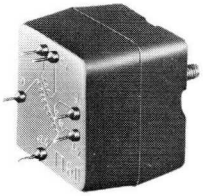
RZ 31051-3



A 55713-1



A 51993



The 61-series circuit modules (above), DCT61 direct current transformer (lower left) and TT60 trigger transformer (lower right) are common elements in power control.

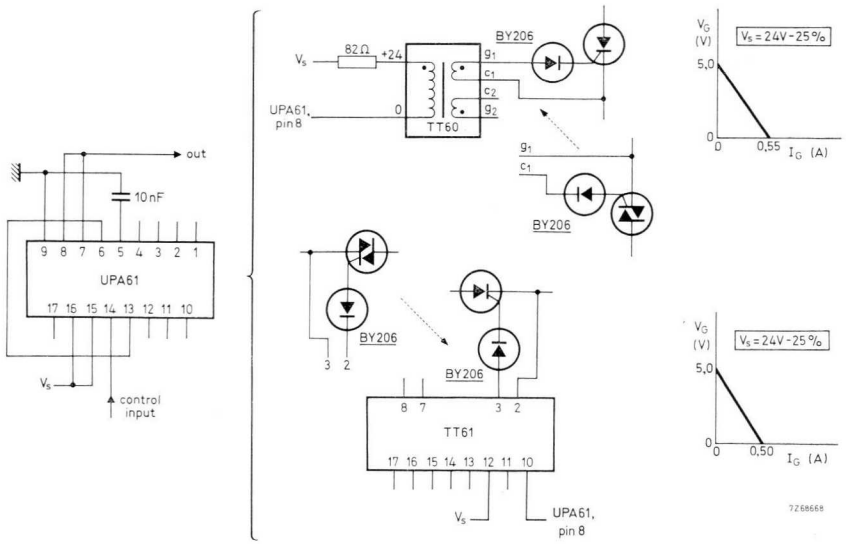


Fig.2-16 Low-power single-thyristor (or triac) trigger source.

Fig. 2-17a – In Fig. 2-17*a*, *b* and *c*, the pulse oscillator is connected to drive a 15Ω load. The conditions required to ensure safe operation are described in Section 2.4.4. The circuit in Fig. 2-17*a* is a low-voltage, high-current source (see the I_G/V_G characteristics), which reliably triggers all thyristors and triacs, even at a junction temperature of −55 °C.

Fig. 2-17b – This circuit, intended to trigger two thyristors simultaneously, can deliver a fairly high output current when equipped with the TT61. Use of the TT60 requires 10Ω current-sharing resistors, reducing the trigger power.

Fig. 2-17c – Powerful triggering is achieved by series connection of the secondary windings. The circuits are ideal for triggering an ignistor or for simultaneous triggering of two thyristors.

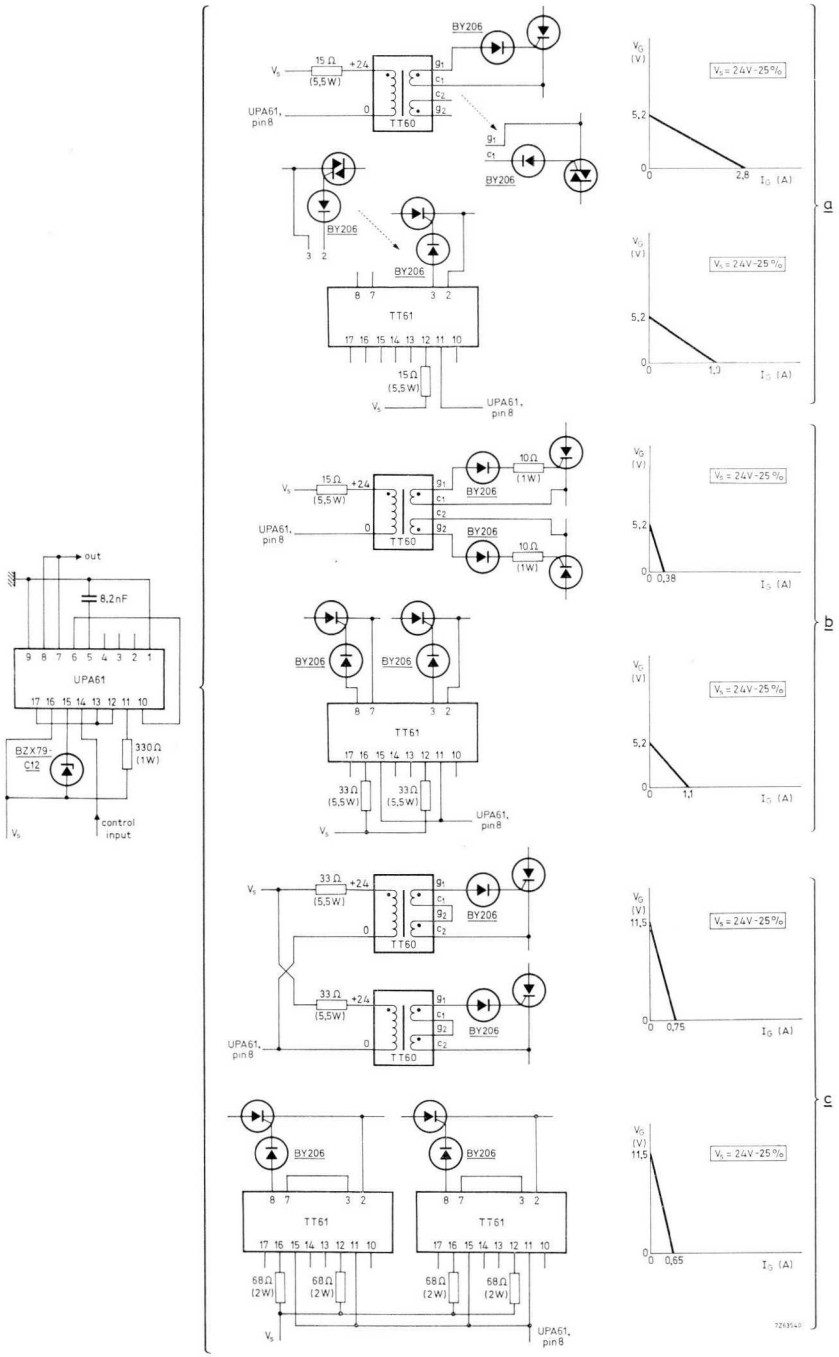


Fig.2-17 Pulse sources for triggering: (a) a thyristor or triac (high-power triggering) (b) two thyristors, (c) two thyristors or an ignistor (high-power triggering).

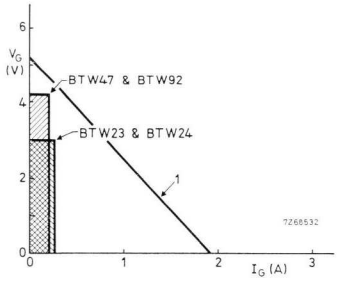


Fig.2-18 Areas of uncertain triggering (shaded) of diffused thyristors in comparison with I_G/V_G characteristic 1.

Fig. 2-18 shows how reliability of triggering can be predicted. It gives the areas of certain triggering of the indicated diffused thyristor types at −55 °C junction temperature in comparison with the I_G/V_G characteristic of Fig. 2-17*a* (TT61 trigger transformer) as an example. Because the areas of certain triggering are below the I_G/V_G characteristic, triggering will be ensured.

2.7 DOA61 differential amplifier

Functions – differential amplifier
comparator
operational amplifier.

The DOA61 contains a high-gain, low-drift operational amplifier, around which resistive components are grouped to form the most common circuit configurations; see Fig. 2-19, which also shows the resistor values. The operational amplifier is frequency-compensated (6 dB/octave roll-off) and, therefore, does not oscillate even with heavy negative feedback, provided that the load capacitance does not exceed 1 nF. Gain-bandwidth product is 1 MHz; with the amplifier connected as an inverter with 20 dB gain, the roll-off frequency is 10 kHz.

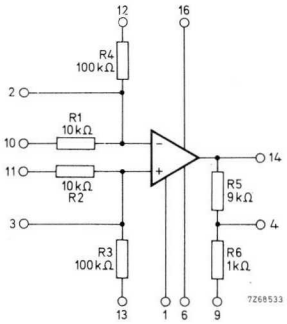


Fig.2-19 DOA61-circuit diagram.

Performance is specified in the Data Handbook for d.c. supply voltages of $\pm$ 12 V and $\pm$ 15 V, for which the open-loop gain is 32000 and 45000, respectively. Protection is included against reversed supply voltages, excessive differential input signals, and output short-circuits of indefinite duration. Typical input voltage drift is 10 μV/°C.

Minimum output voltage swing is $\pm$ 9 V with a 10 kΩ load, or $\pm$ 7 V with a 2 kΩ load, and output current capability is 5 mA minimum ($\pm$ 12 V d.c. supply). Current consumption is $2 \times 2{,}2$ mA at $\pm$ 12 V d.c. and $2 \times 2{,}7$ mA at $\pm$ 15 V d.c.

A few examples of the numerous applications[2]) are given in the sections that follow.

2.7.1 DOA61 AS AN INVERTING AMPLIFIER

Fig. 2-20 shows the DOA61 as an inverter with a gain of -100, and Fig. 2-21 shows a similar configuration for an arbitrary gain. In the circuit of Fig. 2-20, bias current compensation is obtained by means of R_2 and R_3 whose parallel resistance is equal to that of R_1 and R_4 in parallel, and in the circuit of Fig. 2-21 with the aid of resistance $R_i \; R_f/(R_i + R_f)$. Voltage offset is eliminated by adjustment of the 100 kΩ potentiometer.

[2]) Application Book, ordering code 9399 263 05901 - Measurement and Control using 40-series Modules.

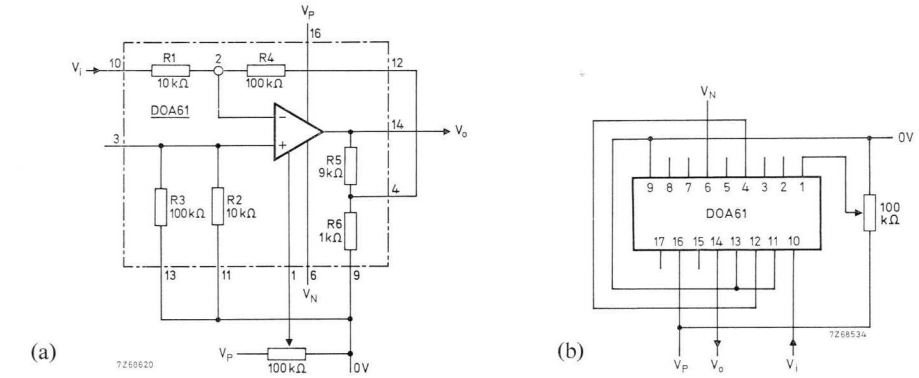


Fig.2-20 DOA61 as an inverting amplifier with a gain of -100: (a) circuit diagram, (b) wiring diagram. The positive and negative supply voltages are denoted V_P and V_N.

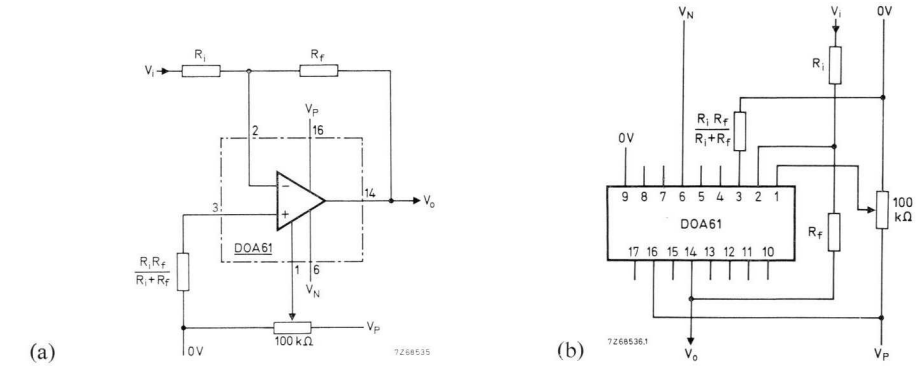


Fig.2-21 DOA61 as an inverting amplifier with a gain of $-R_f/R_i$. (a) circuit diagram, (b) wiring diagram.

2.7.2 DOA61 AS A NON-INVERTING AMPLIFIER

For operation of the DOA61 as a non-inverting amplifier with arbitrary gain, the circuit of Fig. 2-22 is used. The permissible input voltage range is $+7$ V to -7 V at ± 12 V d.c. supply.

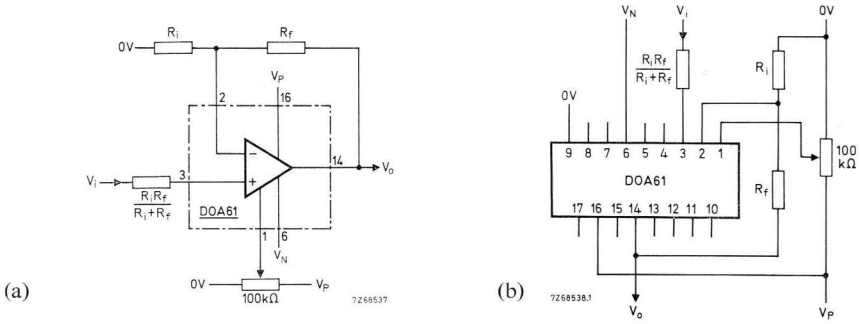


Fig.2-22 DOA61 as a non-inverting amplifier with a gain of $(R_f + R_i)/R_i$: (a) circuit diagram, (b) wiring diagram.

2.7.3 DOA61 AS A DIFFERENCE AMPLIFIER

Fig. 2-23 illustrates the DOA61 working as a difference or error amplifier. The output voltage in this circuit is $10(V_{i2}\text{-}V_{i1})$, where V_{i2} and V_{i1} are the input signals at pins 11 and 10. Clearly, the circuit may be looked upon as a subtractor with a weighting factor of 10. At $\pm$12 V d.c. supply and a gain of 10 times, the permissible input voltage range is $+7$ V to -7 V in common mode and $+17$ V to -17 V in differential mode.

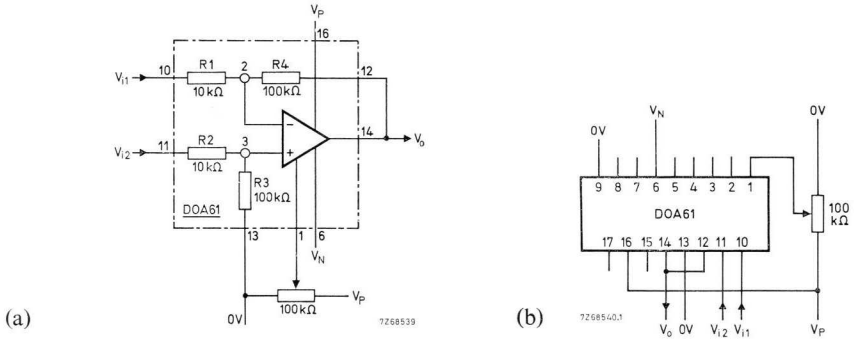


Fig.2-23 DOA61 as a difference amplifier (subtractor) with a gain of 10: (a) circuit diagram, (b) wiring diagram.

2.7.4 DOA61 AS A COMPARATOR

Figs 2-24 and 2-25 are examples of the DOA61 operating as a comparator. Because there is no degenerative feedback, the gain is extremely high, and the output voltage will swing between its extreme positive and negative values when the input signal V_i passes the level of reference voltage V_{ref}. For the circuit of Fig. 2-24, the permissible V_i- and V_{ref}-range is $+7$ V to -7 V at ± 12 V d.c. supply. Because the circuit of Fig. 2-25 is ten times less sensitive, its permissible input range is $+70$ V to -70 V.

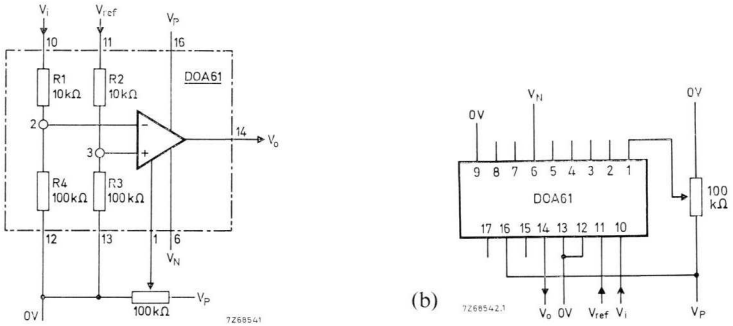


Fig.2-24 DOA61 as a high-sensitivity comparator: (a) circuit diagram, (b) wiring diagram.

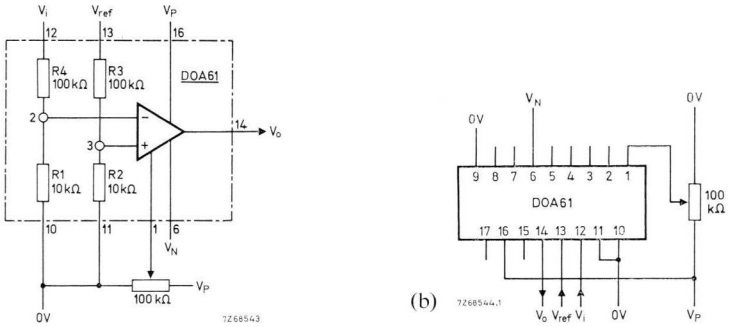


Fig.2-25 DOA61 as a low-sensitivity comparator: (a) circuit diagram, (b) wiring diagram.

2.8 2.NOR61 dual NOR gate with diode resistor networks

Functions – Logic operations.

Fig. 2-26 gives the circuit diagram of the 2.NOR61 logic circuit module. The diodes can be used to increase the number of gate inputs in parallel. The elements shown are combined to create the various logic functions, a few of which are discussed here.

Current consumption is 7,2 mA maximum at a 24 V + 25% d.c. supply and 3,1 mA maximum at a 12 V + 5% d.c. supply.

The input and output levels are specified in Table 2-5.

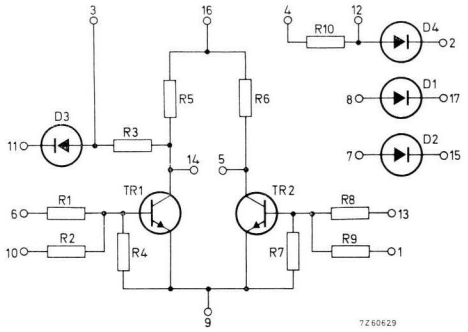


Fig.2-26 2.NOR61-circuit diagram.

Table 2-5. Input and output levels

	d.c. supply voltage	
	12 V ± 5%	24 V ± 25%
required input drive (pin 1, 6, 10 or 13)	2 D.U.*	2 D.U.
output capability (pin 5 or 14)	6 D.U.	10 D.U.

* Section 2.2.

2.8.1 2.NOR61 AS A NOT GATE

A NOR gate inverts the input signal and thus can function as a NOT gate. Fig. 2-27 illustrates such a circuit using the 2.NOR61. Input drive required and output capability are given in Table 2-5.

Fig.2-27 2.NOR61 as a NOT gate: (a) circuit diagram, (b) wiring diagram.

2.8.2 2.NOR61 AS AN AND GATE

Fig. 2-28 shows the 2.NOR61 as a low-power AND gate. The output capability is 1 D.U. at a d.c. supply voltage of 12 V $\pm 5\%$, or 2 D.U. at 24 V ± 25 V d.c. supply. If 2 D.U. output capability is insufficient, the circuit of Fig. 2-29 should be used; see Table 2-5. In these circuits, diode D_4 improves noise immunity.

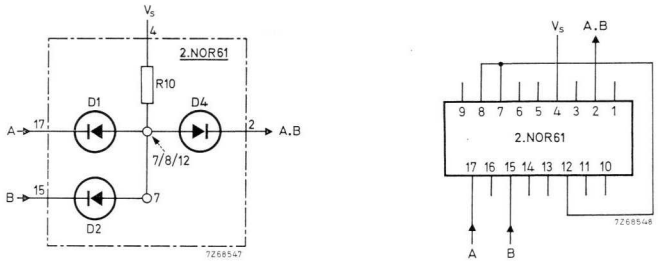
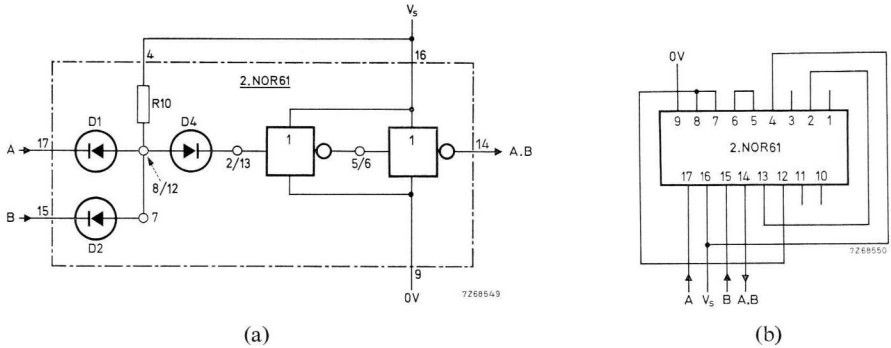


Fig.2-28 2.NOR61 as a low-power AND gate: (a) circuit diagram, (b) wiring diagram.

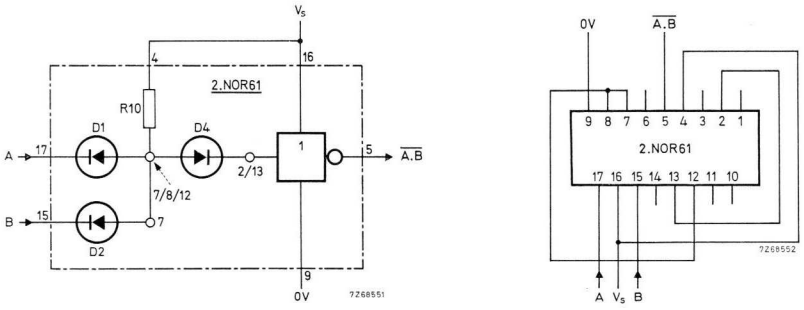


(a) (b)

Fig.2-29 2.NOR61 as a high-power AND gate: (a) circuit diagram, (b) wiring diagram.

2.8.3 2.NOR61 AS A NAND GATE

For use as a NAND gate, the 2.NOR61 is connected according to Fig. 2-30. Output capability is specified in Table 2-5.



(a) (b)

Fig.2-30 2.NOR61 as a NAND gate: (a) circuit diagram, (b) wiring diagram.

2.8.4 2.NOR61 AS A NOR GATE

Figs 2-31 and 2-32 show the 2.NOR61 operating as a dual-input or quadruple-input NOR gate, respectively. Table 2-6 gives the output capability of these circuits.

Fig.2-31 2.NOR61 as a dual-input NOR gate: (a) circuit diagram, (b) wiring diagram.

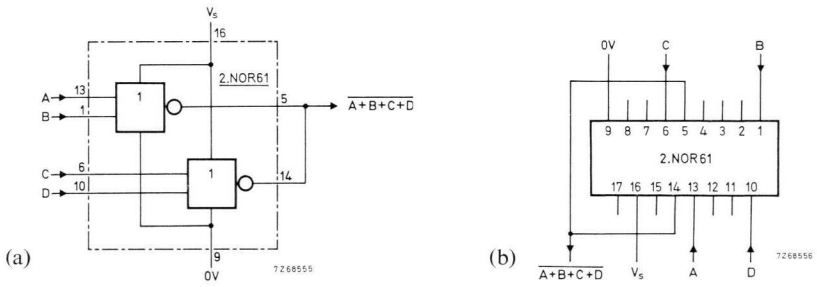


Fig.2-32 2.NOR61 as a quadruple-input NOR gate: (a) circuit diagram, (b) wiring diagram.

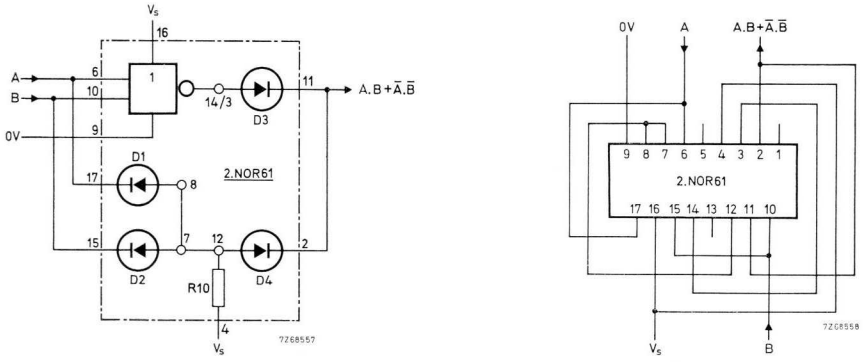
Table 2-6 Output capabilities

	d.c. supply voltage	
	12 V ± 5%	24 V ± 25%
dual-input NOR gate (Fig. 2-31)	6 D.U.	10 D.U.
quadruple-input NOR gate (Fig. 2-32)	12 D.U.	20 D.U.

2.8.5 2.NOR61 AS A COINCIDENCE GATE

The gate circuit of Fig. 2-33 has the logic function $F = A \cdot B + \overline{A} \cdot \overline{B}$. As seen from Table 2-7, a logic "1" output is produced at *coincidence of equal logic levels* at inputs *A* and *B*. Output capability is 2 D.U. at a d.c. supply voltage of 24 V $\pm$ 25% and 1 D.U. at 12 V $\pm$ 5%.

The circuit is useful in a safety system using two input devices which should give the same logic level.



(a) (b)

Fig.2-33 2.NOR61 as a coincidence gate: (a) circuit diagram, (b) wiring diagram.

Table 2-7 Truth table of coincidence gate (Fig. 2-33).

A	*B*	$A \cdot B + \overline{A} \cdot \overline{B}$
0	0	1
0	1	0
1	0	0
1	1	1

2.8.6 2.NOR61 AS AN EXCLUSIVE OR GATE

In an OR gate, one or more inputs will give an output. The function becomes that of an exclusive-OR or EXOR gate, when an output is only produced with *one and only one input present*. The logic function of the two-input EXOR gate is expressed as $F = A \cdot \overline{B} + \overline{A} \cdot B$, which is the inverse of that of the coincidence gate: compare Tables 2-8 and 2-7. Fig. 2-34 shows an EXOR gate using the 2.NOR61; output capability is given in Table 2-5.

The EXOR gate is useful in control systems, where the coincidence of conflicting commands from two or more stations is intolerable.

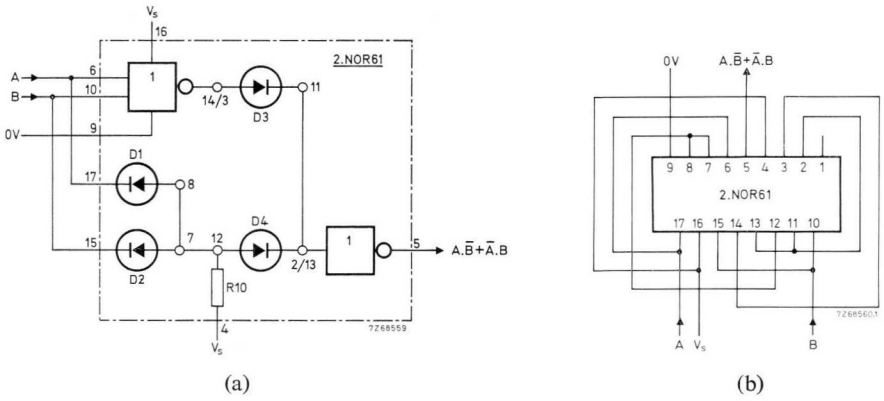


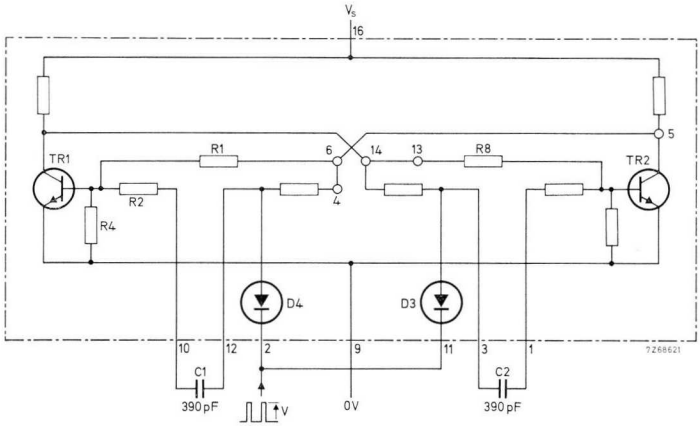
Fig.2-34 2.NOR61 as a exclusive-OR gate: (a) circuit diagram, (b) wiring diagram.

Table 2-8 Truth table of EXOR gate.

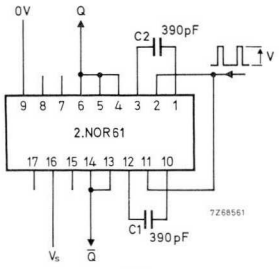
A	B	$A \cdot \overline{B} + \overline{A} \cdot B$
0	0	0
0	1	1
1	0	1
1	1	0

2.8.7 2.NOR61 AS A BISTABLE

In logic systems, bistables are useful as memory elements, scalers, or binary counter stages. Fig. 2-35 illustrates a bistable circuit using the 2.NOR61. The drive pulses are a.c. coupled via C_1 C_2 to the transistor bases, and the circuit changes state coincidently with the trailing edge of the positive pulses applied via input diodes D_3D_4. Resistors R_1 and R_8 provide d.c. feedback so that either TR_1 or TR_2 conducts.



(a)



(b)

Fig.2-35 2.NOR61 as a bistable: (a) circuit diagram, (b) wiring diagram.

Fig. 2-36 is the pulse-pattern diagram of the circuit operating as a binary counter stage. If TR_1 in Fig. 2-35 conducts, TR_2 is cut off. The collector of TR_2 is HIGH, but turn-off capacitor C_1 cannot charge until the input level goes HIGH. When this occurs, the voltage across C_1 rises to a value equal to the amplitude V of the positive input pulse (D_4 operating as a clamping diode).

At the end of the count pulse, the input returns to LOW level, the base of TR_1 is pulled negative, and this transistor is cut off. Simultaneously, C_1 starts to discharge through R_4, R_2 and D_4. Because the collector of TR_1 is HIGH, base current is supplied to TR_2 through coupling resistor R_8, causing this transistor to saturate.

During the next positive count pulse, C_2 is charged which cuts TR_2 off when the pulse ceases, etc.

The pulse width must be sufficient for the turn-off capacitors to charge to the pulse amplitude V; otherwise, circuit switching becomes uncertain. Fig. 2-37 gives the input waveform required to achieve reliable counting to 10 kHz[3]).

The capability per output is 4 D.U. at a d.c. supply voltage of 24 V $\pm$ 25%.

[3]) AI No. 462, ordering code 9399 264 46201 - Scalers of 2 to 8.

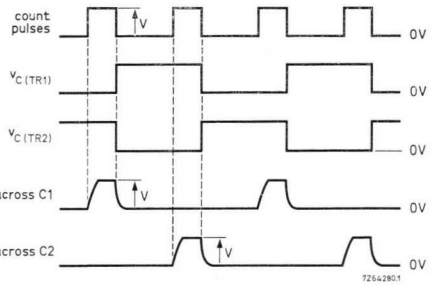


Fig.2-36 Pulse-pattern diagram of bistable circuit in Fig. 2-35.

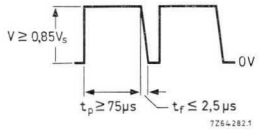


Fig.2-37 Required input waveform for up to 10 kHz count rate (d.c. supply voltage V_s 10 V to 30 V).

2.9 DCT61 direct current transformer

Function – measurement of direct current with the measuring circuit isolated from the current carrying conductor.

The DCT61 direct current transformer is used in a 5 kHz chopper circuit, the sampling pulses from which are rectified to provide a d.c. voltage proportional to the measured direct current. A circuit arrangement is discussed in section 4.9.2.

Fig. 2-38 shows the outline of the DCT61. This transformer is a moulded, twin-toroid assembly, the toroids being made from high-grade Ferroxcube with low hysteresis and high permeability. The current carrying conductor is passed through the aperture in the mould. The measuring range is 0 A to 120 A, but lower ranges can be simply obtained by increasing the number of primary turns (for instance, a range of 0 A to 12 A requires 10 turns). Brief specifications are:

primary current	0 to 120 A
output linearity obtainable	2 %
sampling frequency	5 kHz
test voltage	5 kV
no. of secondary turns	2×150
secondary terminals	Faston 0,25 inch.

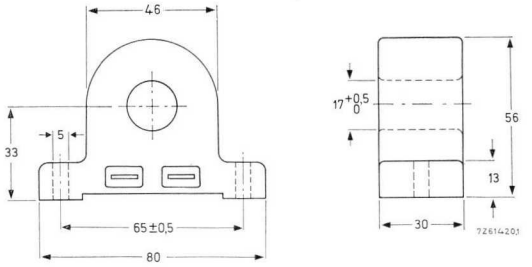


Fig.2-38 Outline of DCT61 direct current transformer.

3 Thyristor and triac operation

3.1 Introduction

Thyristors and triacs have modernized power control. Because of their reliability they are very popular in both industrial and domestic areas. Examples of their innumerable applications are (*industrial*) temperature control, machine tool control, static power switches, (*domestic*) lamp dimmers, panel radiators, household cookers and refrigerators, hobby tools and even vacuum cleaners (suction control). It is no exaggeration to say that power control is, nowadays, unthinkable without thyristors or triacs.

The Silicon Controlled Rectifier (SCR) or *thyristor* (short for reverse blocking triode thyristor) is a four-layer device. The bidirectional triode thyristor or *triac*, a five-layer device, is another of the various members of the thyristor family. As the unabbreviated names say, the thyristor, once triggered into conduction, can carry load current only in one direction, but the triac can pass load current in either direction. These devices have a feedback mechanism ensuring that they will conduct fully after triggering; imperfect conduction would entail a large voltage loss, resulting in heavy dissipation and, consequently, complete destruction.

General purpose and fast turn-off (sometimes called "inverter grade") thyristors are available for the user. The *general-purpose* types are designed for use in power control systems operating from a 50 Hz or 400 Hz mains supply. Average current ratings are from 1 A to 160 A, and rated voltage is between 100 V and 1600 V. *Fast turn-off* thyristors are intended for circuits working at a high frequency, such as choppers and inverters. Rated average current is between 16 A and 80 A, and voltage classification is from 300 V to 1200 V.

The *triac* series BTW37, BTX94 and BTW34 are rated to carry an r.m.s. current of 12 A, 25 A and 55 A, respectively, and voltage ratings are from 400 V to 1200 V (to 1600 V for BTW34).

This Chapter deals briefly with thyristor and triac operation, further details having been published earlier[1,2]). The main power control circuits are also discussed.

[1]) PI No. 17, ordering code 9399 254 01701 - Triacs; Operation and Use.

[2]) Product Book, ordering code 9399 256 00701 - Thyristors.

3.2 The thyristor, a unidirectional power control device

3.2.1 OPERATION

Turn-on by gate drive

Fig. 3-1 gives a simple illustration of the p-n-p-n thyristor structure as well as the thyristor symbol. There are three terminals: the anode and cathode (main current carrying electrodes) and the gate (trigger electrode). With forward voltage applied (anode made positive with respect to cathode), control junction J2 is reverse-biased and only a low leakage current will flow: *the thyristor is in the off-state.*

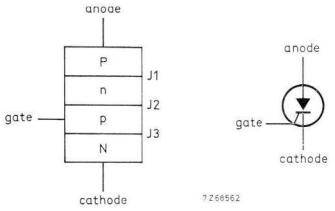


Fig.3-1 Simple representation of *P*-gate thyristor (compare with symbol). J_1 = anode junction, J_2 = control (or switching) junction, J_3 = cathode junction, *P*, *N* = heavily doped outer layers, *p*, *n* = lightly doped inner layers.

When a positive signal is supplied to the gate, a substantial current starts to flow across the control junction; this causes the current gains of the p-n-p and n-p-n transistor structures (top three and bottom three layers in Fig. 3-1) to increase. As soon as the sum of the current gains reaches unity, the voltage barrier at the control junction will collapse, and junctions J1 and J3 become strongly forward biased. As a result, the heavily doped outer layers, P and N, inject multitudes of charge carriers into the lightly doped inner layers, p and n, making these conduct heavily: *the thyristor is in the on-state* (thyristor current mainly sustained by the charge carriers from the outer layers).

The current gains depend on the gate current; there should be sufficient gate drive to ensure that these become high enough, otherwise turn-on (switching to the on-state) will not ensue.

Uncontrolled turn-on

The anode current at which the thyristor latches into conduction is called the *latching* (or *pick-up*) *current*. Latching level can be reached for reasons other than gate triggering. This, then, will result in uncontrolled turn-on.

At a large enough off-state voltage the leakage current becomes so high that avalanche breakdown occurs, resulting in turn-on. The off-state voltage at which turn-on occurs is called the *breakover voltage*.

A high leakage current causing turn-on could also be the result of a very high junction temperature (leakage current doubling for any 10 °C to 15 °C rise in junction temperature). At a certain critical temperature (above the rated maximum) the thyristor will not support a substantial voltage at all.

If the off-state voltage is a ramp function, the junction capacitance C_j will be charged by a current $i = C_j\ (\mathrm{d}V_D/\mathrm{d}t)$, where $\mathrm{d}V_D/\mathrm{d}t$ is the rate of rise of off-state voltage. At an excessive rate of voltage rise the charge current will be so large that turn-on may follow.

Voltage transients (mains-borne or generated internally by commutation) can cause uncontrolled turn-on. To prevent such contingencies, RC-series networks are connected across each of the thyristors and a suppression filter is included on the a.c. side. This filter also prevents interference due to thyristor switching from entering into the mains.

Spreading velocity of current

After triggering, time is needed for the control junction to break down entirely. That is, there is a limited velocity with which the on-state current spreads laterally from the gate area across the whole wafer. So, if the rate of rise of thyristor current, $\mathrm{d}I_T/\mathrm{d}t$, is very large, as may well be the case in an ohmic circuit, a small wafer area (in the region of the gate connection) will have to carry nearly the full current; as a result, hot spots can occur with consequent damage to the device. The $\mathrm{d}I_T/\mathrm{d}t$ rating is established for protection against this type of overload. The spreading velocity, and thus the $\mathrm{d}I_T/\mathrm{d}t$ capability, increases with the rate of rise and the level of gate current I_G; the $\mathrm{d}I_T/\mathrm{d}t$ rating is given for specified values of I_G, on-state current I_T and often $\mathrm{d}I_G/\mathrm{d}t$. The permitted $\mathrm{d}I_T/\mathrm{d}t$ is lower when the device is turned on by breakover. Series chokes must sometimes be used to restrict $\mathrm{d}I_T/\mathrm{d}t$.

Length of trigger pulse

As soon as the gate (trigger) signal is applied, the anode current starts to rise; the rise rate of current is determined by the inductive time constant of the load and, to a lesser extent, by the gate drive level. The gate signal must be maintained until the anode current has reached latching level (see Fig. 3-2), otherwise the thyristor will turn off after termination of the gate pulse. For a very inductive load, a long gate pulse must be used. (Section 1.2.1 discusses the advantage of using a train of trigger pulses.) The trigger pulse is ineffective and can therefore be discontinued when the anode current is greater than the latching value.

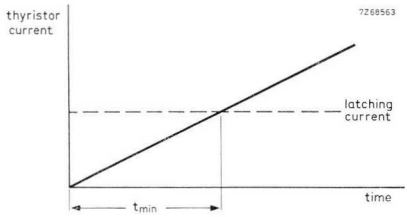


Fig.3-2 Trigger pulse width must exceed t_{min}.

Turn-off

The current gain decreases with the thyristor current. Since the homogeneity of a thyristor wafer is never perfect, conduction at low current is restricted to those areas where the current gain is largest. With a further decrease of current, conduction is concentrated in thin "filaments" of the thyristor wafer where the current gain is just sufficient to maintain conduction. *Holding current* is the value of thyristor current at which conduction is just possible. At any lower current the thyristor turns off.

Turn-off methods

The thyristor can only be turned off by letting its anode current drop below holding level. This can be done by reducing the anode voltage to zero or reversing it. In the latter case a reverse current is forced through the thyristor (forced

turn-off). Because part of the charge carriers remaining after conduction is swept out by the reverse current, the thyristor turns off much more rapidly. Rapid turn-off (giving low turn-off losses) is essential in inverters and choppers which normally operate at a high frequency. Forced turn-off is the method normally used.

Turn-off time

After conduction, residual charge carriers are still present in the thyristor wafer. Forward voltage should not be re-applied until these carriers have disappeared (carrier clean-up by recombination and trapping); otherwise the thyristor will turn on because of the substantial current induced. The turn-off time t_q of the thyristor is defined as the time between the instant the thyristor current reverses and the instant forward voltage can be re-applied without turn-on to follow (Fig. 3-3). The turn-off time t_q is specified in the thyristor data under accurately defined values of junction temperature, I_T, $-(\mathrm{d}I_T/\mathrm{d}t)$, V_R and $\mathrm{d}V_D/\mathrm{d}t$ (ref. Fig. 3-3); the turn-off time imposed by the circuit in which the thyristor works must be larger than the specified t_q-value.

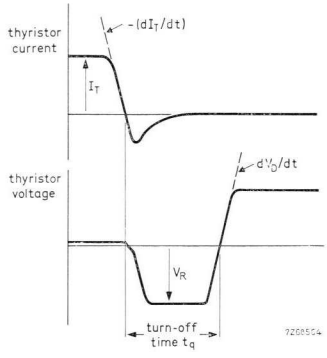


Fig.3-3 Simplified thyristor current and voltage curves showing turn-off time. The period of thyristor turn-off is called the commutation interval.

Latching current versus holding current

After conduction in the gate area has been established, the current spreads across the whole wafer cross section. Therefore, the latching current is related to the current gain near the gate connection, whereas the holding current is related to the largest current gain. Because the current gain in the gate area is not necessarily the largest, the latching current is greater than the holding current. The ratio of latching current to holding current is a measure of wafer homogeneity, and a ratio of 2 : 1 is quite normal. (For a perfectly homogeneous wafer, the latching and holding currents would be equal.)

3.2.2 Static thyristor characteristic

Fig. 3-4 shows the thyristor current/voltage characteristic for static condition or slowly changing variables. The reverse characteristic (quadrant 3) is similar to that of a semiconductor diode. For low reverse voltage, a small leakage current flows. When the reverse voltage is high, avalanching occurs. In the forward direction (quadrant 1) the thyristor blocks off-state voltage, if it is not triggered, and only a small leakage current flows until the breakover voltage, $V_{(BO)}$ is reached. At this voltage the thyristor current exceeds latching level I_L, and the thyristor switches into conduction, its voltage abruptly dropping to a very low level. The normal method of triggering a thyristor is by applying a positive gate signal.

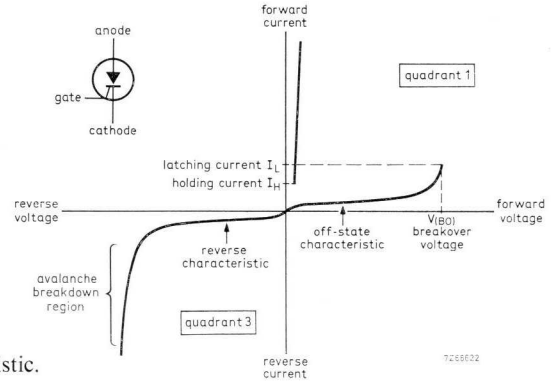


Fig.3-4 Thyristor static characteristic.

The thyristor on-state characteristic is somewhat similar to that of a diode, as seen in the diagram.

Also seen in the graph is the holding current I_H, below which the thyristor turns off. To give an idea of the values of these currents, the maximum values of I_L and I_H for the BTW24 series are 300 mA and 200 mA, respectively.

It should be noted that operation in the unnumbered quadrants is impossible.

3.2.3 Gate forward characteristic

The gate forward characteristic is that of a p-n diode, and the spread in gate characteristics for a given thyristor series is schematically illustrated by the boundary curves in Fig. 3-5.

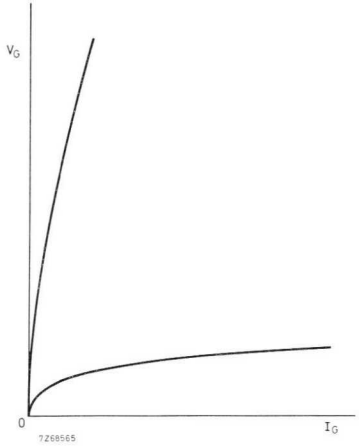


Fig.3-5 Curves showing spread in $V_G I_G$ characteristic.

To prevent damage to the p-n junction by excessive gate dissipation, the average and peak gate power should not exceed a rated maximum; this is represented in Fig. 3-6 by the hyperbolic curves marked $P_{G(AV)\max}$ and $P_{GM\max}$.

Continuous operation is only allowed in the region below the $P_{G(AV)max}$-curve, and pulsed operation should occur when the area between the $P_{G(AV)max}$- and P_{GMmax}-curves is used. The latter area gives greater triggering certainty, as will be clear from the following. If $\hat{P}_G$ is the peak gate power dissipation, the permissible maximum duty cycle of pulsed operation is: $\delta_{max} = P_{G(AV)max}/\hat{P}_G$, ($\hat{P}_G$ must not exceed P_{GMmax}).

Thyristor triggering becomes uncertain for a weak gate signal. The $V_G\,I_G$ area of uncertain triggering is shown hatched in Fig. 3-7. The parameters V_{GT} and I_{GT} are the minimum values of gate voltage and gate current that will trigger all devices in the series. A powerful gate drive is mandatory in cases where a high rate of rise of on-state current occurs; This implies that the load line of the trigger source should be located close to the P_{GMmax}-curve (pulsatory gate drive).

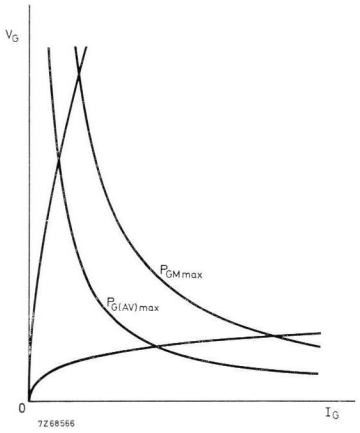


Fig.3-6 Diagram illustrating gate power ratings.

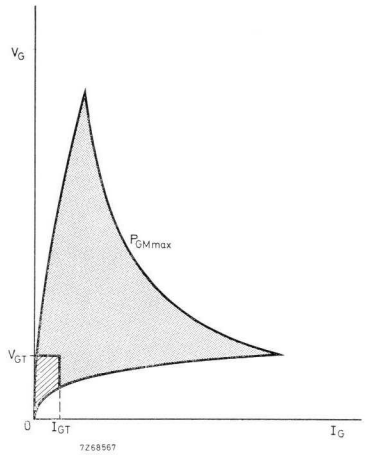


Fig.3-7 Areas of certain triggering (large shaded area) and uncertain triggering (small hatched area).

The levels of V_{GT} and I_{GT} depend on the junction temperature, as shown schematically in Fig. 3-8 for extreme values of −55 °C and 125 °C. The area of uncertain triggering becomes larger at a lower junction temperature; this should be accounted for where triggering is marginal. Thyristors will not be triggered by a gate voltage equal to V_{GD} or lower (black area).

As an example, Fig. 3-9 shows the gate characteristic of the BTW24 series.

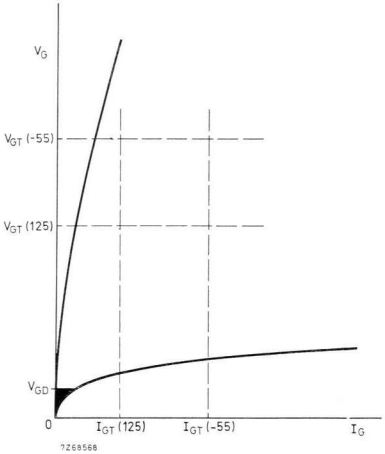
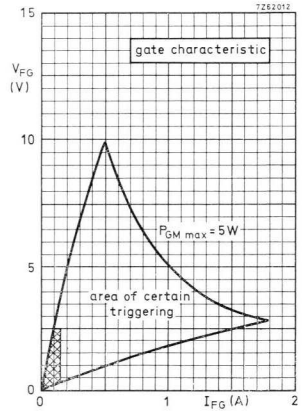


Fig.3-8 Boundaries of area of uncertain triggering depend on junction temperature. Non-triggering area shown in black.



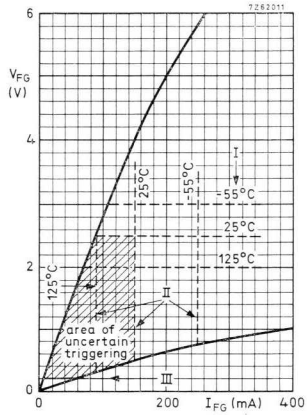


Fig.3-9 Gate characteristic of BTW24 series. I = values of V_{GT} for various junction temperatures, II = values of I_{GT} for various junction temperatures, III = value of V_{GD}.

3.3 The Triac, a bidirectional power control device

3.3.1 General

The triac passes current in both directions and is, therefore, an a.c. power control device. As such, it is equivalent to two thyristors in anti-parallel, and it needs only one heatsink compared with two required for the anti-parallel thyristor configuration. Consequently, the triac saves both space and cost in a.c. applications. Because the triac can be triggered with either polarity of input voltage, close attention must be paid to the design of its trigger circuit to ensure reliable control[3]).

3.3.2 Static triac characteristic

The triac bidirectional properties are illustrated by the current/voltage characteristic of Fig. 3-10 which also shows the symbol for the device. As with the thyristor, the triac turns on when its current exceeds latching level (owing to either a gate signal or the triac voltage exceeding breakover level $V_{(BO)}$); turn-off occurs when the triac current falls below holding level. Operation in quadrant 1 occurs when main terminal 2 is at a *higher* potential than main terminal 1; the triac operates in quadrant 3 when main terminal 2 is at a *lower* potential than main terminal 1. The single gate electrode controls the conduction in either direction.

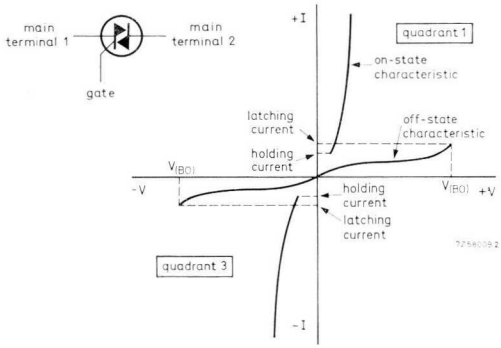


Fig.3-10 Static characteristic of triac, and triac symbol.

[3]) AI No. 467, ordering code 9399 254 46701 - Continuous Three-phase Control System with Triacs.

3.3.3 Gate forward characteristic

Fig. 3-11 illustrates the boundary curves of the spread in gate forward characteristic and the areas of uncertain triggering (shown hatched). It is seen that the triac can be triggered by either a positive or a negative gate signal*. The areas of uncertain triggering are shown for both cases ($+I_G$ $+V_G$ and $-I_G$ $-V_G$) and moreover for operation of the triac in the first quadrant ("terminal 2 positive") and in the third quadrant ("terminal 2 negative"). It follows that triggering with a *negative* signal is preferable when the trigger power is limited. Another motive for favouring a negative gate signal will be clear from the following.

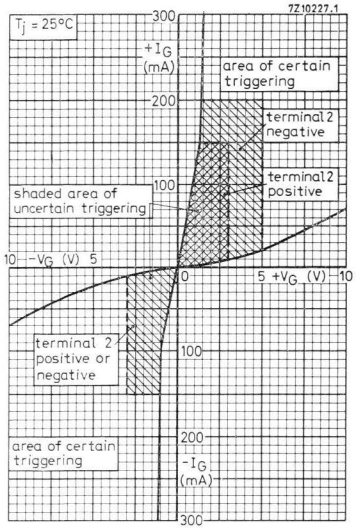


Fig.3-11 Gate characteristic of BTX94.

3.3.4 Connecting the gate

Like thyristors, triacs are advantageously triggered from a pulse source (see Section 1.2.1). Basically, the gate can be driven by a positive or negative signal.

* polarity of gate signal referred to terminal 1.

Fig. 3-12*a* illustrates the former case. With the main current flowing into terminal 1 (solid arrow in Fig. 3-12*b*) a parallel gate current can occur (see dashed arrow). The parallel gate current has two undesirable effects. First, it can saturate the trigger transformer. Second, during turn-off the parallel current will cease fairly abruptly; the induced voltage spike (Fig. 3-12*c*) re-triggers the triac, and uncontrolled conduction results. This deficiency is eliminated by using a negative gate drive: see Fig. 3-12*d*. The BY206 diode blocks the parallel current.

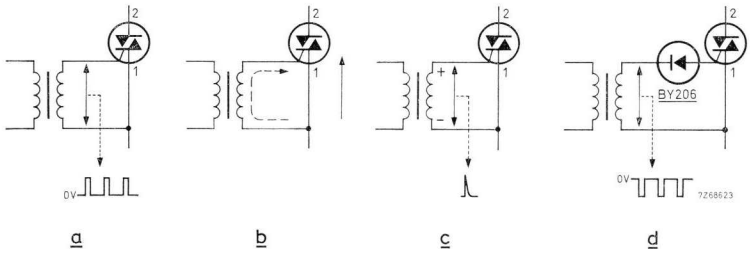


Fig.3-12 (a), (b), (c) gate coupling to positive trigger source; (d) gate coupling to negative trigger source.

3.3.5 How to get reliable turn-off[4])

Unlike thyristors, triacs do not have a circuit-imposed turn-off time. This is because the triac will conduct regardless of the polarity of the applied voltage. To ensure turn-off, the current decay rate during the commutation interval (turn-off period) and the rate of rise of voltage re-applied after commutation must both be restricted. An excessive current decay rate has a profound effect on the tolerable rate of voltage rise as it causes a large number of residual charge carriers to be available to initiate turn-on when the voltage rises (Section 3.2.1: Turn-off time). The BTX94 can safely withstand 30 V/μs rise rate of re-applied voltage at the rated junction temperature (125 °C) provided the current decay rate does not exceed 50 A/ms.

[4]) AN No. 127, ordering code 9399 250 62701 - Triac Control of D.C. Inductive Loads.

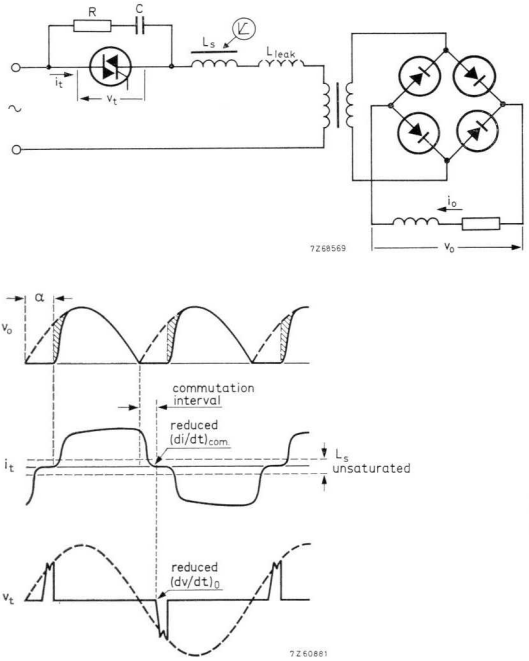


Fig.3-13 Incorporation of saturable choke to ensure commutation.

Transformer loads are notorious for causing commutation problems, especially when supplying an inductively loaded bridge rectifier. To "soften" commutation (reduction of decay rate of thyristor current and rise rate of re-applied voltage), a choke should be connected in series with the triac, a saturable type being preferred to minimize the voltage loss. The choke delays the voltage rise, so a quiescent period of a few tens of microseconds is interposed during which the triac can recover[5]). Fig. 3-13 illustrates the circuit and the relevant waveforms.

Clearly, triggering should cease before current commutation takes place; if not, the triac will continue to conduct for the whole of the next half cycle, and loss of control will result.

[5]) Elektronik 1970, Heft 5, pp. 161 to 164, K. Brückmüller - Steuerung induktiver Verbraucher mit Triacs.

3.4 Thermal considerations

In a power semiconductor device, power is dissipated in the junction area because the forward current causes a voltage drop across the junction; further sources of power loss are the gate dissipation, the leakage in the off-state and reverse-biased state and switching losses. Power is converted into heat, and the heat flows away from the junction to ambient because the ambient temperature is lower than that of the junction. Fig. 3-14 gives the thermal-resistance diagram, in which the power P_{tot} represents the total dissipation. As seen from Fig. 3-14*a*, a portion, P_1, flows away via the heatsink ($R_{th\ h-a}$), and the remainder, P_2, is dissipated through the thermal resistance $R_{th\ d-a}$ between device envelope and the surrounding air. The contribution by $R_{th\ d-a}$ in removing heat is by no means negligible. In Fig. 3-14*b*, $R'_{th\ h-a}$ is taken to be lower than $R_{th\ h-a}$, to account for the parallel resistance $R_{th\ d-a}$.

To prevent damage, the junction temperature T_j must not exceed a rated maximum. Because the junction temperature cannot be measured, the mounting-base temperature T_{mb} is taken as a reference when specifying rated current.

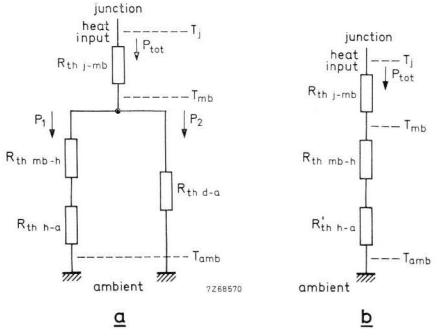


Fig.3-14 Thermal model of thyristor (triac) on its heatsink. T_j = junction temperature, T_{mb} = mounting-base temperature, $R_{th\ j\text{-}mb}$ = junction-to-mounting base thermal resistance, $R_{th\ d\text{-}a}$ = device-to-ambient thermal resistance, $R_{th\ mb\text{-}h}$ = mounting base-to-heatsink thermal contact resistance, $R_{th\ h\text{-}a}$ = heatsink thermal resistance, $R'_{th\ h\text{-}a}$ = heatsink thermal resistance accounting for $R_{th\ d\text{-}a}$ ($R'_{th\ h\text{-}a} < R_{th\ h\text{-}a}$).

According to Fig. 3-14, the relationship between allowable maximum mounting-base temperature and junction temperature, $T_{mb\ max}$ and $T_{j\ max}$, is:

$$T_{mb\ max} = T_{j\ max} - P_{tot} \cdot R_{th\ j-mb}.$$

The size of the heatsink must be such that the allowable maximum mounting-base temperature is not exceeded. With $T_{mb\ max}$ known, the thermal resistance of the heatsink follows from (see Fig. 3-14*b*):

$$R'_{th\ h-a} \leqslant \frac{T_{mb\ max} - T_{amb}}{P_{tot}} - R_{th\ mb-h},$$

where the expected maximum value should be used for T_{amb}.

Heatsink size is determined from nomograms which account for the heat removal via the device envelope, so that the heatsink does not become unnecessarily large. The thermal resistance is expressed in °C/W.

3.5 Ratings and characteristics

According to I.E.C. publication 134 the following definitions apply:

"*Rating*: A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specific values of environment and operation".

"*Characteristic*: A characteristic is an inherent and measurable property of a device . . . . . A characteristic may also be a set of related values, usually shown in graphical form."

Thyristor and triac ratings accord with the "absolute maximum rating system". Again quoting I.E.C. publication 134:

"Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the *worst possible conditions**."

It is noted that ratings are mostly maxima but they can also be minima.

Ratings and characteristics are expressed by symbols, symbol letter designations being specified in Table 3-1 (compare with Fig. 3-15).

Ratings will now be described.

* Editor's italics.

Table 3-1. Symbol letter designation code

quantity symbol	1st subscript	2nd subscript	3rd subscript
I = current	(BO) = breakover value	(AV) = average value	M = peak value
I^2t = *I* squared *t*	D = off-state (forward blocking)	D = value not triggering any device	(RMS) = root-mean-square value
P = power	F = forward-biased state (only for gate)	M = peak value	
T = temperature	G = gate	max = permissible maximum value	
V = voltage	H = holding value	R = repetitive value	
	j = junction	(RMS) = root-mean-square value	
	L = latching value		
	R = reverse-biased state	S = surge (non-repetitive) value	
	stg = storage condition (non-operational)	T = value triggering all devices	
	T = on-state	W = working value (excluding repetitive and non-repetitive transients)	

3.5.1 VOLTAGE

V_{DWM}, V_{RWM} (crest working off-state and reverse voltage) refer to the peak value of the sinusoidal supply voltage (ref. Fig. 3-15).

V_{DRM}, V_{RRM} (repetitive peak off-state and reverse voltage) refer to regular transients on the mains voltage; these transients may be mains-borne or generated internally (e.g. by commutation).

V_{DSM}, V_{RSM} (non-repetitive peak off-state and reverse voltage) refer to irregular transients on the mains voltage; these transients can be caused by switching.

V_D, V_R (continuous off-state and reverse voltage) refer to a d.c. voltage. These parameters are important when using thyristors in choppers and inverters which are supplied from a d.c. source.

Thyristors and triacs are classified according to their *repetitive* voltage rating; for instance, the BTW24-1600RM has 1600 V repetitive peak voltage rating (working voltage rating equal to 1200 V).

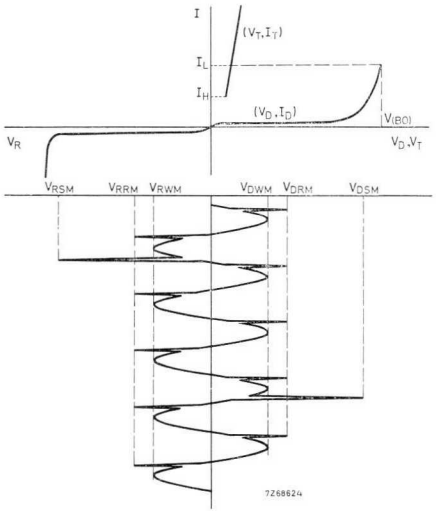


Fig.3-15 Diagram with symbols for thyristor voltage and current.

3.5.2 Current

I_T (d.c. on state current) refers to a pure d.c. current.

$I_{T(AV)}$ (average on-state current) refers to the current averaged over any 20 ms period (continuous load).

$I_{T(RMS)}$ (r.m.s. on-state current) refers to the r.m.s. value of a d.c. (thyristor) or a.c. (triac) current, under continuous load.

I_{TRM} (repetitive peak on-state current) refers to the peak value of on-state current including repetitive transients due to commutation; the "duty cycle" of the repetitive peak on-state current is limited by the r.m.s. on-state current rating. The repetitive current rating is essential for inrush conditions.

I_{TSM} (non-repetitive peak on-state current) refers to the peak value of a semi-sinusoidal (thyristor) or sinusoidal (triac) overload current. In the graphs showing non-repetitive current rating versus overload time, the r.m.s. value $I_{TS(RMS)}$ is given rather than the peak value. The non-repetitive (surge) current rating is important for fusing.

$I^2 t$ (I squared t) refers to the A^2 s content of a single non-repetitive on-state current surge of sub-cycle duration. The $I^2 t$ rating is specified for a semi-sinusoidal current surge lasting 10 ms, and is essential for coordination with fuses.

dI_T/dt (current rise rate) refers to the rate of rise of on-state current after triggering. A maximum limit is established to prevent the occurrence of hot spots in the wafer (see Section 3.2.1: Spreading velocity of current).

The current ratings for continuous operation are determined by the allowable maximum junction temperature; they are, therefore, specified for a given mounting-base temperature (related to the junction temperature). The non-repetitive ratings assume a junction temperature equal to the rated maximum prior to overload; because during overload the junction temperature can rise far above rated level, the non-repetitive ratings apply to current levels occurring only a few times during the lifetime of the device.

3.5.3 Temperature

T_{stg} is the storage temperature.
T_j is the junction temperature.

3.5.4 Gate ratings

Gate forward ratings were discussed in Section 3.2.3. Another important rating is the allowed peak reverse gate voltage. If this rating were exceeded, avalanche breakdown of the gate junction with accompanying high dissipation might occur. The gate can be protected against this type of overload by a parallel diode that is forward biased by reverse gate voltage.

3.6 Choosing the power device

The choice of the power device(s) – thyristors or triac – is determined by the following:

1. a.c. input voltage
2. nominal load current
3. inrush current
4. fusing
5. cooling method.

1. To allow for transients, the voltage classification of the device is taken as about *three times* the r.m.s. input voltage. Transient suppression is still necessary, but the size of the required transient suppression elements will be moderate.
2. Clearly, the continuous current rating must be at least equal to the maximum load current. The average thyristor current allowed depends on the current form factor. An example is worked out below.
3. Inrush currents occur when the load is a motor or an incandescent lamp. It will generally be safe to use a device whose continuous current rating is $1\frac{1}{2}$ to 2 times the current carried under nominal load. The lamp inrush current can be 10 to 15 times the nominal value. Because the inrush condition lasts only a few a.c. cycles, the repetitive current rating is chosen to equal inrush current.
4. For protection, fast-acting fuses should be used. In a few cases, a larger power device must be used to obtain coordination between fuse characteristics and surge ratings.
5. The method of cooling (free convection, forced-air cooling, water cooling) determines the loading capability of the power device.

Example

A three-phase bridge must deliver 70 A. Select suitable thyristors, and design their heatsinks for 45 °C maximum ambient temperature.

The average thyristor current is 70/3 = 23 A, and its form factor is approximately 1,8. Consulting the BTW24 characteristic of Fig. 3-16, it is seen that for the form factor a equal to 1,9 the allowed maximum average current $I_{T(AV)}$ is 30 A (the point at which the curve ends). The BTW24 is thus suitable for this application. Drawing the dashed lines for $I_{T(AV)} = 23$ A, $a = 1{,}9$ and $T_{amb} = 45$ °C, we derive: power dissipation $P = 40$ W, required thermal resistance between mounting base and ambient $R_{th\ mb-a} = 1{,}45$ °C/W. The BTW24 thermal resistance between mounting base and heatsink $R_{th\ mb-h} \leqslant 0{,}2$ °C/W. The heatsink thermal resistance follows now from:

$$R_{th\ h-a} = R_{th\ mb-a} - R_{th\ mb-h} = 1{,}45 - 0{,}2 = 1{,}25\ °C/W.$$

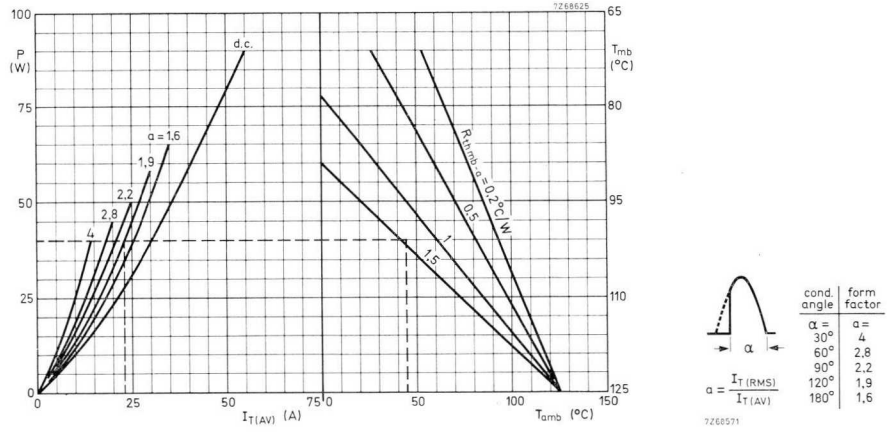


Fig.3-16 Graph for BTW24 thyristor for determining power dissipation and heatsink thermal resistance.

For a blackened 56230 extruded aluminium heatsink, the graph of Fig. 3-17 will apply. Heat removal may occur by free convection or forced cooling. The former method suffices here, and curves are given for 3 W to 100 W power dissipation. Entering into the graph $R_{th\ h-a} = 1{,}25$ °C/W and $P = 40$ W, we obtain from the dashed line: Heatsink length $l = 8$ cm.

Note: If the calculated heatsink is unacceptable, a larger thyristor should be used. The power dissipation and the device thermal resistance will then both become lower, so that a smaller heatsink (larger heatsink thermal resistance) suffices.

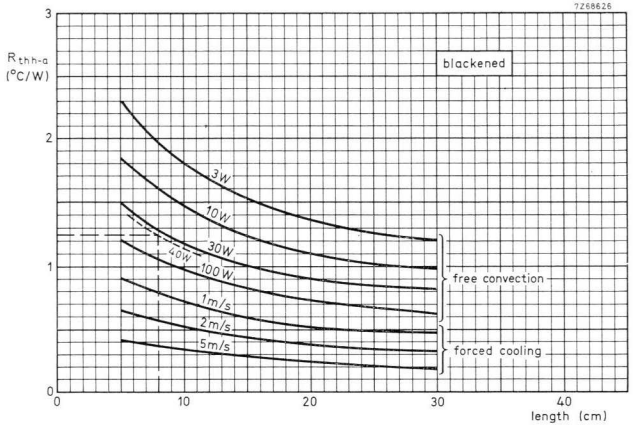


Fig.3-17 Graph for blackened 56230 heatsink extrusion.

4 Power control circuits

4.1 How power is controlled

Power can be controlled intermittently (on/off control – see Section 4.2) or continuously. Systems which provide continuous power control (often called power converters) can deliver either a.c. or d.c. power, regardless of whether their supply is a.c. or d.c. They are subdivided, therefore, as follows:

- a.c. to d.c. converters or controlled rectifiers (Sections 4.4.1 and 4.4.2)
- a.c. to a.c. converters or a.c. controllers (Sections 4.4.1 and 4.4.3)
- d.c. to a.c. converters or inverters (Section 4.5.1)
- d.c. to d.c. converters or choppers (Section 4.5.1)

(The bracketed sections discuss the circuit principle.)

4.2 A.C. static switches

4.2.1 Discussion and circuit survey

A.C. static switches use thyristors or triacs as power control elements and are very useful in on/off control and time-proportional control. Unlike their mechanical counterparts, they do not spark and therefore have an infinitely longer life; further, they are noiseless in operation.

This section gives circuit information for single-phase and three-phase static switches. As with mechanical switches, single-phase types are only suitable for controlling a limited amount of power, because they cause unbalanced loading of the three-phase supply. Where high powers are involved (for instance, industrial heating), three-phase static switches are necessary.

Table 4-1 gives the features of the switches discussed in the following sections, a few explanatory notes being given here. Static switches are synchronous or asynchronous in operation, dependent on whether or not the thyristors are triggered at the mains zero cross-over points. Asynchronous switches are the least expensive, but the jump in thyristor voltage during turn-on, and particularly the high rise rate of current in a resistive load causes considerable radio-frequency interference; in addition, the allowable turn-on di/dt can be easily exceeded. These disadvantages are overcome by using synchronous switches.

Table 4-1 Features of a.c. static switches.

circuit	load
full-wave asynchronous switch, Section 4.2.2	resistive to strongly inductive.
full-wave synchronous switch, Section 4.2.3	approx. 8° max. load phase angle.
half-wave synchronous switch, Section 4.2.4	resistive to strongly inductive.
full-wave synchronous switch for heavily inductive load, Section 4.2.5	approx. 85° max. load phase angle (cos $\varphi = 0{,}1$).
three-phase synchronous switch, Section 4.2.6	resistive to strongly inductive (star or delta).

Because the trigger pulses start *coincidently with the mains zero cross-over points*, the thyristor voltage that occurs during turn-on does not exceed the conduction level, turn-on di/dt is low, and interference is greatly reduced. To prevent the occurrence of one-way conduction and consequent rectification of the load current, the maximum phase angle specified in Table 4-1 must not be exceeded.

An RC-series network should be connected in parallel with the load if the latter is heavily inductive. In this way, rapid turn-on of the controlling power device will be ensured. A 100 Ω (10 W) resistor and a 1,5 μF capacitor in series will suffice in most cases (see Section 1.2.1).

The static switches given here can be controlled by a contact, or by the d.c. output voltage of a circuit block from the 30-series (high noise immunity logic modules), the 60-series or 61-series. In all switches, the control circuit is isolated from the mains supply.

4.2.2 Full-wave asynchronous switch[1])

In the circuit of Fig. 4-1 thyristors TH_1 and TH_2 are triggered immediately when control switch S_1 closes. Operation is therefore asynchronous. The UPA61 functions as the trigger pulse source. Its operation is explained in Section 1.2.1, and further details are given in Section 2.4.3. The p.r.f. of the trigger

[1]) AN No. 131, ordering code 9399 260 63101 - A.C. Static Switch.

pulses is 10 kHz. After S_1 is closed, capacitor C_1 charges via R_1, and trigger pulses are initiated. Alternatively, a switch, or the output of a 60- (61-) series circuit block or a 30-series module, can be connected in parallel with C_1. Also, pin 14 of the UPA61 can be connected to a NOR gate of the 60- or 61-series for logic control (S_1 omitted). In all cases, no trigger pulses occur when C_1 cannot charge.

Fig. 4-2 shows the alternative circuit using a triac. The wiring diagram is given in Fig. 4-3. Table 4-2 gives the a.c. power levels that can be switched (thyristor current not to exceed rated level at 220 V +10%).

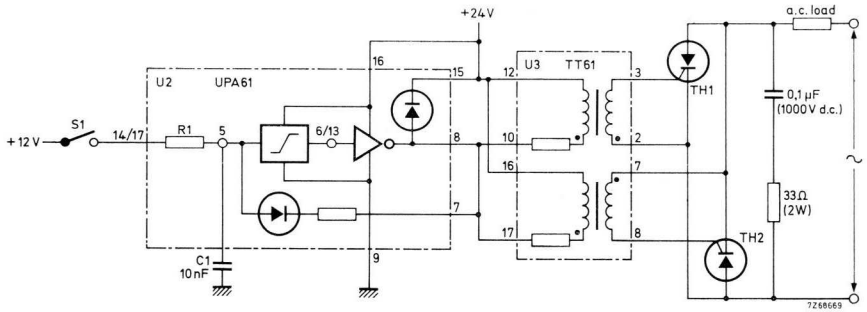


Fig.4-1 Full-wave asynchronous switch.

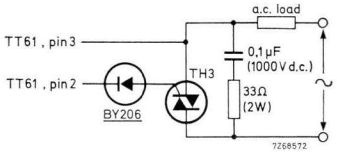


Fig.4-2 Set-up using triac.

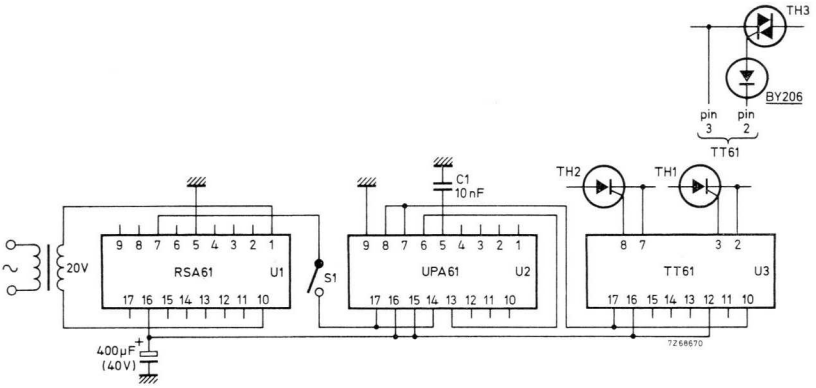


Fig.4-3 Wiring diagram of full-wave asynchronous switch.

Table 4-2 Switched a.c. power for resistive load, 85 °C mounting-base temperature and 220 V ± 10% (single-phase full-wave static switch).

power device	maximum power at 220 V
BTY79-800R*	2,8 kW
BTW38-800RM*	3,9 kW
BTY87-800R*	4,4 kW
BTY91-800R*	6,1 kW
BTW47-800RM*	6,1 kW
BTW92-800RM*	8,8 kW
BTW24-800RM*	15 kW
BTW23-800RM*	39 kW
BTW37-800M**	2,3 kW
BTX94-800**	5,0 kW
BTW34-800M**	9,0 kW

* Two in parallel opposition.
** Triac.

730726-04-01

Automatic assembling of resistors on NORbit p.c. boards.

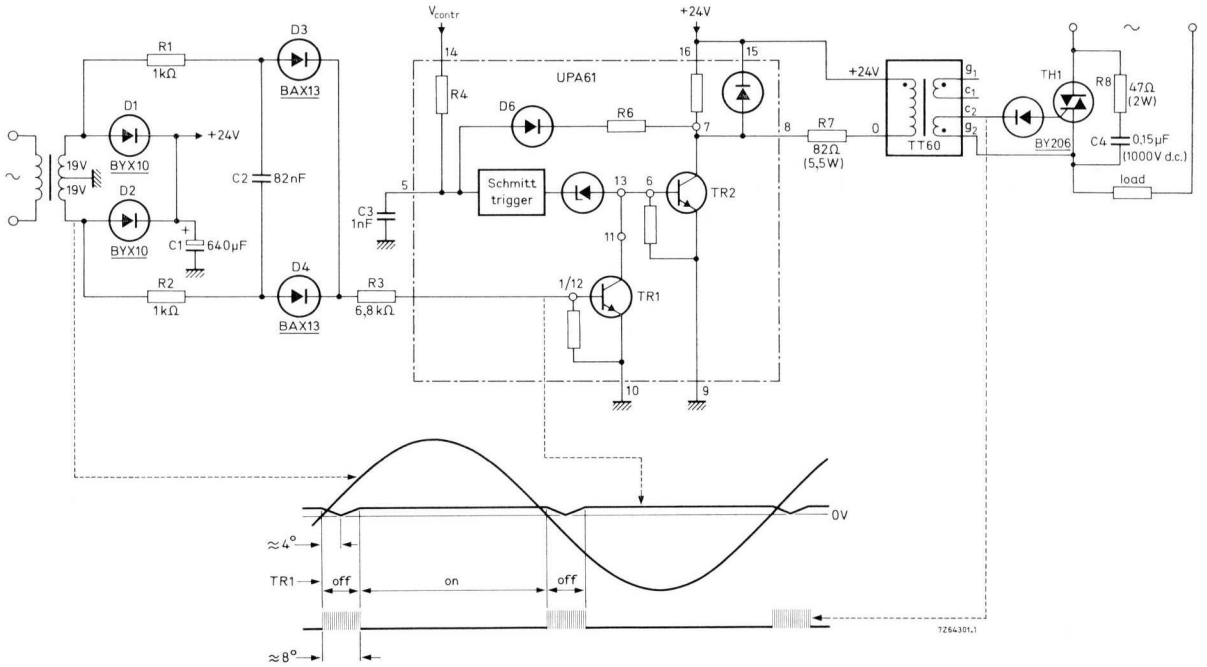


Fig.4-4 Circuit diagram and waveforms of full-wave synchronous switch using triac.

4.2.3 Full-wave synchronous switch[2])

This circuit, illustrated in Fig. 4-4 together with its waveforms, produces short trigger pulse bursts each half cycle, to trigger a triac (or two thyristors in parallel opposition) for full-wave power control. The pulse bursts start coincidently with the mains zero cross-over points (see the waveforms), so that synchronous triggering results. Because the pulse bursts are short, resistive to only slightly inductive loads can be driven (max. load phase angle equal to 8°, which is the pulse burst length).

As seen from the waveforms, the circuit only oscillates during the brief periods whilst there is no base drive to shorting transistor TR_1. The voltage across the secondary of the transformer in Fig. 4-4 is delayed in phase by R_1 C_2 R_2, rectified by D_3 D_4, then applied to the base of TR_1. By proper selection of the value of C_2, oscillations are made to start at the mains zero cross-over points.

Triggering is certain to occur for $V_{contr} \geqslant 11{,}4$ V, and triggering will certainly not take place for $V_{contr} \leqslant 1{,}8$ V.

Figs 4-5 and 4-6 give oscillograms clearly illustrating the operation of the switch. Table 4-2 in Section 4.2.2 gives the levels of power that can be switched.

Adjustment (Fig. 4-7):

If necessary increase (decrease) the value of C_2 to retard (advance) the onset of the trigger pulse bursts, so that triggering starts coincidently with the mains zero cross-over points.

4.2.4 Half-wave synchronous switch[2])

In the circuit of Fig. 4-8, a 90° trigger pulse train is produced once each full cycle, so that 50 Hz unidirectional output pulses will result. One specific application of this circuit producing a d.c. output is in screening equipment for sorting coal, etc. Triggering occurs as long as S_1 is closed. Alternatively, a contact, or the output of a 30-series, 60-series or 61-series circuit block can be connected in parallel with C_{13}. No trigger pulses occur as long as C_{13} cannot charge.

[2]) AN No. 155, ordering code 9399 260 65501 - Truly Synchronous Switches.

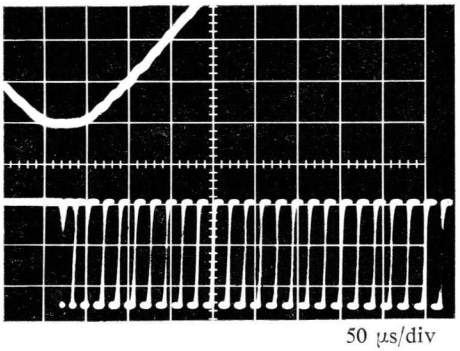


Fig.4-5 Oscillogram showing start of trigger pulse bursts and dip in full-wave rectified voltage (dip coinciding with mains zero cross-over point); it demonstrates synchronous triggering.

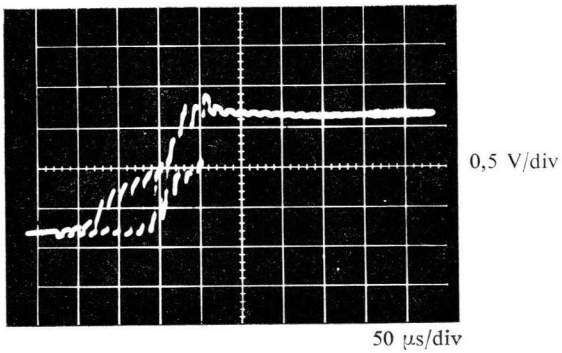


Fig.4-6 During current reversal, triac voltage does not rise above 1 V; so interference-free operation results.

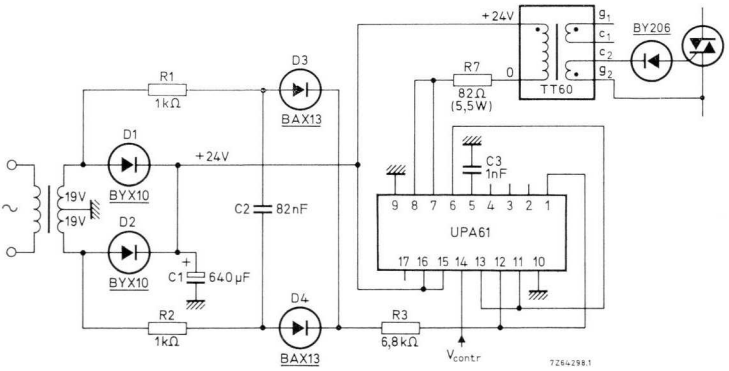


Fig.4-7 Wiring diagram of full-wave synchronous switch.

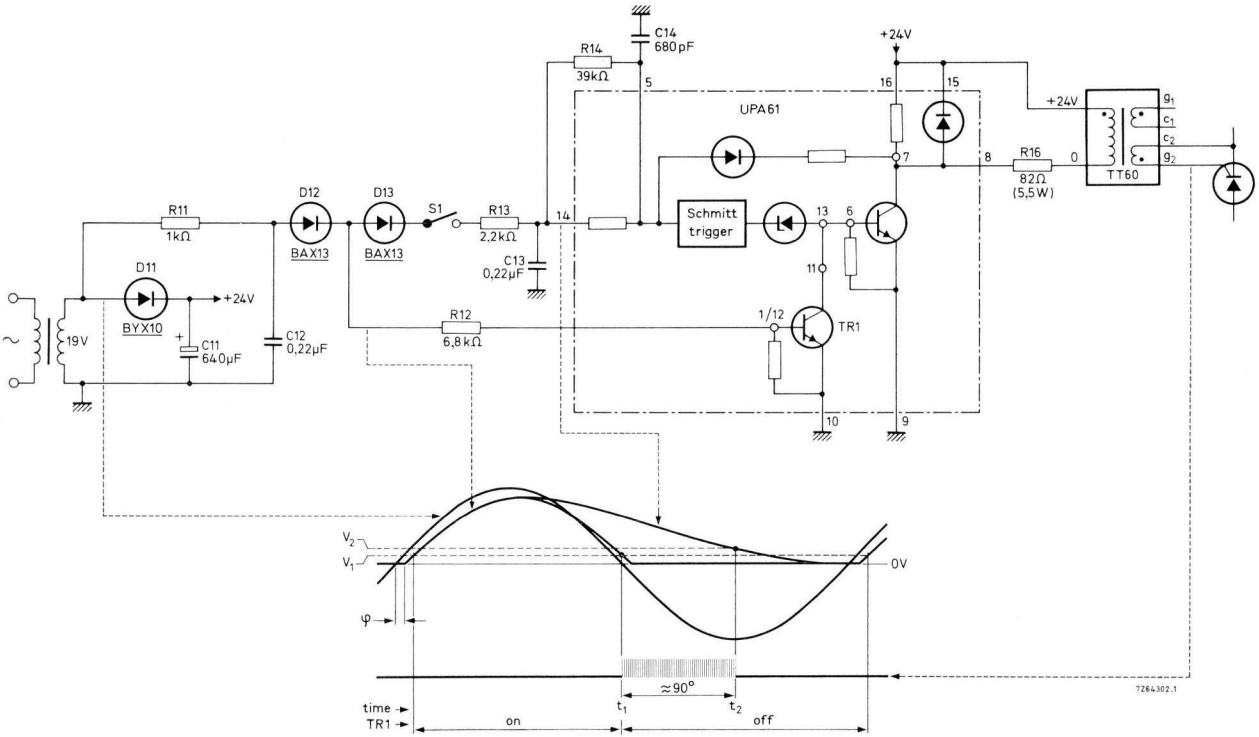


Fig.4-8 Circuit diagram and waveforms of half-wave synchronous switch.
V_1 = switching level of TR_1, V_2 = voltage at which the Schmitt trigger is no longer triggered.

The synchronization voltage is delayed in phase by R_{11} C_{12} and rectified by D_{12}. Capacitor C_{13} is charged via D_{13}, switch S_1 and R_{13}; D_{13} prevents the capacitor from discharging otherwise than into the pulse oscillator input. Trigger pulses are generated from instant t_1 when shorting transistor TR_1 is cut-off until instant t_2 when the voltage across C_{13} is too low to excite the Schmitt trigger. The value of phase-shift capacitor C_{12} is selected so that triggering starts at the mains zero cross-over points.

Table 4-3 gives the allowable levels of switched average current; the current should not exceed rated level when the mains voltage is 10% above its nominal value.

Adjustment (Fig. 4-9):

If necessary increase (decrease) the value of C_{12} to retard (advance) the onset of the trigger pulse bursts, so that triggering starts coincidently with the mains zero passages.

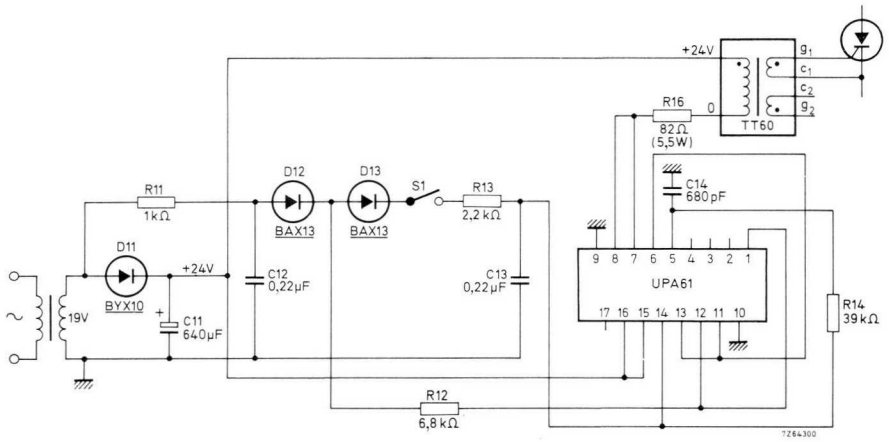


Fig.4-9 Wiring diagram of half-wave synchronous switch.

Table 4-3 Switched average current for 85 °C mounting-base temperature and 220 V ± 10% (single-phase half-wave static switch).

power device	maximum average current at 220 V
BTY79-800R	5,7 A
BTW38-800RM	8,1 A
BTY87-800R	9,0 A
BTY91-800R	12,6 A
BTW47-800RM	12,6 A
BTW92-800RM	18 A
BTW24-800RM	27 A

4.2.5 Full-wave synchronous switch for heavily inductive load[3])

The circuit in Fig. 4-10 generates a trigger pulse burst during about 300° of each a.c. cycle, and is therefore suitable for controlling a load with a phase angle up to 85° (cos φ equal to 0,1). It comprises a synchronization unit, a monostable (see Section 1.2.2) and a 10 kHz pulse generator (see Section 2.4.3). Triggering occurs for the d.c. control voltage $V_{contr} \leqslant 2$ V, and is inhibited when $V_{contr} \geqslant 5$ V.

The emitter follower of the UPA61 functions as a feedback link, so that the width of the monostable output pulses is not greatly influenced by mains voltage and temperature fluctuations. As soon as the Schmitt trigger trips on (Schmitt trigger output becoming HIGH) the emitter follower drives the inverting stage into saturation so that charging of C_3 stops abruptly at the trip-on level. The width of the output pulses is almost constant because it depends solely on the ratio of the Schmitt trigger trip-on and trip-off levels, this ratio changing little with variations in the d.c. supply voltage and temperature. Adjustment of R_3 varies the pulse width by setting the discharge rate of C_3.

Switched power levels are given in Table 4-2 (Section 4.2.2).

Adjustment (Fig. 4-11):

Set R_3 to make the length of the trigger pulse bursts (U_3, pin 8) equal to about 300° (17 ms at 50 Hz supply).

[3]) AN No. 138, ordering code 9399 260 63801 - Synchronous On/off and Time-proportional Controllers.

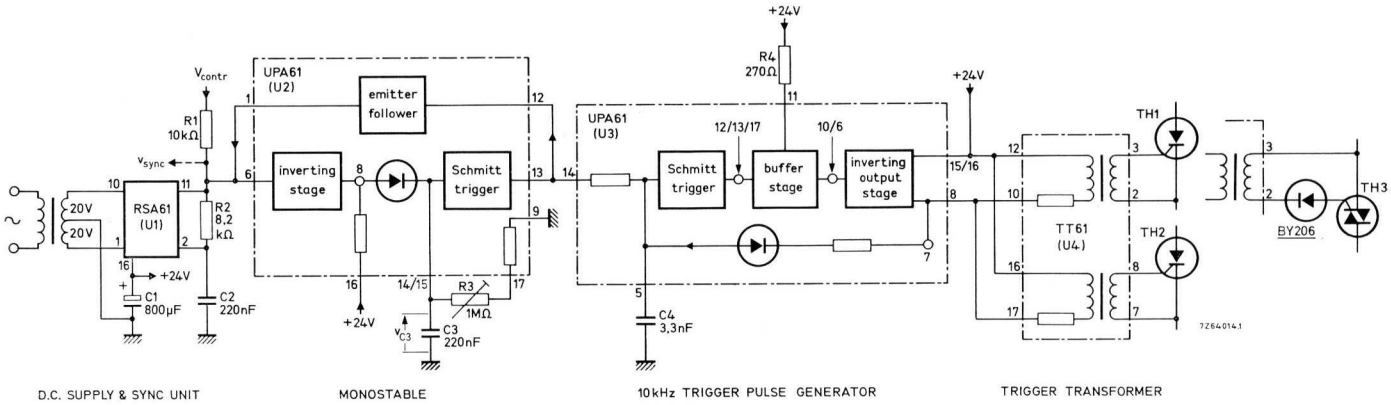


Fig.4-10 Full-wave synchronous switch for very inductive load.

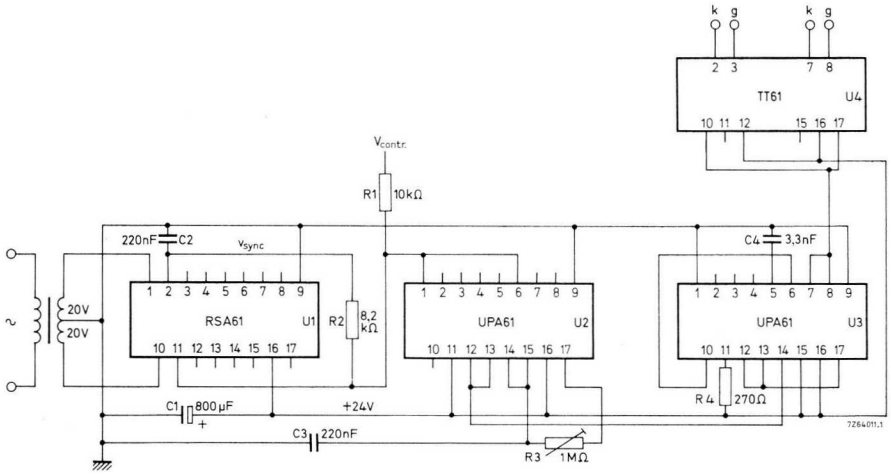


Fig. 4-11 Wiring diagram of full-wave synchronous switch for very inductive load.

4.2.6 Three-phase synchronous switch[4])

The three-phase synchronous switch discussed here uses only two triacs, but it requires symmetrical loading, otherwise synchronous switching will not occur and r.f. interference will result.

Fig. 4-12 shows the basic circuit. For $V_{contr} \leqslant 2$ V the circuits triggering *TH(Y)* and *TH(R)* are operative, and power is supplied to the load. The trigger signals for *TH(Y)* and *TH(R)* are denoted *(Y)* and *(R)*, respectively. First, *TH(Y)* is triggered at t_1 when phase-to-phase voltage *B-Y* passes through zero (trigger circuit I synchronized by *B-Y*). Then, *TH(R)* is triggered at t_2, the zero cross-over point of phase *R* (trigger circuit II synchronized by phase-to-neutral voltage *R-O*).

[4]) AN No. 191, ordering code 9399 260 69101 - Three-phase Synchronous Time-proportional Controller.

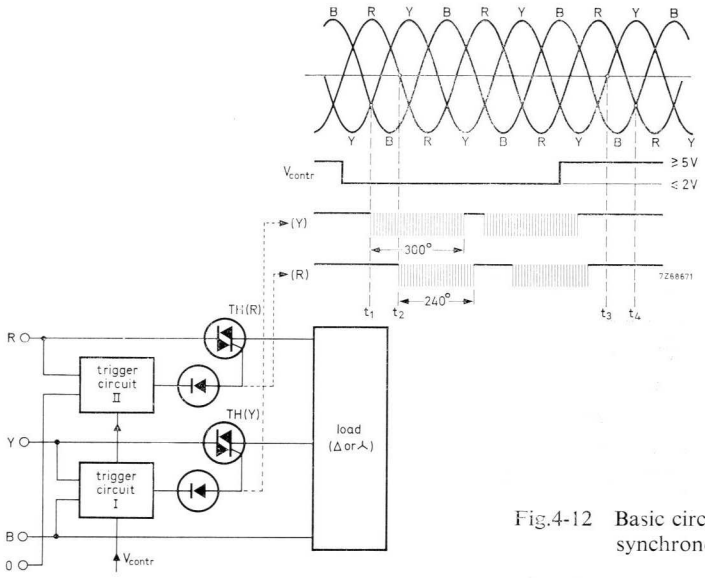


Fig.4-12 Basic circuit of three-phase synchronous switch.

With $V_{contr} \geqslant 5$ V, *TH(Y)* turns off when the current in phase *Y* drops to zero (time t_3). Current now only flows between phases *R* and *B*. Consequently, *TH(R)* ceases to conduct when the instantaneous voltages of phases *R* and *B* become equal (time t_4).

The waveforms *(Y)* and *(R)* in Fig. 4-12 show that triggering is maintained over at least 240°, which ensures that the triacs conduct every half cycle even when driving a highly inductive load.

Fig. 4-13 is a more elaborate diagram. The upper half represents trigger circuit I in Fig. 4-12 triggering *TH(Y)*, and the lower half is trigger circuit II triggering *TH(R)*. Synchronization voltages $v_{sync\ I}$ and $v_{sync\ II}$ are derived from *B-Y* and *R-O*. The operation of the synchronization circuit and the monostable was described in Section 1.2.2. The pulse generator is connected as a high-power pulse source (Section 2.4.4). Waveforms *(Y)* and *(R)* represent the trigger signals (compare with the waveforms in Fig. 4-12).

Monostable I has positive feedback via R_7 to maintain the duration of the trigger pulse bursts at about 300° independent of d.c. supply voltage fluctuations. (This method of stabilizing pulse burst duration is discussed in Section

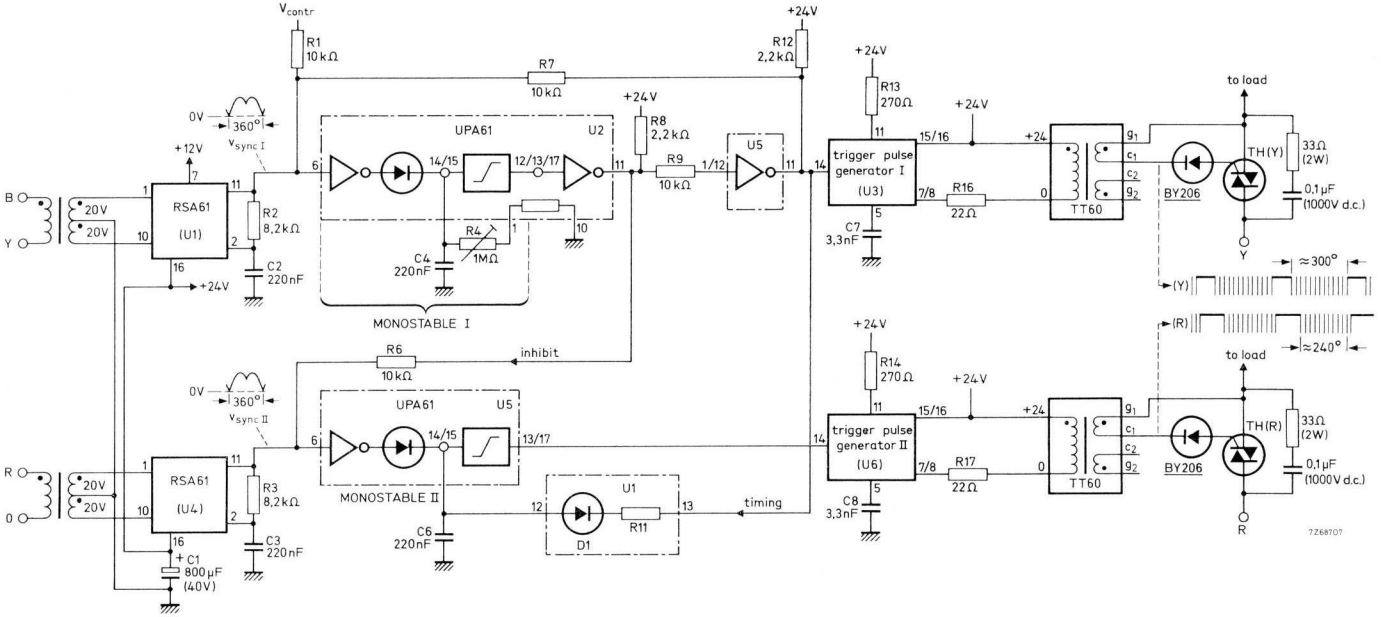


Fig.4-13 Three-phase synchronous switch.

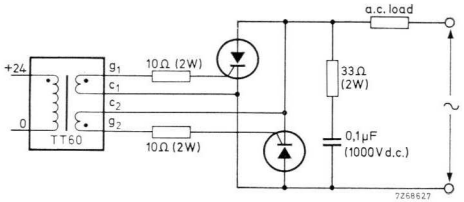


Fig.4-14 Circuit modification for thyristors in anti-parallel.

4.2.5.) The pulse burst duration of monostable II is "timed" by discharge of timing capacitor C_6 via D_1 R_{11}; that is, the capacitor starts to discharge as soon as the output of monostable I, and thus U_5 pin 11, goes LOW (pulse bursts *(R)* about 240° long).

Inhibiting via R_6 ensures that the lower half of the circuit cannot produce trigger pulses while the upper half is in standby.

Fig. 4-14 shows a circuit modification for the use of thyristors in anti-parallel rather than triacs. Note the polarity of the transformer connections on the left of the lay-out in Fig. 4-15. Table 4-4 gives the allowable switched power levels.

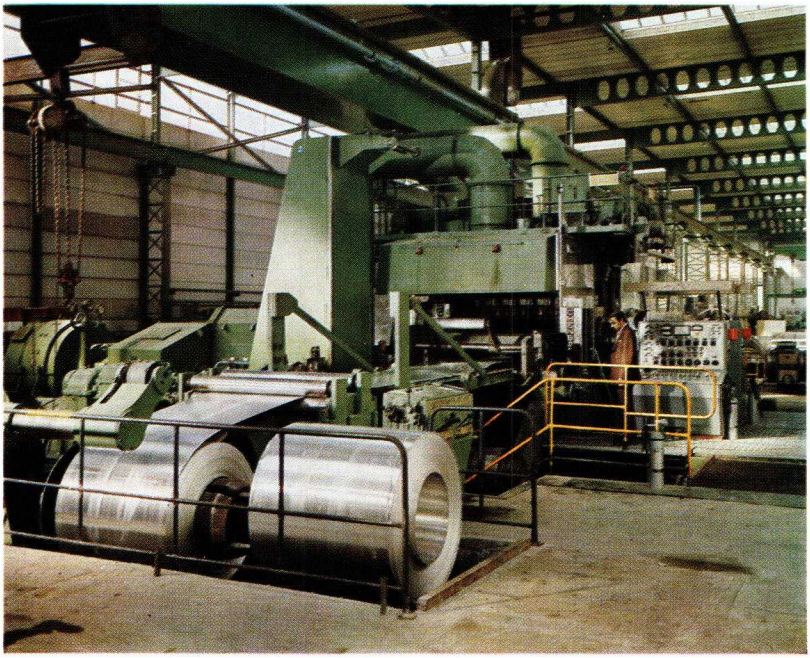
Adjustment (Fig. 4-15):

1. *Check that the phase sequence is R-Y-B (Fig. 4-12); if necessary, exchange the connections of two phases.*
2. *Adjust R_4 so that the length of the pulse bursts at U_3 pin 8 is about 300°.*

Table 4-4. Switched a.c. power for resistive load, 85 °C mounting-base temperature and 380 V ± 10% phase-to-phase voltage (three-phase full-wave static switch).

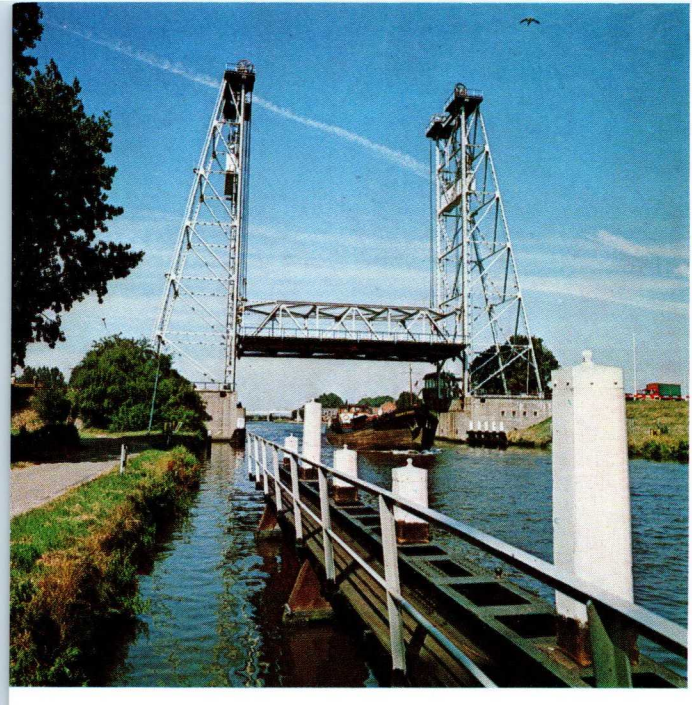
power device	maximum power at 380 V
BTY79-1000R*	8,4 kW
BTW38-1200RM*	11,8 kW
BTW47-1200RM*	18 kW
BTW92-1200RM*	26 kW
BTW24-1200RM*	46 kW
BTW23-1200RM*	118 kW
BTX41-1200R*	210 kW
BTW37-1200M**	7,1 kW
BTX94-1200*	15 kW
BTW34-1200M**	27 kW

* Two in parallel-opposition.
** Triac.



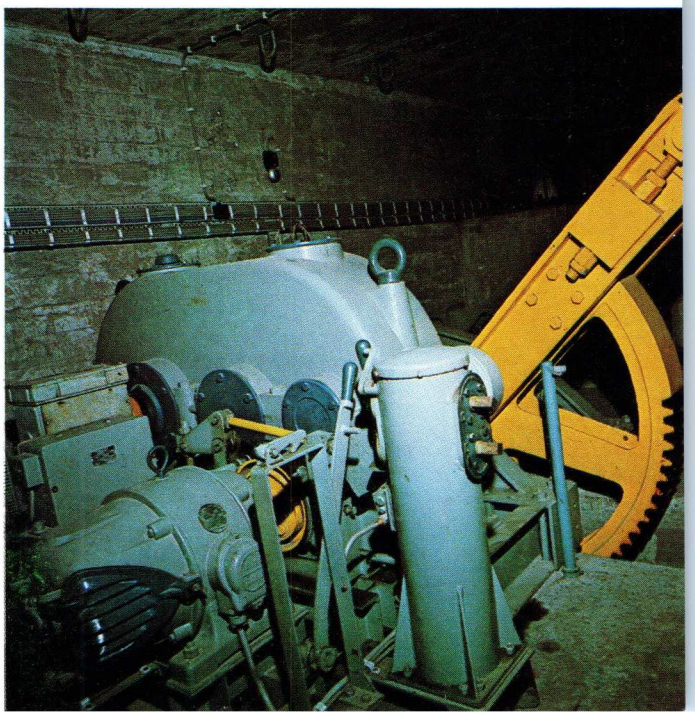
This 3-ton reversing aluminium rolling mill has a triple electronic Ward-Leonard drive. The power fed to the rolling motor is 1,2 MW and that to each of the reel motors 0,46 MW. Control is obtained by armature current and field strength variation.

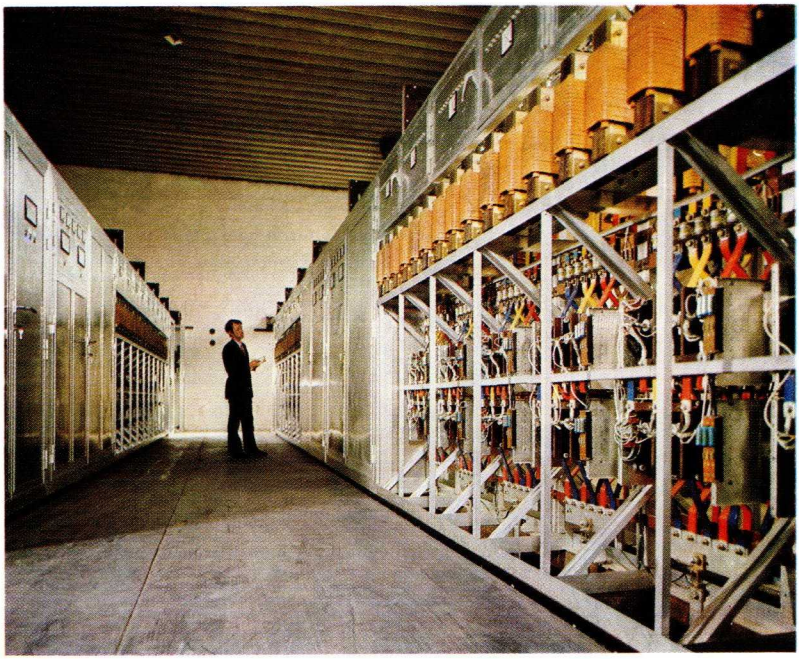
Courtesy of N.V. Remi, Claeys, Lichtervelde, Belgium.



Lift bridge (upper picture) and draw bridge (lower picture) are interlocked so that their opening will cause minimum traffic congestion. NORbit control system also ensures safe operation of remote-controlled draw bridge.

Central control desk (upper picture) and draw bridge drive motor (lower picture). *Courtesy of Elektrotechnisch Bureau Langezaal & Inniger, Leiden, The Netherlands.*





The triple motor control system for the 10-ton reversing aluminium rolling mill (picture facing p. 92) uses 276 thyristors BTX41 arranged in 46 three-phase, full-controlled bridges. The rolling motor takes 3350 A at 300 V and each reel motor 2500 A at 185 V.

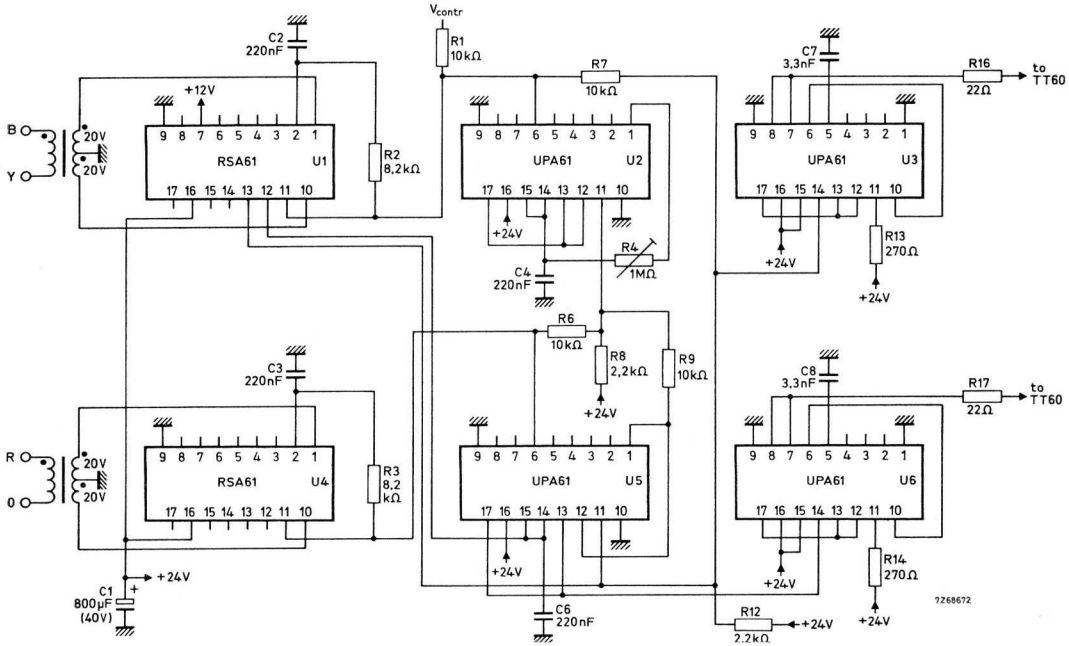


Fig.4-15 Wiring diagram of three-phase synchronous switch. B-Y = phase-to-phase voltage, R-O = phase-to-neutral voltage.

4.3 Time-proportional controllers

4.3.1 Discussion and circuit survey

Time-proportional control has gained wide popularity because it is as simple as on/off control but has the accuracy of the much more complex proportional control system. An outstanding property is its inherently linear performance, which ensures a constant open-loop gain in automatic control. Advantages, prominent where high powers are involved, are an optimum power factor and little radio-frequency interference. Further, the controlling power devices are subjected to a low di/dt during turn-on. The principle of time-proportional control was discussed in Section 1.2.2. This control method is suitable for processes having a reaction time down to a few a.c. cycles, and the largest application area is in industrial heating. However, time-proportional control may give rise to unacceptable light flicker owing to the rhythmic voltage variations it causes. It should be noted that these disturbances may be particularly irritating for power switching rates between 0,1 Hz and 30 Hz.

Time-proportional control is, to all intents and purposes, on/off control with a fixed repetition rate. That is, a rectangular-wave generator can be used to control an a.c. static switch, the average output power passed by the switch being determined by the duty cycle of the generator output. One such circuit set-up was evolved in Section 1.2.2, and similar arrangements, partially based on the switches discussed in Section 4.2, are given here. The survey in Table 4-5

Table 4-5 Features of time-proportional controllers.

circuit	load	notes
single-phase controller, Section 4.3.2	approx. 85° max. load phase angle ($\cos \varphi = 0{,}1$)	—
single-phase controller with adjustable trigger delay, Section 4.3.3.	approx. 85° max. load phase angle ($\cos \varphi = 0{,}1$).	avoids inrush currents associated with an iron-cored load.
three-phase controller, Section 4.3.4.	resistive to strongly inductive (star or delta).	—
single-phase temperature controller, Section 4.3.5.	max. 25 kW; resistive.	closed loop; $\pm$ 1 °C accuracy over a 18 °C to 23 °C range.

will be helpful in the choice for any particular application. Controller operation is synchronous with the exception of the controller having an adjustable trigger delay, this being necessary to suppress the high saturation current associated with an iron-cored load. The power levels that can be controlled are given in Table 4-2 (Section 4.2.2) and Table 4-4 (Section 4.2.6).

4.3.2 Single-phase time-proportional controller[5])

The synchronous controller circuit in Fig. 4-16 is grouped around the switch discussed in Section 4.2.5. The time base generator, U_5, is free-running and its sawtooth output is converted (by the rectangular-wave generator, U_6) into a rectangular signal commanding the a.c. static switch, U_1 to U_4. Control voltage V_{contr} applied to U_6 determines the average a.c. output power. This circuit diagram resembles Fig. 1-8, and reference is made to Section 1.2.2 for a full circuit description.

Fig. 4-17 gives the relationship between the power switching rate, f, and the capacitor charging resistor, R_5 (denoted R). For R_5 equal to 1 MΩ, f is 1,5 Hz and thus the repetition period t_o is 1/1,5 s or about 0,65 s (see the waveforms in Fig. 4-16). The linear relationship between average controller output power (proportional to the controller output duty cycle δ) and control voltage V_{contr} is clearly demonstrated by the plot of Fig. 4-18.

Adjustment (Fig. 4-19):

1. *Set R_3 to obtain a trigger pulse burst duration (U_3 pin 8) of about 300° (17 ms at 50 Hz supply).*
2. *Set the repetition period of time-proportional control, t_o, to the desired value by changing the resistance of R_5 (consult Fig. 4-17); if necessary increase C_5 to obtain a higher value for t_o.*

[5]) AN No. 138, ordering code 9399 260 63801 - Synchronous On/off and Time-proportional Controllers.

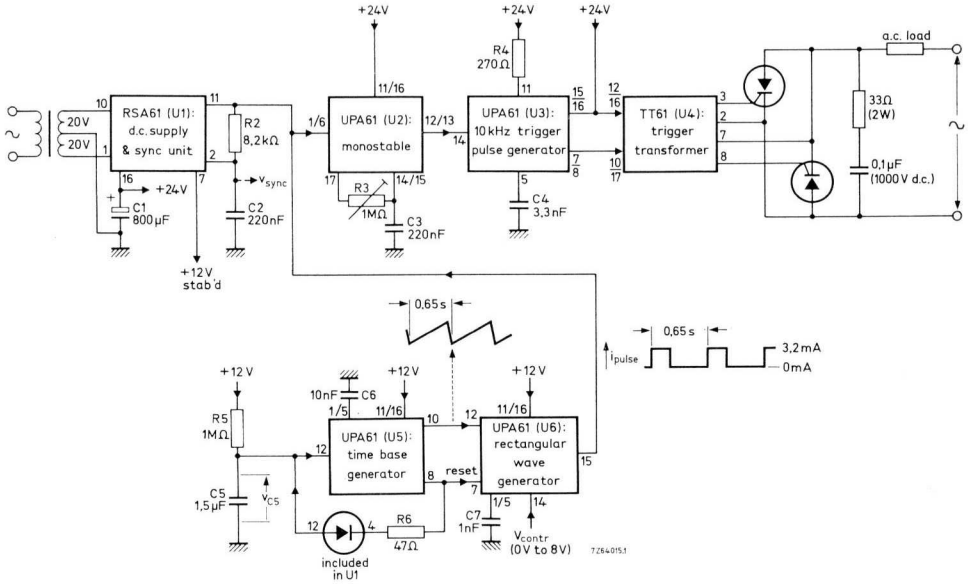


Fig.4-16 Synchronous time-proportional controller.

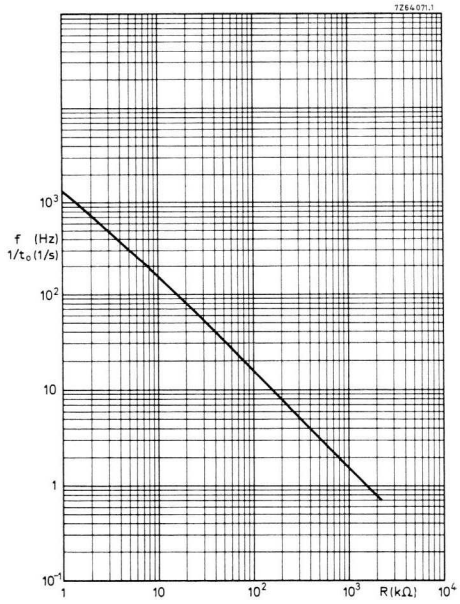


Fig.4-17 Power switching rate *(f)* and repetition period *(t_o)* of time-proportional control vs. capacitor charging resistor *R* (R_5 in Fig.4-16); timing capacitor (C_5) equal to 1,5 μF.

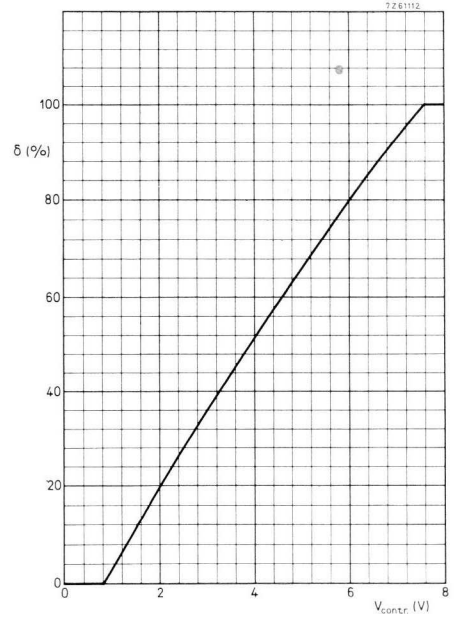


Fig.4-18 Plot showing linearity between duty cycle δ of controller output and V_{contr} (10 Hz switching rate).

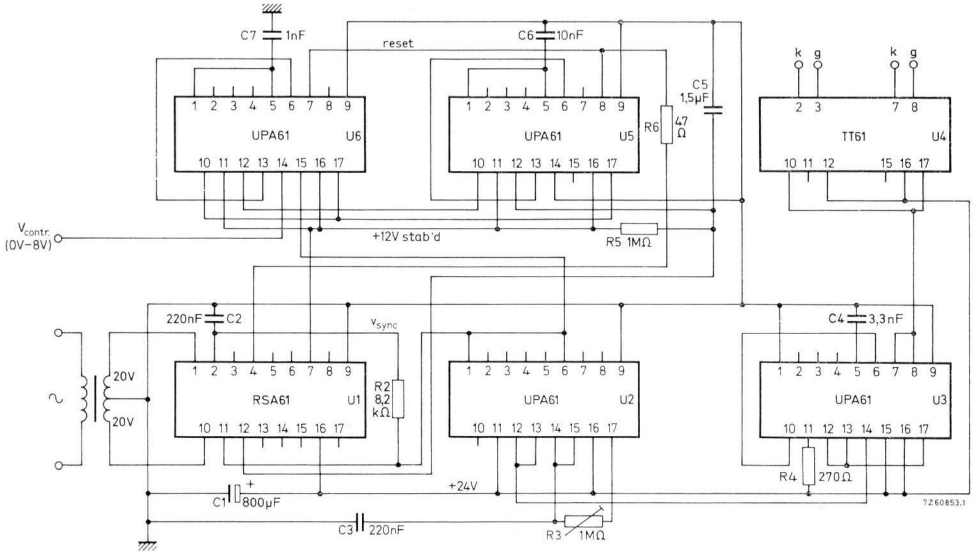


Fig.4-19 Wiring diagram of synchronous time-proportional controller.

4.3.3 SINGLE-PHASE TIME-PROPORTIONAL CONTROLLER WITH ADJUSTABLE TRIGGER DELAY[6])

Synchronous switching of an iron-cored load (e.g. a transformer) causes a large repetitive inrush current owing to core saturation. Where repetitive ratings are jeopardized, trigger delay should be used. Saturation currents will be avoided when the trigger delay is roughly equal to the load phase angle. (If the trigger delay is excessive, core saturation in the opposite direction will occur!).

Fig. 4-20 shows a circuit, which prevents core saturation. Trigger delay is adjustable between 0° and about 50°. Circuit operation is clear from the waveforms. The leading edges of the monostable output pulses are delayed while being passed through charging network R_9 C_7 R_{10} and the trigger pulse delay gate. The amount of trigger delay, ϑ, depends on the charge rate of C_7 and is adjusted with R_9. Diode D_1 ensures a rapid discharge of C_7 at the end of the monostable output pulses, and D_2 provides level shifting. The output of the trigger pulse delay gate will certainly be HIGH (trigger pulses generated) for a d.c. gate input of 4 V or higher; it will become LOW with certainty (trigger pulses inhibited) when the d.c. gate input is 0,4 V, or lower.

Fig. 4-21 gives oscillograms showing clearly the beneficial effect of the circuit. Linearity of control follows from Fig. 4-18 in the previous section.

[6]) AN No. 142, ordering code 9399 260 64201 - Time-proportional Controller for Transformer Loads.

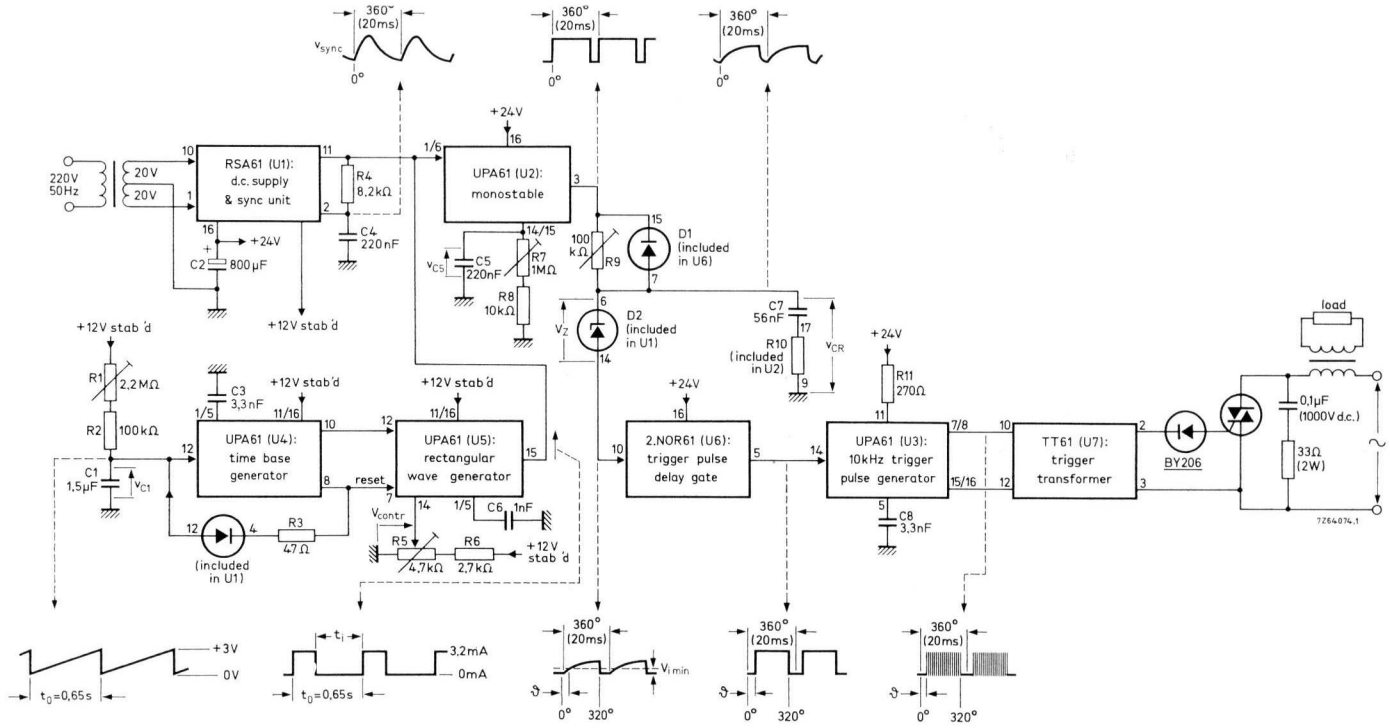


Fig.4-20 Time-proportional controller with adjustable trigger delay (ϑ). For R_1 set at 900 kΩ, the repetition period, t_o, is 0,65 s as shown.

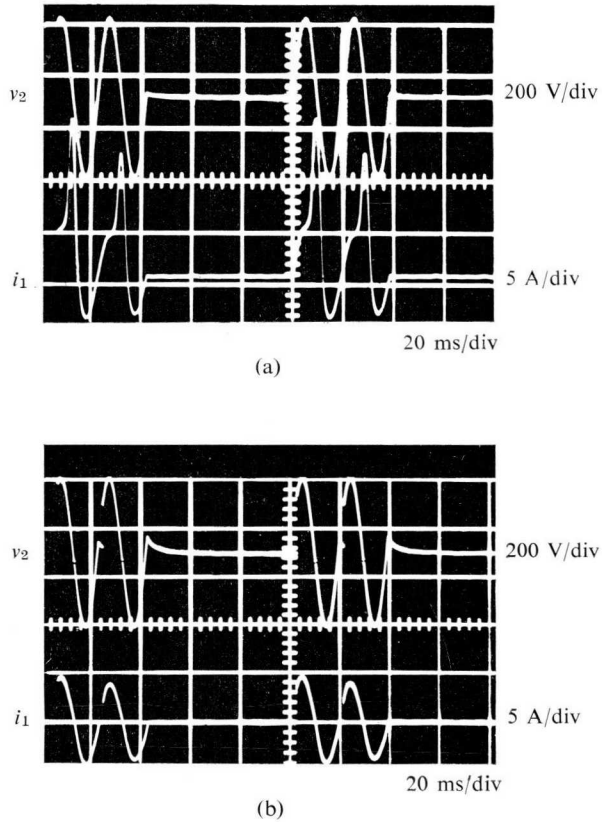


Fig.4-21 Secondary voltage v_2 and primary current i_1 of triac-controlled transformer. Inrush current (oscillogram *a*) disappears when applying trigger delay (oscillogram *b*).

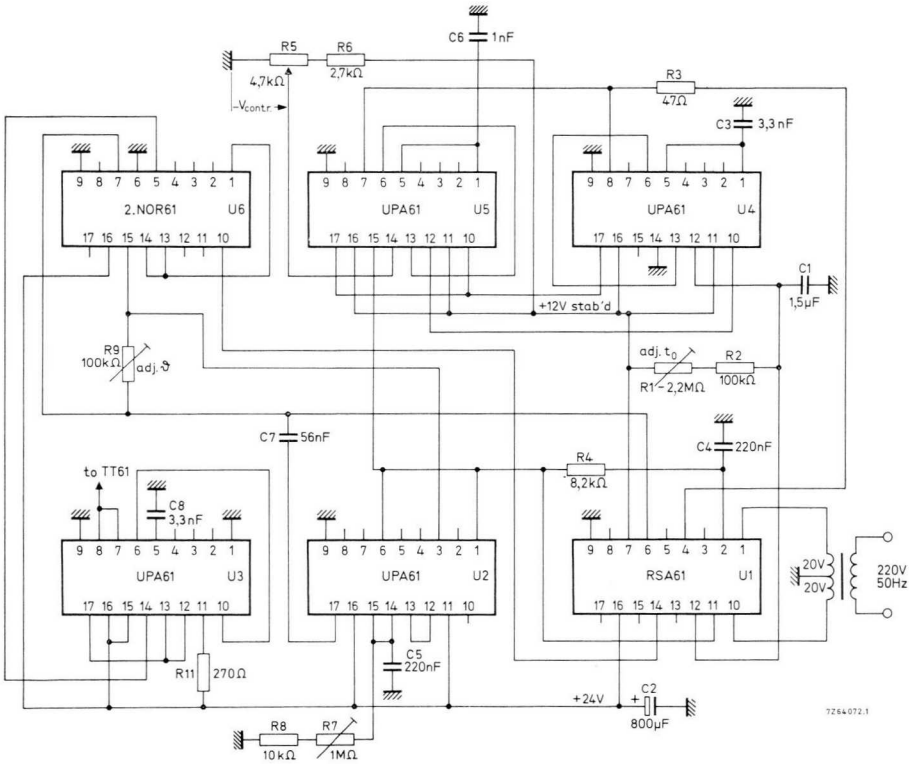


Fig.4-22 Wiring diagram of time-proportional controller with adjustable trigger delay.

Adjustment (Fig. 4-22):

1. *Set the repetition period of time-proportional control, t_o, to the desired value by adjusting R_1 (t_o read from Fig. 3-17 when taking $R_1 + R_2$ for R); if necessary increase C_1 to obtain a higher value for t_o.*
2. *Set R_7 to obtain a trigger pulse burst duration (U_3 pin 8) of about 300° (17 ms at a 50 Hz supply).*
3. *The trigger delay required to prevent a repetitive transformer inrush current is obtained as follows:*
   - 3a. *Connect a d.c. voltmeter, with not less than 10 kΩ/V resistance, across the transformer primary through a 100 kΩ, 10 µF smoothing filter (the capacitor should be an a.c. type).*
   - 3b. *Adjust R_5 so that one or only a few a.c. cycles occur per repetition period t_o.*
   - 3c. *With R_9 set the trigger delay so that at the intended transformer load the meter deflection becomes zero.*

   Note: Re-adjustment of R_9 may be necessary if the transformer load changes.

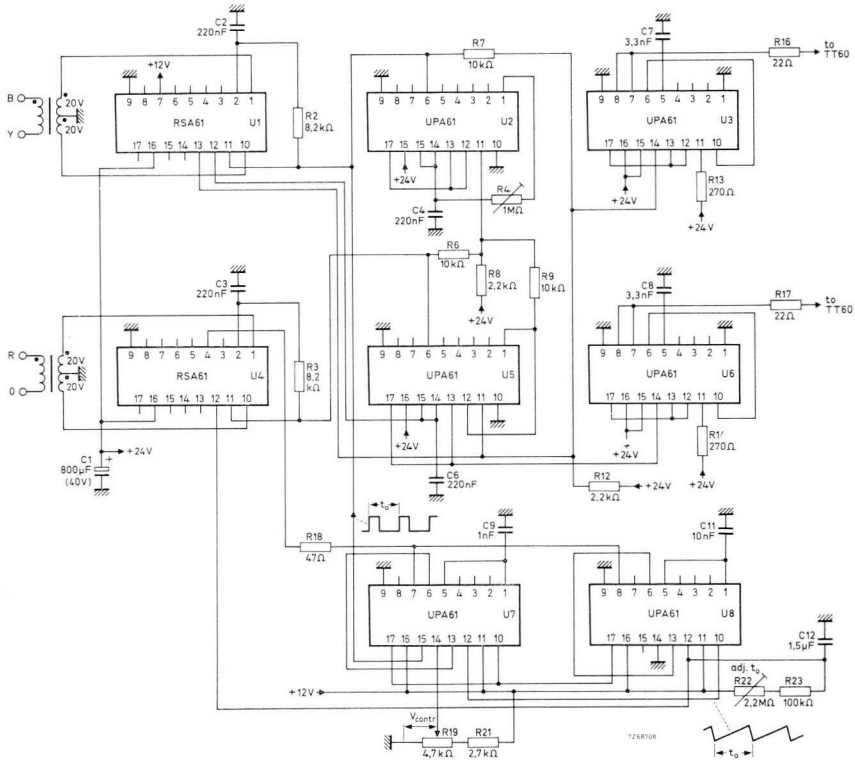


Fig.4-23 Wiring diagram of three-phase time-proportional controller.
B-Y = phase-to-phase voltage, R-O = phase-to-neutral voltage.

4.3.4 Three-phase time-proportional controller

Fig. 4-23 shows the lay-out of a three-phase controller based on the three-phase switch given in Section 4.2.6. The switch is controlled by a rectangular-wave generator, U_7, whose output current from pin 15 is shown by the waveform (t_o is the repetition period of time-proportional control). This generator derives its sawtooth input from the output at pin 10 of the time base generator, U_8 (see waveform). The duty cycle of the rectangular output, and thus the average power in the load, increases with V_{contr} applied to U_7 pin 14.

Adjustment (Fig. 4-23):

1. *Check that the phase sequence is R-Y-B (Fig. 4-12. Section 4.2.6): if necessary, exchange the connections of two phases.*
2. *Set R_4 to obtain a trigger pulse burst duration at U_3 pin 8 of about 300° (17 ms at a 50 Hz supply).*
3. *Set the repetition period of time-proportional control, t_o, to the desired value by adjusting R_{22} (t_o read from Fig. 4-17 when taking $R_{22} + R_{23}$ for R); if necessary increase C_{12} to obtain a higher value for t_o.*

4.3.5 SINGLE-PHASE TEMPERATURE CONTROLLER[7])

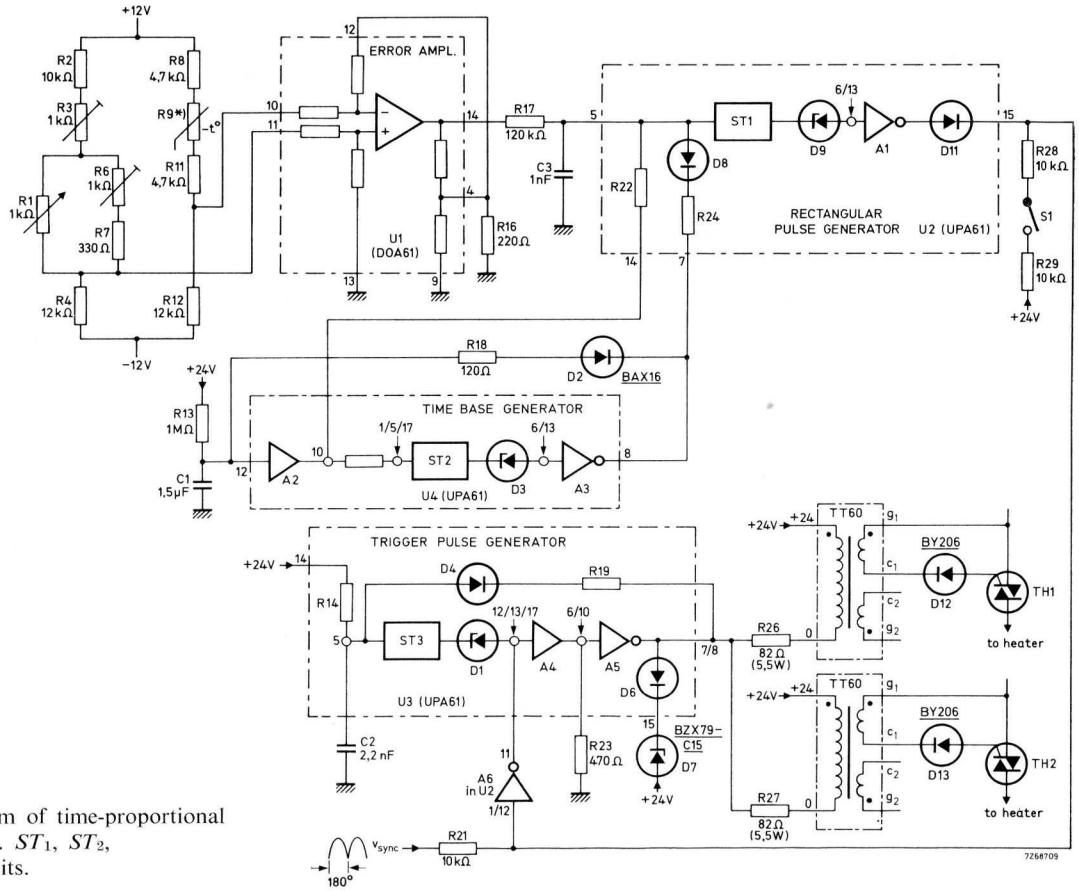
In the automatic temperature controller shown in Fig. 4-24, the error amplifier is fed by the temperature-conscious bridge, R_1 to R_{12}; R_9 is the temperature sensor, and temperature is adjusted with R_1. Control accuracy is $\pm$ 1 °C over the range 18 °C to 23 °C. The system accepts $\pm$ 30% mains fluctuations. Circuit operation is as follows.

While the output of the rectangular-pulse generator is LOW, amplifier A_6 is held in saturation by the synchronization voltage V_{sync}, except for the short intervals coinciding with the zero cross-over points of the mains voltage. During these intervals, A_6 is cut off and thus cannot short the input to A_4. The pulse generator triggers the triacs which supply power to the heaters. (Because the pulse bursts have a short duration, only a resistive load can be controlled.) The HIGH output of the rectangular-pulse generator supplies base current to A_6 keeping it in saturation, the trigger pulse generator cannot function, and the triacs do not conduct.

With decreasing temperature, the potential at the inverting input of the error amplifier decreases and that at the amplifier output increases. As a result, the duty cycle of the rectangular-pulse generator output decreases and more average power is supplied to the heaters, counteracting the decrease in temperature. Closure of S_1 switches off the heater supply.

Fig. 4-25 shows the d.c. supply and synchronization circuit. Network R_{53} C_{53} R_{54} delays v_{sync}, so that triac triggering starts at the mains zero cross-over points. Fig. 4-26 shows the power circuit. Mounted on an 11 cm modular heatsink (see the Appendix), each triac can handle 6,25 kW, taking into account 35 °C max. ambient temperature and $\pm$ 30% a.c. input fluctuations. Because up to four triacs can be triggered, the total power handling capacity is 25 kW.

[7]) AN No. 167, ordering code 9399 260 66701 - Time-proportional Temperature Controller.



*) NTC resistor
code no: 2322 640 90002

Fig.4-24 Schematic diagram of time-proportional temperature control system. ST_1, ST_2, ST_3 = Schmitt trigger cricuits.

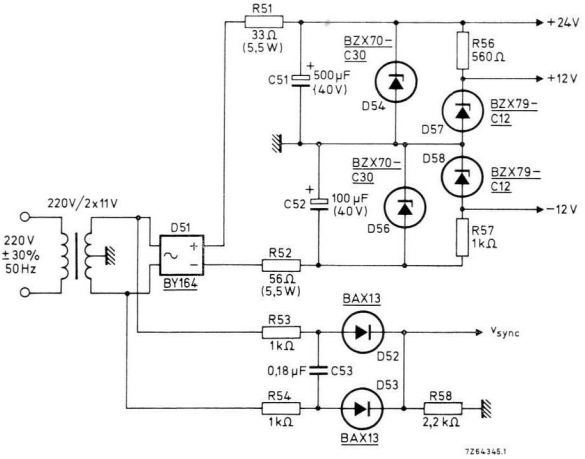


Fig.4-25 D.C. supply and synchronization circuit.

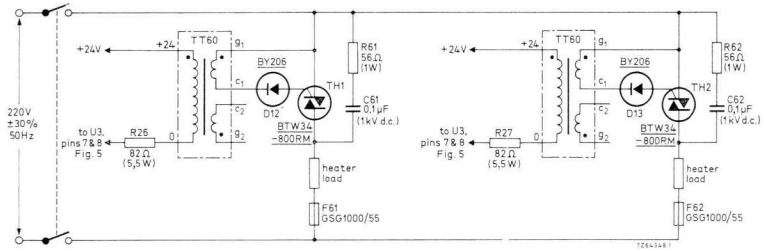


Fig.4-26 Power circuit.

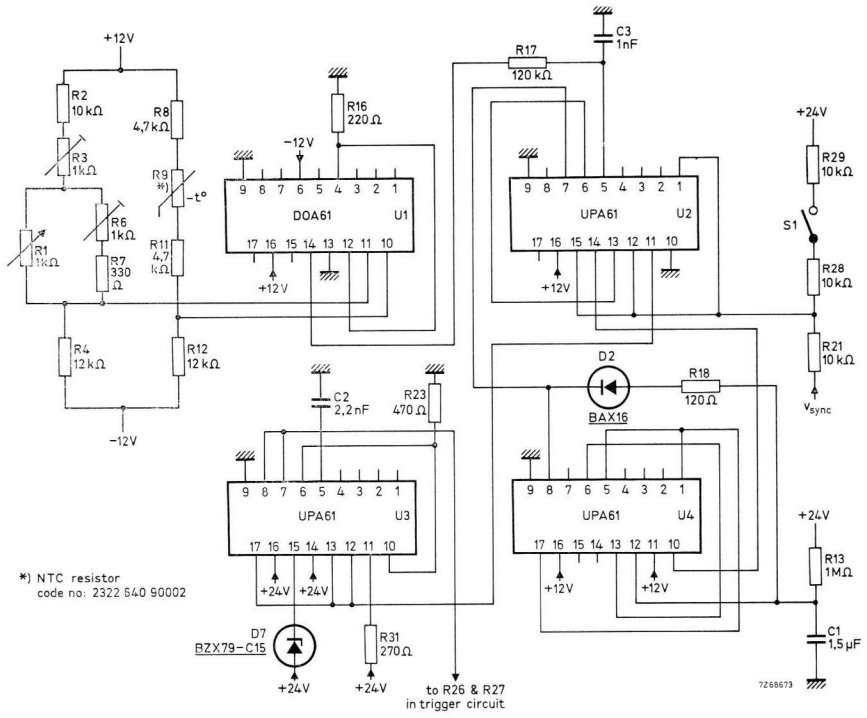


Fig.4-27 Wiring diagram of time-proportional temperature control system.

Adjustment (Fig. 4-27):

1. *Set R_1 R_3 and R_6 to minimum resistance.*
2. *Expose temperature sensor R_9 to 23 °C and adjust R_3 so that the output of the error amplifier (U_1 pin 14) is zero.*
3. *Set temperature-adjust potentiometer R_1 to maximum resistance.*
4. *Expose temperature sensor R_9 to 18 °C and adjust R_6 so that the output of the error amplifier is zero.*
5. *Increase the value of R_{16} if control instability arises; a value of R_{16} up to 1 kΩ will be satisfactory in most cases.*
6. *It may be necessary for optimum control performance to change the repetition period of the time-proportional control system; this is achieved by changing the value of R_{13} (repetition period t_o read from Fig. 4-17 when taking R_{13} for R); if necessary, increase C_1 to obtain a large value for t_o.*

4.4 Phase-shift controllers

4.4.1 Control principle

Phase control is indispenable where d.c. power is involved or where a short reaction time is essential, for instance, for motor control. Phase control is characterized by:

(1) low power factor,
(2) high turn-on di/dt under resistive load and under d.c. inductive load using a free-wheeling diode,
(3) radio-frequency interference due to step changes in thyristor voltage and current during turn-on.

Excessive turn-on di/dt is avoided by connecting small reactors (a few mH) in series with the power devices, saturable types giving the least voltage loss; use of a suppression filter in the a.c. input lines reduces radio-frequency interference.

Phase-shift controllers are fed from a sinusoidal power source, usually the 50 Hz mains supply, and they control d.c. or a.c. power by varying the trigger angle and thus the conduction angle of the control element(s) in series with the load: see Fig. 4-28. This control method is known as phase control. The most important phase shift controller types – controlled rectifier and a.c. controller circuits – will be discussed in Sections 4.4.2 and 4.4.3.

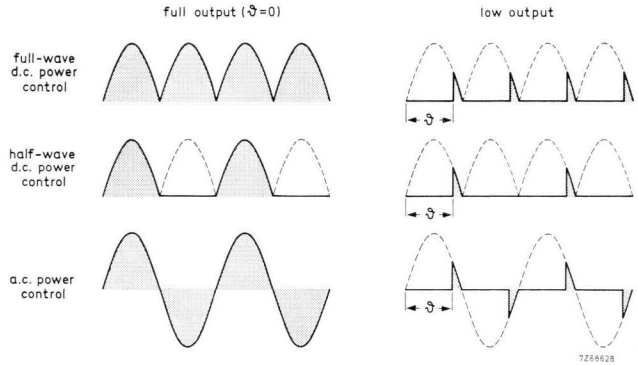


Fig.4-28 D.C. and a.c. phase control; ϑ = trigger angle.

4.4.2 Basic controlled rectifier circuits

There are controlled rectifier circuits suitable for single-phase and three-phase input. The hatched waveforms given in the following illustrations show the rectifier output for the thyristor trigger angle, ϑ, equal to 90°, and for a resistive load.

Single-phase half-wave circuit

The simplest controlled rectifier circuit is shown in Fig. 4-29. It uses only one thyristor. Disadvantages are its low power factor, the existence of a d.c. input current, and difficulty in smoothing the d.c. output. The circuit is useful in low-power, transformerless applications, such as the control of universal motors.

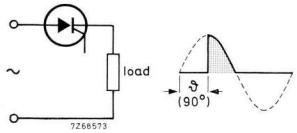


Fig.4-29 Single-phase half-wave controlled rectifier.

Single-phase half-controlled bridge

The circuit of Fig. 4-30 has a much higher power factor, and it does not cause a d.c. input current; it is, therefore, suitable to control powers up to several kW. (For high power levels a three-phase supplied system would be preferable.) It is called a half-controlled bridge because only two of the four bridge legs are controlled. Load current is carried during alternate half cycles by D_1 TH_2 and D_2 TH_1. The d.c. output voltage changes according to: $V_o=(V_i/\pi)\,(1+\cos\vartheta)/2$ (V_i = r.m.s. input voltage, ϑ = trigger angle); the required range of trigger angle is 180°, as seen from the output waveform.

With a heavily inductive load, a continuous flow of load current could result if there were no free-wheeling diode in the circuit. If TH_2 were the last to

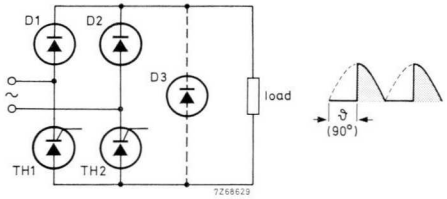


Fig.4-30 Single-phase half-controlled bridge.

conduct, current would be forced (by the load inductance) through this thyristor and D_2 during the negative half cycles during which TH_2 should not conduct. During the positive half cycles, load current would be maintained by the circuit input voltage. Thus, the circuit would operate indefinitely with one thyristor conducting continuously, and loss of control would result. This drawback is overcome by adding the free-wheeling diode D_3 which takes over the load current, allowing the last conducting thyristor to turn off. The circuit needs only two heatsinks, one for D_1 D_2 D_3 and one for TH_1 TH_2.

Where mains impedance is very low, a saturable series reactor is required to limit $\mathrm{d}I_T/\mathrm{d}t$ occurring while TH_1 or TH_2 takes over current from D_3.

Three-phase half-controlled bridge

The three-phase half-controlled bridge (Fig. 4-31) is very popular because it has a high power factor and a low output ripple. Free-wheeling diode D_4 serves the same purpose as described for the previous circuit. The d.c. output voltage is: $V_o = 3\ V_{LL}\ (1 + \cos\ \vartheta)/(\pi/2)$, ($V_{LL}$ = phase-to-phase r.m.s. voltage), and the required range of trigger angle is 180°.

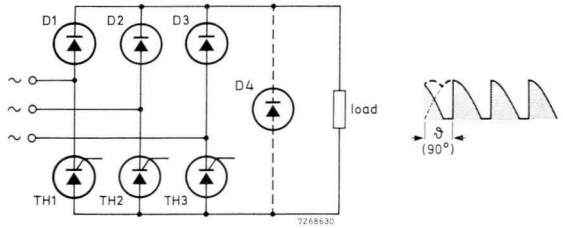


Fig.4-31 Three-phase half-controlled bridge.

Three-phase full-controlled bridge

The three-phase full-controlled bridge (Fig. 4-32) – so called because all six legs of the bridge are controlled – is capable of regeneration. That is, it can feed energy back from the load to the three-phase input. This is a very desirable feature for lifts, hoisting gear, etc., since it provides loss-free braking (four-quadrant motor control).

Comparing the output waveform of Fig. 4-32 with that of Fig. 4-31, it is seen that the ripple frequency is twice that of the half-controlled bridge; further, the ripple percentage is lower. When the load is inductive, the ripple content of output current is greatly reduced as a result. This is attractive for motor control as the ripple components do not contribute to the motor torque and, thus, cause undesirable dissipation.

Because two thyristors must turn on simultaneously, it is essential that the trigger pulses coincide; a central trigger pulse generator is, therefore, necessary. The range of trigger angle is 120° for a resistive or partially inductive load and 180° for an active load (Fig. 4-107); in the latter case the d.c. output voltage is: $V_o = (3V_{LL}\sqrt{2}/\pi)\cos\vartheta$ (V_{LL} = phase-to-phase r.m.s. voltage).

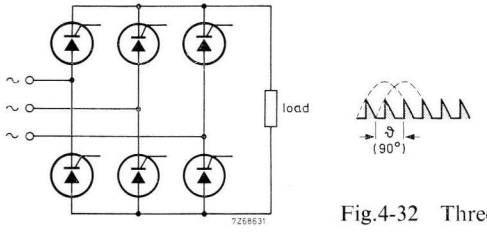


Fig.4-32 Three-phase full-controlled bridge.

4.4.3 Basic a.c. controller circuits

A.C. controllers are frequently used to control rectifier systems delivering an output voltage or current far above the capability of thyristors. A transformer is placed before the rectifier for compatibility between the load demand and the ratings of the power devices in the controller. One specific example is the d.c. supply to a transmitter. Further, a.c. controllers are very useful in light dimming equipment. The most important controller circuits are the subject of discussion here.

Single-phase a.c. controller

The single-phase a.c. controller (Fig. 4-33) uses either a pair of thyristors in anti-parallel or a triac. To ensure two-way conduction even when the load is very inductive and the trigger angle small, triggering by pulse bursts extending to the end of the half cycles is required. If single trigger pulses were to be used, one-way conduction (rectification) would result for trigger angles smaller than the load phase angle. See Fig. 4-34. Thyristor TH_1 is triggered at times t_1 t_3. At times t_2 t_4 thyristor TH_2 cannot be triggered as it is negatively biased by the on-state voltage of TH_1. Thus, only TH_1 will conduct saturating the inductive load.

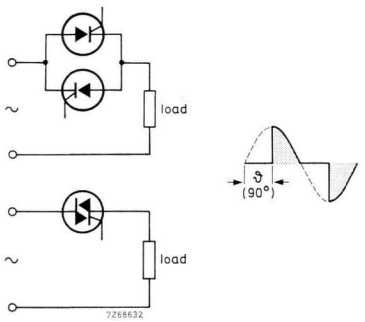


Fig.4-33 Single-phase a.c. controller using thyristors or a triac, and output waveform.

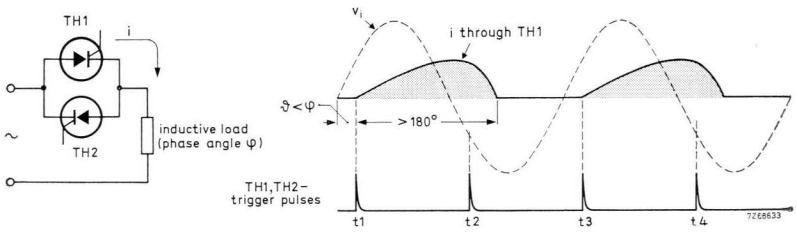


Fig.4-34 Rectification in an a.c. controller.

With an iron-cored load, the trigger angles occurring during the opposite half cycles should differ as little as possible, otherwise core saturation will result. The range of trigger angle is 180° as is clear from the output waveform. The r.m.s. output voltage is $V_{o\,rms} = V_i\sqrt{[(\pi - \vartheta + \frac{1}{2}\sin 2\vartheta)/\pi]}$ (V_i = r.m.s. input voltage).

Three-phase half-controlled a.c. controller

The three-phase half-controlled a.c. controller of Fig. 4-35 uses thyristors and diodes in anti-parallel. Only three of the six legs are controlled (half-controlled circuit type). Thyristors TH_1 TH_2 TH_3 are triggered at 120° intervals; the required range of trigger angle is 210°. The load may be connected in star or delta; the star point should be kept floating, otherwise a d.c. load current component will occur because of the presence of non-controlled elements D_1 D_2 D_3. It is difficult to make the difference of the trigger angles of TH_1 TH_2 TH_3 so small that an inductive load would not saturate. This problem is avoided when using the full-controlled circuit.

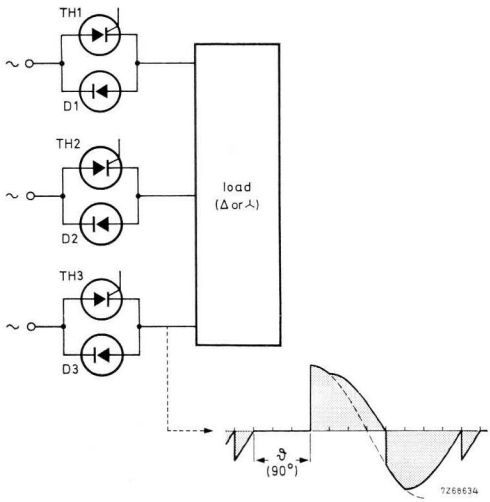


Fig.4-35 Three-phase half-controlled a.c. controller.

Three-phase full-controlled a.c. controller

In the full-controlled a.c. controller, all six legs are controlled (see Fig. 4-36). Alternatively, triacs can be used. The conduction periods of the thyristors in each pair are shifted 180°, and the thyristor pairs in the successive input lines are triggered at 120° intervals.

Earthing of the star point of a star-connected load does not cause a d.c. component in the output. The trigger angles in the different phases may differ, but each thyristor pair should be controlled as symmetrically as possible, so that the output will not contain any d.c. component. Two thyristors must turn on simultaneously; if the trigger pulses do not coincide, thyristor triggering will be impossible. Consequently, a central pulse generator common to all phases is needed.

Because of the symmetrical waveform, there are no even harmonics. This is an advantage in a.c. motor control, as less motor heating results.

The required range of trigger angle is 150°; however, for trigger angles of 90° and larger the trigger pulses should extend to 210° to prevent an abrupt drop in output power for high values of trigger angle.

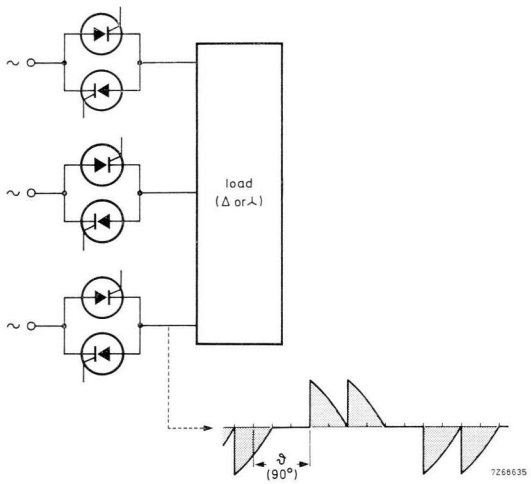


Fig.4-36 Three-phase full-controlled a.c. controller.

Three-phase full-controlled a.c. controller for a delta-connected load

The three-phase a.c. controller in Fig. 4-37 needs only a fairly simple trigger system (one trigger circuit per leg). However, the load should be delta-connected. This is disadvantageous in the case of a.c. motors whose stator windings are inaccessible.

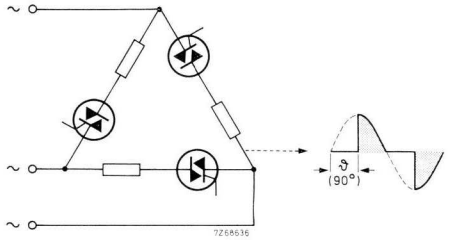


Fig.4-37 Three-phase full-controlled a.c. controller for a delta-connected load.

4.4.4 Survey of circuits discussed

Linear rather than cosinusoidal phase control is often preferred because of its greater simplicity. The linear phase control circuits recommended here provide a linear change of conduction angle over a range of 15° to 160° in response to a d.c. control voltage varying between 0,4 V and 5 V; these circuits can control d.c. or a.c. power, and they can handle heavily inductive loads, because the trigger pulses last until the end of the conduction periods. The circuit given in Section 4.4.7 is intended for control of a.c. power only. For a circuit survey, reference is made to Table 4-6. Maximum power levels that can be handled are specified in Table 4-2 (Section 4.2.2) and Table 4-4 (Section 4.2.6).

Table 4-6. Features of phase-shift controllers.

circuit	load	notes
single-phase linear controller, Section 4.4.5	resistive to strongly inductive.	D.C. or a.c. power control
three-phase linear controller, Section 4.4.6	resistive to strongly inductive.	half-controlled d.c. or a.c. power control system
three-phase a.c. controller using triacs, Section 4.4.7	resistive to strongly inductive (star or delta)	full-controlled a.c. power control system.

4.4.5 SINGLE-PHASE LINEAR CONTROLLER[8])

Fig. 4-38 gives the single-phase linear controller diagram and the associated power circuits. Operation is clear from the waveforms (see Section 1.2.1 for full description). Data of the trigger pulse generator are given in Section 2.4.3. If necessary, the generator circuit can be modified to produce high-energy trigger pulses (ref. Section 2.4.4). Various trigger circuits are specified in Section 2.6. Control linearity is demonstrated by the plot of Fig. 4-39 (resistive load); control threshold is 0,2 V at nominal supply voltage. To eliminate the effect of mains voltage fluctuations, V_{contr} should be derived from the stabilized voltage at pin 7 of the RSA61.

[8]) AN No. 121, ordering code 9399 260 62101 - Simple Linear Phase Control Circuits.

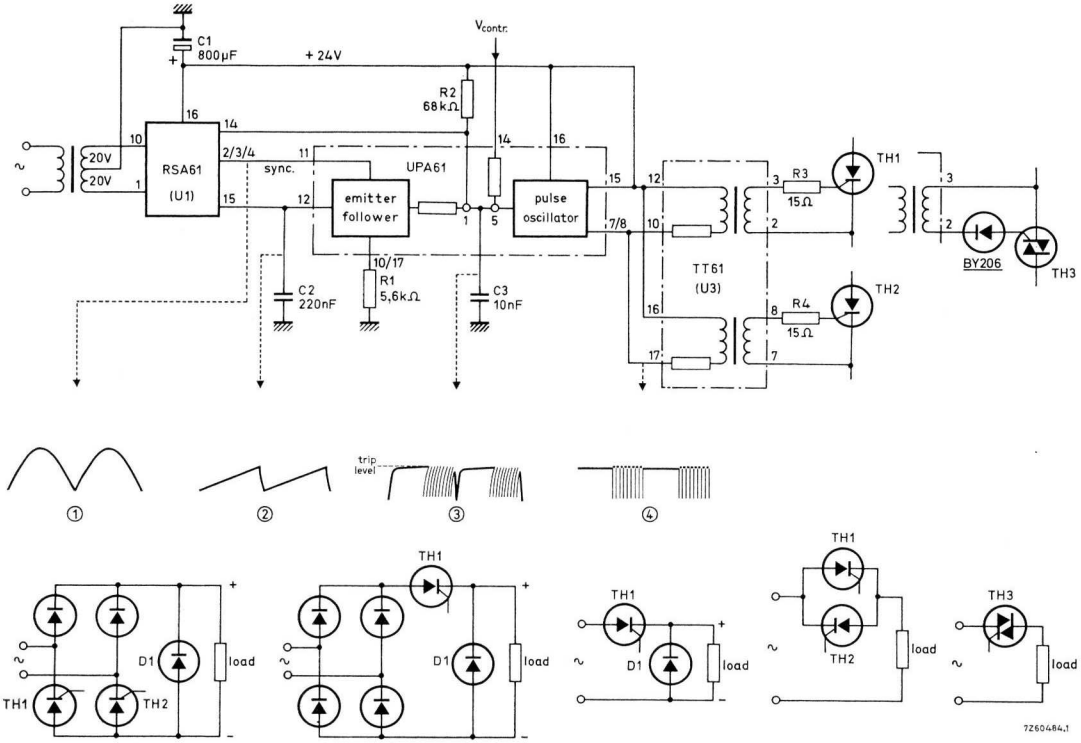


Fig.4-38 Single-phase linear controller with power circuits.

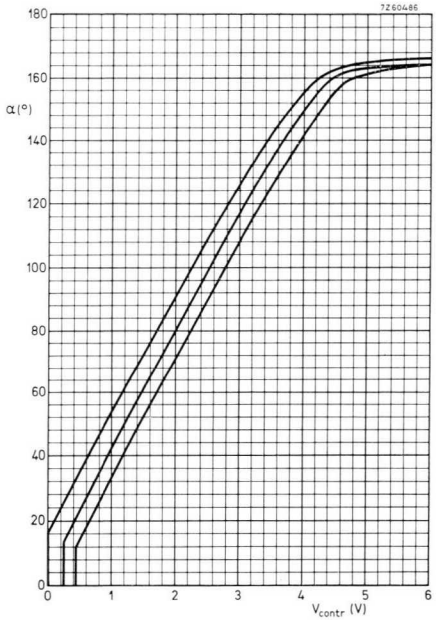


Fig.4-39 Conduction angle α vs. V_{contr} for the a.c. supply voltage equal to 180 V (upper curve), 200 V (centre curve), 220 V and 240 V (lower curve). Resistive load.

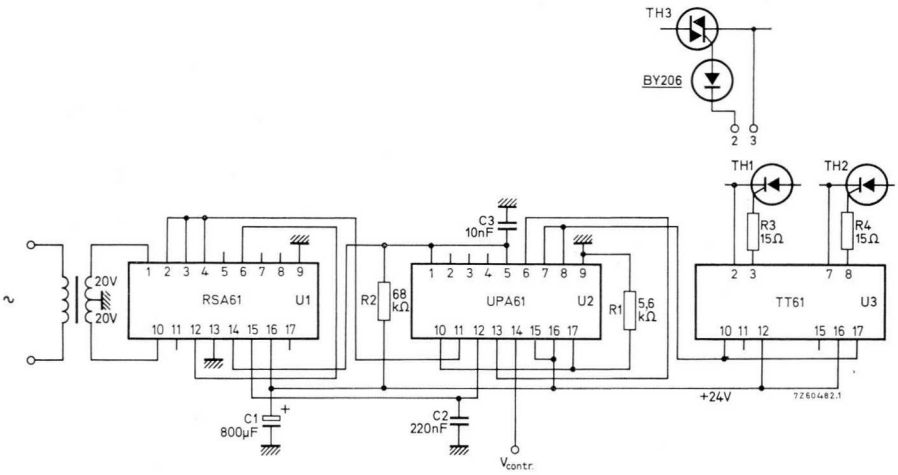
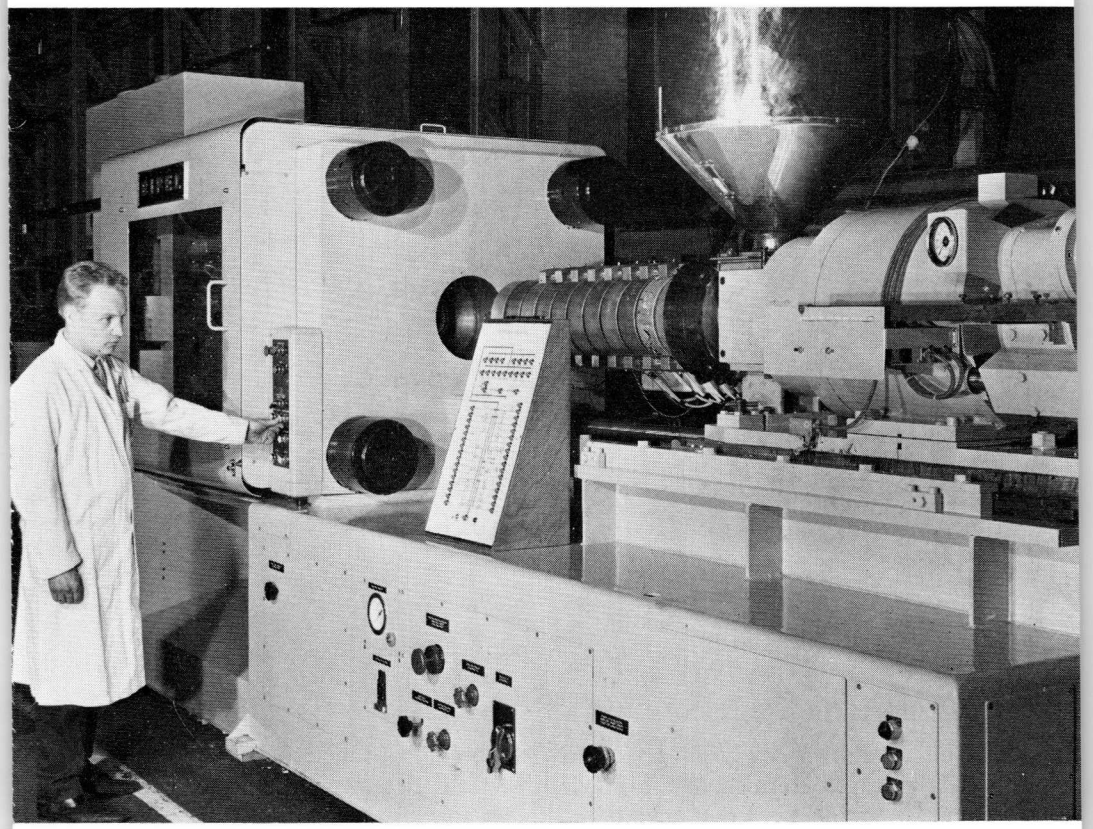


Fig.4-40 Wiring diagram of single-phase linear controller.

Adjustment (Fig. 4-40):

If desired, increase the control threshold (0,2 V according to Fig. 4-39) by increasing or decreasing the value of R_2.



This 650 tons injection moulding machine is controlled by NORbits.
Courtesy of BIP Engineering Ltd, Sutton Coldfield, Birmingham, England.

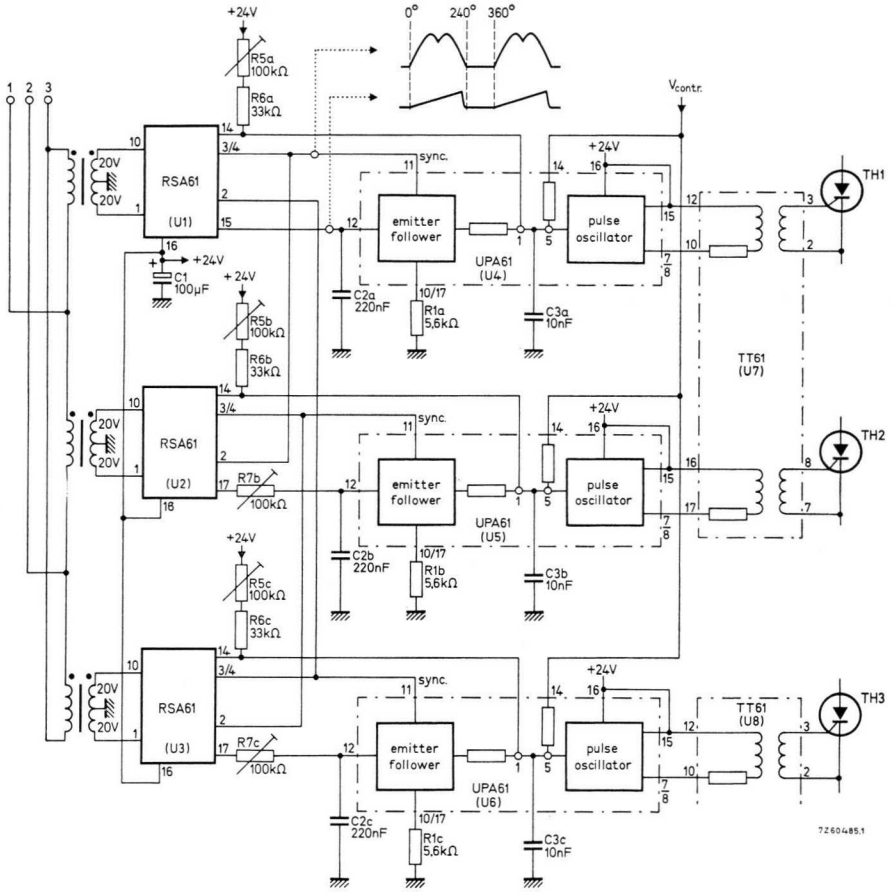


Fig.4-41 Three-phase linear controller.

4.4.6 Three-phase linear controller[8])

The circuit shown in Fig. 4-41 for three-phase control functions in a manner similar to that described in the previous section. Potentiometer adjustments provide for tracking of the conduction angles; see "Adjustment". The trigger circuit is capable of controlling a half-controlled three-phase bridge or a.c. controller from almost zero to full output power; circuit performance is independent of phase sequence. To this end the synchronization voltages are made to extend over 240° (see upper waveform) by half-wave rectification of the voltages derived from two succeeding phases. The +24 V supply is obtained by multi-phase rectification (interconnection of the RSA61 outputs) so that the smoothing capacitor can be small in value. The control voltage V_{contr} must be obtained from the stabilized voltage at pin 7 of the RSA61.

[8]) AN No. 121, ordening code 9399 260 62101 - Simple Linear Phase Control Circuits.

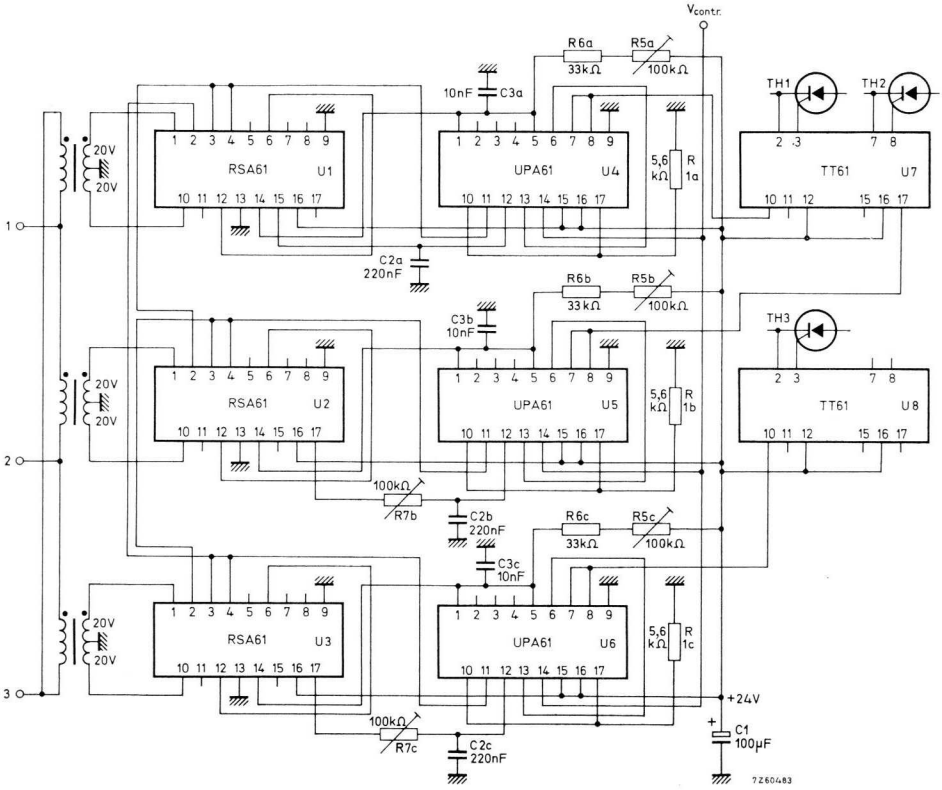


Fig.4-42 Wiring diagram of three-phase linear controller.

Adjustment (Fig. 4-42):

1. *Set R_{7b} R_{7c} to mid position.*
2. *Adjust V_{contr} to the value at which control should start (for example 0,3 V).*
3. *Adjust R_{5a} so that trigger pulses just appear at output terminal 8 of U_4.*
4. *Increase V_{contr} until the pulses at the output of U_4 extend over about 150° (three-phase bridge) or 180° (a.c. controller).*
5. *Adjust R_{5b} R_{5c} so that the length of the pulse bursts at the outputs of U_5 U_6 is equal to that at the output of U_4.*
6. *Decrease V_{contr} until the pulses at the output of U_4 extend over about 20°.*
7. *Adjust R_{7b} R_{7c} so that the length of the pulse bursts at the outputs of U_5 U_6 is equal to that at the output of U_4.*

4.4.7 THREE-PHASE A.C. CONTROLLER USING TRIACS[9])

This fully-controlled three-phase controller is intended for handling a resistive or mixed resistive/inductive load connected in star or delta. It uses triacs, which reduces the number of power devices needed but requires a skilfully designed trigger circuit.

In the power circuit of Fig. 4-43, saturable reactors minimizing voltage loss are included in the phase lines to "soften" commutation, that is, reducing commutation di/dt and re-applied dv/dt to obtain reliable turn-off[10]); these reactors have an inductance of about 3 mH. Controlled power is 15 kW when using BTX94 and 27 kW when using BTW34.

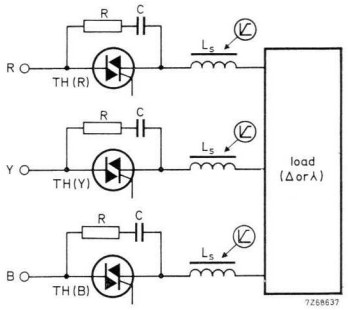


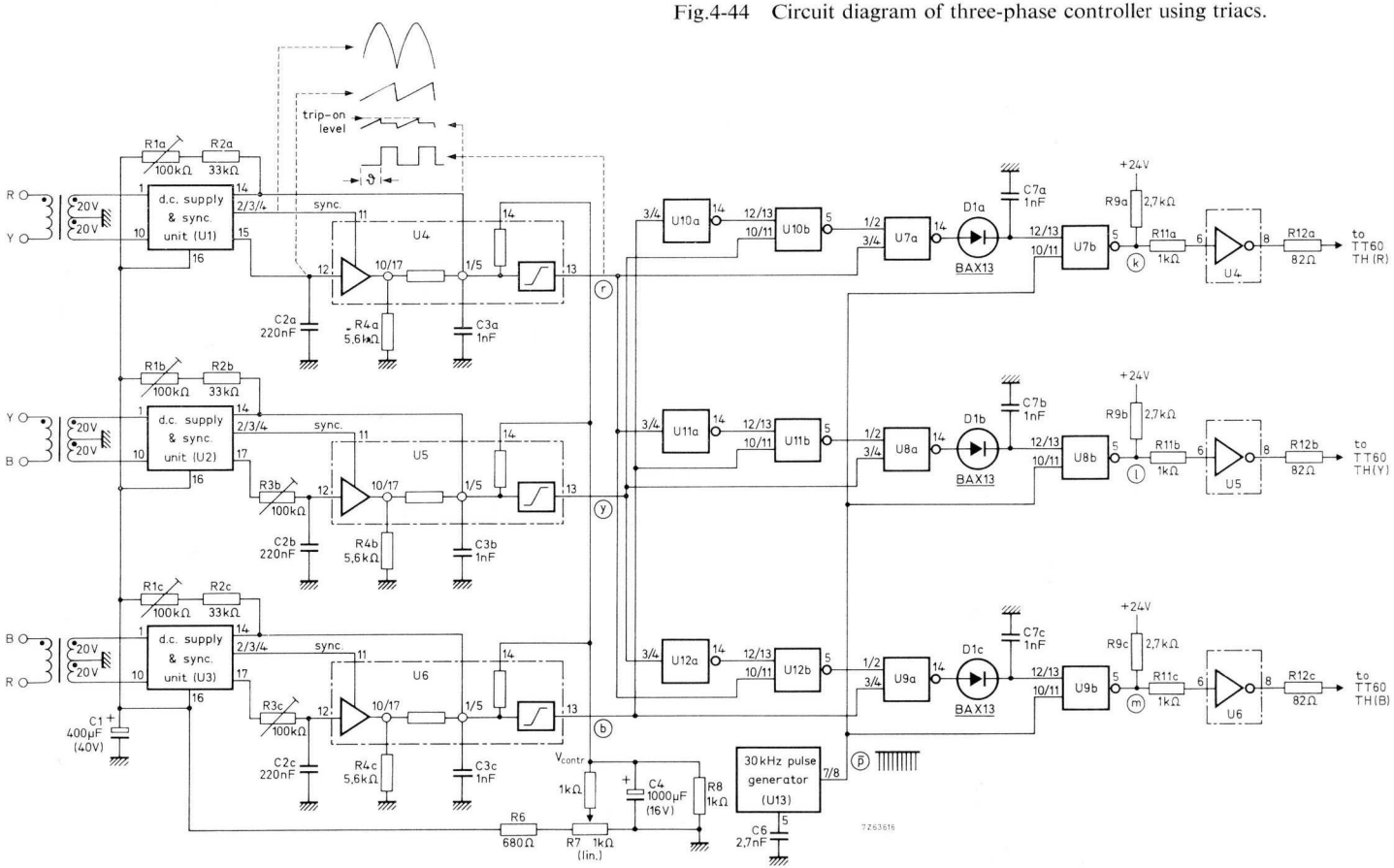
Fig.4-43 Power circuit of three-phase controller. $R = 33\ \Omega$, 2 W; $C = 0{,}1\ \mu$F, 1600 V d.c.; $L_s \approx 3$ mH.

In Fig. 4-44, U_4 U_5 U_6 are the phase shift units whose principle of operation is described in Section 1.2.1. The waveforms give further information on circuit operation. The instant, at which each of the output pulses r, y and b from the Schmitt trigger circuits commences, determines the trigger angle ϑ and is governed by the level of V_{contr} adjusted with R_7. These pulses are mixed in the NOR-gates to obtain the correct mode of triac triggering.

[9]) AI. No. 467, ordering code 9399 254 46701 - Continuous Three-phase Control System with Triacs.

[10]) AN No. 127, ordering code 9399 250 62701 - Triac Control of D.C. Inductive Load.

Fig.4-44 Circuit diagram of three-phase controller using triacs.



Two triacs must turn on simultaneously in a full-controlled system, so triggering by coinciding pulses is essential. Therefore, a central pulse generator, U_{13}, is used as the common trigger source (output signal $\bar{p}$). The length of the h.f. trigger pulse trains (30 kHz repetition frequency) passed to the triac gates depends on the opening time of NOR-gates U_{7b} U_{8b} U_{9b}.

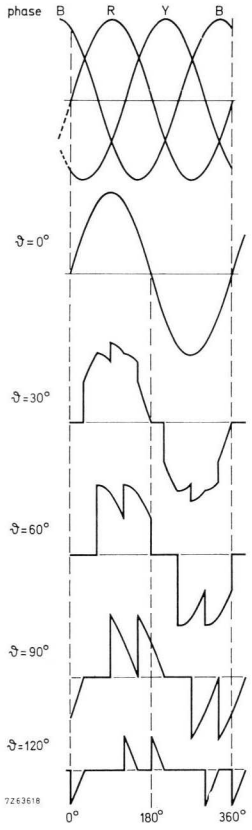


Fig.4-45 Current waveforms of triac TH(R) compared with phase voltages (ϑ = trigger angle); Ohmic load assumed.

Current waveshapes for triac *TH(R)* in relation to the phase voltage *R*, *Y* and *B* are shown in Fig. 4-45. The following logic expression is valid for the trigger signal of triac *TR(R)* connected to phase *R*:

$$k = p \cdot (r + b \cdot \bar{y}),$$

where r, b and y are the Schmitt trigger output pulses and p represents the complement of the common trigger pulse source output (see Fig. 4-44). The signals r and b are both needed because, as seen from Fig. 4-45, triggering should occur from 0° minimum to 210° maximum. Because r is derived from the voltage between phases *R* and *Y*, triggering can start already at −30° (V_{contr} at maximum value); as a result, interference will be very low at full a.c. power.

In the logic expression, the term $\bar{y}$ accounts for the fact that for $60° < \vartheta < 90°$ triggering of *TH(R)* must cease when *TH(Y)* turns on. When sustaining triggering of *TH(R)*, it will start to conduct again with a reversed current, and an abrupt rise in power will result. To prevent this, y is used inhibiting the trigger signal of *TH(R)*. Using de Morgan's theorem, the above expression becomes:

$$k = \overline{\bar{p} + r + \overline{\bar{b} + \bar{y}}},$$

which condition is fulfilled by NOR-gate network U_{10a} U_{10b} U_{7a} U_{7b}. Similar conditions and NOR-gate arrangements are valid for *TH(Y)* and *TH(B)*.

Figs 4-46 and 4-47 give the wiring lay-outs for the circuits discussed.

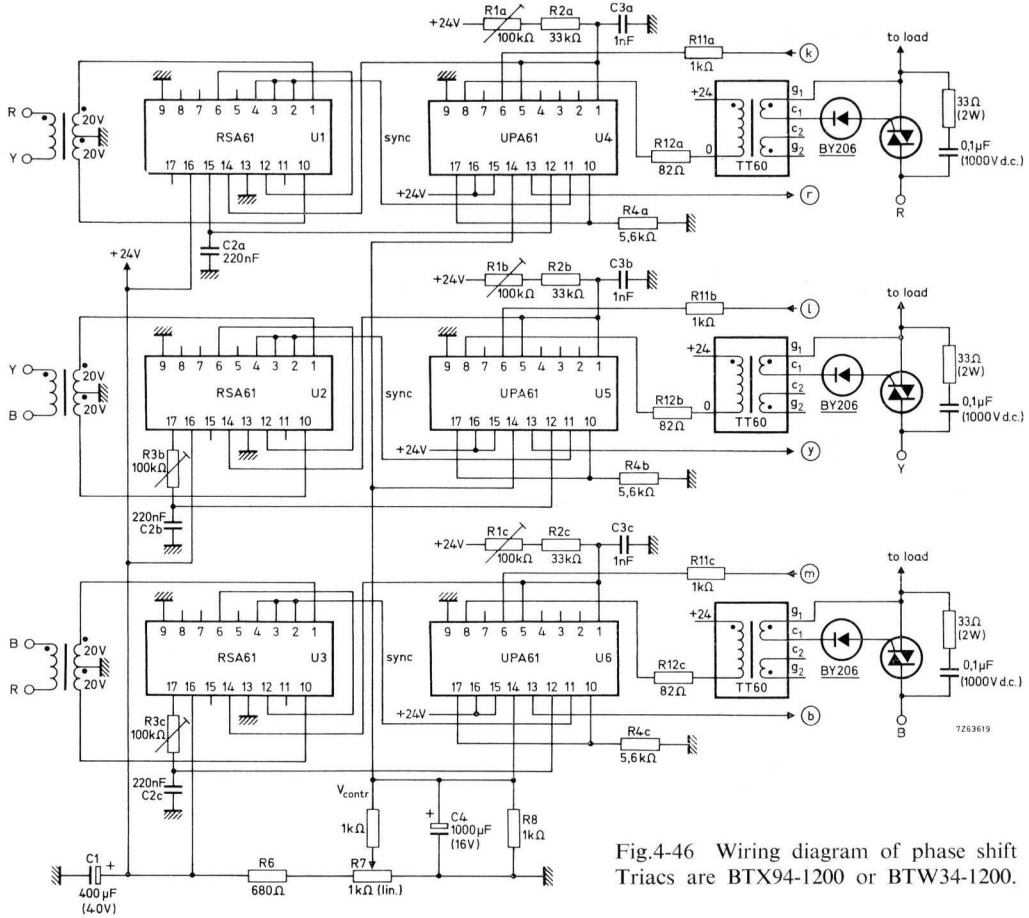


Fig.4-46 Wiring diagram of phase shift and trigger section. Triacs are BTX94-1200 or BTW34-1200.

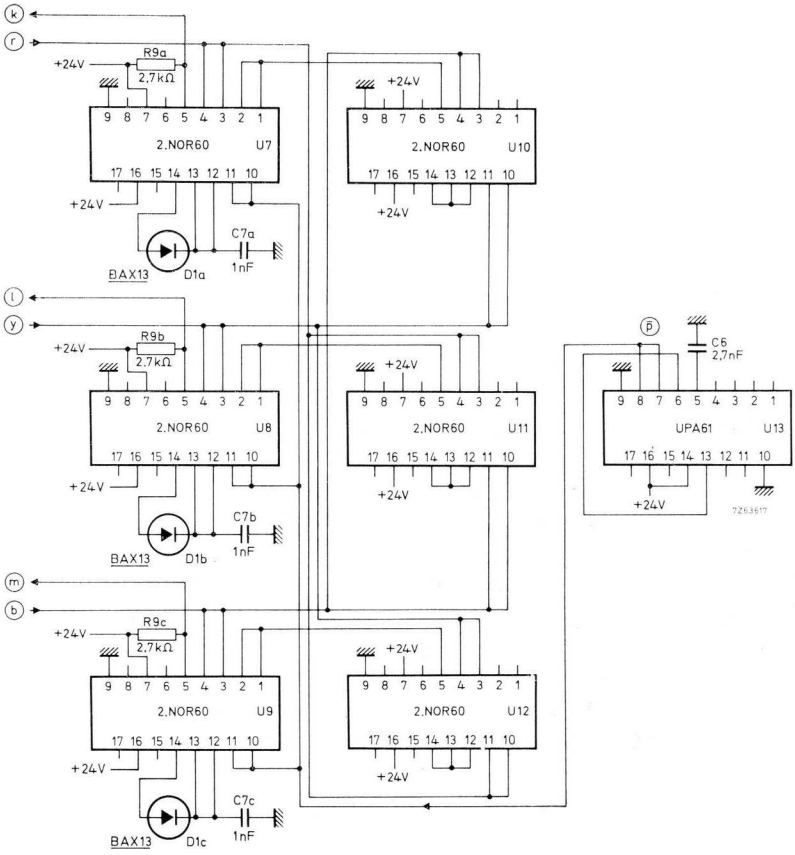


Fig.4-47 Wiring diagram of logic section.

Adjustment (Fig. 4-46):

1. *Check that the phase sequence is R-Y-B (Fig. 4-45); if necessary, exchange the connections of two phases.*
2. *Set all potentiometers in their mid position.*
3. *With R_7 adjust V_{contr} to the threshold value at which control should start (for example, 0,2 V).*
4. *Adjust R_{1a} so that the pulses at pin 13 of U_4 are about 0,2 ms long.*
5. *Increase V_{contr} until the pulses at pin 13 of U_4 extend over about 8 ms.*
6. *Adjust R_{1b} R_{1c} so that the pulses at pin 13 of U_5 U_6 have the same width.*
7. *Reduce V_{contr} so that the pulses at pin 13 of U_4 have again about 0,2 ms width.*
8. *Adjust R_{3b} R_{3c} so that the pulses at pin 13 of U_5 U_6 have the same width.*

4.5 Choppers and inverters

4.5.1 Discussion and circuit survey

In this section choppers[11]) and inverters are discussed and circuits given. Fed from a d.c. source, the chopper provides loss-free d.c. power control. Inverters convert d.c. into a.c. and are used where a.c. is not available; also, inverters are quite useful in applications needing a variable supply frequency, or a supply frequency different from that of the a.c. mains.

The chopper in its most simple form is a thyristor switch between a d.c. source and its load that opens and closes periodically. See Fig. 4-48. Average load voltage is controlled by varying the ratio of the thyristor conduction period t_p (output pulse width) and the repetition period t_o (chopper operating frequency inverse of t_o). This can be achieved by pulse with modulation (PWM), that is, pulse width varied but pulse repetition period held constant, or by pulse rate modulation (PRM), that is, pulse repetition period varied but pulse width held constant. Fig. 4-49 clearly illustrates both methods. If V_i is the d.c. input voltage, the average chopper output voltage $V_{o\ avg}$ is determined by

$$V_{o\ avg} = \frac{t_p}{t_o} V_i.$$

A combination of PWM and PRM is, of course, possible.

A chopper that is capable of feeding power back into its d.c. supply is said to be regenerative. A condition of regeneration occurs when a d.c. motor is driven by its load: the motor acts as a d.c. generator returning power to the d.c. input. Because with a d.c. supply regeneration is only possible by reversing the load current, a regenerative chopper is necessarily one that can pass current bidirectionally. Regeneration can be of a transient nature (motor braking) or of a longer duration (hoist motor driven by its load). When a battery functions as the supply source, regeneration over long periods is no problem. The situation is different, however, for a rectifier system; the buffer capacitors must accumulate recovered energy because the rectifier blocks reversed current, but their storage capacity is limited. A voltage regulator diode (or avalanche thyristor)/resistor arrangement can absorb recovered energy indefinitely; at an excessive output voltage, the diode (or thyristor) avalanches and braking energy

[11]) AI No. 459, ordering code 9399 254 45901 - Basic Thyristor Chopper Circuits.

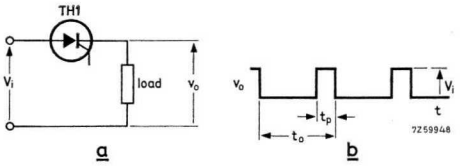


Fig.4-48 Basic chopper circuit (a) and output waveform (b).
t_p = conduction period of TH_1 (output pulse width), t_o = repetition period.

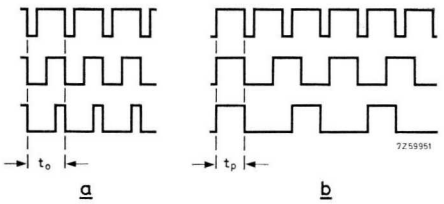


Fig.4-49 Chopper output waveforms. (a) PWM: t_o = constant, (b) PRM: t_p = constant.

is dissipated in the current-limiting series resistor. The diode and resistor ratings are decisive for the maximum power that can be handled during regeneration. Choppers are classified as follows:

- Forced-commutation choppers using an auxiliary thyristor to turn the main thyristor off. The output pulse width is variable, because it depends on the time between the instants the main and auxiliary thyristor are triggered; so the chopper output can be controlled by PWM as well as PRM.
- Self-commutation choppers using a resonant circuit to turn the thyristor off. As soon as the resonance current reverses, the thyristor stops conducting, so an auxiliary thyristor is not necessary. The pulse width is fixed because it depends solely on the resonance period, and the output can only be controlled by PRM.

Table 4-7 gives a survey of the discussed chopper circuits and contains suggestions for their use. The regenerative two-thyristor chopper is quite universal and may be used for building single-phase and three-phase inverters (see Sections 4.5.6 and 4.6.3).

It may be preferable, for d.c. power control, to use an uncontrolled rectifier followed by a chopper instead of using a controlled rectifier alone. Advantages of the chopper-and-rectifier configuration are: (1) better cos φ and power factor – (2) lower ripple content as the chopper operates at a high frequency; this is desirable in motor control because of reduced dissipation – (3) fewer thyristors needed – (4) reduced mains pollution because the buffer capacitors across the rectifier output also serve as suppressors.

Table 4-7 Chopper circuits.

circuit	regenerative	output control	applications
self-commutation chopper, section 4.5.2	no	PRM	— power function generation. — high- frequency supply (1 kHz to 10 kHz) of resistance welders.
two-thyristor chopper, Section 4.5.3	no	PRM, PWM	— D.C. motor control. — battery chargers. — stabilized d.c. power supplies.
regenerative two-thyristor chopper, Section 4.5.4	yes	PRM, PWM	— two-quadrant motor control. — bidirectional chopper circuit.

Table 4-8 gives a survey of the discussed inverter circuits and their applications. The 400 Hz bridge inverter (Fig. 4-50*a*) employs two choppers of the type described in Section 4.5.4. An output filter is included to remove harmonics. Output voltage stabilization is used to compensate for the voltage loss across the filter series impedance, and to eliminate the influence of fluctuations of the d.c. input voltage; control is achieved by varying the phase relationship between the two square-wave chopper outputs (Fig. 4-50b).

Fast turn-off thyristors (series BTW30, BTW31, BTW32 and BTW33) are required in high-frequency choppers and inverters, because of the short turn-off times needed in these circuits.

Table 4-8. Inverter circuits.

circuit	output power	applications
50 kVA, 1 kHz inverter, Section 4.5.5	50 kVA (*reactive* load)	large-scale capacitor-kVA testing.
400 Hz, 110 V bridge inverter, Section 4.5.6	2 kW	stabilized a.c. power supply.
3 h.p. induction motor controller, Section 4.6.2	3 kW	variable-speed a.c. motor control.

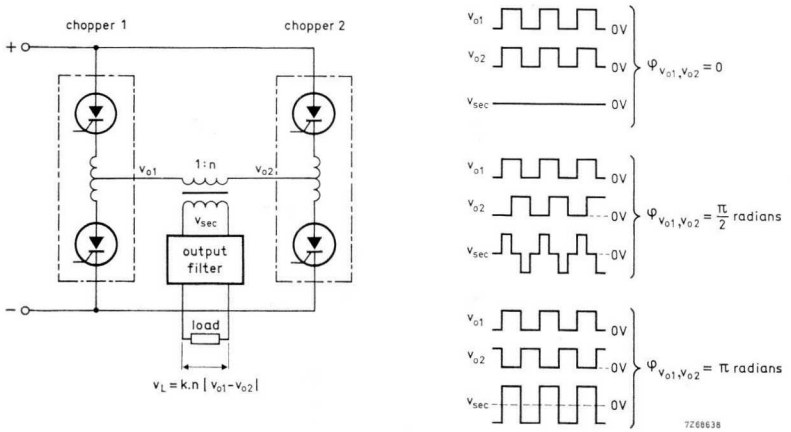


Fig.4-50 **Bridge inverter** using choppers (a), and waveforms (b).

4.5.2 SELF-COMMUTATION CHOPPER

Power circuit

The chopper circuit in Fig. 4-51 is capable of supplying 4,5 kW output power. The power rise time is only 1 ms (determined by the response of smoothing filter L_2 C_3). By varying the triggering rate for TH_1, power functions of various waveforms can be generated, such as triangular, trapezoidal, rectangular or semi-sinusoidal time functions.

The waveforms in Fig. 4-51 illustrate circuit operation schematically. Load current flows through L_1, D_3, D_4 and L_2. After triggering, TH_1 takes over the load current, and the resonant circuit L_1 C_2 is excited. When the resonance current reverses, D_1 D_2 conduct and TH_1 turns off (self-commutation). Diode D_4 prevents the commutation capacitor C_2 being charged by the output voltage; otherwise, the swing of resonance current would be reduced and commutation failure could result.

The pulse time t_p (see output waveform in Fig. 4-51), over which power is supplied to the load, is very nearly equal to the resonance period of L_1 C_2. If t_o is the pulse repetition period and V_i the input voltage, the average output voltage $V_{o\ avg}$ is:

$$V_{o\ avg} \approx \frac{2\,\pi\,\sqrt{(L_1 C_2)}}{t_o}\,V_i.$$

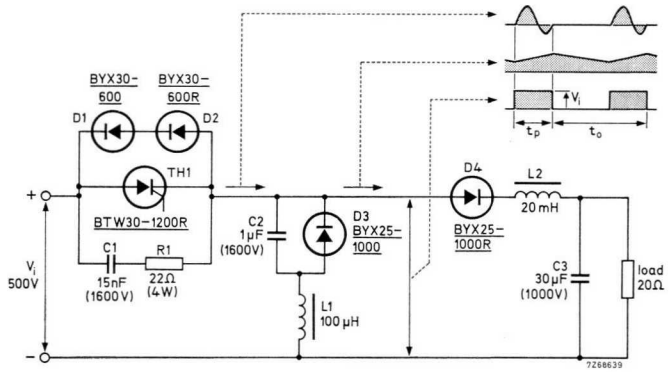


Fig.4-51 300 V, 15 A self-commutation chopper, and waveforms.

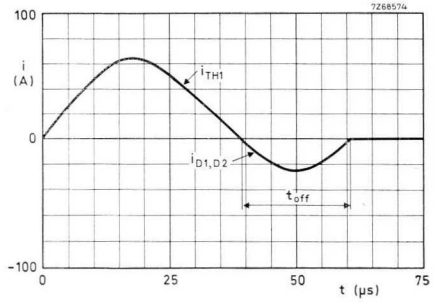


Fig.4-52 Plot of current through TH_1 D_1 D_2 at full chopper output (15 A).

Clearly, $V_{o\ avg}$ is proportional to the pulse rate $1/t_o$.

Fig. 4-52 shows the thyristor/diode current waveform at 15 A d.c. load current, with the quality factor of the resonant circuit equal to 10. If the peak resonance current $\hat{I}_{res}$ is not less than three to four times the maximum output current $I_{o\ max}$, the circuit-imposed turn-off time t_{off} (which is the time over which D_1 D_2 conduct, keeping TH_1 reverse-biased) will be at least 30% of the resonance period $2\pi\sqrt{(L_1C_2)}$; see the waveform. The circuit-imposed turn-off time must exceed the specified thyristor turn-off time t_q. Taking $2\pi\sqrt{(L_1C_2)}$ as $4\ t_q$, to provide a safe margin, the following formulae can be used to calculate L_1 and C_2:

$$L_1 = \frac{2\ t_q\ V_i}{\pi\ \hat{I}_{res}}, \qquad C_2 = \frac{2\ t_q\ \hat{I}_{res}}{\pi\ V_i}$$

where $3\ I_{o\ max} \leqslant \hat{I}_{res} \leqslant 4\ I_{o\ max}$.

It should be noted that the sum of $I_{o\ max}$ and $\hat{I}_{res}$ must not exceed the repetitive current rating of TH_1.

Excessive ripple in the output current due to thyristor switching can reduce t_{off} to the extent that commutation failure might occur. If at zero output voltage the peak-to-peak ripple is not more than 10% of the maximum output current $I_{o\ max}$, problems will not be encountered. So, smoothing inductance L_2 follows from:

$$L_2 \geqslant \frac{40\ t_q\ V_i}{I_{o\ max}}.$$

Trigger circuits

Fig. 4-53 shows the trigger pulse generator for the self-commutation chopper; circuit operation is described in Section 1.2.2. The emitter follower gives an increased input resistance. Capacitor C_2 suppresses interference which would otherwise occur at the sensitive Schmitt trigger input. Single trigger pulses are produced during "flyback". Variable resistance R_1 adjusts the trigger frequency (chopper operating frequency); see Fig. 4-54. The chopper output is proportional to the trigger frequency, the latter being inversely proportional to $C_1(R_1 + R_2)$.

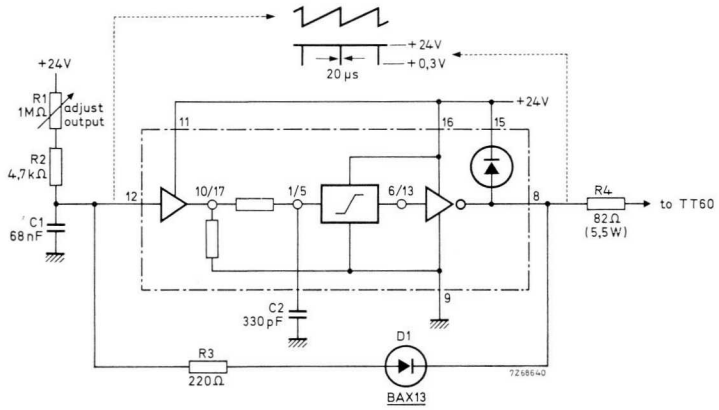


Fig.4-53 Trigger circuit for self-commutation chopper using resistance control.

Adjustment (Fig. 4-55):
The frequency range is changed by altering the value of C_1.

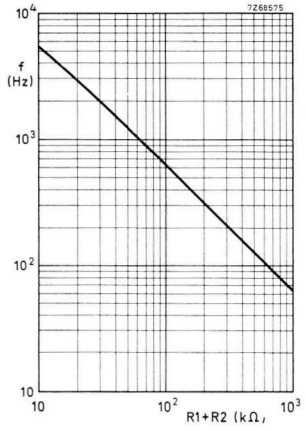


Fig.4-54 Trigger frequency, f, vs. charging resistance $R_1 + R_2$ (ref. Fig.4-53).

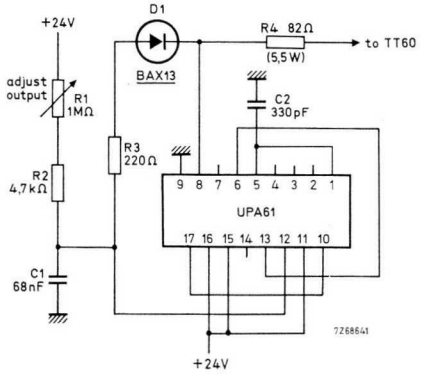


Fig.4-55 Wiring diagram of trigger circuit according to Fig.4-53.

The circuit of Fig. 4-56 uses the same pulse generator as that illustrated in Fig. 4-53, but a variable voltage V_{contr} controls the chopper output. The DOA61 works as an integrator charging timing capacitor C_1 with a constant current of roughly V_{contr}/R_2. Because the charge rate is proportional to V_{contr}, linear chopper output control results. Fig. 4-57 shows the relationship between trigger frequency and control voltage; the value of V_{contr} is adjusted with R_1 in Fig.4-56. The trigger frequency is inversely proportional to C_1.

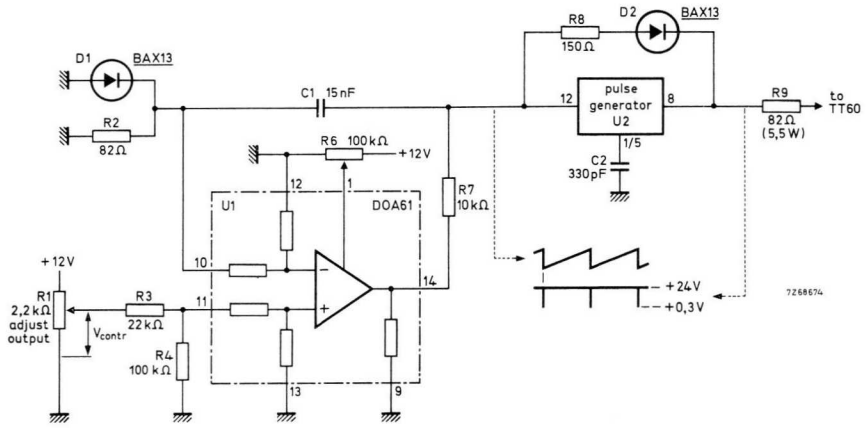


Fig.4-56 Trigger circuit for self-commutation chopper using voltage control.

Adjustment (Fig. 4-58):

1. *The frequency range is set by choice of* C_1.
2. *The minimum trigger frequency with* R_1 *set to zero resistance can be changed by adjusting bias potentiometer* R_6.

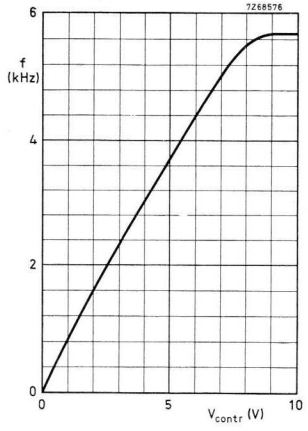


Fig.4-57 Trigger frequency, f, vs. d.c. control voltage V_{contr} (ref. Fig.4-56).

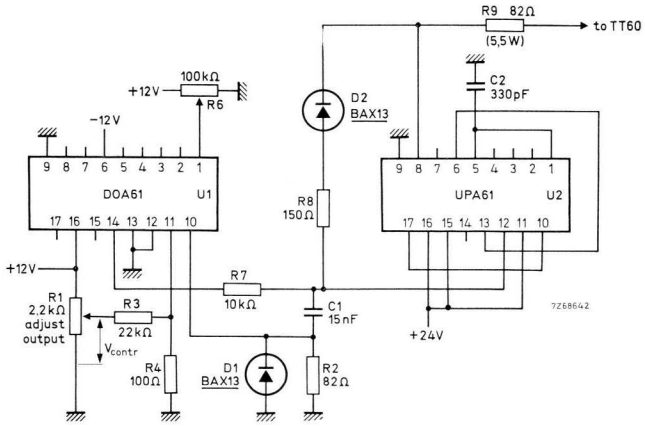


Fig.4-58 Wiring diagram of trigger circuit according to Fig.4-56.

4.5.3 Two-thyristor chopper

Fig. 4-59 shows a 400 Hz two-thyristor chopper which can deliver 23 kW output power. The continuous output current rating is 50 A, but up to 100 A will be safely commutated by the circuit. The waveforms show the thyristor current and the output voltage. The motor current flows through free-wheeling diode D_3 and commutation inductor L_1.When triggered, thyristor TH_1 takes over the load current and remains in conduction until turned off by TH_2. When the latter is triggered, resonance current will start to flow through TH_1 L_1 C_1 TH_2. First, the resonance current through TH_2 reverses, D_2 conducts and TH_2 turns off; a few μs later, the same happens to TH_1, diode D_1 taking over the current from this thyristor. After D_1 has ceased conducting, the load current is carried again by D_3 and L_1. Power is supplied to the load as long as TH_1 and D_1 conduct. After each pulse of output power, C_1 is fully discharged via R_3, to ensure thyristor turn-off.

When the amplitude of the resonance current, $\hat{I}_{res}$, is equal to twice the maximum load current, and the quality factor of the resonant circuit is 10, the current through TH_1 and D_1 is according to Fig. 4-60. It is seen that the time t_{off1}, presented to TH_1 for turning off, exceeds $1{,}5\sqrt{(L_1C_1)}$ (about one-quarter resonance period). The value of t_{off1} should be equal to at least the specified thyristor turn-off time t_q. (The turn-off time offered to TH_2 is larger than t_{off1}.) Taking $2\pi\sqrt{(L_1C_1)}$ as $5\,t_q$ for adequate safety margin, we find:

$$L_1 = \frac{5\,t_q\,V_i}{2\pi\,\hat{I}_{res}}, \quad C_1 = \frac{5\,t_q\,\hat{I}_{res}}{2\pi\,V_i},$$

where $\hat{I}_{res} = 2 \times$ maximum load current

To ensure discharge of C_1, the time constant $C_1\,R_3$ (Fig. 4-59) is made equal to the repetition period. If f is the chopper operating frequency, the expression for R_3 becomes:

$$R_3 = \frac{1}{f\,C_1}.$$

The output pulse time cannot become shorter than the resonance period $2\pi/(L_1C_1)$; this situation arises when TH_2 is triggered immediately after TH_1.

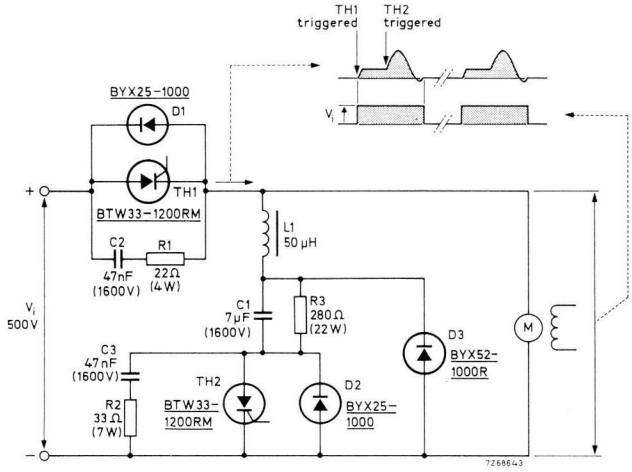


Fig.4-59 450 V, 50 A two-thyristor chopper with motor load, and waveforms. Operating frequency is 400 Hz. $C_1 = 12 \times 5$ μF, 2222 326 50505 (3 in series, 4 in parallel); $R_3 = 2 \times 560$ Ω, 2322 330 42561 in parallel.

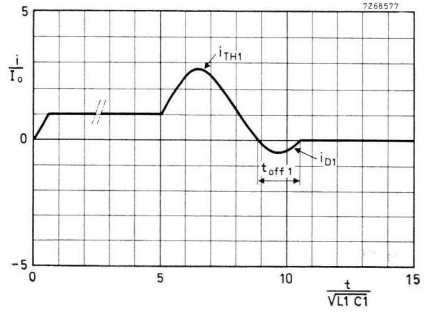


Fig.4-60 Plot of current through TH_1 D_1. I_o = d.c. output current.

If f is the chopper working frequency, and again assuming $2\pi\sqrt{(L_1C_1)}$ to be equal to $5\ t_q$, the minimum output voltage becomes:

$$V_{o\ min} = 5 f\ t_q\ V_i.$$

For C_1 to discharge completely, there should be a minimum interval between the output pulses. Therefore, the maximum output voltage $V_{o\ max}$ is established at:

$$V_{o\ max} = 0.9\ V_i.$$

Fig. 4-61 gives the construction of the commutation inductance L_1.

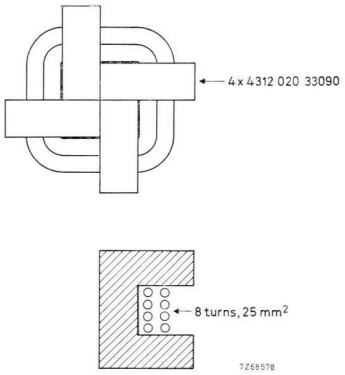


Fig.4-61 Construction of commutation coil used in two-thyristor chopper.

Trigger circuit using PWM

The trigger circuit of Fig. 4-62 is suitable for controlling the two-thyristor chopper; Fig. 4-63 shows some circuit waveforms. Section 1.2.2 discusses the operation of the sawtooth generator and the comparator, and the trigger pulse generator is described in Section 2.4.3. Thyristor TH_1 is fed by repetitive trigger pulses to obtain turn-on even under strongly inductive load; single pulses suffice for commutation thyristor TH_2. Trigger pulses are applied to TH_1 until the comparator is reset when TH_2 is triggered. The delay between triggering TH_1 and TH_2 increases with V_{contr}, as shown by the arrow in the lowermost waveform of Fig.4-63. The chopper output is proportional to the control voltage.

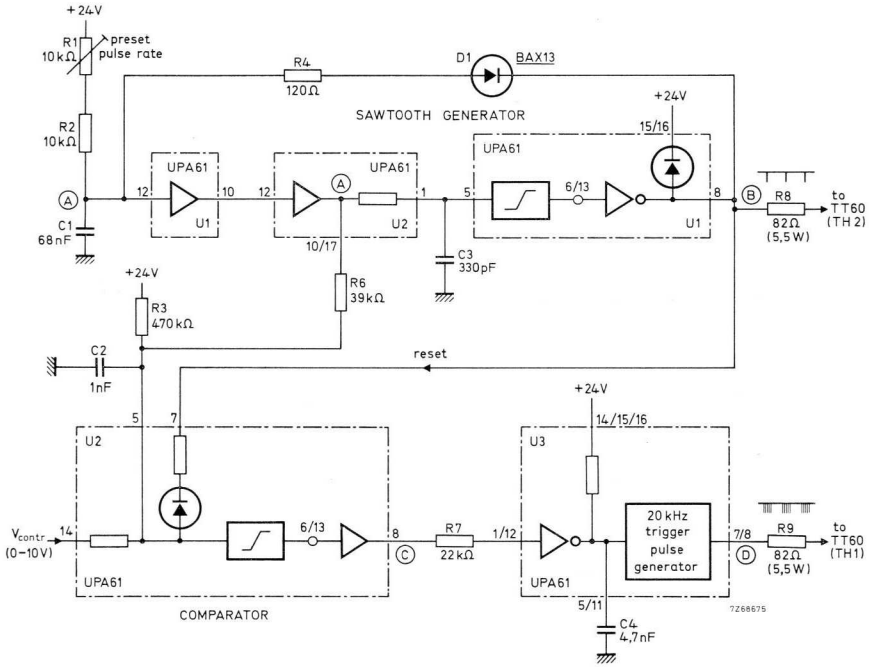


Fig.4-62 Trigger circuit for two-thyristor chopper using PWM; waveforms given in Fig.4-63.

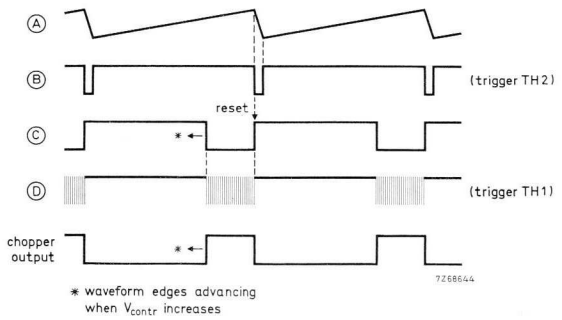


Fig.4-63 Waveforms for Fig.4-62.

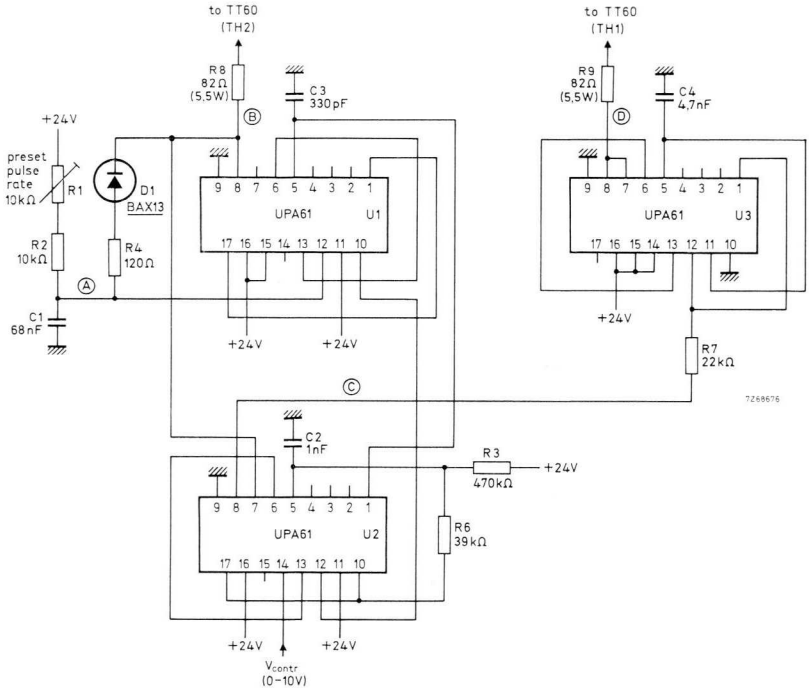


Fig.4-64 Wiring diagram of trigger circuit in Fig.4-62; A to D refer to the waveforms in Fig.4-63.

Adjustment (Fig.4-64):

1. *Chopper working frequency is adjusted with R_1; extrapolating in Fig.4-54, we see that the chopper operates at 400 Hz with R_1 set at 6 kΩ.*
2. *The threshold of V_{contr} at which chopper output control starts can be shifted by changing the value of R_3.*

4.5.4 Regenerative two-thyristor chopper

Power circuit

The 5,5 kW chopper of Fig.4-65, shown with a series motor load, can pass current bidirectionally and is, therefore, a regenerative type. The field coils are fed via a bridge rectifier so that there is a unidirectional flow of field current. Two-quadrant motor control results, that is, there is a condition of motoring (average chopper output higher than armature e.m.f.) and regeneration or braking (average chopper output lower than armature e.m.f.). Thyristors TH_1 and TH_2 are triggered in turn; this causes the upper and lower chopper legs to conduct alternately. The chopper is suitable for PWM as well as PRM, and its maximum operating frequency is 2 kHz.

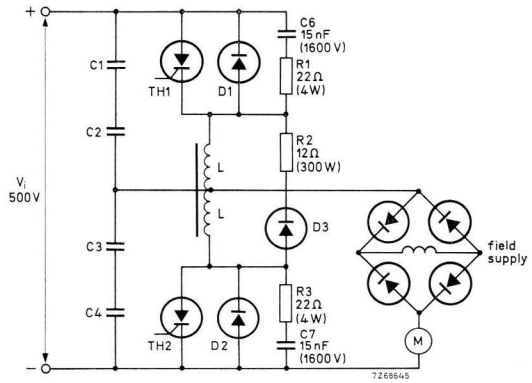


Fig.4-65 450 V, 12 A regenerative two-thyristor chopper, feeding d.c. series motor. C_1 to C_4 = 10 μF, cat. no. 2222 327 50106; L = 280 μH (see Fig.4-70); TH_1, TH_2 = BTW30-1200RM; D_1, D_2 = BYX25-1000; D_3 = BYX25-1000R.

Four power semiconductor devices (TH_1, TH_2, D_1, D_2) can carry the load current, so there are four conduction states; see Fig.4-66. The capacitors and the coupled inductors are the commutation elements. Resistor R_2 causes critical damping; this ensures a minimum commutation time and, consequently, the widest control range of output voltage.

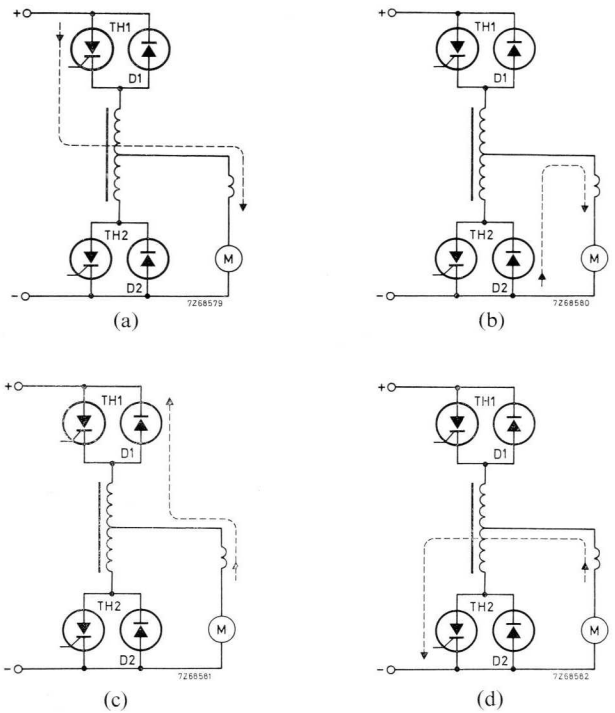


Fig.4-66 The four conduction states of the regenerative two-thyristor chopper. (a) upper leg conducting, motoring; (b) lower leg conducting, free-wheeling (current sustained by circuit inductance; (c) upper leg conducting, regeneration; (d) lower leg conducting, free-wheeling.

The waveforms of Figs.4-67 and 4-68, which are valid for a *pure d.c. load current*, show how the load current is resonantly transferred between the upper and lower chopper legs, as a result of TH_1 and TH_2 being triggered in turn. As seen from the $i_{TH\,1}$-waveform in Fig.4-67 and that for $i_{TH\,2}$ in Fig.4-68, the thyristor current tends to drop to zero after the half resonant period of current commutation; this may lead to premature thyristor turn-off. It is therefore essential that the gating pulses should continue during the entire thyristor conduction period.

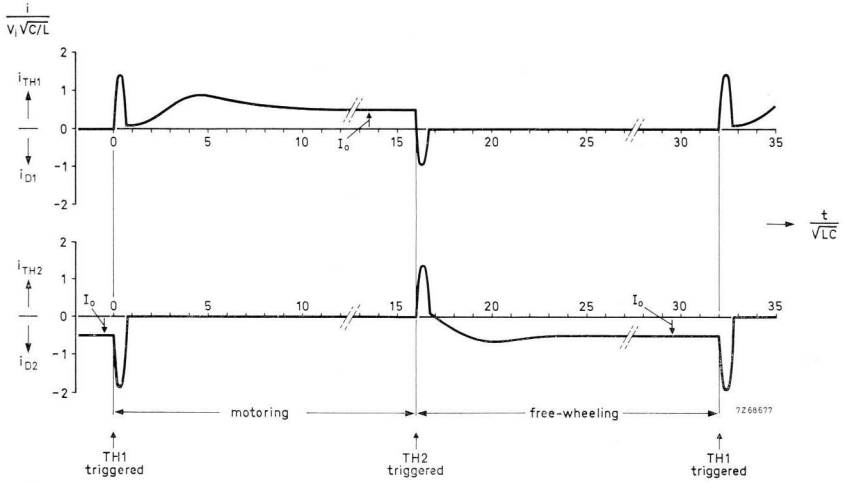


Fig.4-67 Showing transfer between both chopper legs of load current I_o for motoring condition (ref. Fig.4-66a, b).

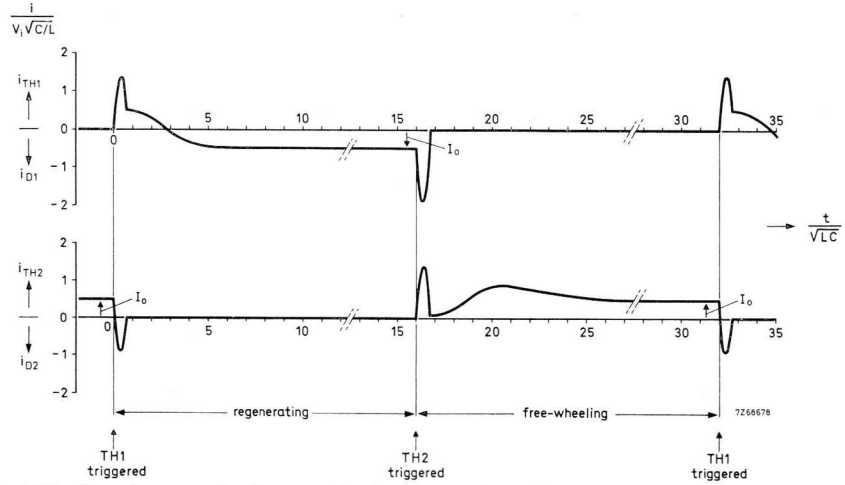


Fig.4-68 Showing transfer between both chopper legs of load current I_o for regeneration (ref. Fig.4-66c, d).

Assuming the commutation inductor to have six percent leakage inductance per winding, the circuit-imposed turn-off time t_{off} versus load current follows from Fig.4-69, where C is the commutation capacitance, L the commutation inductance (Fig.4-65), I_o the load current and V_i the d.c. input voltage. It is seen that the turn-off time does not drop below $0{,}35\sqrt{(LC)}$ if the load current is limited to half the resonance current $V_i\sqrt{(C/L)}$.

For six percent leakage inductance and taking the maximum load current $I_{o\ max}$ to be:

$I_{o\ max} = 0{,}5\ V_i\sqrt{(C/L)}$,

the following expressions can be drawn up:

Circuit-imposed turn-off time $t_{off} = 0{,}35\sqrt{(LC)}$ (Fig.4-69).
Peak repetitive thyristor current $I_{TRM} = 2{,}8\ I_{o\ max}$ (Figs.4-67 and 4-68).
Damping resistor $R_2 \approx 2\sqrt{(L/C)}$.

According to Fig.4-65: $V_i = 500$ V, $L = 280$ µH, $C = 10$ µF. So we obtain:

$I_{o\ max} = 47$ A, $t_{off} = 18{,}5$ µs, $I_{TRM} = 132$ A, $R_2 \approx 11\ \Omega$.

The BTW30-1200RM thyristor has 12 µs turn-off time and is, thus, suitable for this chopper; its average current rating is 12 A. Currents up to 47 A will be safely commutated; this current can be carried by the BTW30 at low duty cycle and under inrush condition.

Fig.4-70 shows the construction of the commutation inductance.

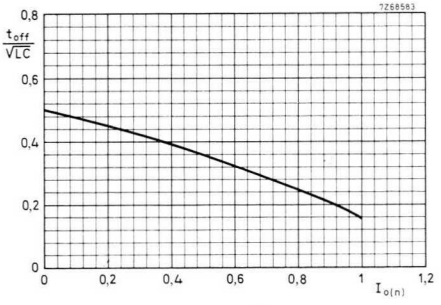


Fig.4-69 Plot of normalized turn-off time $t_{off}/\sqrt{(LC)}$ vs. normalized load current $I_{o(n)} = (I_o/V_i)\sqrt{(L/C)}$ for six percent leakage inductance.

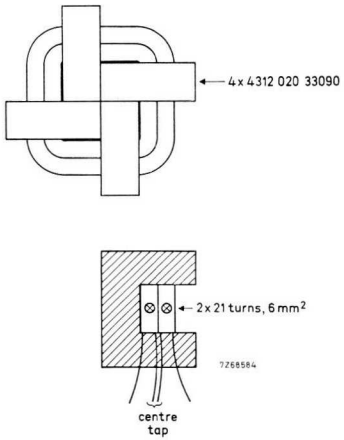


Fig.4-70 Construction of commutation coil for regenerative two-thyristor chopper.

Trigger circuit using PWM

For reasons previously cited, the trigger circuit of Fig.4-71 generates trigger pulses during the entire thyristor conduction period. Fig.4-72 shows the waveshapes. The operation of the sawtooth generator and the comparator is described in Section 1.2.2. Comparator output, waveform C, controls the pulse generator triggering TH_2, and inverted output, waveform F, controls the pulse generator triggering TH_1. So, thyristors TH_1 and TH_2 are triggered in turn. Delay networks R_{11} C_4 and R_{12} C_6 create 80 μs dead zones between the periods of thyristor triggering (compare trigger signals E and H). Therefore, a thyristor cannot be triggered during the previous interval of current commutation (about 40 μs). If premature triggering were to occur, the current through the thyristor to be turned off may well fail to reverse; both thyristors would then conduct and the chopper d.c. supply would become shorted. The arrows in the waveforms show the effect of an increase in the input control signal V_{contr} (chopper output changing linearly with the control voltage).

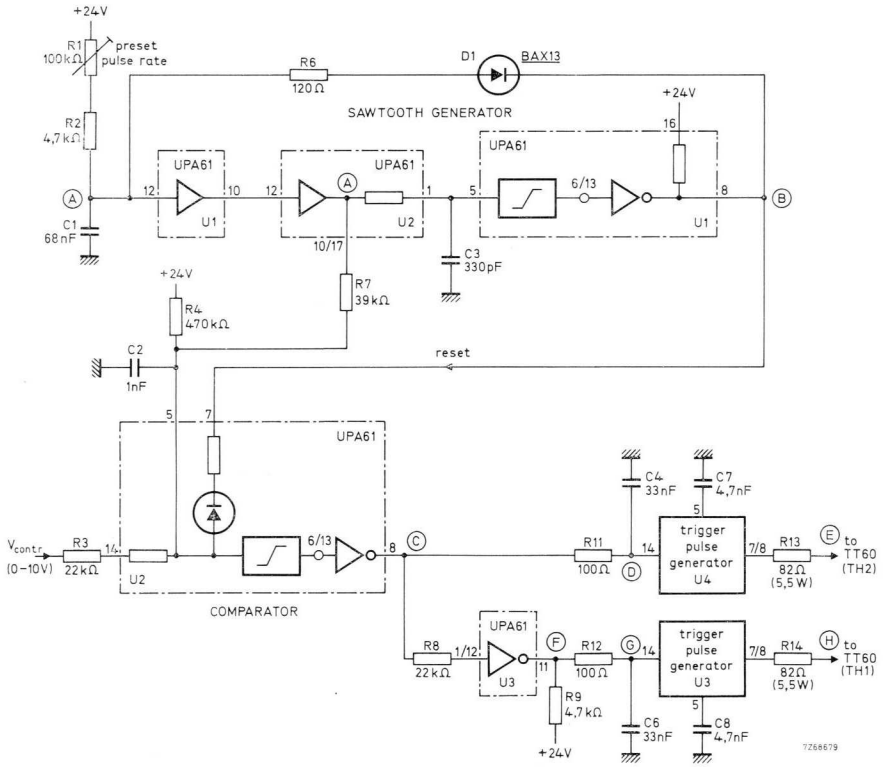


Fig.4-71 Trigger circuit for regenerative two-thyristor chopper using PWM.

Adjustment (Fig.4-73):

1. *Preset the chopper operating frequency with R_1, 400 Hz being a suitable value.*
2. *The threshold of V_{contr} at which copper output control starts can be shifted by changing the value of R_4.*

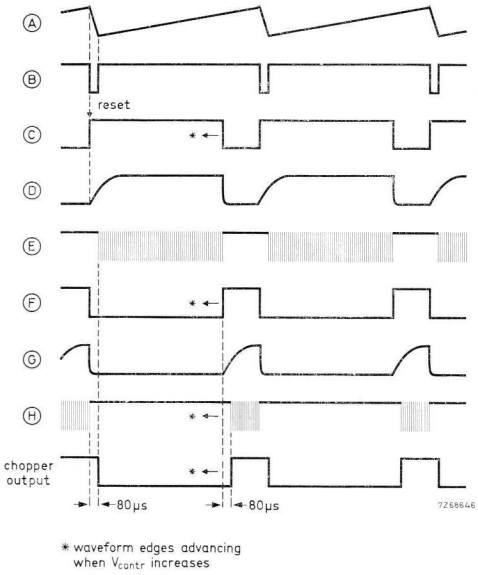


Fig.4-72 Waveforms to Fig.4-71.

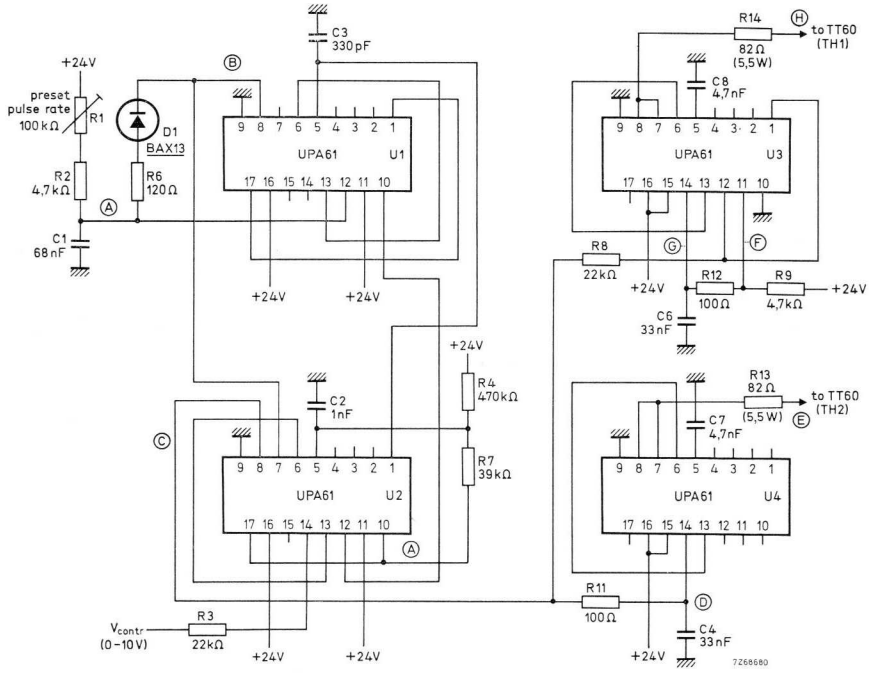


Fig.4-73 Wiring diagram of trigger circuit in Fig.4-71. A, B etc. refer to the waveforms in Fig.4-72.

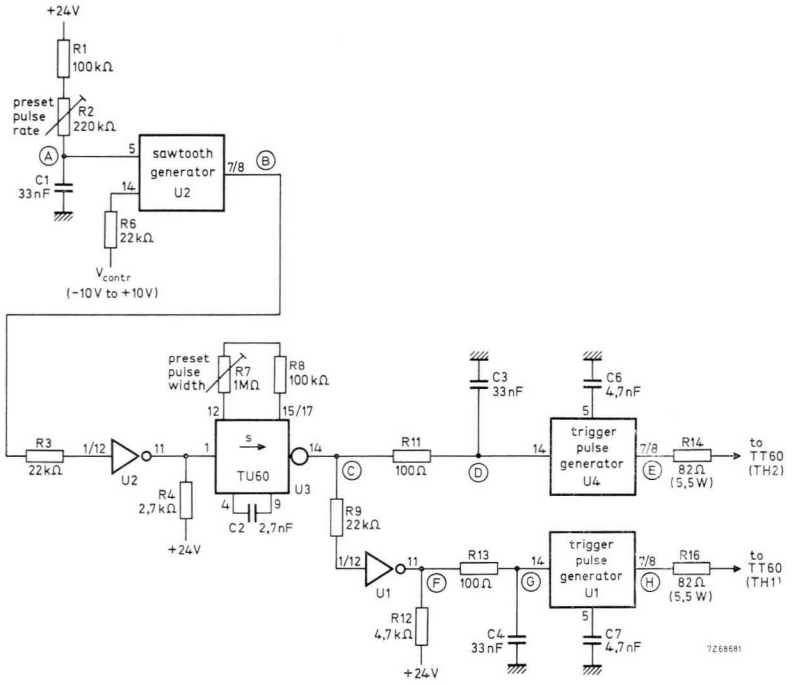


Fig.4-74 Trigger circuit for regenerative two-thyristor chopper using PRM.

Trigger circuit using PRM

The trigger circuit is shown in Fig.4-74, and the waveforms are seen in Fig.4-75. With V_{contr} increasing, C_1 charges to a lower level because the trip-on point of the sawtooth generator is advanced; as a result, the circuit operates at a higher repetition frequency, and the chopper yields a higher output voltage. As in the previous circuit, trigger pulse generators U_1 and U_4 are driven by complementary signals, waveforms *C* and *F*. Networks R_{11} C_3 and R_{13} C_4 produce the 80 µs dead zones required to ensure safe chopper operation. The pulse width of the chopper output is 55 µs + t_d, as can be seen from the waveforms; delay time t_d is approximately equal to C_2 $(R_7 + R_8)$.

Adjustment (Fig.4-76):

1. *Chopper operating frequency for a given value of V_{contr} is pre-adjusted with R_2.*
2. *Chopper output pulse width is adjusted with R_7; wider pulses are obtained by increasing the value of C_2.*

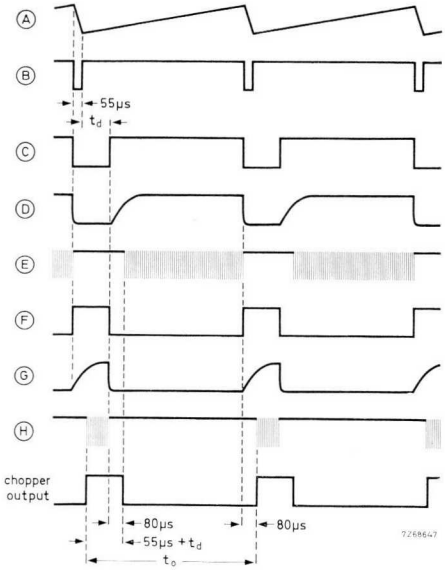


Fig.4-75 Waveforms for Fig.4-74. With the control voltage increasing, repetition period t_o becomes shorter, which results in a higher chopper output.

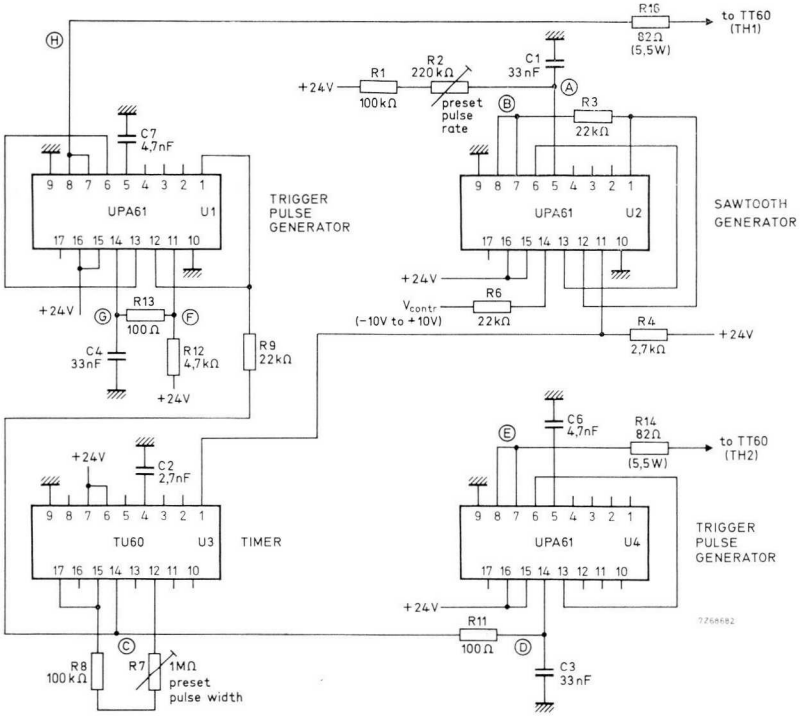


Fig.4-76 Wiring diagram of trigger circuit in Fig.4-74. A, B etc refer to the waveforms in Fig.4-75.

4.5.5 50 kVA, 1 kHz INVERTER[12])

Power circuit

The inverter circuit of Fig.4-77 can deliver 125 A in a *capacitive* load at 400 V maximum output voltage. The load resonates with the inductance of the output transformer and is excited by full-wave current pulses i_{e1} and i_{e2} passed by TH_1 D_1 and TH_2 D_2 respectively (see the waveforms of Fig.4-78). Because the quality factor of the load is about 100, thyristors and diodes of moderate current rating suffice to obtain a high reactive output power.

The output voltage is variable between 100 V and 400 V by changing its phase delay φ with respect to the instants of thyristor triggering. This influences the degree of off-resonance operation, and thus changes the reactive power pumped into the load. The phase angle φ should not be greater than $-10°$, to have a safe margin of operation; for φ becoming positive, the turn-off time presented to the thyristors would drop sharply.

Fig.4-79 illustrates the construction of the 50 kVA output transformer.

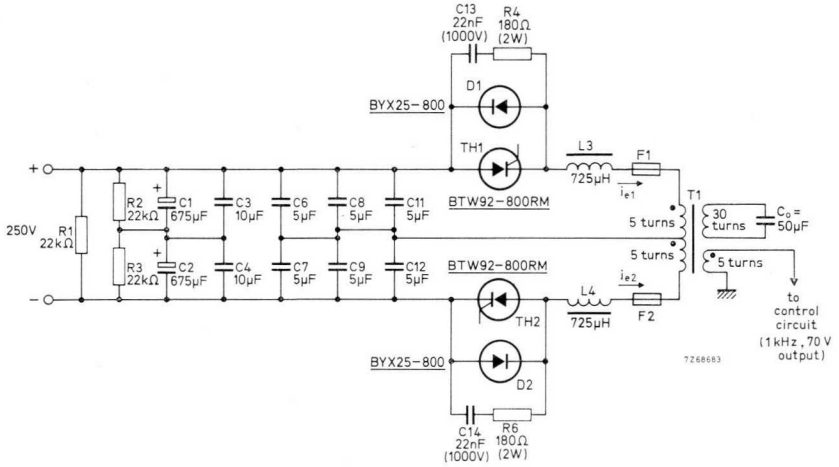


Fig.4-77 50 kVA, 1 kHz inverter. F_1, F_2 = 16 A, fast fuse.

[12]) AI No. 464, ordering code 9399 264 46401 – 50 kVA, 1 kHz Inverter.

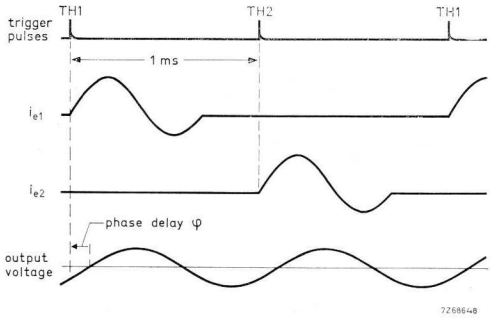


Fig.4-78 50 kVA, 1 kHz inverter waveforms.

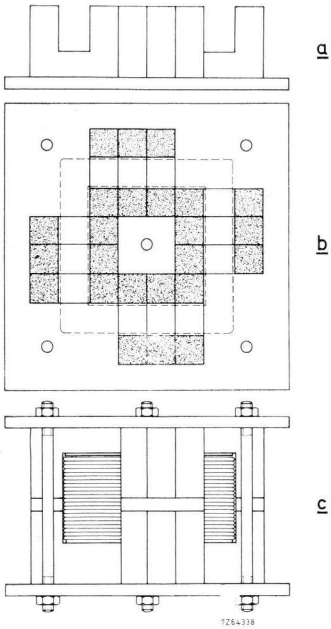


Fig.4-79 50 kVA output transformer; (a) (b) show one half of the transformer consisting of U-shaped Ferroxcube cores 4312 020 33090 and (c) shows the complete unit.

Trigger and control circuit

The operation of the trigger circuit in Fig.4-80 is seen from waveforms A to D_2 in Fig.4-81, and the operation of the 1 kHz pulse oscillator and the scaler of two is explained in Sections 1.2.2 and 2.8.7, respectively. The trigger gates deliver a trigger signal (output LOW) only during the periods when both their inputs (pins 7 and 14) are HIGH. Signals C and $\bar{C}$ are complementary, so thyristors TH_1 and TH_2 are triggered in turn.

The function of the control circuit is to keep the phase shift of output voltage and, thus, the output voltage itself constant. Waveforms E to $\bar{G}$ show the operation of this circuit. The 1 kHz, 70 V input signal, obtained from a separate winding on the inverter output transformer in Fig.4-77, is rectified (waveform

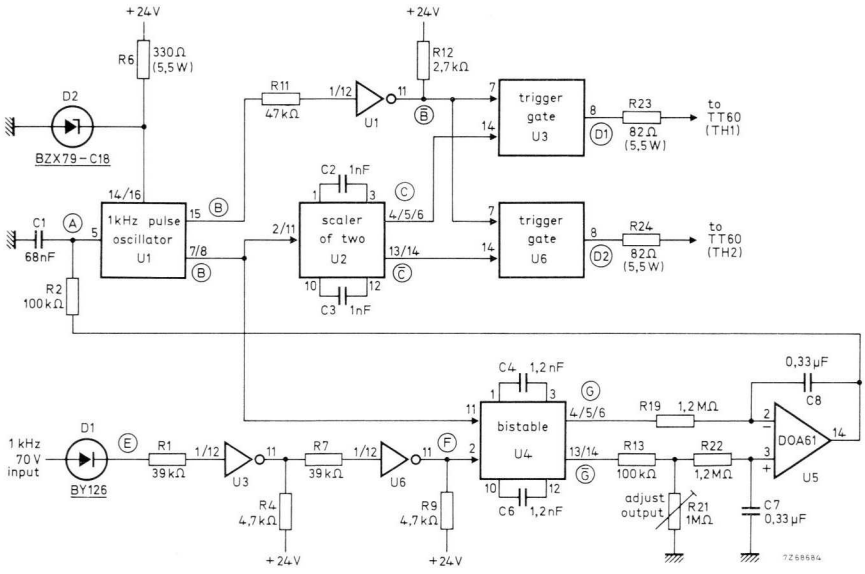


Fig.4-80 Trigger and control circuit of 50 kVA, 1 kHz inverter. Waveforms are given in Fig.4-81.

E), squared (waveform F) and fed to the bistable together with the 1 kHz pulse oscillator output (waveform B). The bistable output and, as a consequence, the d.c. output from the DOA61 is directly related to the phase delay φ of the inverter output voltage. Suppose φ tends to increase. According to waveforms G and $\bar{G}$, the average value of the signal at the inverting DOA61 input increases and that of the signal at the non-inverting DOA61 input decreases. As a result, the d.c. output from the DOA61 decreases, C_1 is charged at a lower rate, and the thyristor trigger pulses are delayed. This counteracts the increase of phase angle φ. The phase delay and thus the inverter output voltage depends on the setting of R_{21} (lower output when decreasing the resistance).

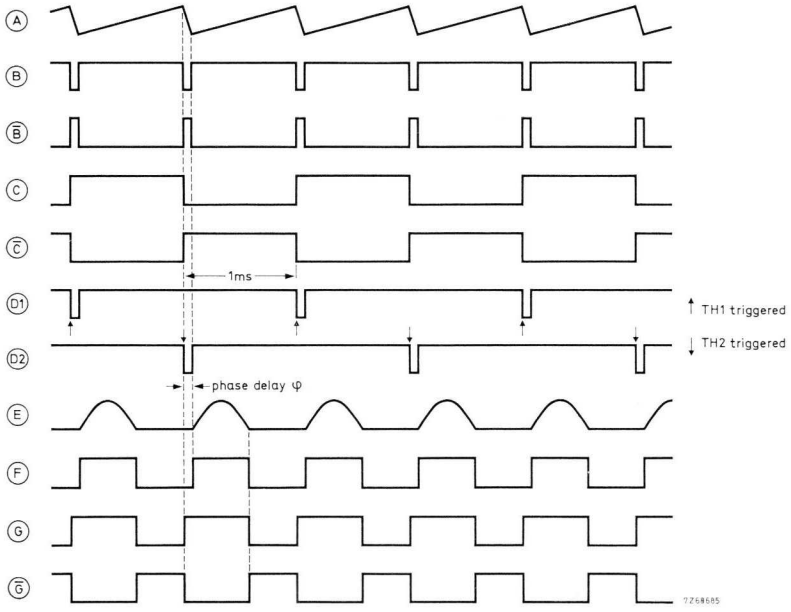


Fig.4-81 Waveforms for Fig.4-80.

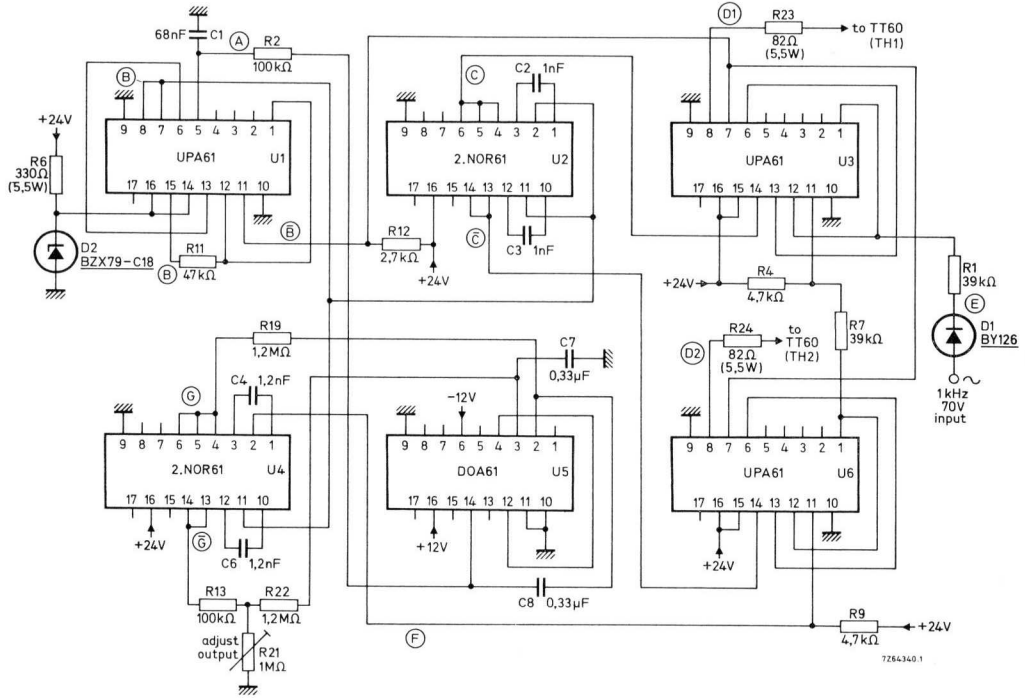


Fig.4-82 Wiring diagram of trigger and control circuit for 50 kVA, 1 kHz inverter. For waveforms A, B, etc., see Fig.4-81.

Adjustment (Fig.4-82):

Use R_{21} to adjust the inverter output.

4.5.6 400 HZ, 110 V BRIDGE INVERTER

Power circuit

The 400 Hz inverter circuit of Fig.4-83 can deliver 2 kW at 110 V r.m.s. output. An alternative output voltage can be obtained by changing the turns ratio of T_1. The circuit principle has been previously explained with the aid of Fig.4-50 in Section 4.5.1. Choppers 1 and 2 each deliver a square-wave output (50% thyristor duty cycle) whose phase relationship is determined by the control circuit in such a way that the a.c. output voltage remains constant despite load or d.c. input fluctuations (d.c. input maximum 540 V). Harmonics are suppressed by band-pass filter C_7 L_2 C_6 L_3 so that the output will be sinusoidal. Four heat-sinks are needed, namely for D_1 TH_1, D_2 TH_2 D_3, TH_3 D_6, D_4 TH_4 D_7. The advantage of this inverter over the McMurry Bedford type is that the turn-off time presented to the thyristors depends less on the load phase angle because this time is determined by the period that the parallel diodes conduct; however, the efficiency is somewhat lower. The choppers must be able to pass current in both directions, therefore the regenerative type discussed in Section 4.5.4 is used.

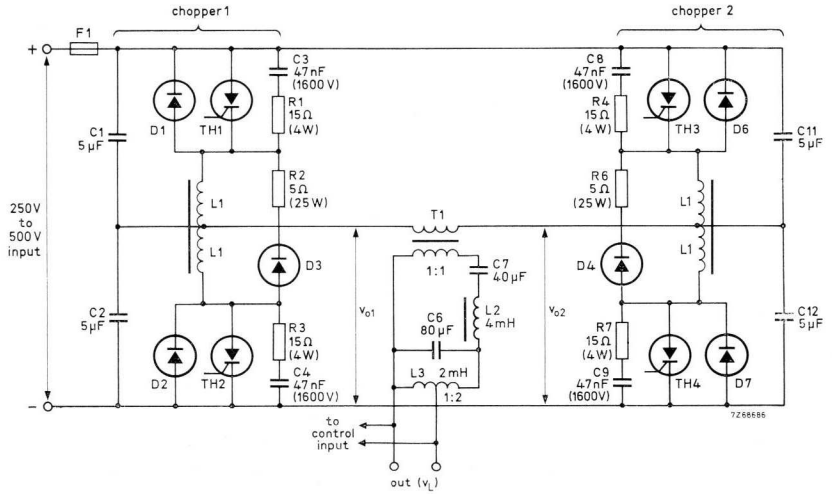


Fig.4-83 400 Hz, 110 V, 2 kW bridge inverter. D_1 D_2 D_6 D_7 = BYX25-1000; D_3 D_4 = BYX25-1000R; TH_1 to TH_4 = BTW30-1200R; F_1 = 20 A fast fuse; L_1 = 170 μH, 20 μH leakage inductance per winding.

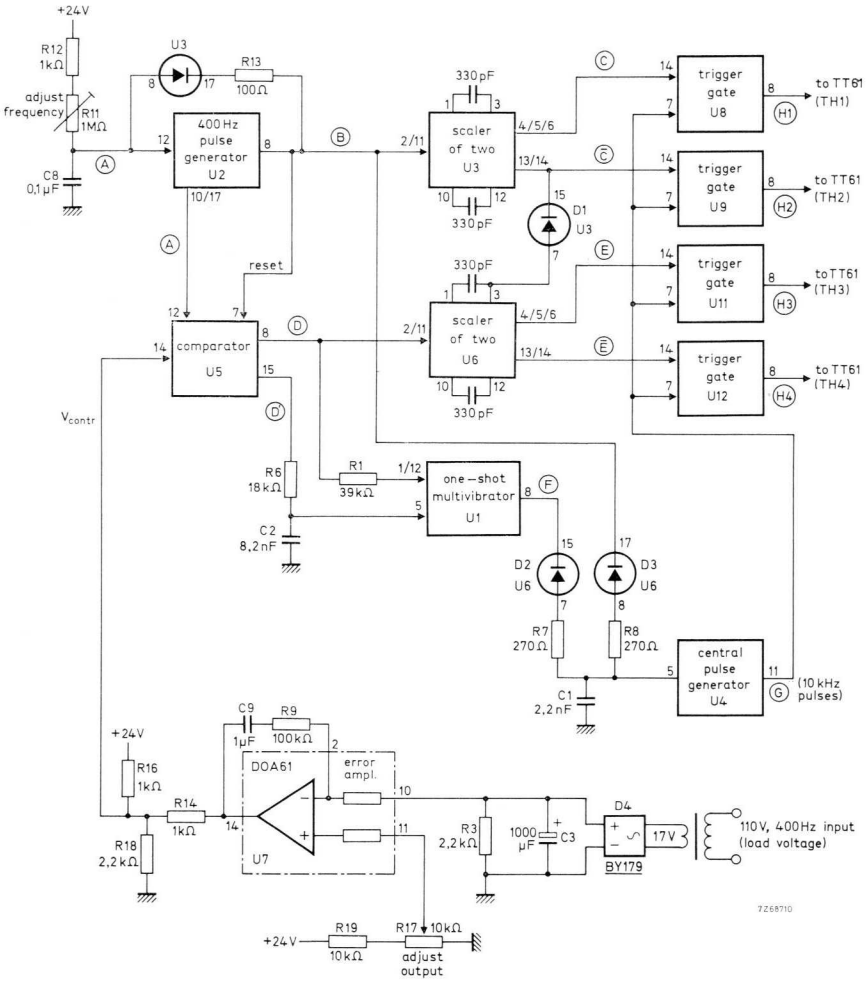


Fig.4-84 Trigger and control circuit of 400 Hz, 110 V bridge inverter. See waveforms of Fig.4-85.

Trigger and control circuit

Fig.4-84 illustrates a trigger and control circuit providing stabilization of the inverter output. The 400 Hz pulse generator and comparator operate in the same manner as the circuit of Fig.4-62 (Section 4.5.3). In this circuit the control voltage V_{contr}, obtained from the DOA61 op amp, is the result of comparison between the reference voltage at the wiper of R_{17} and the a.c. load voltage rectified by D_4 and smoothed by C_3. Circuit waveforms are according to Fig.4-85, which also shows the chopper outputs v_{o1} and v_{o2} and the load voltage v_L.

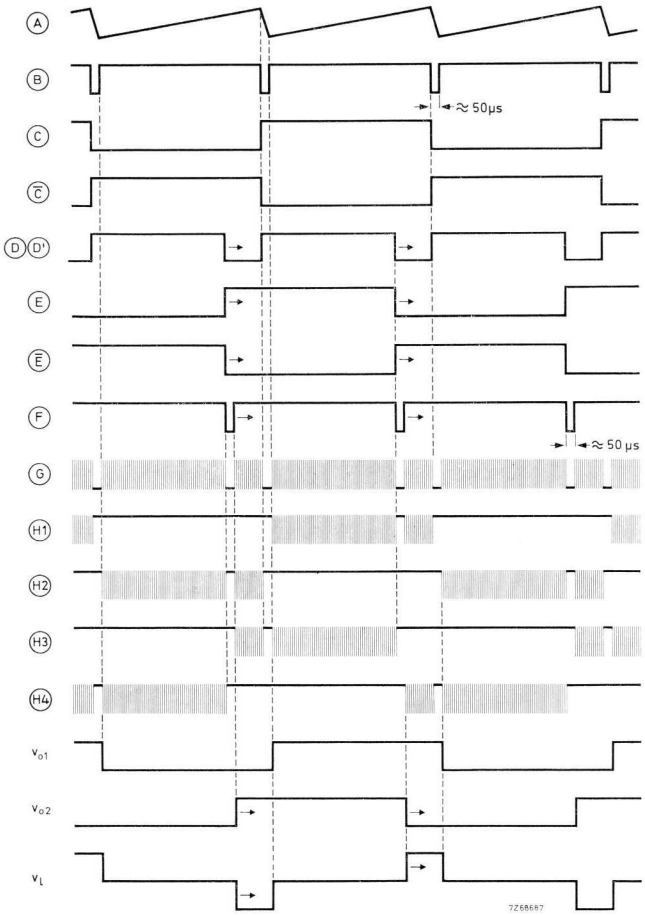


Fig.4-85 Waveforms for Fig.4-84. Arrows indicate shift of waveform edges when the inverter output voltage tends to rise.

A central pulse generator is necessary for thyristor triggering because two devices must be turned on simultaneously. The scalers of two cause the choppers to produce square-wave outputs. Diode D_1 ensures the correct phase relationship between the outputs of the scalers of two. The thyristor trigger gates are supplied by the central pulse generator and the scaler-of-two outputs. When the scaler-of-two output at input pin 14 of any trigger gate becomes HIGH, the 10 kHz pulses from the central pulse generator are passed through the trigger gate to the trigger transformer and thyristor triggering occurs. To obtain a jitter-free sinewave output, the central pulse generator is synchronized with outputs *B* and *D* via gating diodes D_2 D_3. The one-shot multivibrator is needed to obtain synchronization pulses from output *D*.

Output stabilization occurs as follows (see arrows in Fig. 4-85). If the load voltage v_L tends to increase, the DOA61 output decreases and the trailing edges of waveforms D and D' are retarded. As a result output v_{o2} is delayed with respect to output v_{o1}, so that the increase in v_L is counteracted.

Figs.4-86 and 4-87 show the wiring diagram of the trigger and control circuit.

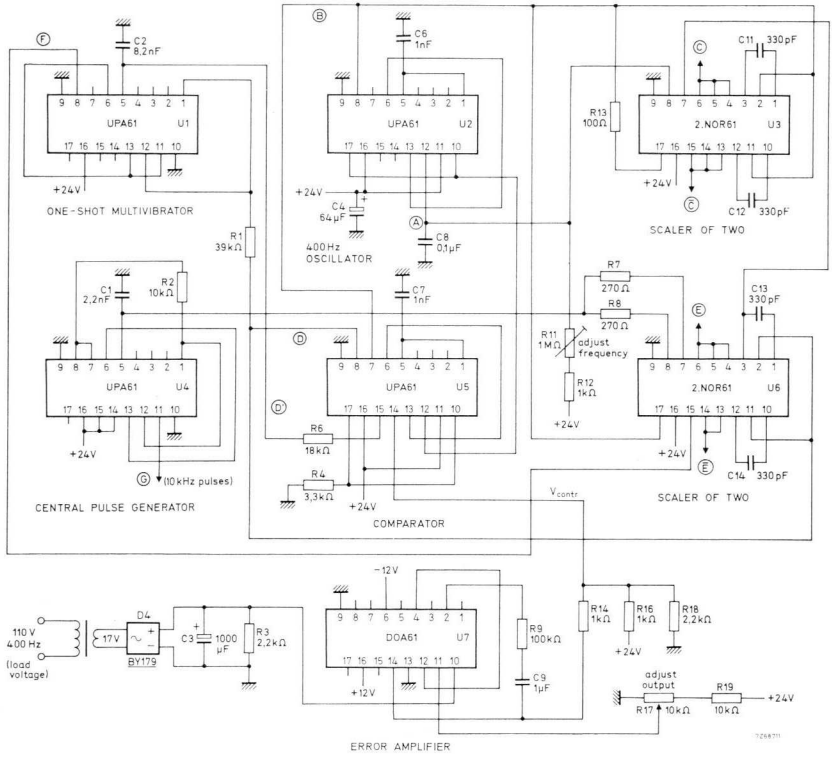


Fig.4-86 Wiring diagram of U_1 to U_7. See waveforms of Fig.4-85.

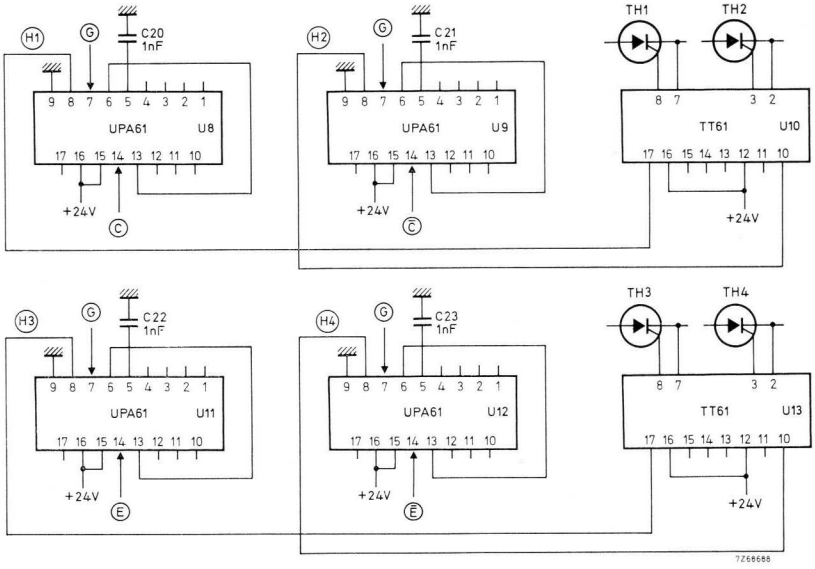


Fig.4-87 Wiring diagram of U_8 to U_{13}. See waveforms of Fig.4-85.

Adjustment (Fig.4-86):

1. *With R_{11} adjust the inverter output frequency to 400 Hz.*
2. *With R_{17} adjust the inverter output voltage to the desired value (about 100 V r.m.s.).*

4.6 A.C. Motor controllers

4.6.1 Discussion and circuit survey

A.C. mains distribution systems have been in wide-spread use for many years and a.c. motors are well established as reliable electro/mechanical power converters. A.C. motors may be subdivided into synchronous and asynchronous types. Synchronous motors are more expensive than asynchronous types and are generally used in those applications only where speed must be load-independent e.g. frequency converters. Asynchronous motors are most commonly used. Because the speed of an asynchronous motor does not change significantly with load variations, this motor is well-suited to drive machine tools.

In an asynchronous motor, the rotor can be a squirrel-cage type or it can have windings terminated with slip-rings. The latter type is intended for rotor resistance control where a high starting torque and full-range speed control is required. The squirrel-cage motor is by far the least expensive and, therefore, the most widely used.

The invention of the double-cage rotor has allowed a substantial improvement in motor performance. See Fig.4-88. The high-ohmic cage improves the rotor $\cos \varphi$ at high rotor slip, thus providing a high torque at low speeds down to zero r.p.m.; the low-ohmic cage yields a high torque at speeds close to synchronous speed. Consequently, double-cage motors have the advantages of a high starting torque and low rotor losses (because of low slip).

A.C. motors are less expensive than d.c. motors, because they do not have a commutator, but their speed range is more limited. For applications needing a very high starting torque, for instance traction, the d.c. series motor is still the best proposition.

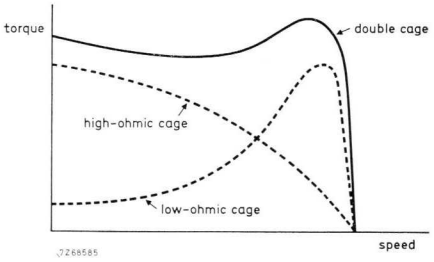


Fig.4-88 Torque/speed characteristics of double-cage motor.

A.C. motor speed control may be achieved by varying the stator supply voltage, the rotor resistance or the stator supply frequency. The latter method is the only one allowing control of synchronous motors.

Slip control by varying the stator supply voltage[13]). This type of control is easily achieved by using triacs or thyristors. Its principle is shown in Fig.4-89. The motor working points P_1 to P_5 for an increasing stator supply voltage are the intersections between the motor torque/speed characteristics and the load characteristic. For point P_4, the rotor slip is expressed as $(n_s\text{-}n_4)/n_s$, where n_s is the synchronous speed; likewise, for P_3 the rotor slip is $(n_s\text{-}n_3)/n_s$, etc. It is seen that the slip is high at a low stator supply voltage, which results in large rotor currents and, thus, large rotor losses. The type of load schematically shown is that which occurs with fan control (torque approximately proportional to square of speed). Provided the starting torque is zero, full-range speed control results. This is not true, however, for other load types, as demonstrated by Fig.4-90.

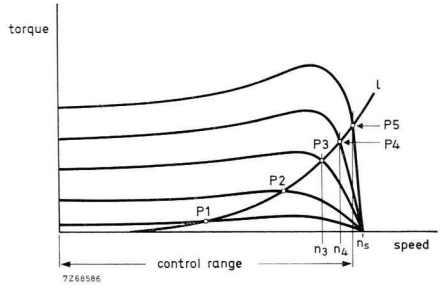


Fig.4-89 Slip control by varying the stator supply voltage. A lower curve accords with a lower stator voltage. *l* = load characteristic.

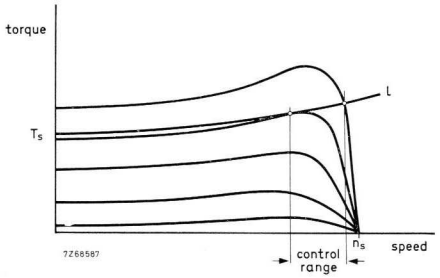


Fig.4-90 This diagram illustrates the very restricted speed control range when a high starting torque T_s is required. *l* = load characteristic.

[13]) AI No. 449, ordering 9399 214 44901 – Modular Power Control, Half-control Systems.
AI No. 453, ordering 9399 214 45301 – Modular Power Control, Full-control Systems.

Characteristics of this control method are: (a) it is simple and it is suitable for controlling the popular squirrel-cage motor, (b) it has a low efficiency because of the high rotor losses involved, (c) except for a fan load[14]) it has a limited speed control range.

Slip control by varying the rotor resistance. The principle of this control method, which is only applicable to slip-ring motors, is clear from Fig.4-91. It is seen that insertion of rotor resistance increases the starting torque (because of improved rotor cos φ). Owing to the high torque attainable over the whole speed range, the slip-ring motor/variable rotor resistance arrangement is valuable for hoists.

Characteristics of this control method are: (a) it provides full-range control for any load type – see load lines l_1 and l_2 in Fig.4-91, (b) it has a poor efficiency at low speeds because of the power dissipation in the rotor resistance*.

Speed control by varying the stator supply frequency. Speed control of asynchronous motors can best be achieved by varying the stator supply frequency, because then slip and hence rotor losses are kept low. This control mode offers four-quadrant control and is, therefore, universal. By changing the stator supply voltage in direct proportion to the frequency, saturation of the stator core at low frequencies is avoided.

To understand this control method, Fig.4-92 should first be examined. The diagram shows the motor torque/speed curve now extended with the areas of regeneration and "plugging"; the stator current curve has also been added. For the motor r.p.m. between zero and synchronous speed n_s, motoring occurs. If the motor r.p.m. exceed the synchronous speed, the motor torque reverses, which means that the motor is driven by its load. Further, the phase angle of the stator current shifts 180 °; the current "flows back" into the stator supply source (stator current curve passing the horizontal axis). Because power is returned to the stator supply, a condition of regeneration (regenerative braking)

[14]) AN No. 80, ordering code 9399 250 58001 – A.C. Fan Motor Control.

* Efficiency is improved by regenerating the rotor energy via a three-phase diode bridge (connected to the rotor output) and a three-phase full-controlled bridge (connected to the three-phase a.c. supply); see AI No. 453, ordering code 9399 214 45301 – Modular Power Control, Full-control Systems.

arises. "Plugging" occurs when interchanging two phases (which causes the stator field to rotate in opposite direction to the rotor). This method of speed reversal causes high stator currents with the risk of damaging the motor; it is similar to "plugging" a d.c. motor, that is, interchanging the two supply leads to a running motor.

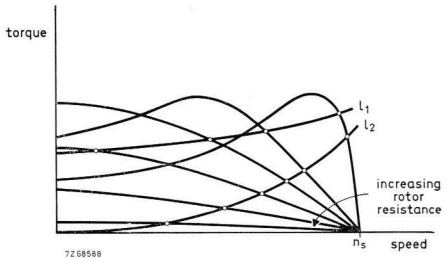


Fig.4-91 Slip control by varying the rotor resistance. Dots show working points for load characteristics l_1 and l_2.

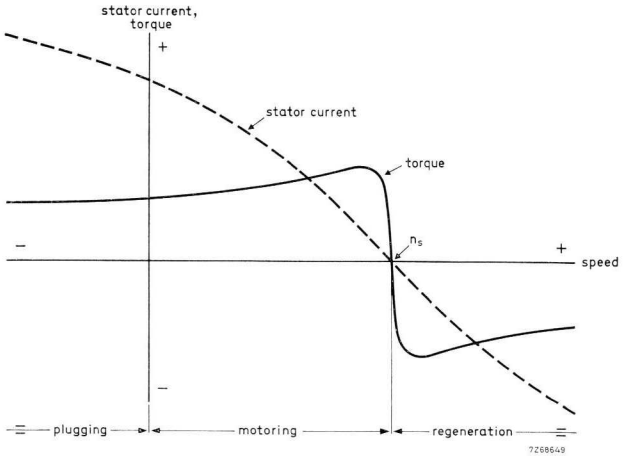


Fig.4-92 A.C. motor diagram showing the three working areas.

When the stator supply frequency is varied, the motor torque/speed curve shifts horizontally, its shape remaining approximately the same; see Fig.4-93. The abscissa of the intersection point (synchronous speed) with the horizontal axis changes in proportion to frequency, i.e. the intersection point will be close to the origin if the frequency is low. The diagram also gives the four quadrants, I to IV, of motor control. Suppose the motor is working in point P_1 (quadrant I). The heavy line between P_1 and P_2 shows the shift of the working point as the result of speed reversal. When the stator supply frequency is reduced, the motor torque/speed curve shifts to the left. The speed corresponding to P_1 is then greater than synchronous speed, so that regeneration occurs and the working point is shifted to quadrant IV. When motor speed has dropped to almost zero, two of the three stator supply phases are reversed, then the frequency is increased; this causes the motor torque/speed curve to shift further to the left and the working point to move into quadrant III (motoring at reversed speed) until P_2 is reached. The dotted line shows the shift of the working point as the result of the original motor working condition being re-assumed.

Characteristics of this control mode are: (a) it provides *four-quadrant* control with the associated advantages of motor control from full forward speed to full reverse speed, rapid speed changes are possible, regenerative braking with little energy loss is provided, (b) efficiency is high because rotor losses are low, (c) the inexpensive squirrel-cage motor can be used.

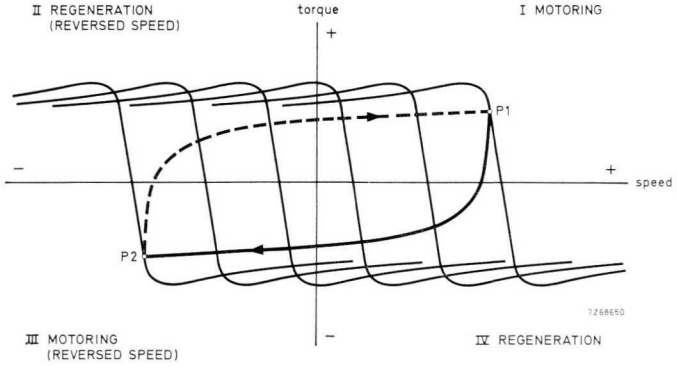


Fig.4-93 Four-quadrant a.c. motor control.

With electronic control, almost any motor characteristic can be reproduced; for instance, that of a synchronous motor is obtained by speed stabilization. Using an inverter with continuously variable frequency gives both a large speed control range (typical of d.c. motors) and four-quadrant a.c. motor control. Facilities can be included in a single control system to provide speed, torque or power control. The merit of electronic motor control is its flexibility, so that the simple squirrel-cage motor can be used to solve any control problem.

Table 4-9 gives a survey of the a.c. motor controllers discussed here; all controllers are supplied from a rectified a.c. voltage.

Table 4-9. A.C. motor controllers.

circuit	regenerative	output power	output frequency	applications
3 h.p. induction motor controller, Section 4.6.2	no	3 kVA	250 Hz, 300 Hz, 400 Hz.	high speed drive of single-phase motors.
three-phase motor controller, Section 4.6.3.	yes	10 kVA	5 Hz to 50 Hz.	four-quadrant a.c. motor control.

4.6.2 3 H.P. INDUCTION-MOTOR CONTROLLER[15])

Power circuit

The McMurry Bedford inverter of Fig.4-94 is intended for supplying a 3 h.p. induction motor at a frequency of 250 Hz, 300 Hz or 400 Hz, to obtain a high-speed drive system, motor speeds to 24 000 r.p.m. being possible. The trigger

[15]) AN No. 150, ordering code 9399 260 65001 – Parallel Inverter for 3 h.p. Induction Motors.

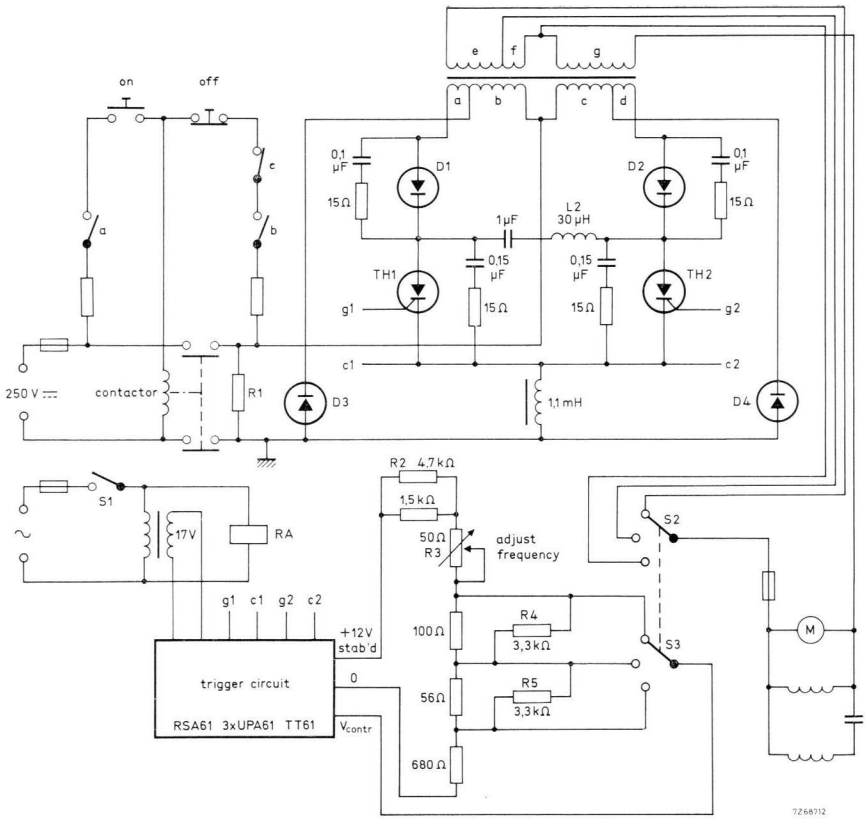


Fig.4-94 3 H.P. induction motor controller. D_1 D_2 = BYX25-1000, D_3 D_4 = BYX25-1000R, TH_1 TH_2 = BTW30-800R, R_1 = 4,7 kΩ, 15 W. Transformer windings: *a b* and *c d* bifilar-wound, *a d* each 18 turns, *b c* each 97 turns, *e* 26 turns, *f* 13 turns, *g* 63 turns. Contacts *a* and *b* are on the relay marked „RA"; contact *c* opens when S_2 S_3 is operated.

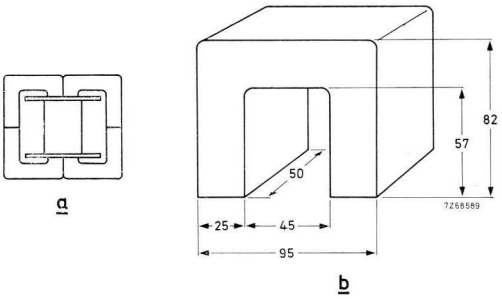


Fig.4-95 Inverter output transformer (a) consists of four identical core sections (b) „C" type, 0,01 cm strip.

rate of TH_1 and TH_2 and, thus, the inverter working frequency is determined by the control voltage V_{contr} which is switched with S_3. Switch S_2 coupled to S_3 adjusts the square-wave output to 137 V, 165 V or 220 V, in proportion to the frequency chosen. In this way, stator core saturation at the lower frequencies is prevented. (If the motor is amply rated, the control circuit can be modified to obtain three overlapping frequency ranges for continuous speed control; trimmer R_3 is then increased in value and R_2 correspondingly decreased.)

The inverter cannot be connected to its d.c. supply unless the trigger circuit has been energized (closure of S_1). Further, frequency switching interrupts the d.c. supply (contact c opened while S_2 S_3 is operated), to exclude the risk of commutation failure and, thus, damage to the thyristors.

With the transformer depicted in Fig.4-95, 3 kW output power can be produced in a 20 Ω resistive load at more than 90% efficiency. Winding data is given in the caption to Fig.4-94.

Adjustment (Fig.4-94):

1. *Use R_3 to adjust the inverter operating frequency to 250 Hz with S_2 S_3 in the lowest position (magnitude of V_{contr} equal to 4,1 V).*
2. *With S_2 S_3 in mid position, change the value of R_5, if necessary, to obtain 300 Hz operating frequency (magnitude of V_{contr} equal to 4,5 V).*
3. *With S_2 S_3 in the highest position, change the value of R_4, if necessary, to obtain 400 Hz operating frequency (magnitude of V_{contr} equal to 5,0 V).*
4. *Repeat the above steps if necessary.*

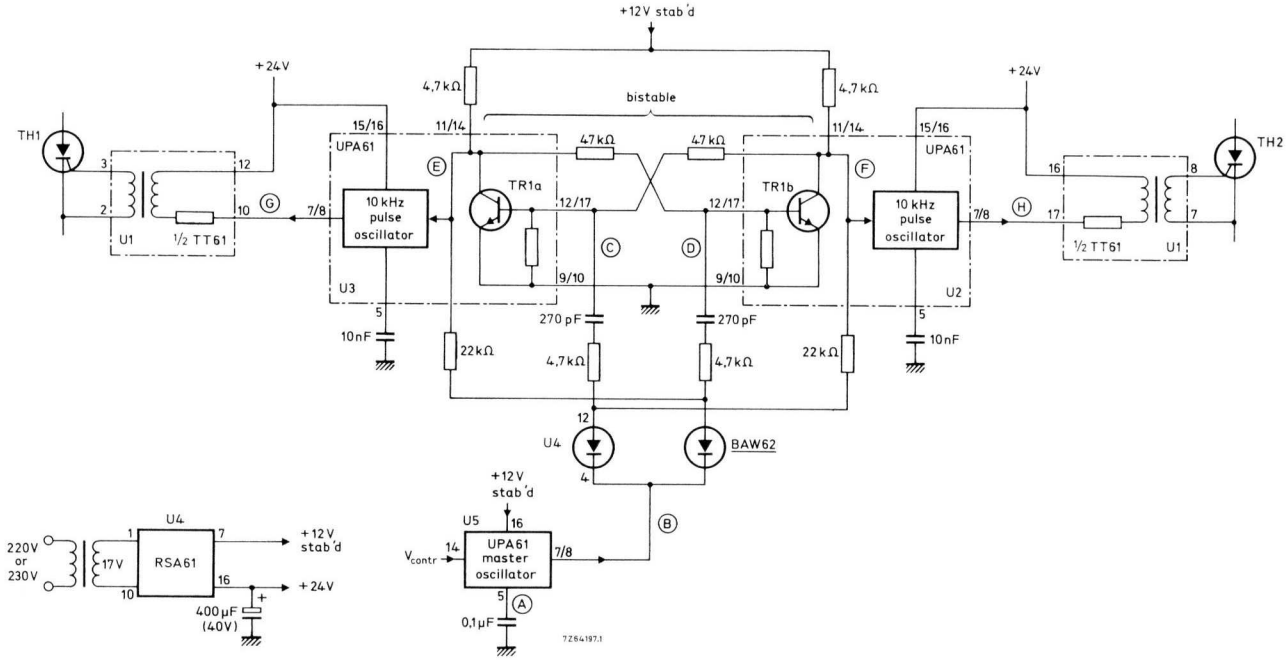


Fig.4-96 Trigger circuit for 3 H.P. induction motor controller. Waveforms A to H are given in Fig.4-97.

Trigger circuit

The thyristor trigger circuit is given in Fig.4-96, and its waveforms are shown in Fig.4-97. The master oscillator has been described in Section 1.2.2 and the operation of the 10 kHz pulse oscillator is outlined in Section 2.4.3. Bistable circuit TR_{1a} TR_{1b} is driven by the master oscillator output pulses (waveform *B*). Because the bistable outputs (waveforms *E* and *F*) switch in turn to HIGH level, trigger pulses are supplied alternately to TH_1 and TH_2 (waveforms *G* and *H*). The p.r.f. of the master oscillator, and thus the trigger rate of TH_1 and TH_2 depends on the magnitude of the control voltage V_{contr}; 180 ° trigger pulse bursts are produced, ensuring thyristor turn-on despite the inductive load. A stabilized 12 V supply is used to feed the master oscillator and the control network (Fig.4-94), so that mains voltage fluctuations do not affect the inverter operating frequency.

Fig.4-98 gives the wiring diagram of the trigger circuit.

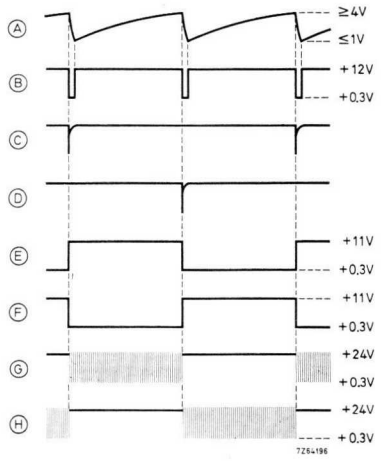


Fig.4-97 Voltage waveforms for Fig.4-96.

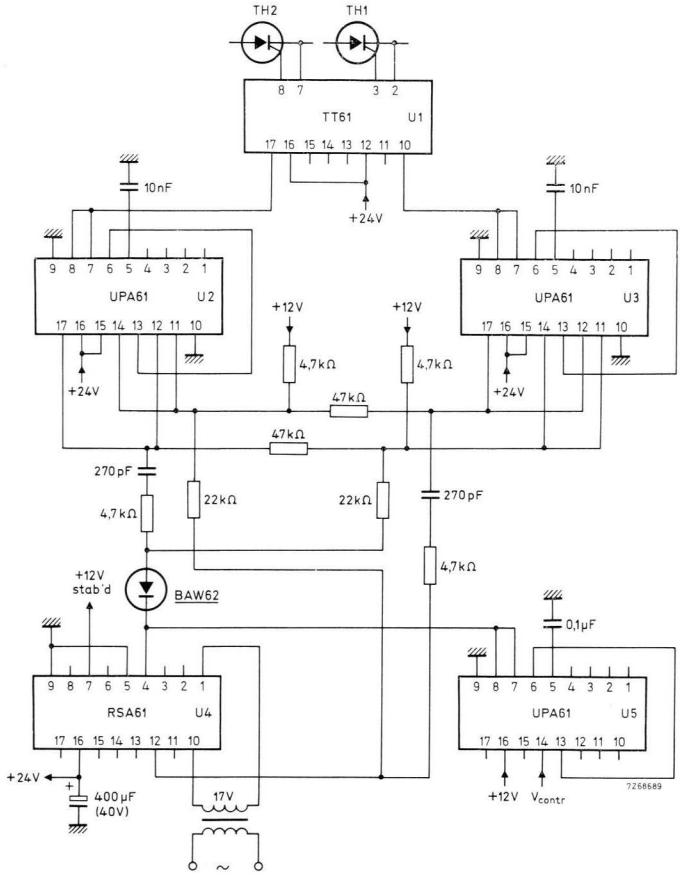


Fig.4-98 Wiring diagram for Fig.4-96.

4.6.3 THREE-PHASE MOTOR CONTROLLER [16])

Power circuit

The motor speed controller discussed here is a three-phase bridge inverter supplying a.c. power at a variable frequency (between 5 Hz and 50 Hz); it, therefore, offers the facility of four-quadrant three-phase motor control. Continuous output rating is 7,5 kW. The circuit consists of choppers, which allow bidirectional passage of load current in conformity with a.c. operation. (This chopper type is discussed in Section 4.5.4). The phase shift between the chopper outputs is 120°, to obtain a three-phase supply. Fig.4-99 gives the inverter circuit, and the principle of operation of the controller will be explained with the aid of Fig.4-100.

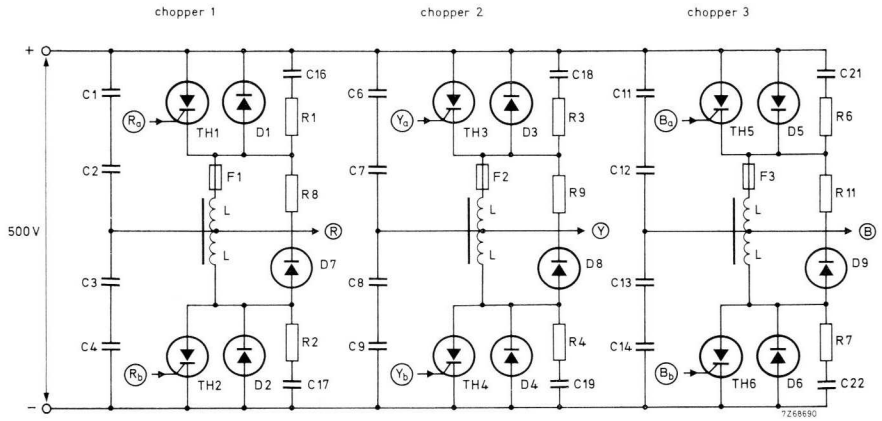


Fig.4-99 Three-phase inverter for a.c. motor controller consists of three choppers. R, Y and B are the stator terminals. C_1 to C_{14} = 10 μF, cat. no. 2222 327 50106; C_{16} to C_{22} = 47 nF, 1600 V d.c.; R_1 to R_7 = 8,2 Ω, 7 W; R_8 to R_{11} = 12 Ω, 300 W; L = 280 μH (see Fig.4-70); TH_1 to TH_6 = BTW30-1200RM; D_1 to D_6 = BYX25-1000; D_7 to D_9 = BYX25-1000R; F_1 to F_3 = 25 A fast fuse.

[16]) AI No. 468, ordering code 9399 264 46801 — A Variable - frequency Control System for A.C. Motors.

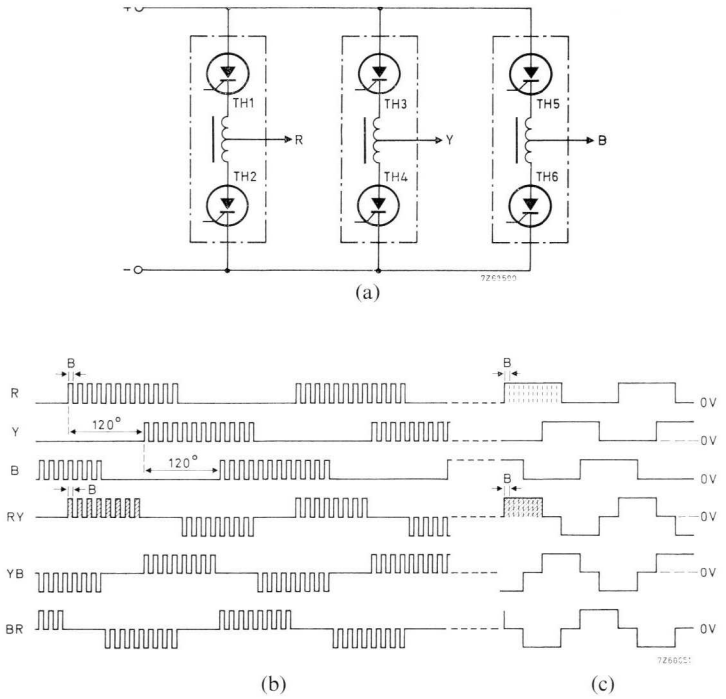


Fig.4-100 Simplified three-phase motor controller circuit (a) and multi-pulse output waveform: (b) for frequency $f_1/2$, (c) for frequency f_1; f_1 = motor supply frequency (about 50 Hz) at which the pulses merge.

A phase-phase voltage is produced whenever one chopper output is at the potential of the positive input terminal and the other at the potential of the negative input terminal; voltages of opposite polarity are, therefore, supplied to output RY when either TH_1 and TH_4 or TH_3 and TH_2 conduct (Fig.4-100*a*).

It was recognized that a square-wave chopper output would give rise to enormous peak stator currents at a low stator supply frequency and thus lead to unacceptable motor heating. The system has, therefore, been designed to

produce a multi-pulse output. Twelve chopper output pulses per half cycle proved a good compromise between the peak stator currents produced and thyristor switching losses (1,2 kHz switching frequency at a 50 Hz inverter output); see the chopper output waveform in Fig.4-100*b* marked *R*, *Y* and *B*. Because some chopper pulses "cancel", there are eight pulses per half cycle at the phase-phase outputs *RY*, *YB* and *BR*.

The output pulses have a constant width *B*. So the amount of volt-seconds per half cycle does not change with the stator supply frequency: compare the hatched areas in the *RY*-waveform of Fig.4-100*b* and *c*. If the stator supply voltage has been adjusted to the correct value, stator saturation at the low-frequency end cannot occur. At frequency f_1 the pulses merge (Fig.4-100*c*) and, at higher frequencies, the amount of volt-seconds per half cycle diminishes in inverse proportion to the frequency.

If the circuit is supplied from a rectifier, regeneration capabilities will be limited (ref. Section 4.5.1).

Drive circuit

There are twenty-eight circuit blocks contained in the controller, namely: 10 × UPA61, 7 × 2.NOR61, 4 × DOA61, 4 × 2.NOR60 and 3 × 2.IA60. Fig.4-101 is a simplified block diagram of the circuit, and Fig.4-102 gives the most important waveforms.

Motor speed depends on the level of speed control signal V_f, and the direction of speed is determined by the polarity of this signal. The signal V_f is passed through the INTEGRATOR, which smoothes out abrupt signal changes so that high currents due to motor start-up, speed change or reversal are avoided. For level sensing, the INTEGRATOR output is rectified and amplified by the RECTIFYING AMP and fed to the PULSE OSCILLATOR to control the frequency of output α. (A 120 Hz to 1200 Hz frequency range of α corresponds to a 5 Hz to 50 Hz frequency range of the stator supply voltage.) The output α is inverted and divided; it ultimately controls the Johnson counter to obtain the three-phase signals $\bar{U}$, $\bar{V}$ and $\bar{W}$ for thyristor control. Because of negative feedback between the RECTIFYING AMP and the PULSE OSCILLATOR, there is a linear relationship between control voltage V_f and motor speed. For the inverter output frequency to become 50 Hz, the value of V_f must be increased to about ± 8 V.

The phase sequence of thyristor control signals $\bar{U}$, $\bar{V}$ and $\bar{W}$, and thus the direction of motor rotation, is determined by the position of the LOGIC SWITCH. For one position: $\bar{U}' = \bar{U}$, $\bar{V}' = \bar{V}$, and for the other position: $\bar{U}' = \bar{V}$, $\bar{V}' = \bar{U}$. Depending on the polarity of signal V_f, the CW/CCW COMMAND CIRCUIT emits either a "*CW*" (clockwise rotation) or a "*CCW*" (counterclockwise rotation) signal to set the LOGIC SWITCH.

Because two thyristors are in series with the a.c. load, simultaneous triggering is necessary for turn-on. Therefore, a CENTRAL PULSE OSCILLATOR is used, feeding a 40 kHz trigger signal to each TRIGGER GATE.

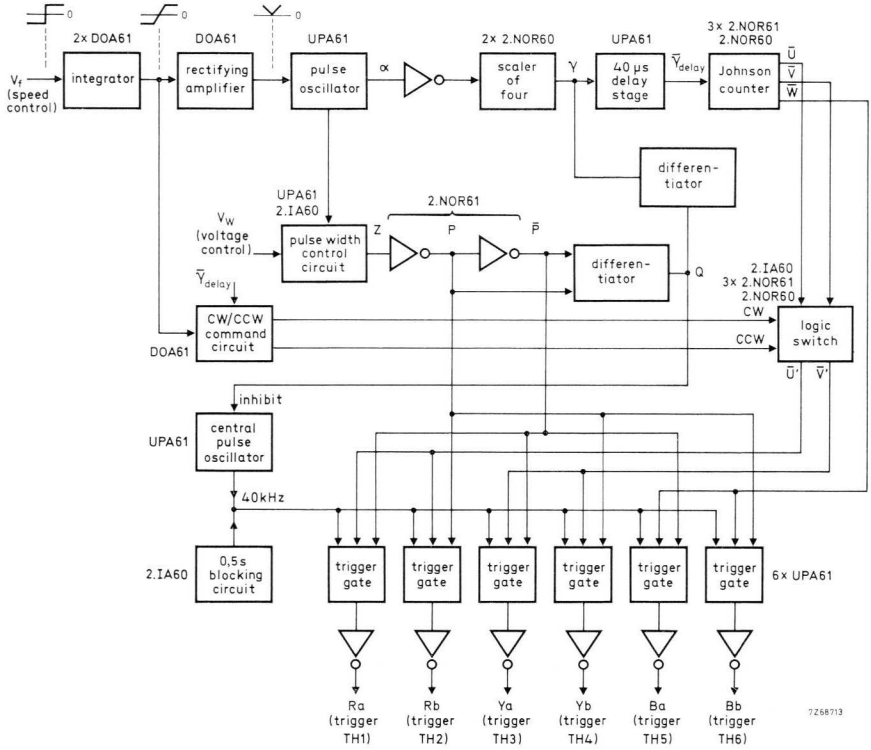


Fig.4-101 Drive circuit for three-phase motor controller. See the waveforms of Fig.4-102.

The inverter output voltage is pre-adjusted by changing V_W. Signals Z, P and $\bar{P}$ originate from the PULSE WIDTH CONTROL CIRCUIT, which is driven by the PULSE OSCILLATOR. The logic functions for the outputs of the two most left hand TRIGGER GATES are expressed as:

$$R_a = U' \cdot \bar{P} \cdot (40\ \text{kHz}) \qquad \text{(trigger } TH_1\text{)},$$
$$R_b = U' \cdot \bar{P} \cdot (40\ \text{kHz}) + \bar{U}' \cdot (40\ \text{kHz}) \qquad \text{(trigger } TH_2\text{)}.$$

Consulting these equations, it is seen that an increase of the width of P (by decreasing V_w from 0 V towards the minimum value of -8 V) increases the duty cycle of trigger signal R_a and, consequently, the conduction time of TH_1; the conduction time of TH_2 decreases correspondingly. As a result, the chopper output rises. The above is also clear when examining the R_a- and R_b-waveforms in Fig.4-102, which are valid for the conditions $\bar{U}' = \bar{U}$, $\bar{V}' = \bar{V}$.

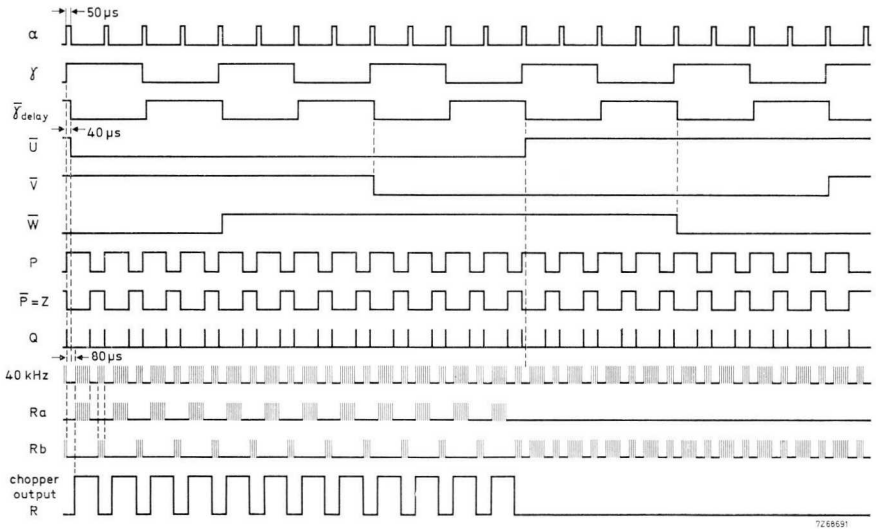


Fig.4-102 Pulse diagram of the drive circuit (Fig.4-101).

Signals P, $\bar{P}$ and γ are differentiated by the DIFFERENTIATOR stages. Whenever a pulse appears at DIFFERENTIATOR output Q, the CENTRAL PULSE GENERATOR is inhibited during an 80 μs interval: see the dead zones in the 40 kHz waveform. Owing to the action of the 40 μs DELAY STAGE, phase switching occurs in the centre of the dead zones (compare the $\bar{U}$- and 40 kHz waveforms). Because of these measures, the following results:

- Commutation of current between the chopper thyristors is ensured, as either thyristor will conduct over at least 80 μs or not conduct at all.
- Commutation of current between choppers (phase switching) is not jeopardized.

If commutation should fail, the inverter d.c. supply would be shorted. Fast fuses in series with the thyristors are recommended.

The 0,5 s BLOCKING CIRCUIT ensures that, after switch-on, trigger pulses cannot occur until the d.c. supply for the drive circuit has settled.

Provisions have been made so that the drive circuit remains in operation until the voltage across the buffer capacitors of the rectifier feeding the inverter has decreased to about 20% of its full value. As a result, the discharge current of these capacitors cannot reach a dangerous level when the upper thyristor in one of the inverter choppers is left conducting (because triggering ceases after switching off the mains).

4.7 D.C. Motor controllers

4.7.1 Discussion and circuit survey

D.C. motors have always been very popular for control purposes because their speed can be controlled simply by varying the armature current (rheostat in series with the armature) or by varying the excitation (change of field current).

BENEFIT 1 OF ELECTRONIC MOTOR CONTROL: Even field control is "lossy". Thyristors and triacs used in electronic motor control have negligible losses, thus ensuring high efficiency.

Distinction is made between the following motor types:

- series-wound motor (field windings in series with armature)
- shunt-wound motor (field windings in parallel with armature)
- compound-wound motor (field windings in series and in parallel with armature)
- separately excited motor (field windings isolated from armature)
- permanent-magnet motor (field windings replaced by permanent magnet).

Fig.4-103 illustrates load characteristics of various motor types (armature current I_a representative of load). The speed of the series motor is very load-dependent (curve *a*). That of the shunt motor still has load-dependency (curve *b*) because of armature voltage drop. Speed stabilization is improved by compounding (curve *c*). The performance of the separately excited and the permanent-magnet motor is similar to that of the shunt motor. Series motors have a high starting torque and a wide speed range; they are, therefore, ideal for traction. Series motors with laminated poles are usable with a.c.; these "universal" machines are widely used in hobby and household equipment.

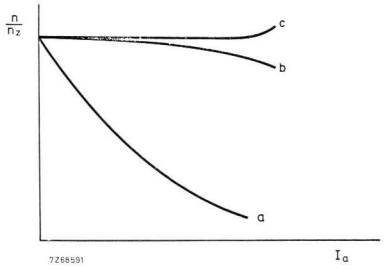


Fig.4-103 Load characteristics of (a) series motor, (b) shunt motor, (c) compound motor. n_z = speed at zero load, I_a = armature current.

BENEFIT 2 OF ELECTRONIC MOTOR CONTROL: The compound motor is expensive. With electronic control, any motor characteristic can be simulated, so the least expensive machine will be resorted to.

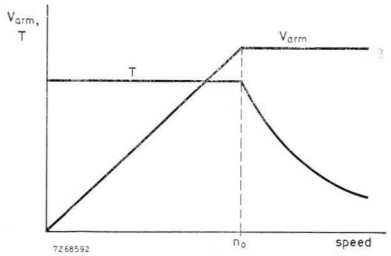


Fig.4-104 Shunt motor characteristics (field weakening for r.p.m. exceeding nominal value n_o); T = torque, V_{arm} = armature voltage.

According to Fig.4-104 (valid for a constant armature current), motor speed can be controlled by varying the armature voltage for its r.p.m. below nominal value and by varying the field strength for its r.p.m. above nominal value.

BENEFIT 3 OF ELECTRONIC MOTOR CONTROL: With rheostat control, motor characteristics change appreciably; for instance, the speed of a shunt motor becomes very load-dependent when inserting resistance in the armature circuit. With electronic speed control, constant speed is obtainable at any speed setting.

The Ward-Leonard system features a perfected mode of motor control, in which speed is controlled by varying the armature voltage, the excitation being normally held constant. It is a regenerative system providing control of speed between maximum forward and reverse limits as well as controlled motor deceleration and reversing. This system may have a combustion engine or electric motor as the prime mover. Specific examples are generators for diesel-electric locomotives, elevator controls, rolling mills, etc.

BENEFIT 4 OF ELECTRONIC MOTOR CONTROL: The efficiency of the Ward-Leonard drive is limited because of power conversion through three machines. In the electronic equivalent (four-quadrant control circuits — see Sections 4.7.4 and 4.7.5), system efficiency is mainly determined by the efficiency of the controlled motor. Further features of the electronic variant are lower cost and higher flexibility: constant-speed, constant-torque or constant-power control may be obtained.

ELECTRONIC MOTOR CONTROL is achieved by varying the armature voltage. The following basic power control methods, discussed previously, are listed:

d.c. power source: chopper (Section 4.5)
a.c. power source: (1) controlled rectifier (Section 4.4.2)
(2) diode rectifier + chopper (Section 4.5.1).

The three-phase bridge is preferable for power control, because it can handle high powers, contains a low output ripple and has a favourable power factor. Distinction must be made between the half-controlled and full-controlled type. Fig.4-105 and Fig.4-106 show the circuits and the conduction diagrams, as well as the output waveforms; full treatment of these circuits is given in a previous publication[17]). *The full-controlled bridge* incorporates six thyristors, hence, is more expensive but it offers the following advantages:

- At a supply frequency of 50 Hz it has a fundamental ripple frequency of 300 Hz as compared with 150 Hz when using the half-controlled type (compare output waveforms in Figs.4-105*c* and 4-106*c*). Consequently, output ripple content is reduced and less motor heating occurs.
- Every 60° a thyristor is triggered (every 120° in the half-controlled circuit) as seen in the conduction diagram; this allows the fast response required for some servo systems.
- It is capable of regeneration, that is, it provides braking by returning power to the a.c. source; this ensures motor control under all operating conditions, increases system efficiency and solves the problem of dissipation due to waste of power.

Because of the last property, the full-controlled type is often called a regenerative bridge, whereas the half-controlled type is said to be non-regenerative.

Output curves of the half-controlled and full-controlled bridge are plotted in Fig.4-107.

[17]) Product Book, ordering code 9399 256 00701 – Thyristors.

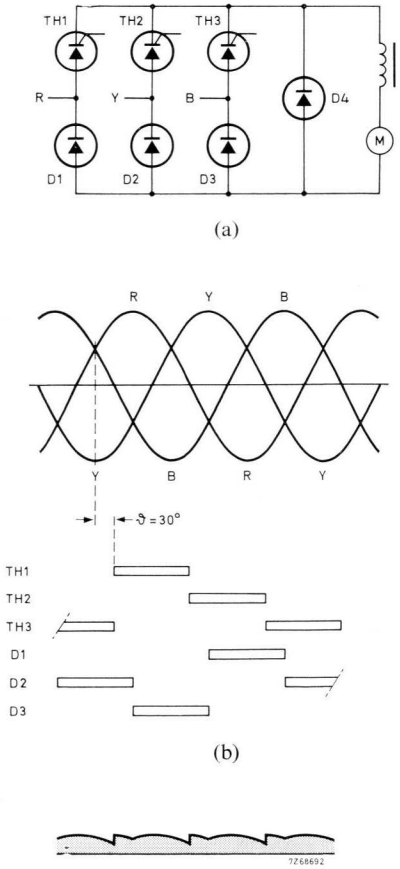


Fig.4-105
(a) half-controlled three-phase bridge,
(b) conduction diagram for trigger angle $\vartheta = 30°$,
(c) output waveforms.
Trigger angle range is 180°.

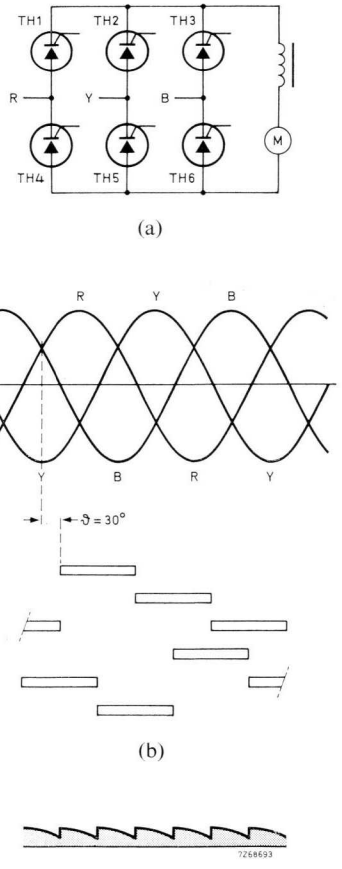


Fig.4-106
(a) full-controlled three-phase bridge,
(b) conduction diagram for trigger angle $\vartheta = 30°$,
(c) output waveform.
Trigger angle range is 180°.

The *half-controlled bridge* of Fig.4-105 needs a free-wheeling diode, D_4, to maintain control and smooth the armature current (Section 4.4.2). This bridge is *not* intended for regeneration. With the motor driven in reverse by its load (reversed armature e.m.f.), D_4 would conduct continuously; the rise in armature current would be unlimited resulting in damage to the diode and the motor.

As seen from Fig.4-107, curve *d*, the *full-controlled bridge* can deliver a negative voltage for trigger angles exceeding $\pi/2$ radians; it is, therefore, able to pass power from the load to the a.c. source, as will be seen from the following. It should be kept in mind that load current can only flow unidirectionally.

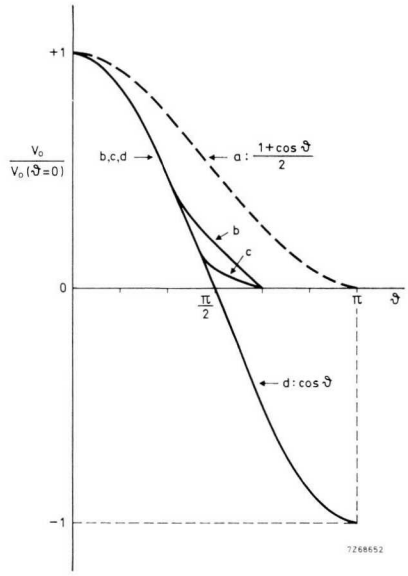


Fig.4-107 Output curves for three-phase bridge: (a) half-controlled type, (b) full-controlled type & resistive load, (c) full-controlled type & mixed resistive/inductive load, (d) full-controlled type & purely inductive or active load. ϑ = trigger angle.

Fig.4-108 then shows the three possible states. For the motoring condition (Fig.4-108*a*), power flows from the a.c. input to the motor; the circuit produces a positive output voltage, because the trigger angle is always less than $\pi/2$ radians. For the regenerating condition (Fig.4-108*b*), power flows from the output to the a.c. input. Because the polarity of the motor e.m.f. is reversed, the trigger angle must exceed $\pi/2$ radians (negative rectifier output). The motor current is then restricted by the opposing rectifier voltage. If the bridge output were held positive, motor e.m.f. and rectifier output voltage would aid in building up a very large current, as suggested by the heavy arrow in Fig.4-108*c*. Power would be delivered both by the a.c. source and the motor, and abrupt speed reversal would result. This condition is identical to that of "plugging", which is a primitive method of reversing motor rotation by interchanging the motor connections.

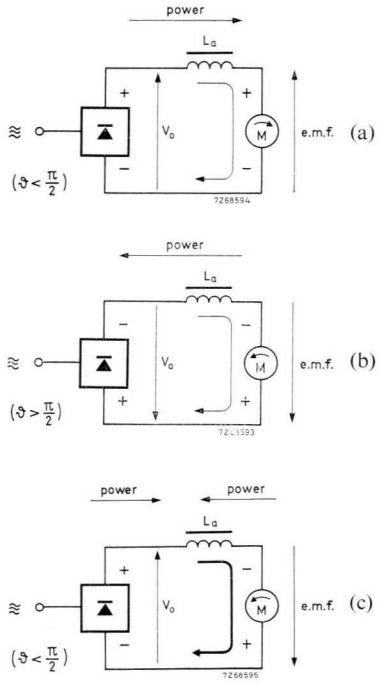


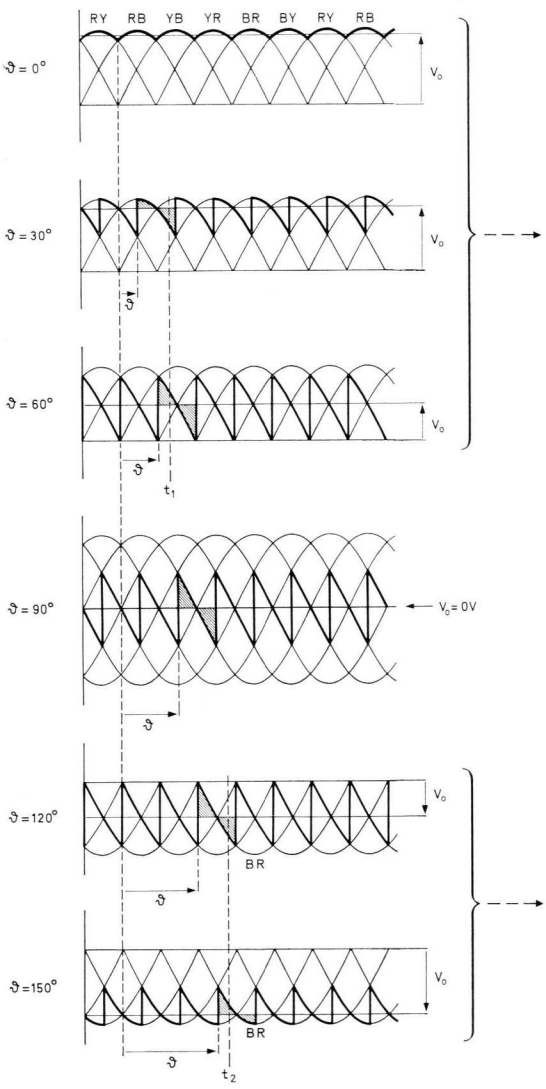
Fig.4-108 Illustrating the three possible states of a full-controlled bridge: (a) motoring, $V_o >$ e.m.f., (b) regenerating, e.m.f. $> V_o$, (c) „plugging". Upper arrows indicate direction of power flow.

Two-quadrant control is possible when using a full-controlled bridge or a regenerative chopper, as will be clear from the following examples. The first quadrant conforms to the condition of motoring and the second quadrant to that of regenerative braking. (Non-regenerative circuits – a.c. or d.c. – exert only one-quadrant control; that is, braking must be achieved by dissipative means, such as friction pads, a braking resistor across the armature or eddy-current brakes).

The full-controlled bridge is suitable for controlling hoists and similar gear requiring braking at a *reversed* speed. Fig.4-109 illustrates the situation; the waveforms show the phase-phase voltages, where "RY" indicates that the instantaneous voltage of phase R is larger than that of phase Y, etc.

When the trigger angle ϑ is smaller than $\pi/2$ radians, power is delivered to the motor for hoisting, the direction of the load current being determined by the rectifier output voltage: see the upper right-hand diagram (valid for t_1). The output power decreases as triggering is delayed until, for ϑ exceeding $\pi/2$ radians, regeneration occurs. Under this condition, the mechanical load drives the motor in the opposite direction causing it to function as a d.c. generator (reversed armature e.m.f.). As seen from the lower right-hand diagram (valid for t_2), the direction of the motor current is dictated by the armature e.m.f. The current flows against the voltage between phases R and B, and power is delivered back to the a.c. supply. Because the d.c. voltage drop across the armature inductance is ideally zero, the steady-state load current at a given trigger angle is determined by the condition that the hatched area in each of the waveforms must be zero. Fig.4-110 is a two-quadrant representation of this type of control.

Motor control which requires both motoring and braking with the motor rotating in the *same* direction is achieved when using a regenerative chopper. A regenerative chopper allows the load current to flow in both directions (Section 4.5.1). An obvious application is in battery-powered vehicles. During motoring, the chopper delivers a controlled amount of power to the motor; during braking, the motor acts as a dynamo returning power to the battery via the chopper (reversed load current). The two-quadrant representation of this type of control is shown in Fig.4-111. A motor reversing switch is necessary to reverse the vehicle.


RY RB YB YR BR BY RY RB
ϑ = 0°
V₀
ϑ = 30°
V₀
ϑ
ϑ = 60°
V₀
ϑ
t₁
ϑ = 90°
V₀ = 0V
ϑ
ϑ = 120°
V₀
BR
ϑ
ϑ = 150°
V₀
BR
ϑ
t₂

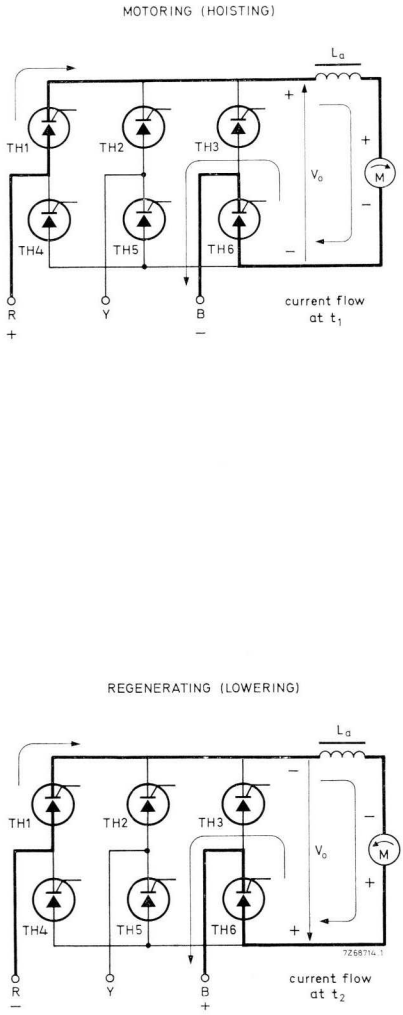


Fig.4-109 Waveforms and circuit conditions for hoisting and lowering. Heavy line is rectifier output waveform. V_o = average rectifier output voltage (approximately equal to armature e.m.f.).

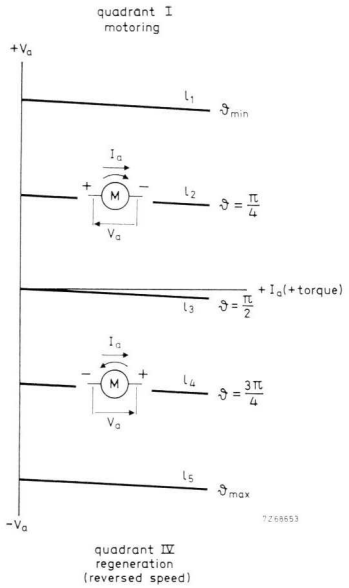


Fig.4-110 Two-quadrant representation of hoisting control. l_1 to l_5 = rectifier output vs. load current.

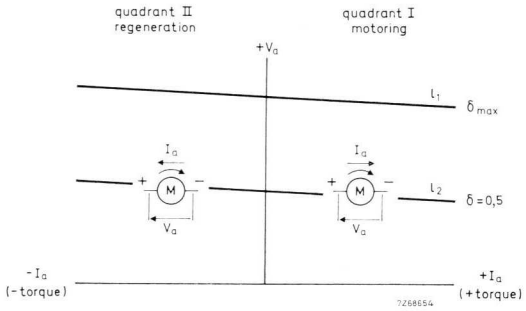


Fig.4-111 Two-quadrant representation of vehicle control. δ = duty cycle of chopper, l_1 l_2 = chopper output vs. load current.

Four-quadrant control can be obtained by arranging two regenerative bridges in anti-parallel as depicted in Fig.4-112; the four quadrants are shown in Fig.113 (compare with Figs.4-110 and 4-111). Motoring occurs in quadrants I and III, and regeneration is obtained in quadrants II and IV. Bridge 1 operates

in quadrants I and IV and bridge 2 in quadrants II and III; the current flow of each of the bridges is shown in Fig.4-112. Four-quadrant operation allows motor control over the full range from maximum forward speed to maximum reverse speed. Moreover, regenerative braking results in rapid deceleration so that motor rotation can be rapidly reversed.

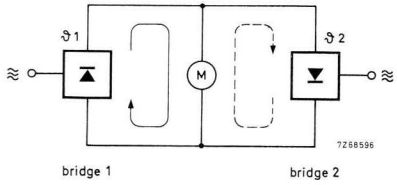


Fig.4-112
Anti-parallel connected regenerative bridge pair yielding four-quadrant control.

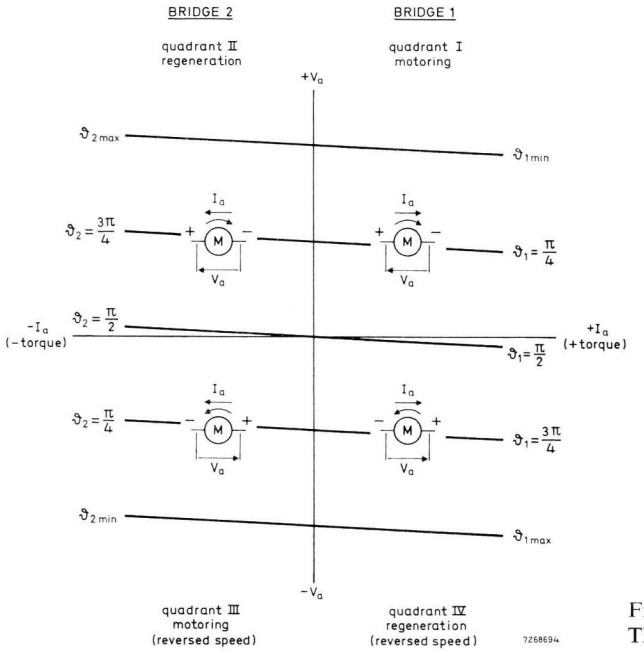


Fig.4-113
The four control quadrants.

The following system variants yield four-quadrant control:

- Anti-parallel thyristor twin bridge (Fig.4-114); this system was discussed previously.
- Thyristor bridge and reversing contactor (Fig.4-115); the contactor will have a long life when switching only takes place at zero load current.
- Thyristor bridge and solid-state reversing switch (Fig.4-116); the current distributed over the three thyristors in the three-phase bridge must be carried by each of the thyristors in the reversing switch.
- Motor field reversal.
- Bridge arrangement of regenerative choppers (Fig.4-117); by varying the chopper output duty cycle, the magnitude of V_{o1} and V_{o2} can be adapted so that both the value and polarity of motor voltage is controlled.

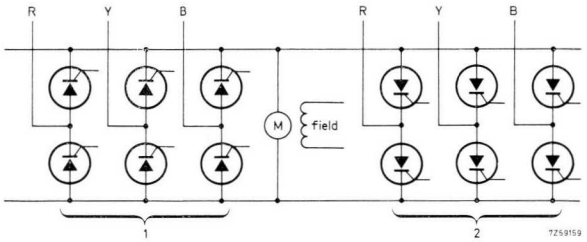


Fig.4-114 Four-quadrant control circuit using thyristor bridges in anti-parallel (compare with Fig.4-112).

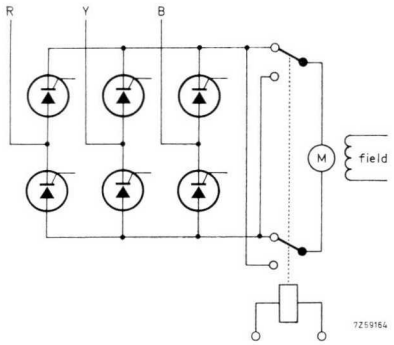


Fig.4-115 Four-quadrant control circuit using reversal of armature connections.

The systems shown in Figs.4-114 and 4-117 are the most economic and provide the greatest control flexibility. They are discussed in Sections 4.7.4 and 4.7.5.

Four-quadrant motor control is valuable in rolling mills, lifts and hoists, and in production processes requiring an accurately controlled flow of raw materials, etc.

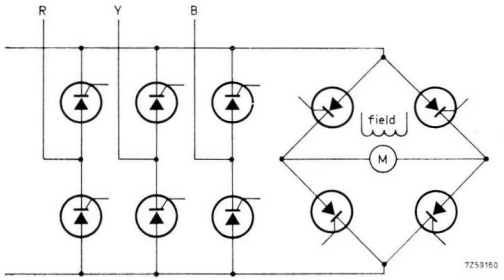


Fig.4-116 Four-quadrant control circuit using reversing thyristor-switch.

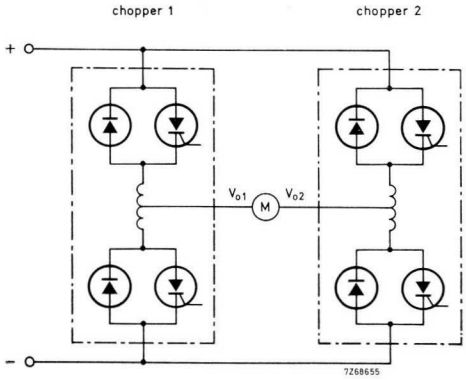


Fig.4-117 Four-quadrant control circuit using bridge arrangement of regenerative choppers.

Commutation (or end-stop) pulses are necessary to prevent a disastrous motor current during regeneration if the normal trigger pulses fail. The commutation pulses ensure current transfer from thyristor to thyristor, so that the regenerative motor current always flows against an opposing mains voltage. They must be located 20° to 30° before the latest possible point (180°) of thyristor triggering; this margin of a few tens of degrees caters for the commutation interval and for the shift in the mains zero cross-over points due to interference and asymmetrical loading. Alternatively, the trigger circuit can be so designed that thyristor triggering is delayed to about 150° in the event of interruption of the control voltage.

The various circuits discussed in this Chapter are listed in Table 4-10.

Table 4-10. D.C. motor controllers.

circuit	one-quadrant control	two-quadrant control	four-quadrant control
chopper	section 4.5.3	section 4.5.4	section 4.7.5
controlled rectifier bridge	sections 4.7.2 and 4.7.3	—	section 4.7.4

Modular heatsinks accommodating thyristors for motor control are discussed at the end of this book in an appendix.

4.7.2 Wire planishing attachment[18])

The planisher described here can treat wire of between 0,2 mm and 1 mm diameter. With the wire shaped to a profile 0,75 × 1,05 times its diameter, about 15% saving in winding space is gained; in addition, heat dissipation to ambient is improved because of greater copper density.

[18]) AN No. 124, ordering code 9399 260 62401 – Thyristor Controlled Wire Planishing Attachment.

Set-up (Fig.4-118). To maintain the wire tension, the motor driving the rollers for wire planishing should accurately keep pace with winding speed. Discrepancy between wire throughput and wire supply demanded by the winder is sensed by the angular displacement transducer. The transducer output v_ψ together with motor-speed proportional signal v_m is fed to the DOA61 error amplifier. If motor speed is low, v_ψ increases, v_{contr} passes the 2,5 V threshold and drive power is fed to the motor via TH_1. Input disturbances, for instance jerky reel rotation, are rapidly damped out by this control loop (proportional and integrating control). If motor speed is high, v_ψ decreases, v_{contr} drops below 0,6 V and TH_2 is switched into conduction for motor braking (on/off control). Integrating transducer action cancels offset errors. The 0,6 V to 2,5 V dead zone eliminates the influence of motor commutator ripple on the control.

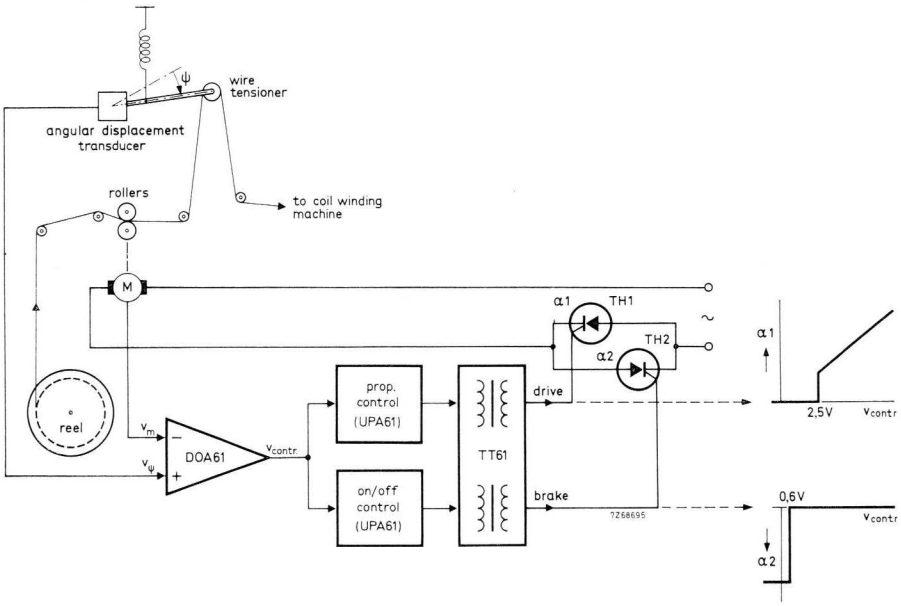


Fig.4-118 Functional sketch of wire planishing attachment; α_1 α_2 are the conduction angles of TH_1 TH_2.

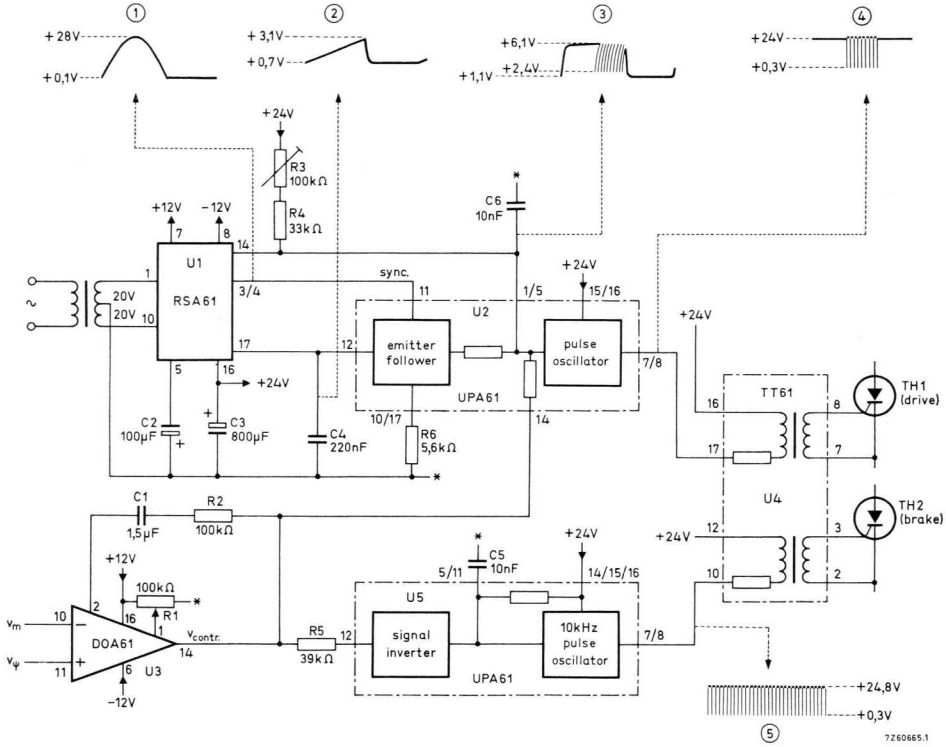
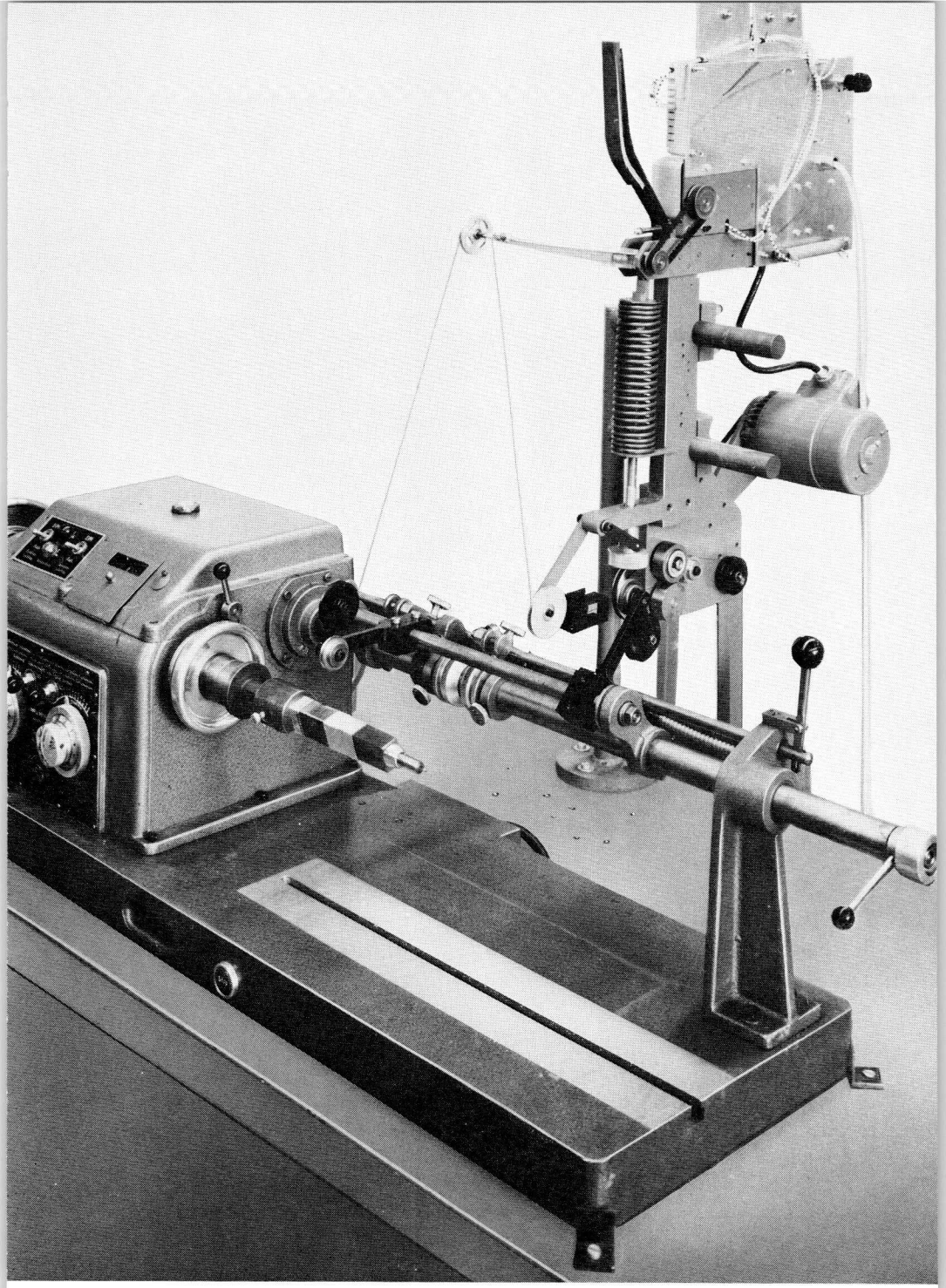


Fig.4-119 Controller circuit diagram and waveforms. * = common point (see also Fig.4-120).

Controller (Fig.4-119). The upper UPA61 is a 10 kHz pulse generator controlling drive thyristor TH_1 in synchronism with the half-wave signal (waveform *1*) delivered by the RSA61. As explained in Section 1.2.1, the trigger angle of TH_1 is determined by the control voltage v_{contr} applied to the pulse generator input; the magnitude and polarity of v_{contr} depend on the difference of v_m and v_ψ at the DOA61 input. For v_{contr} increasing, TH_1 is triggered earlier each alternate half cycle, which results in continuous control. On/off control is achieved as follows. For v_{contr} above 0,6 V, the signal inverter in U_5 is in saturation, C_5 cannot charge and the 10 kHz pulse generator is inhibited. When v_{contr} drops below 0,6 V, the signal inverter comes out of saturation, and C_5 charges so that the trip-on level of the 10 kHz pulse generator is reached; 10 kHz pulses are generated triggering TH_2 for braking action.



Thyristor-controlled wire planisher fitted on coil winder.

730726-04-02

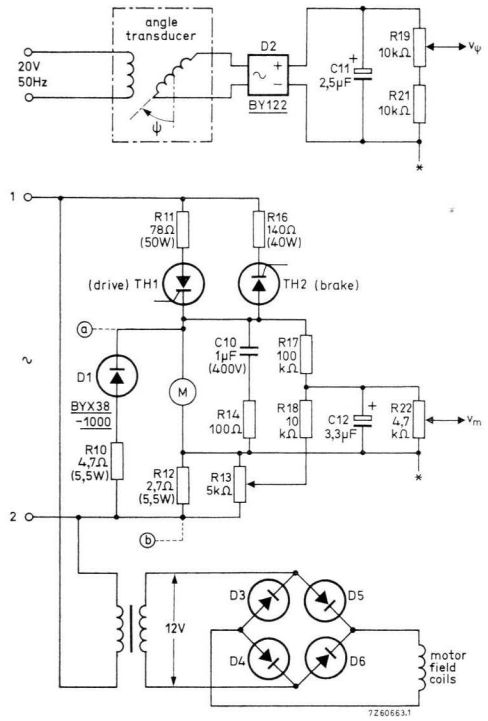


Fig.4-120 Motor and transducer circuit diagram. TH_1 TH_2 = BTY79-800R, D_3 to D_5 = BY126. * = common point (ref. Fig.4-119).

Power circuit (Fig.4-120). A 70 W motor is used for wire planishing. Thyristor TH_1 is the drive thyristor and TH_2 is the brake thyristor, braking being achieved by "plugging". IR compensation (setting of R_{13}) ensures true speed measurement. If R_{13} is assumed to be mid-position, R_{12} follows from:

$$R_{12} = 0{,}2\ R_a,$$

where R_a is the armature resistance.

Free-wheeling diode D_1 increases the torque at low speed, smoothes the armature current and prevents it (and thus the motor) from reversing. The rectified transducer output existing across C_{11} varies almost linearly between 0 V and 6,5 V with angular displacements between 0 ° and 70 °.

Fig.4-121 is the controller wiring diagram (circuit blocks shown as seen from type-number side). For good control performance, mains terminations 1 and 2 should conform to those of the motor control, circuit Fig.4-120. The dots indicate the prescribed phase relationship of the transformer voltages.

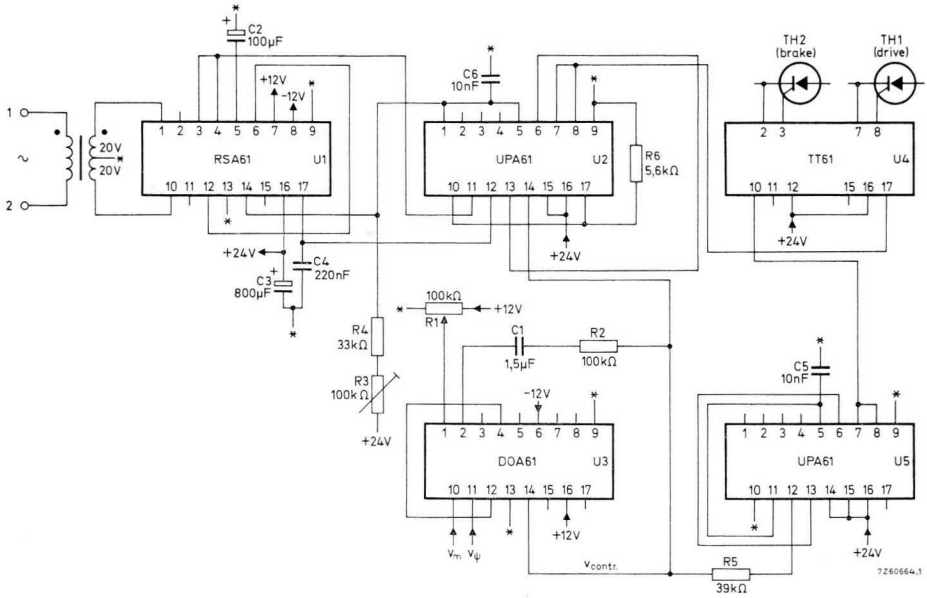


Fig.4-121 Controller wiring diagram. * = common point (ref. Fig.4-119).

Adjustment (Figs.4-120 and 4-121):

1. *With the motor stalled, adjust IR-compensation potentiometer R_{13} (Fig.4-120) so that the voltage drop across R_{22} is zero.*
2. *Set trimmer R_3 (Fig.4-121) to maximum.*
3. *With the circuit operating and the wire tensioner arm in its highest position (zero transducer output) reduce the output at terminal 14 of U_3 (Fig.4-121) by adjustment of bias compensation trimmer R_1. Check that trigger pulses start to appear at output terminal 8 of U_5 as soon as the output of U_3 drops below about 0,6 V.*
4. *With R_1 adjust the output of U_3 so that it lies within the dead zone at 2 V.*
5. *Lower the tensioner arm so that the output of U_3 rises to 2,5 V and adjust R_3 (Fig.4-121) until trigger pulses just appear at output terminal 8 of U_2.*
6. *Set potentiometers R_{19} and R_{22} (Fig.4-120) to maximum. With the wire tensioner arm in its lowest position (maximum transducer output) adjust trimmer R_{22} so that the motor runs at desired maximum speed. Rolling speed at any arm position is set with R_{19}. Lower the setting of R_{22} if maximum rolling speed is too low.*

4.7.3 SINGLE-PHASE D.C. MOTOR CONTROLLERS

The d.c. motor controllers described here are simple yet exhibit good performance. At rated r.p.m., the maximum variation of motor speed is 1% between zero and full load; 10% mains voltage variation affects speed by only about 1%.

Before these circuits are treated in detail – see the survey given in Table 4-11 – a few remarks will be useful.

Table 4-11. Single-phase d.c. motor controllers.

	advance current limiting	speed control by	torque control by	A.C. mains/control circuit isolation
version 1	yes	tachogenerator	—	yes
version 2	yes	armature e.m.f. sensing	armature current sensing via shunt	no
version 3	yes	tachogenerator	armature current sensing via DCT61*	yes

* Section 4.9.2.

All circuits have Advance Current Limiting (ACL). That is, the maximum conduction angle of the thyristors passing power to the load is adjusted in advance so that, with the motor stalled, the armature current can never reach a dangerous level. Though ACL is adjustable, it is *not* suitable for torque control because the current limit may change with speed by 40%. Armature current measuring must be used instead to ensure sufficient control accuracy. ACL is necessary, however, to prevent dangerous current surges such as those occurring when a stationary motor would be connected to the maximum rectified voltage.

Monitoring the armature e.m.f. is one method of speed control. This requires IR compensation to eliminate the effect of the current-dependent armature

voltage drop. However, owing to the temperature dependency of armature resistance, IR compensation can only be obtained at one specific temperature of the armature windings. Moreover, the armature e.m.f. varies with the motor field causing, for instance, higher r.p.m. at weaker excitation. These imperfections are eliminated by using a tachogenerator for r.p.m. measurement.

Because free-wheeling diodes are used in the power circuit, a total armature inductance of 30 mH sufficiently smoothes the armature current to prevent motor overheating.

The circuits are stabilized against fluctuations of mains voltage and temperature.

Version 1[19])

The power circuits of Figs.4-122 and 4-123 include safeguards against thyristor triggering by mains transients. Bridge D_1 to D_4 supplies the field windings, and free-wheeling diodes D_5 D_6 in conjunction with the inductance in the armature circuit smooth the armature current. A tachogenerator is shown connected to the motor shaft for r.p.m. control. Circuit specification is according to Table 4-12.

The trigger section of Fig.4-124 contains an RSA61 (U_1) d.c. supply and synchronization unit, an UPA61 (U_2) pulse generator controlling the thyristors, and an UPA61 (U_3) inhibiting unit. Circuit operation is clear from the waveforms. Unit U_2 causes the thyristor conduction angle to increase linearly with v_{contr} (linear phase control); its operation is described in Section 1.2.1. NTC thermistor R_{18} cancels effects of temperature on motor control and on maximum current level controlled by ACL. Capacitors C_{13} and C_{14} are supplied from +24 V (unstabilized) as well as +12 V (stabilized), to provide compensation against mains voltage variations. Unit U_3 inhibits triggering as long as, after switch-on, the d.c. supply voltages have not yet settled. During the first few seconds of equipment operation, the charge across C_{16} is too low for the Schmitt trigger circuit to trip on; as a result, the output of the inverting stage is held at zero volts, and no trigger pulses can be passed to the output stage.

[19]) AI No. 463, ordering code 9399 264 46301 – Single-phase D.C. Motor Control Circuit.

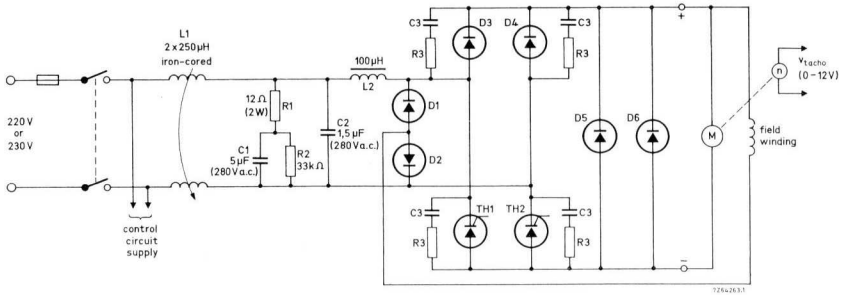


Fig.4-122 D.C. motor power circuit (version 1) using BTY79 or BTY87. D_1 D_2 = BYX45-1000(R) for field currents to 2 A and BYX39-1000(R) for field currents up to 4 A. For further particulars see Table 4-12.

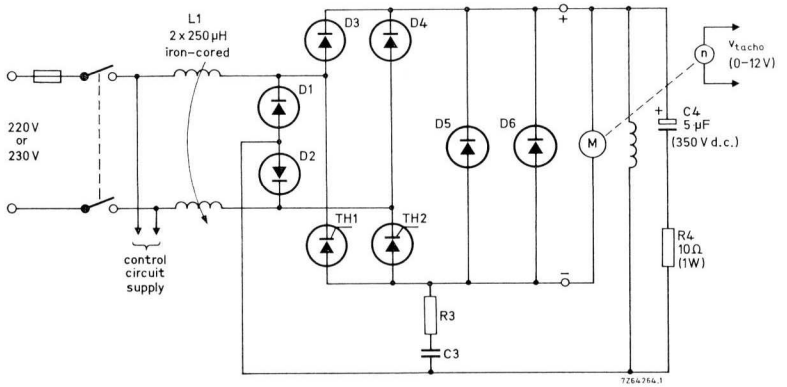


Fig.4-123 D.C. motor power circuit (version 1) using BTW 38, BTW47, BTW92 or BTW24. D_1 D_2 = BYX45-1000(R) for field currents to 2 A and BYX39-1000(R) for field currents to 4 A. For further particulars see Table 4-12.

Table 4-12. Specification to Figs.4-122 and 4-123. Output ratings apply to circuit version 1, and are valid for 220 V ± 10% a.c. input and the diode and thyristor mounting-base temperature not exceeding 125 °C and 85 °C, respectively.

fig.	TH_1, TH_2	D_3 to D_6	R_3	C_3	rated d.c. output current at 220 V a.c.	rated d.c. output power at 220 V a.c.
4-122	BTY79-700R	BYX39-800	33 Ω, 1 W	0,1 μF, 1000 V d.c.	7 A	1,4 kW
4-122	BTY87-700R	BYX40-800	33 Ω, 1 W	0,1 μF, 1000 V d.c.	11 A	2,2 kW
4-123	BTW38-800RM	BYX40-800	82 Ω, 2 W	0,47 μF, 1000 V d.c.	10 A	1,9 kW
4-123	BTW47-800RM	BYX25-800	82 Ω, 2 W	0,47 μF, 1000 V d.c.	15 A	3,0 kW
4-123	BTW92-800RM	BYX25-800	68 Ω, 2 W	0,47 μF, 1000 V d.c.	21 A	4,3 kW
4-123	BTW24-800RM	BYX56-800	56 Ω, 2 W	0,47 μF, 1000 V d.c.	38 A	7,6 kW

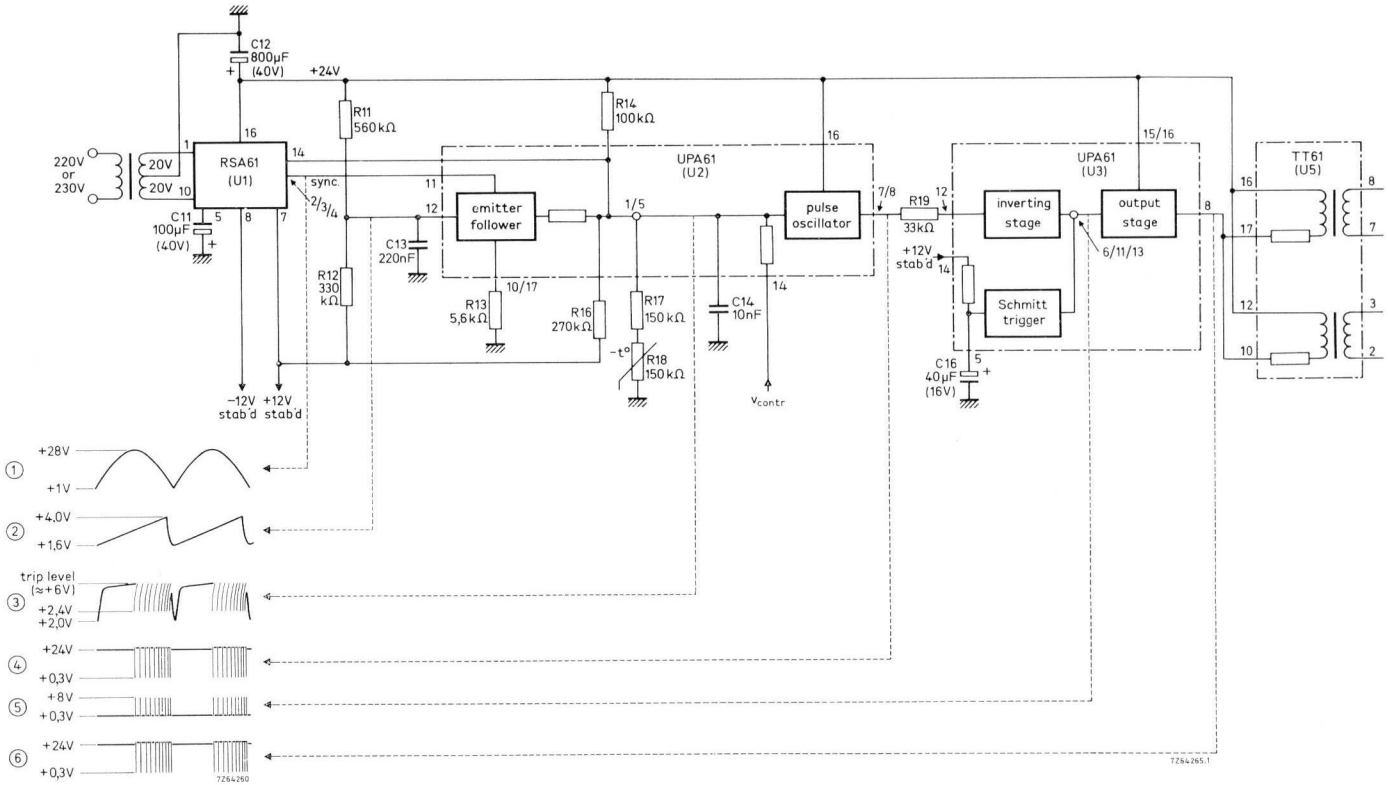


Fig.4-124 Trigger section of d.c. motor control circuit. Points shown earthed are not isolated from the mains supply in circuit version 2; v_{contr} comes from the control section, Fig.4-125, 4-127 or 4-129.

In the control section, Fig.4-125, the DOA61 error amplifier is the central control element. Equilibrium will exist if v_{tacho} and v_{ref} produce equal inputs. Suppose motor speed tends to increase. Signal v_{tacho} increases causing the DOA61 output v_{contr} to decrease. The thyristors are triggered later each half cycle, thus counteracting the speed increase. The DOA61 input and feedback networks contain integrating and differentiating elements to obtain good dynamic response. Owing to the presence of clamping diode D_{21}, the maximum value of v_{contr} and, consequently, the maximum thyristor conduction angle is determined by the ACL adjustment potentiometers R_{21} and R_{22}. The clamping level of v_{contr} increases with v_{tacho} (R_{22}-adjustment) to compensate for the armature e.m.f. which opposes the armature current.

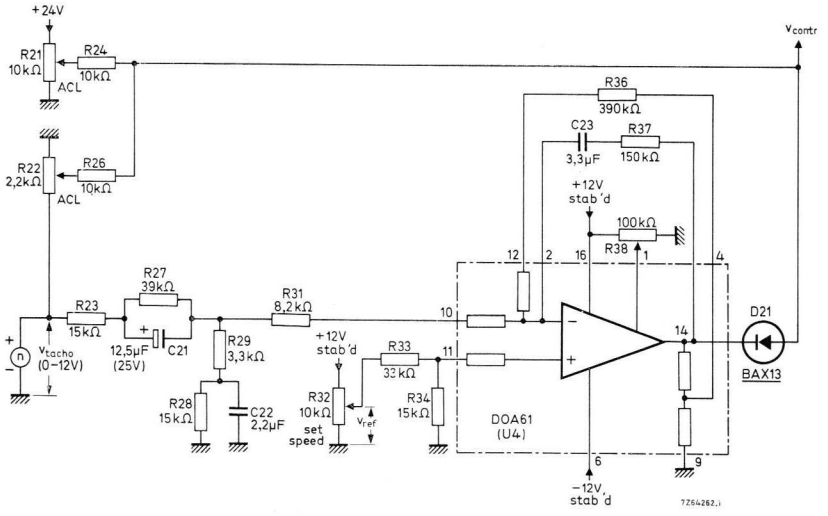


Fig.4-125 Control section of d.c. motor control circuit (version 1); v_{contr} is connected to the trigger section Fig.4-124.

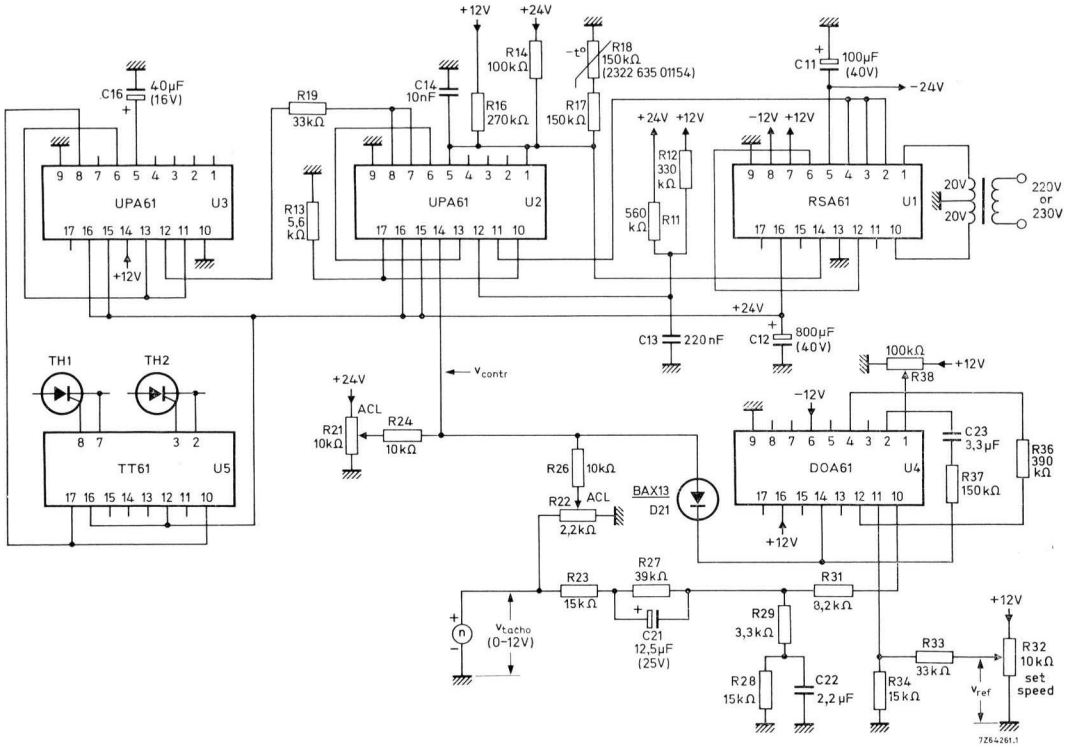


Fig.4-126 Wiring diagram of d.c. motor control circuit (version 1). Power section accords with Fig.4-122 or 4-123.

Adjustment (Fig.4-126):

1. *Set R_{21}, R_{22} and R_{32} to zero position (wipers at earth potential). Because the armature does not carry current, it will not rotate and the tachogenerator produces zero output. Adjust R_{38} to obtain zero output at pin 14 of U_4.*
2. *Set R_{32} to its maximum position so that the output of U_4 is inhibited (D_{21} reverse-biased). Raise the setting of R_{21} so that, with the motor stalled, nominal armature current flows.*
3. *Check the polarity of the tachogenerator signal; if the motor does not run at a low speed with R_{32} set close to zero position, the tachogenerator connections should be reversed.*
4. *Raise the setting of R_{22} so that, with the fully-loaded motor running at nominal speed, nominal armature current flows.*
5. *Re-adjust R_{21} so that, with the motor accelerating to nominal speed, the armature current does not drop below nominal level.*
6. *If necessary, change the value of C_{21} so that the dynamic response shows minimum overshoot or undershoot; it may also be necessary to change the values of C_{23} and R_{37}.*

Version 2

Fig.4-127 illustrates the control section and the armature circuit. The trigger section is shown in Fig.4-124. Because of fairly accurate armature current control (sensing via shunt), the maximum current is fixed between narrow limits. The maximum output allowed is, therefore, higher than that permitted for the previous circuit (compare Tables 4-13 and 4-12).

Assuming R_{44} in Fig.4-127 to be in mid-position for obtaining IR compensation, R_{41} is given by:

$$R_{41} = 0{,}35\ R_a,$$

where R_a is the armature resistance.

Resistor R_{42}, R_{43} in parallel with C_{41}, the portion of R_{44} between wiper and upper terminal, and the armature resistance R_a in series with armature inductance L_a together form a Maxwell bridge, which is balanced by correct choice of C_{41} so that bridge output due to commutator ripple is zero. No commutator ripple will appear at the wiper of R_{48} when C_{41} satisfies:

$$C_{41} = L_a/(R_a\ R_{43}).$$

Substituting $R_{43} = 4700\ \Omega$, $R_a = 2\ \Omega$ and $L_a = 0{,}03$ H, C_{41} becomes 3 μF.

The circuit allows torque control (armature current limiting) or speed control. See Fig.4-127. If torque control is desired, speed potentiometer R_{56} is set to its highest position, and the desired torque is adjusted by maximum current setting potentiometer R_{58}. For a moderate motor speed, the input at pin 10 of U_4 is lower than that at pin 11, and the output of U_4 is high. With D_{42} reverse-biased, v_{contr} is determined by U_6, provided that the armature current does not reach the level set with ACL potentiometers R_{47} and R_{48}. Torque control occurs as a result. If, at a light load, motor speed becomes excessive, the output of U_4 will predominate because it becomes lower than that of U_6 (D_{41} reverse-biased). Consequently, the control circuit proceeds to speed control.

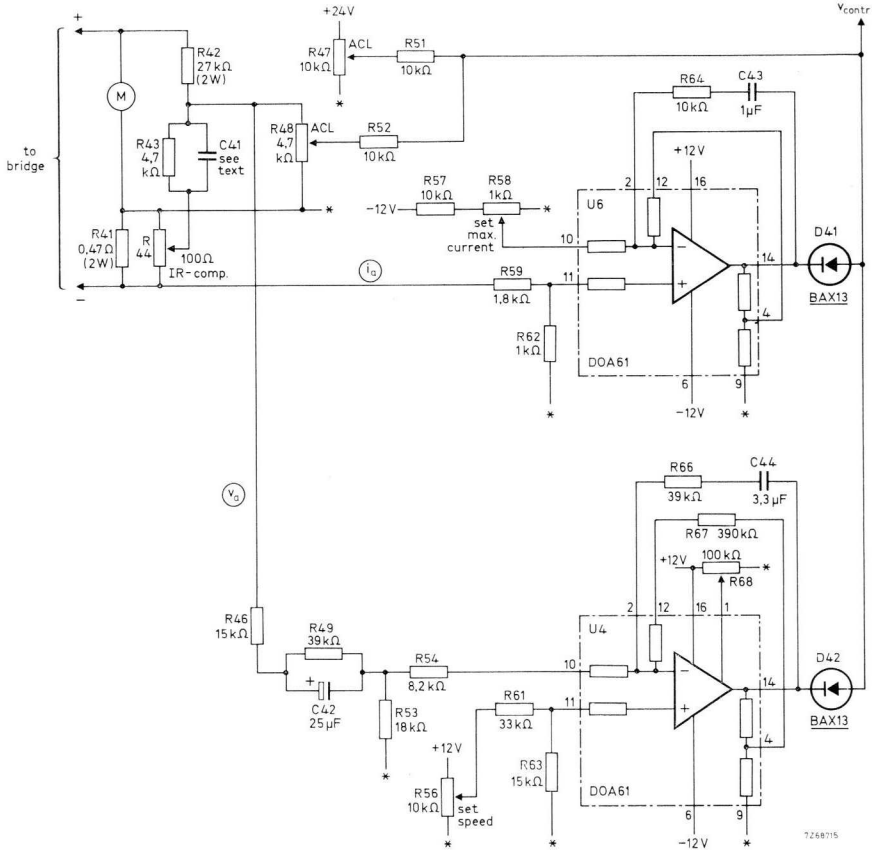


Fig.4-127 Armature connection and control section of d.c. motor control circuit (version 2); v_{contr} is connected to the trigger section, Fig.4-124. * = common point (not isolated from mains); bridge circuit according to Fig.4-122 or 4-123.

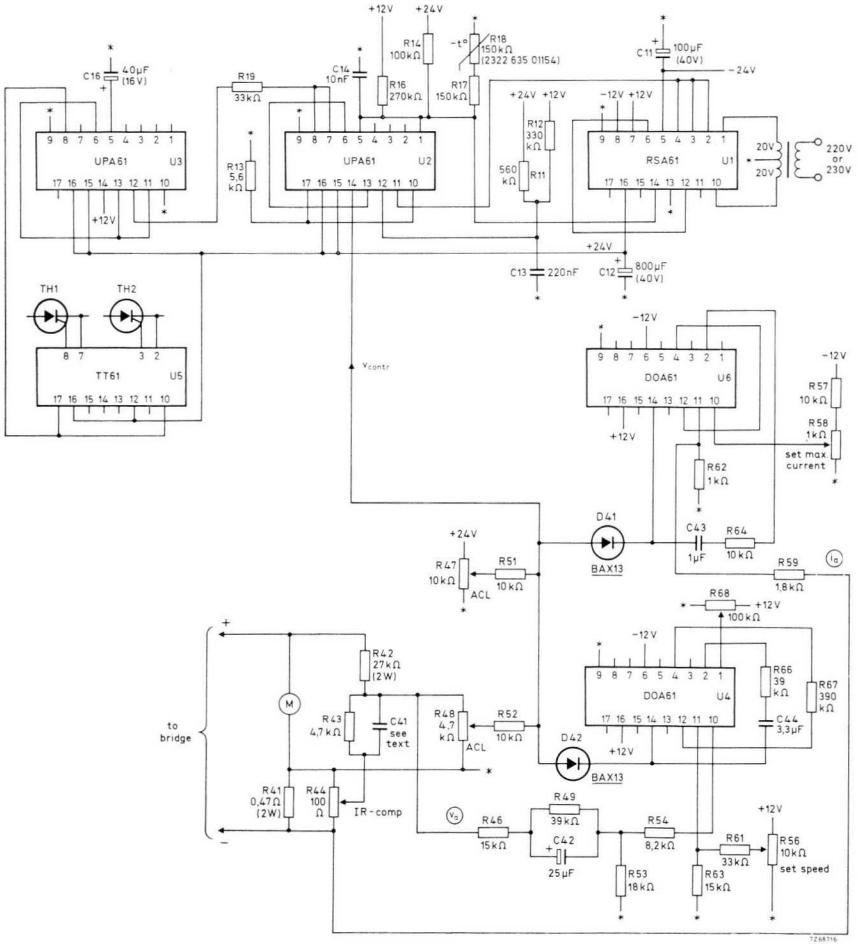


Fig.4-128 Wiring diagram of d.c. motor control circuit (version 2). * = common point; bridge circuit according to Fig.4-122 or 4-123.

Adjustment (Fig.4-128):

1. *Set R_{44}, R_{47}, R_{48} and R_{56} to zero position (wiper at potential of common point). Because the armature does not carry current, it will not rotate and v_a will be zero. Adjust R_{68} to obtain zero output at pin 14 of U_4.*
2. *Adjust R_{56} and R_{58} to their maximum position (R_{58}-wiper set to most negative potentiometer terminal) so that the outputs of U_4 and U_6 are inhibited (D_{41} and D_{42} reverse-biased). Raise the setting of R_{47} so that, with the motor stalled, nominal armature current flows.*
3. *With the motor stalled, adjust IR-compensation potentiometer R_{44} so that the d.c. voltage across R_{48} is zero.*
4. *Raise the setting of R_{48} so that, with the fully-loaded motor running at nominal speed, nominal armature current flows.*
5. *Re-adjust R_{47} so that, with the motor accelerating to nominal speed, the armature current does not drop below nominal level.*
6. *Check if, with stalled motor, the armature current can be varied with R_{58} between zero and nominal level. If necessary, change the value of R_{57}; then set R_{58} again to its maximum position.*
7. *If necessary, change the value of C_{42} so that the dynamic response shows minimum overshoot or undershoot; it may also be necessary to change the value of C_{44} and R_{66}.*

Table 4-13. Specification to Figs.4-122 and 4-123. Output ratings apply to circuit versions 2 and 3, and are valid for 220 V ± 10% a.c. input, and the diode and thyristor mounting-base temperature not exceeding 125 °C and 85 °C, respectively.

fig.	TH_1, TH_2	D_3 to D_6	R_3	C_3	rated output current at 220 V a.c.	rated output power at 220 V a.c.
4-122	BTY79-700R	BYX39-800	33 Ω, 1 W	0,1 μF, 1000 V d.c.	11,5 A	2,3 kW
4-122	BTY87-700R	BYX40-800	33 Ω, 1 W	0,1 μF, 1000 V d.c.	18 A	3,6 kW
4-123	BTW38-800RM	BYX40-800	82 Ω, 2 W	0,47 μF, 1000 V d.c.	16 A	3,2 kW
4-123	BTW47-800RM	BYX25-800	82 Ω, 2 W	0,47 μF, 1000 V d.c.	25 A	5,1 kW
4-123	BTW92-800RM	BYX25-800	68 Ω, 2 W	0,47 μF, 1000 V d.c.	36 A	7,2 kW
4-123	BTW24-800RM	BYX56-800	56 Ω, 2 W	0,47 μF, 1000 V d.c.	63 A	12,7 kW

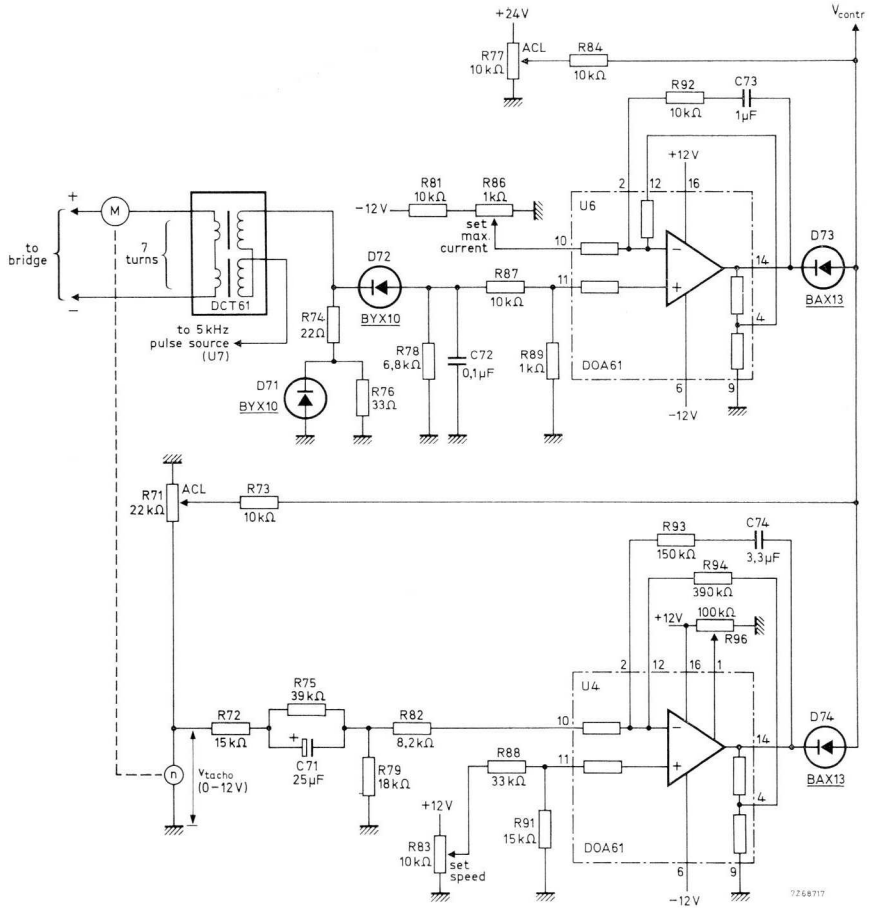


Fig.4-129 Armature connection and control section of d.c. motor control circuit (version 3); v_{contr} goes to the trigger section, Fig.4-124. Bridge circuit is according to Fig.4-122 or Fig.4-123.

Version 3

In the circuit of Fig.4-129, speed is measured by using a tachogenerator, and the armature current is sensed by the DCT61 (Section 4.9.2). In this way, the control circuit is isolated from the a.c. input. The DCT61 has seven primary turns, allowing currents up to about 20 A to be measured. The operation of the control circuit is identical to that described previously. Table 4-13 gives some circuit data.

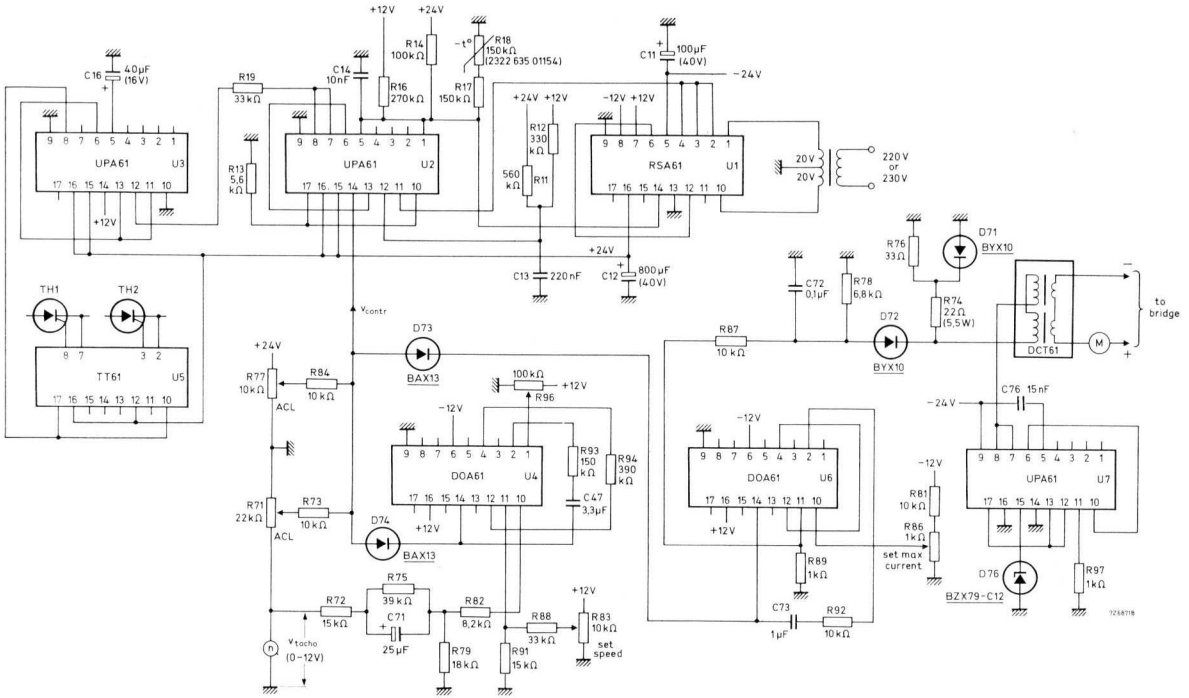


Fig.4-130 Wiring diagram of d.c. motor control circuit (version 3). Bridge circuit is according to Fig.4-122 or 4-123.

Adjustment (Fig.4-130):

1. *Set R_{71}, R_{77} and R_{83} to zero position (wipers at earth potential). Because the armature does not carry current, it will not rotate and the tachogenerator produces zero output. Adjust R_{96} to obtain zero output at pin 14 of U_4.*
2. *Set R_{83} and R_{86} to their maximum position (R_{86}-wiper set to the most negative potentiometer terminal) so that the outputs of U_4 and U_6 are inhibited (D_{73} and D_{74} reverse-biased). Raise the setting of R_{77} so that, with the motor stalled, nominal armature current flows.*
3. *Check the polarity of the tachogenerator signal; if the motor does not run at a low speed with R_{83} set close to zero position, the tachogenerator connections should be reversed.*
4. *Raise the setting of R_{71} so that, with the fully-loaded motor running at nominal speed, nominal armature current flows.*
5. *Re-adjust R_{77} so that, with the motor accelerating to nominal speed, the armature current does not fall below nominal level.*
6. *Check if, with stalled motor, the armature current can be varied between zero and nominal level with R_{86}. If necessary, change the value of R_{81}; then set R_{86} again to its maximum position.*
7. *If necessary, change the value of C_{71} so that the motor dynamic response shows minimum overshoot or undershoot; it may also be necessary to change the value of C_{74} and R_{93}.*

4.7.4 Four-quadrant d.c. motor controller using three-phase thyristor twin bridge

General. The system treated here provides four-quadrant control by using two regenerative three-phase thyristor bridges in anti-parallel (Fig.4-114). It provides motor control over a wide speed range and megawatt output powers have been achieved. System features are:

- Switching from motoring to regenerating occurs at zero armature current. That is, control is transferred from one thyristor bridge to the other after the armature current has been forced down to zero, and then only after 20 ms delay. In this way it is ensured that there is no load current flowing. Switching with armature current present would cause a heavy current to circulate between bridges.
- ACL (Advance Current Limiting) causes the bridge output voltage to follow the motor armature voltage so that the difference between the armature voltage and the bridge output voltage does not exceed the value corresponding to permissible maximum armature current. Thyristor and motor protection is obtained because the surge current during acceleration and reversing is held within safe limits. ACL operates immediately and maintains control until the slower operating peak and average current limit can take over. Average-current limiting is included and can be used for torque control (maximum torque adjustable).
- A tachogenerator is used for accurate speed measurement and control (Section 4.7.3).
- Emphasis has been placed on safe operation. If the controller fails, the thyristors are still triggered by "end-stop" pulses at a trigger angle of 160° to ensure thyristor turn-off during regeneration. A mains on/off logic circuit ensures that safe mains supply switching occurs during regeneration, and also that the internal low-voltage supplies are monitored.
- The control circuit is isolated from the power section.

System operation. Fig.4-131 is a simplified block diagram of the reversible d.c. motor drive. Speed is set by adjusting the reference voltage (−5 V to +5 V). There are three main sections: the controller, the thyristor trigger circuit, and the thyristor twin bridge. The thyristor trigger circuit receives an analogue

signal v_c which determines the trigger angle and, thus, the magnitude of the motor armature voltage; V_{CW} and V_{CCW} are logic signals, only one of them being applied at any time for bridge switching (clockwise or counter-clockwise motor rotation). The trigger circuit input signals depend on the magnitude and polarity of the error signal. This signal is the difference between the reference voltage and the tacho voltage, and equilibrium in control is obtained when the error signal approaches zero.

The diagram shows three control loops: ACL, current or torque control, and speed control. When the motor accelerates or decelerates, ACL initially overrides all other controls to keep the motor surge current at a safe level. Then the current control loop takes over, restricting the rate of change of v_c to limit the average motor current. Speed control ultimately results when motor speed approaches the set value.

The ACL loop has positive feedback and causes the bridge output to follow the armature voltage. It has a gain of slightly less than unity; an integrating network is included for control stability.

Stability and accuracy are the advantages of the control principle described. When the error signal is large, the very narrow proportional band of the speed control loop will be exceeded. This loop is, consequently, inoperative so that stability is maintained. The control action of the ACL loop reduces the error signal causing it to fall within the proportional band of the speed control loop. This loop then resumes control, reducing the remaining error signal to a very low level (high open-loop gain).

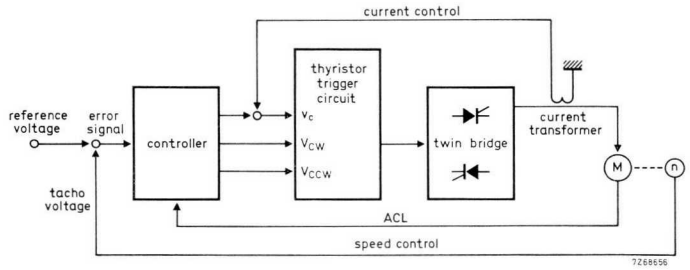


Fig.4-131 Block diagram showing the three control loops.

Trigger angle relation. The two bridges function in anti-parallel: one operates as a rectifier while the other is in standby for regenerative braking. Switching from motoring to regenerating requires that the trigger angles ϑ_1 and ϑ_2 of the two bridges be supplementary, i.e. $\vartheta_1 + \vartheta_2 = 180°$. See Fig.4-132. Linear phase control (linear relation between trigger control voltage and trigger angle) is used over a range of trigger angle from 20° to 160° because any change in control characteristic (with mains voltage or temperature variation) would otherwise cause asymmetrical operation between the motoring and regenerating quadrants of the system. Over this range, the bridge output characteristic is fairly linear; any discrepancy is compensated by a variable-gain amplifier in the controller.

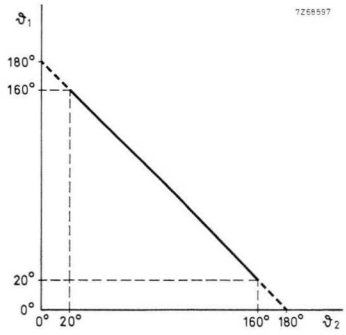


Fig.4-132 Relation between trigger angles ϑ_1 and ϑ_2.

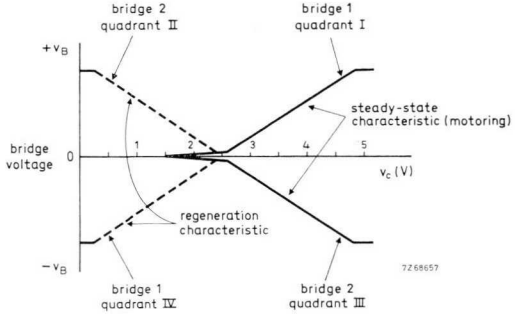


Fig.4-133 Bridge output V_B vs. d.c. control input v_c.

Fig.4-133 illustrates the idealized control characteristics (d.c. control input 0 V to 5 V). The characteristics represent the outputs of the thyristor bridges functioning in anti-parallel. The full lines are the steady-state characteristics, the tails (at a control voltage of about 1,5 V) corresponding to a trigger angle of 120 °; the dashed portions are the transition characteristics representing regenerative braking.

System set-up. The controller uses 36 circuit blocks (3 × RSA61, 19 × UPA61, 4 × DOA61, 7 × 2.NOR61, 2 × 4.NOR60, 1 × TT61). As seen from Fig.4-134, the following section can be distinguished:

No. 1 to 5 printed-circuit boards containing the control and trigger functions
No. 6, 7 regenerative three-phase thyristor bridges no. 1 and 2
No. 8 direct current transformer
No. 9 tachogenerator.

Below, the printed-circuit boards are briefly discussed.

P.E.R.C. (4 × DOA61, 2 × 2.NOR61).
Functions: Power supply
Error amplifier
Regeneration switch
Current limiting.

Inputs are the tachogenerator voltage v_t, the reference voltage v_{ref} (speed setting), the direct current transformer output i_a (proportional to armature current) and the voltage v'_a (proportional to armature voltage), the latter providing ACL. Signals v_{ref} and v_t are compared, and the resulting error voltage V_{ES}, supplied to the B.O.V. board, is used as a switching signal to turn on either bridge 1 or bridge 2. Voltages V_{EX} (derived from V_{ES}) and v_t control the regeneration switch, i.e. whether motoring or regenerating will occur, depending on the change of v_{ref}. Control voltage v_o is the algebraic sum of the amplified error signal (difference of v_{ref} and v_t) and of v'_a. Depending on the position of the regeneration switch, the amplified error signal and v'_a will add for motoring (trigger angle less than 90 °) or subtract for regenerative braking

(trigger angle exceeding 90°). Signal i_L (derived from i_a) provides current limiting; it is variable to obtain an adjustable maximum current level (maximum-torque control).

B.O.V. (3 × UPA61, 2 × 2.NOR61, 2 × 4.NOR60, 1 × TT61)
Functions: Bridge switching
On/off switch
Voltage transformer.

Inputs are the armature voltage v_a, the signal i_a, and the outputs V_{ES}, v_o, and i_L from the P.E.R.C. board. A d.c. voltage transformer converts the armature voltage into a proportional signal v'_a that is isolated from the system a.c. supply. Output signal V_{CW} controls the trigger circuit to turn-on bridge 1 for clockwise rotation, V_{CCW} turning on bridge 2 for counter-clockwise rotation. With V_{ES} reversed in polarity, bridge switching occurs after the armature current has been reduced to zero (i_a sensed by a zero detector) and then only after a 20 ms delay. (Armature current is suppressed by increasing the trigger angle to its maximum value, which causes the bridge output voltage to become negative.) During the delay interval, V_{CW}, V_{CCW}, and v_c are zero so that both thyristor bridges are inoperative. Signal i_L restricts the rate of change of v_c if the motor current tends to exceed the preset limit. The on/off command signal ensures switch-on and switch-off under safe conditions.

T.B.T.U. (3 boards – one for each phase – each containing 5 × UPA61, 1 × RSA61, 1 × 2.NOR61; one board contains an extra UPA61 as the central trigger pulse generator).
Function: Twin Bridge Trigger Unit.

The trigger circuits are synchronized by the phase-phase voltages V_{R-B}, V_{Y-R} and V_{B-Y}, and the thyristors are triggered by 120° pulse trains. For v_c increasing from 0 V to 5 V, the trigger angle decreases from about 160° to 20°. The central pulse generator is necessary, because two thyristors must be turned on simultaneously.

Performance. The brief specification is as follows:

Speed range	> 1000:1
Speed error at maximum speed	± 0,5 % for a ± 10 % variation of mains voltage ± 0,1 % for a torque variation of between 10 % and 100 %.
Torque range	> 10:1.

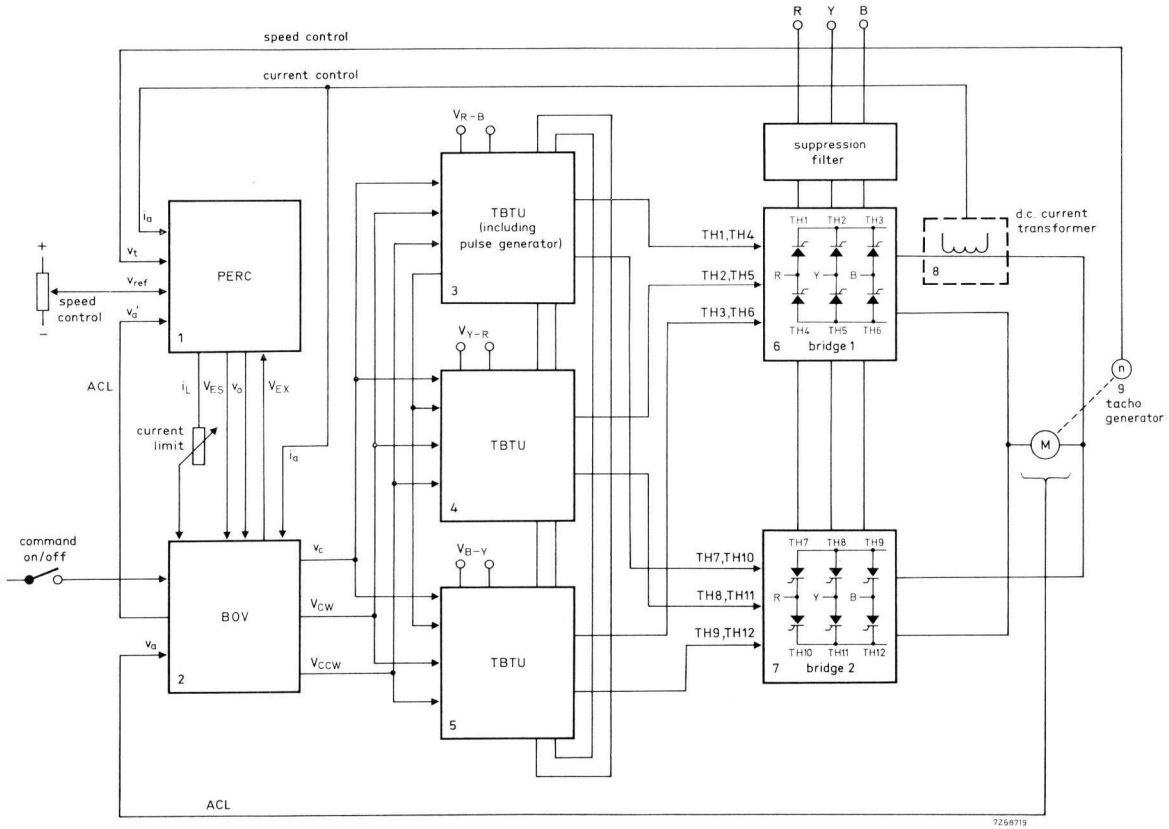


Fig.4-134 Set-up of four-quadrant d.c. motor controller using thyristor twin bridge.

4.7.5 Four-quadrant d.c. motor controller using choppers

Working principle. Four-quadrant motor control can be achieved with fairly simple circuitry when using a dual-chopper controller. Fig.4-135 illustrates the single phase power circuit capable of controlling shunt-wound motors to 1,5 kW (outline of commutation inductance shown in Fig.4-136). Output powers of up to 20 kW can be controlled when adapting chopper and d.c. supply circuitry. Chopper design is discussed in Section 4.5.4. The motor control system uses 15 Norbits (5 × DOA61, 9 × UPA61, 1 × 2.IA60); it contains a speed control loop as well as a current control loop. If the armature current tends to become excessive, current control overrides speed control and provides current limiting. To obtain good control performance, the speed control signal is derived from a tachogenerator. Armature current is monitored by direct current transformers, one for each direction of current. The proposed circuit provides isolation between the a.c. supply and the control section. Circuit operation is as follows.

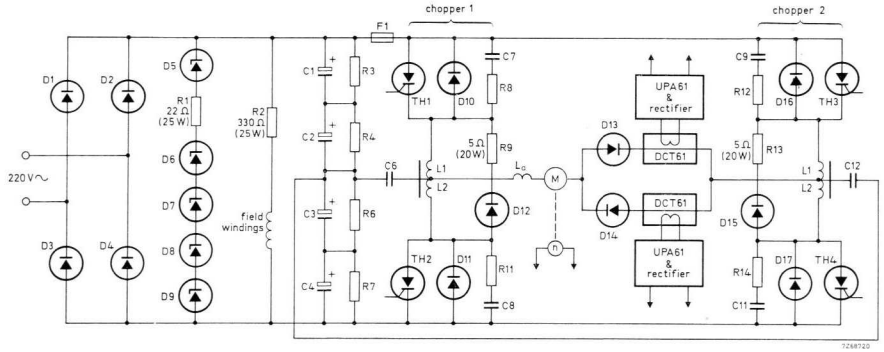


Fig.4-135 Power circuit of 1,5 kW four-quadrant d.c. motor controller. R_3 to R_7 = 4,7 kΩ, 5,5 W; R_8 R_{11} R_{12} R_{14} = 8,2 Ω, 5,5 W; C_1 to C_4 = 10 000 μF, 100 V; C_6 C_{12} = 5 μF, cat no. 2222 327 56505; C_7 C_8 C_9 C_{11} = 47 nF, 1000 V d.c.; D_1 D_2 D_{14} = BYX25-600; D_3 D_4 D_{13} = BYX25-600R; D_5 D_7 D_9 = BZY91-C75; D_6 D_8 = BZY91-C75R; D_{10} D_{11} D_{16} D_{17} = BYX30-600; D_{12} D_{15} = BYX42-600R; TH_1 to TH_4 = BTW30-600RM; L_1 L_2 = 2 × 30 turns, 2,5 mm² litz wire on 6 × 4312 020 33040 ferroxcube pieces (Fig.4-136), F_1 = 25 A fast fuse.

With the motor rotating clockwise, thyristors TH_1 and TH_2 are triggered in turn, and thyristor TH_4 is triggered continuously. Motoring occurs when the average voltage delivered by chopper 1 exceeds the armature e.m.f. Conversely, regeneration results when the average voltage from chopper 1 is reduced to a level lower than that of the armature e.m.f. Regeneration current is maintained by the armature inductance L_a; that is, with D_{17} and D_{10} conducting, the armature voltage becomes higher than that delivered by the rectifier bridge D_1 to D_4. As soon as the d.c. input voltage is made to exceed 325 V (nominal value about 300 V), diodes D_5 to D_9 avalanche and the power recuperated is dissipated in R_1 and the diodes. (The various chopper states and current waveforms both for motoring and regenerating are depicted in Figs. 4-66 to 4-68). Up to 25 A d.c. can be safely commutated.

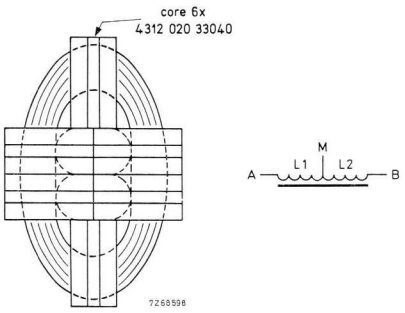


Fig.4-136 Outline (a) and diagram (b) of commutation inductance L_1 L_2 (Fig.4-135). Inductance between A and M or B and M is 275 μH; inductance between A and M (A and B linked) is 10 μH. Number of turns 2 × 30.

For the motor to run counter-clockwise, thyristors TH_3 and TH_4 must be triggered in turn, a continuous trigger signal being supplied to TH_2. Now chopper 2 delivers a d.c. output, and the conditions defining motoring and regenerating are as described above.

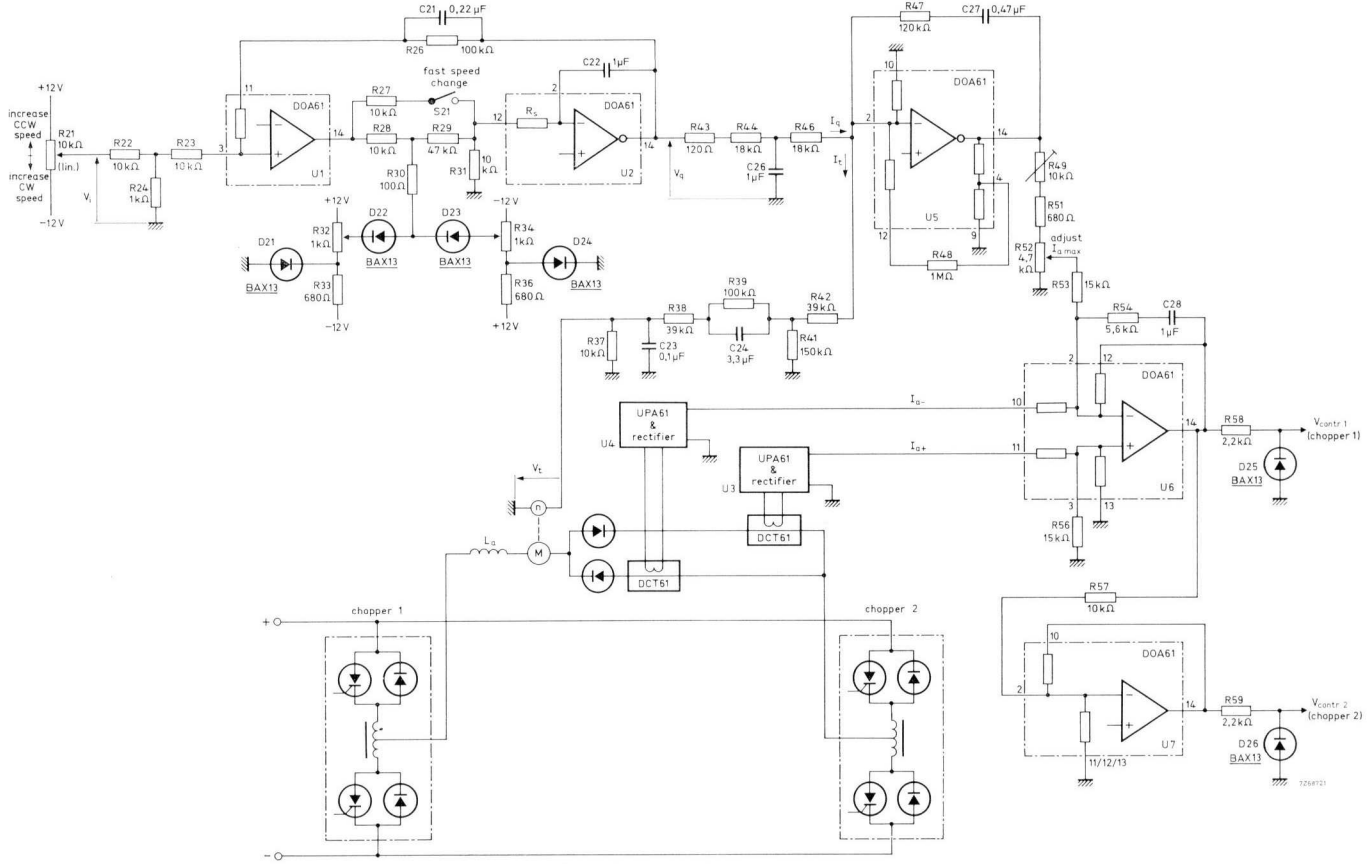


Fig.4-137 Control section of 1,5 kW four-quadrant d.c. motor controller.

Control section. The control section shown in Fig.4-137 has a speed control loop U_1 U_2 U_5 U_6 U_7 and a current control loop U_3 U_4 U_6 U_7. D.C. output voltages V_{contr1} and V_{contr2} control the trigger circuits of chopper 1 and chopper 2, respectively (Fig.4-135), and the average chopper outputs are proportional to these control voltages. The speed control loop will first be described.

Motor speed is proportional to d.c. input signal V_i; change of the polarity of V_i results in reversed rotation. Owing to negative feedback via R_{26}, integrator U_1 U_2 works as an inverting amplifier in steady-state condition, with unity gain; that is: $V_q = -V_i$. Error amplifier U_5 compares currents I_q and I_t originating from V_q and tacho voltage V_t (V_q and V_t of opposite polarity). Since U_5 has high gain, its input voltage is almost zero at equilibrium, which implies that I_q and I_t are equal. Current I_q is proportional to V_i and I_t is proportional to V_t, latter being proportional to motor r.p.m. It follows that system performance is linear.

A negative signal V_i creates a positive V_q-value, causing error amplifier U_5 to produce a negative output. This output is applied to the inverting input of U_6 via R_{49} R_{51} R_{52} R_{53} so that V_{contr1} becomes positive; chopper 1 produces a d.c. voltage causing clockwise (CW) motor rotation. The positive output from U_6 is inverted in U_7; hence, with D_{26} conducting, V_{contr2} becomes zero and the output of chopper 2 is inhibited (only TH_4 in Fig.4-135 triggered). If the motor load increases, V_t tends to decrease in magnitude. The output of U_5 becomes more negative, and V_{contr1} rises. A higher d.c. voltage is supplied to the motor, counteracting the speed decrease due to increased load. Speed stabilization will thus occur.

With V_i positive, amplifier U_6 produces a negative output which is inverted by U_7. As a result, V_{contr1} becomes zero and V_{contr2} assumes a positive value. Thyristor TH_2 in Fig.4-135 being triggered and chopper 2 producing a d.c. output, the motor rotates counter-clockwise (CCW).

When V_i is varied, the output of U_1 is clamped to the voltage at the wiper of either R_{32} or R_{34}, depending on its polarity. The clamped voltage, V_{cl}, at the junction of R_{28} and R_{29} is integrated by U_2, yielding a rate of change of V_q equal to:

$$\frac{dV_q}{dt} = \frac{-V_{cl}}{C_{22}\left[R_s + \frac{R_{29}}{R_{31}}(R_s + R_{31})\right]}.$$

So the maximum speed change rate can be adjusted by varying V_{cl}. Rapid speed changes are obtained when S_{21} is closed.

The speed control signal is mixed at the input of U_6 with the negative current-proportional signal from either U_3 or U_4, depending on the direction of armature current. (Section 4.9.2 describes the operation of direct current transformers U_3 U_4). During acceleration or deceleration, error amplifier U_5 saturates; as a result, current control predominates over speed control and limits the rate at which the chopper output increases (acceleration) or decreases (deceleration). In this way, the current is limited to a value proportional to the angular position of R_{52}.

Trigger section. The trigger section, Fig.4-138, contains a sawtooth generator yielding linear chopper output control, the trigger circuit for chopper 1 (thyristors TH_1 TH_2) and the trigger circuit for chopper 2 (thyristors TH_3 TH_4). Fig.4-139 shows circuit waveforms. The chopper operating frequency is preset with R_{72} to a value between 400 Hz and 1 kHz, so that thyristor switching losses as well as armature ripple current are low. Section 1.2.2 describes the operation of the sawtooth generator and the comparator.

When V_{contr1} is positive, V_{contr2} is zero, and vice versa. For V_{contr2} zero, comparator 2 produces a HIGH output (waveform *K* in Fig.4-139), and TH_4 continuously receives trigger pulses (waveform *L*). As a result, the output of chopper 2 is zero. At the same time, the rectangular-wave output from comparator 1 (waveform *C*) causes thyristors TH_1 TH_2 to be triggered in turn, so chopper 1 delivers a d.c. output (see the waveform). This output increases as the result of V_{contr1} rising; see the arrows. RC-delay networks are included in the input circuit of each trigger pulse generator, to provide an 80 μs dead zone (waveforms *E* and *H*) for safe thyristor turn-off.

Safeguards. Norbit U_{13} in Fig.4-138 inhibits trigger units U_{11} and U_{15} for about one second after switch-on, so that the choppers produce zero output voltage until the d.c. supply voltage for the trigger and control circuit has settled. The a.c. supply for this circuit is obtained via a relay that, after switch-off, remains energized until the d.c. voltage of the chopper supply circuit has dropped to about one-fifth of its nominal level. If triggering were to be prematurely interrupted, the current between thyristors would cease to commutate and could reach a disastrous level.

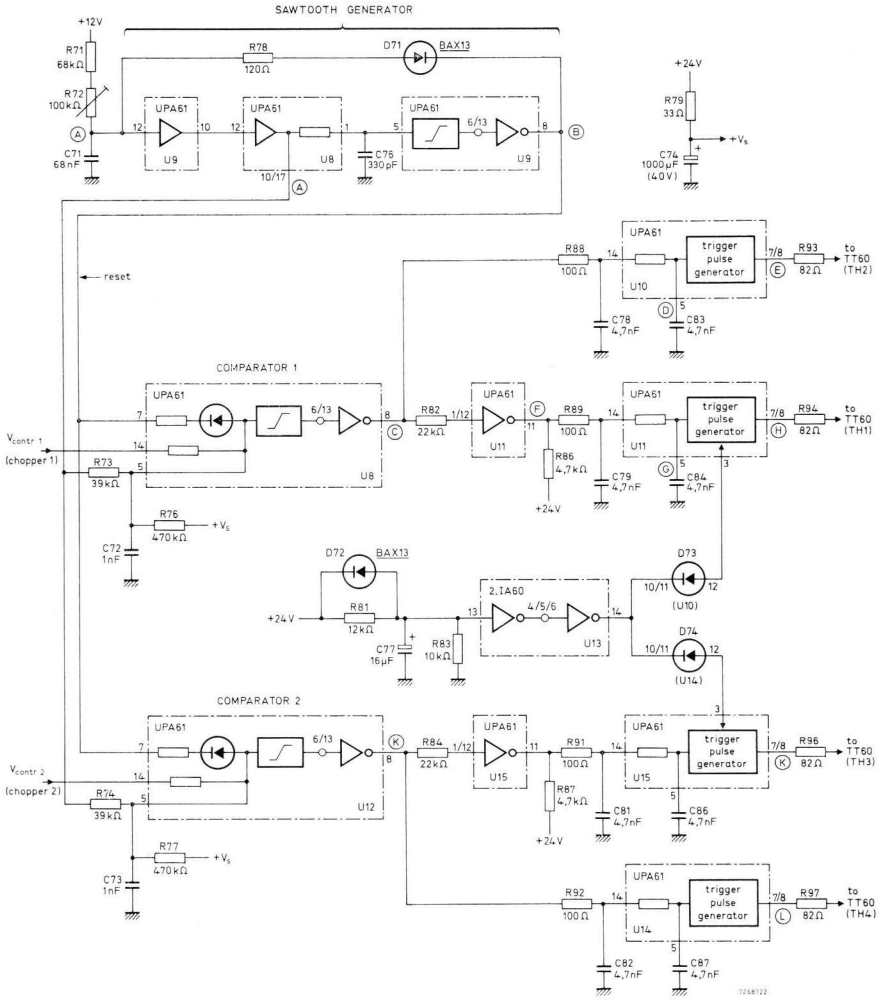


Fig.4-138 Trigger section of 1,5 kW four-quadrant d.c. motor controller. Waveforms shown in Fig.4-139.

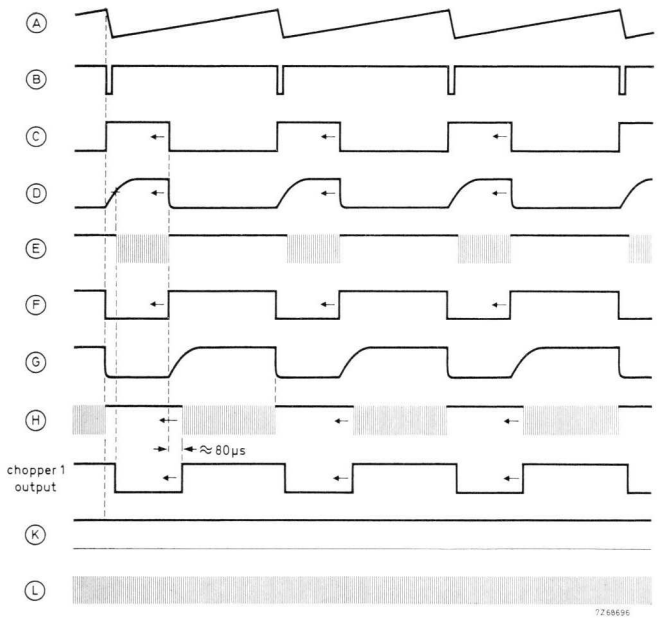


Fig.4-139 Waveforms of trigger section, Fig.4-138.

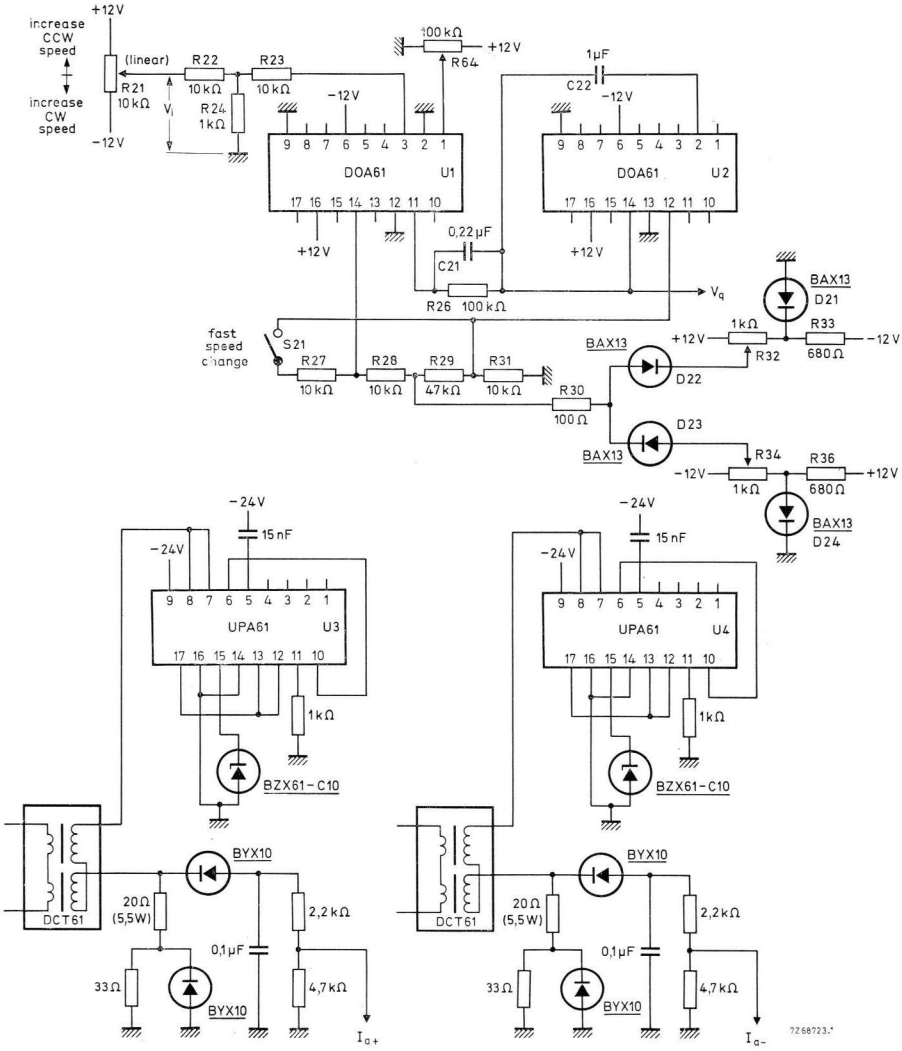


Fig.4-140 Wiring diagram of control section U_1 to U_4 (Fig.4-137).

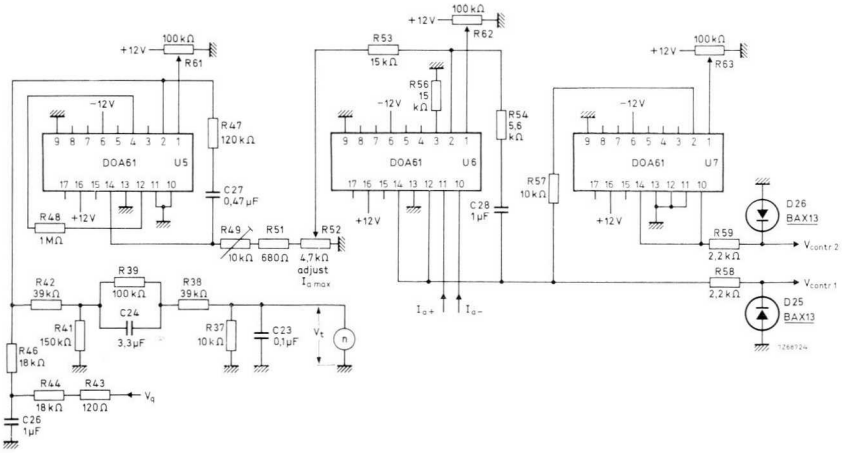


Fig.4-141 Wiring diagram of control section U_5 to U_7 (Fig.4-137).

Adjustment (Figs.4-140, 4-141, 4-142):

1. *Short-circuit R_{24} (Fig.4-140) and adjust R_{64} to obtain zero output at U_1 pin 14.*
2. *Adjust R_{21} (Fig.4-140) so that the voltage V_q at output pin 14 of U_2 becomes zero. Then set R_{61} (Fig.4-141) to obtain zero output at pin 14 of U_5 with the motor circuit out of operation.*
3. *Set R_{52} (Fig.4-141) to zero position. Then adjust R_{62} to obtain zero output voltage at pin 14 of U_6 with the motor circuit out of operation.*
4. *With the output at pin 14 of U_6 (Fig.4-141) at zero, adjust R_{63} so that the output at pin 14 of U_7 becomes zero.*
5. *Adjust R_{72} (Fig.4-142) so that the choppers operate at a frequency (usually between 400 Hz and 1 kHz) for which thyristor switching losses and armature ripple current are both low.*
6. *Check the polarity of the tachogenerator signal V_t (Fig.4-141); if the motor does not run at a low speed with R_{21} (Fig.4-140) at approximately mid-position, the tachogenerator connections should be reversed.*
7. *Adjust R_{34} (Fig.4-140) to limit the rate of change towards clockwise rotation to the desired value.*
8. *Adjust R_{32} (Fig.4-140) to limit the rate of change towards counter-clockwise rotation to the desired value.*
9. *Adjust R_{49} (Fig.4-141) so that, with R_{52} set to its highest position, the armature current does not exceed the allowed maximum value while the motor accelerates or decelerates, (current limit proportional to the setting of R_{52}).*
10. *If necessary, increase the value of C_{24} (Fig.4-141) in case of overshoot in the motor dynamic response; conversely, decrease the value of C_{24} to eliminate undershoot.*

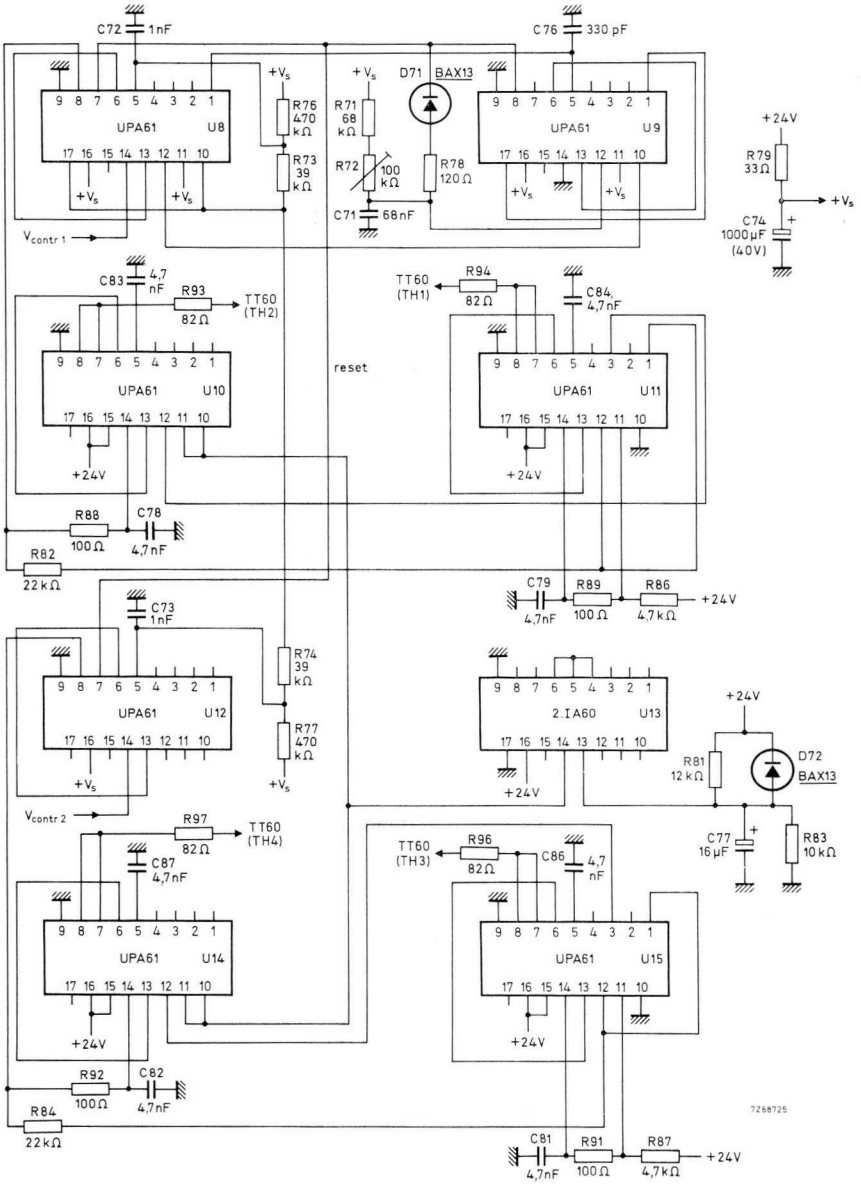


Fig.4-142 Wiring diagram of trigger section, Fig.4-138.

4.8 Welding controllers

4.8.1 Survey of circuits discussed

The welding controllers featured here have the following characteristics:

- "SOFT" START: The welding periods start at a delayed trigger angle. Transformer inrush currents are avoided for the trigger delay angle roughly equal to the phase angle of the transformer with its load connected[20]).
- "SINGLE SHOT"/"REPEAT": Depending on the position of a selector switch, single-shot or repetitive welding will occur, the latter being of importance, e.g., for seam welding operations.
- INTERVAL TIMING: This goes with the "REPEAT" feature, the length of the intervals between the welding periods being so chosen that the power control elements will not become overloaded.
- PROTECTION: Thyristor triggering ceases with heatsink over-temperature or insufficient water flow rate, so that damage is prevented.
- FULL-MAINS CYCLE WELDING PERIODS: The net amount of volt-seconds supplied to the welding transformer is zero, and core saturation does not arise.
- SIGNALLING: A lamp is lit during the welding periods.

Distinction is made between the single-step controller for general purposes and the three-step version developed for fabricating anchor chains (see Table 4-14). A chain link is formed during each welding period. At the start of step 1, maximum electrical power is applied for rapid heating; power is then gradually reduced to limit the temperature. During step 2, the power need be held at a level only sufficient for keeping the material malleable while it is being bent to form the link. To weld the ends of the link together, the power is increased to a higher level (step 3).

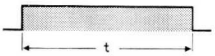
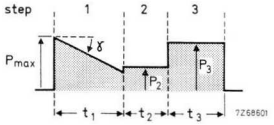
Water-cooled thyristors are recommended because very high power levels are involved. Some of the various devices suitable are mentioned here.

[20]) AN No. 142, ordering code 9399 260 64201 – Time-proportional Controller for Transformer Loads.

- *BTX41 thyristor;* two devices in anti-parallel, each mounted on a heatsink type 56311, are capable of 600 A r.m.s. at a flow rate of 4 l/min. and 40 °C inlet temperature. Voltage classification is 1600 V max.
- *OTH500, OTH800 and OTH1200 ignistors*, designed to deliver 500 A r.m.s., 800 A r.m.s. or 1200 A r.m.s., respectively, at 4 l/min. flow rate and 40 °C inlet temperature. Voltage classification is to 1400 V.

NOTE: To cater for mains transients, the voltage classification is taken as about *three times* the r.m.s. mains voltage.

Table 4-14. Properties of welding controllers.

circuit	power waveforms	variables	notes
single-step welding controller; Section 4.8.2.		t = 1 a.c. cycle to 99 a.c. cycles.	no phase control.
three-step welding controller; Section 4.8.3.		γ adjustable. t_1, t_2, t_3 each adjustable between 0,9 s and 9 s. P_2 and P_3 each adjustable between zero and full power.	phase control.

4.8.2 Single-step welding controller

The single-step welding controller circuit shown in Fig.4-143 is a mains-synchronized timer. Its operation is clear from the waveforms in Fig.4-144. The "tens" and "units" thumbwheel switches indicate the time setting as multiples of the mains period. During welding, the output of U_{3b} is HIGH, causing trigger pulses to be produced. The trigger circuit should be designed according to the gating requirements; suggestions are given in Section 2.6. Gates U_{5a} U_{5b} control lamp L_{a1} to indicate that welding is "on". Diodes of the 2.NOR61 are used to improve noise immunity.

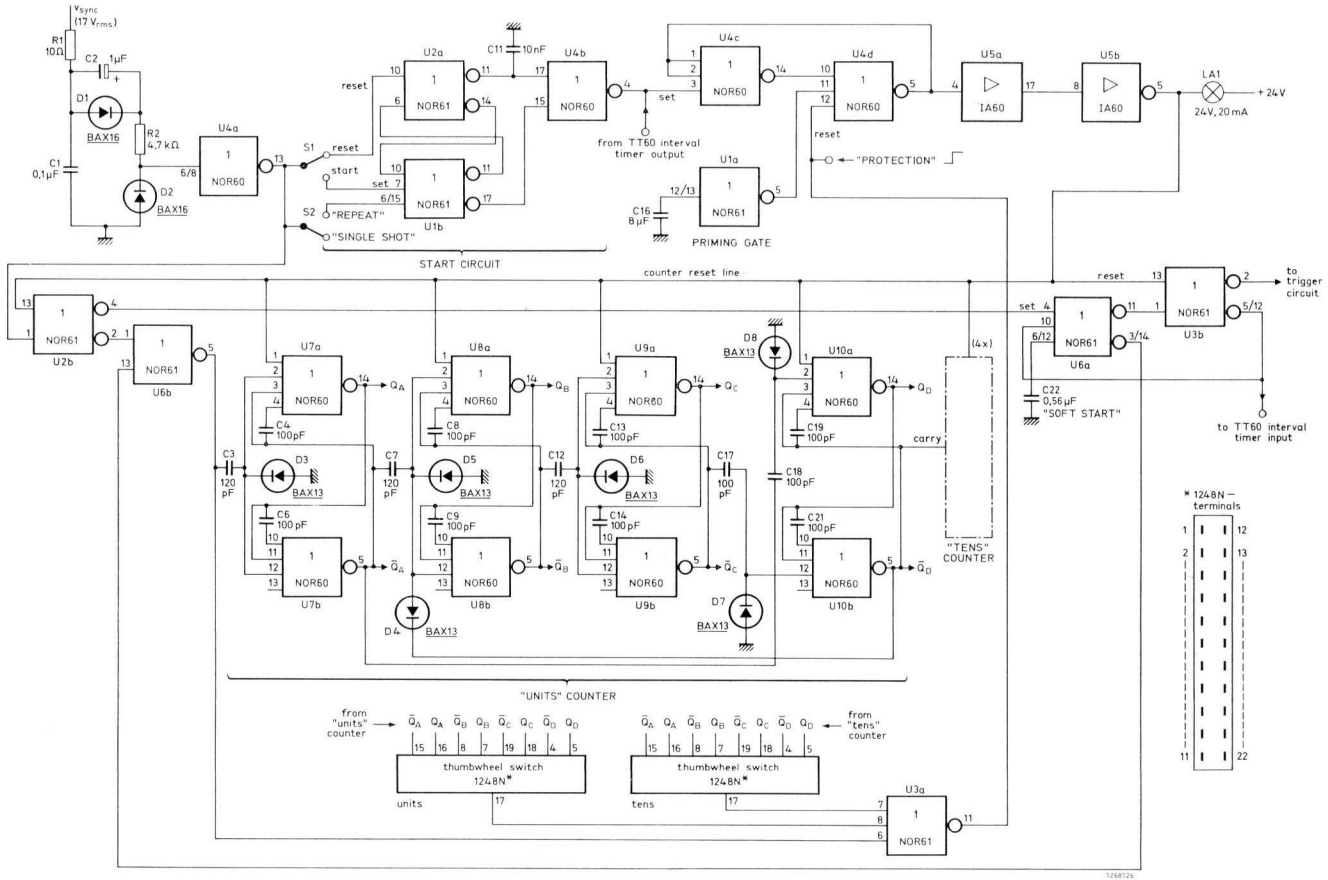


Fig.4-143 Block diagram of single-step welding controller; U_{2a} U_{1b}, $U_{4c\&d}$, U_{6a} U_{3b}, $U_{7a\&b}$ to $U_{10a\&b}$ are bistable flip-flops.

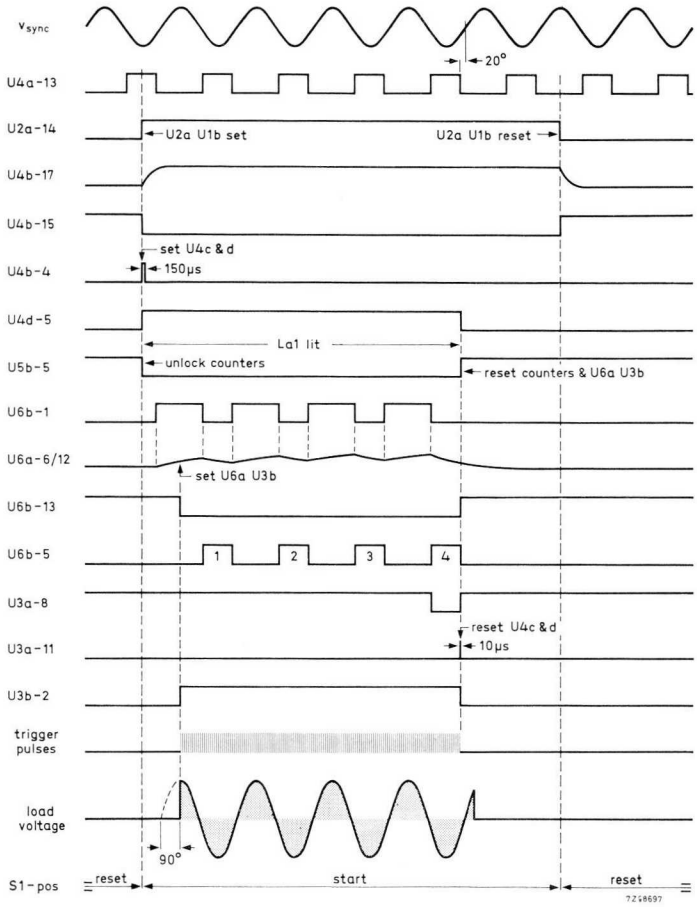


Fig.4-144 Waveforms of single-step welding controller for the thumbwheel switches in position "04".

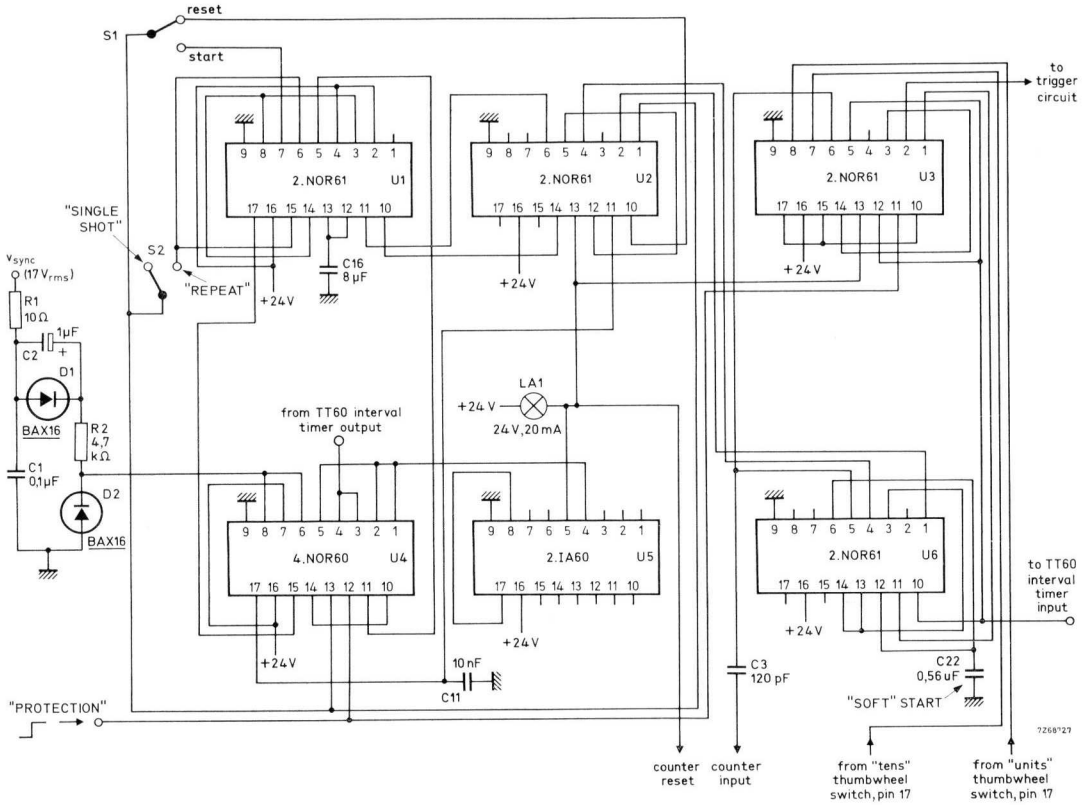


Fig.4-145 Wiring diagram (excluding counter) of single-step welding controller.

Circuit elements D_1 and C_2 in the synchronization input network create a positive pre-bias causing the synchronization pulses at the output of U_{4a} to cease about 20° before the onsets of the positive half mains cycles. Consequently, the load current flows over full cycles so that the welding transformer does not saturate. Filter R_1 C_1 suppresses mains interference.

Switch S_1 is coupled to the welding electrodes. With S_1 in position "start", flip-flop U_{2a} U_{1b} is set, and a single pulse is generated at the output of U_{4b}, starting the timer. (The width of the pulse depends on the value of C_{11}.) Once the counter has reached the position set with the thumbwheel switches, the timer is reset, U_{2a} U_{1b} being reset upon release of S_1.

Priming gate U_{1a} produces a HIGH output during the first 100 ms after switch-on that C_{16} charges, thus preventing erroneous operation due to the unsettled d.c. supply voltage; further, it causes flip-flop $U_{4c,d}$ to assume reset condition when the d.c. supply voltage is applied.

The "PROTECTION" input produces an inhibiting signal (HIGH level) for heatsink over-temperature or insufficient flow rate.

Fig.4-145 is the wiring diagram of the welding controller. The power circuit is shown in Fig.4-153 (Section 4.8.3).

Adjustment:

If transformer inrush currents occur (observe with an oscilloscope) the value of C_{22} in Fig.4-145 must be changed. No inrush condition arises for the welding periods starting at a phase angle roughly equal to that of the load. For C_{22} equal to 0,1 μF no phase delay occurs, and for C_{22} equal to 0,56 μF, as specified, the phase delay is about 90°.

4.8.3 Three-step welding controller

The welding controller discussed here is fully programmable: each of the three steps included in a welding period has individual adjustments (Table 4-14). Timers are used to set the duration of each cycle, and power is controlled by adjusting the trigger angle of the thyristors.

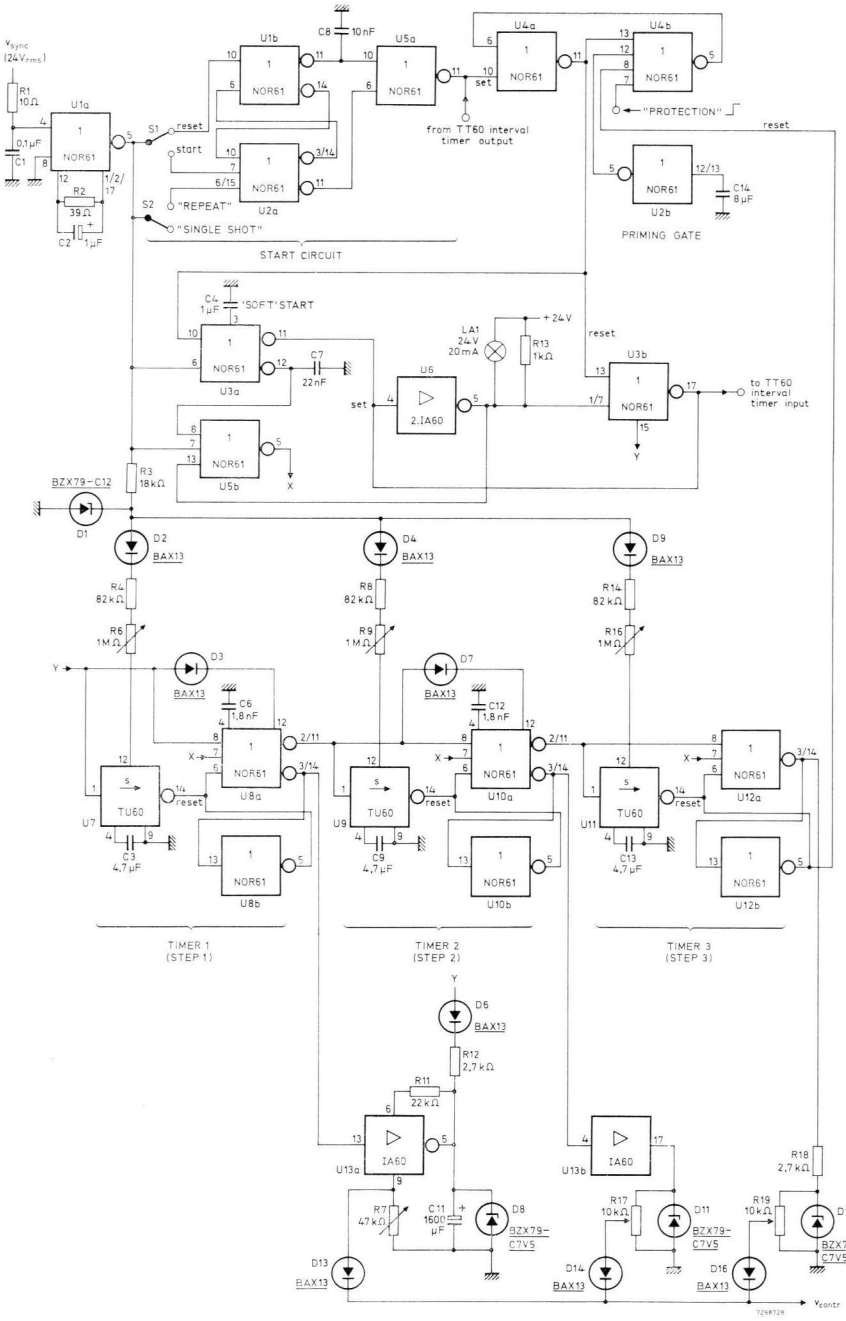


Fig.4-146 General diagram of three-step welding controller; U_{1b} U_{2a}, $U_{4a\&b}$, U_6 U_{3b}, $U_{8a\&b}$, $U_{10a\&b}$, $U_{12a\&b}$ are bistable flip-flops.

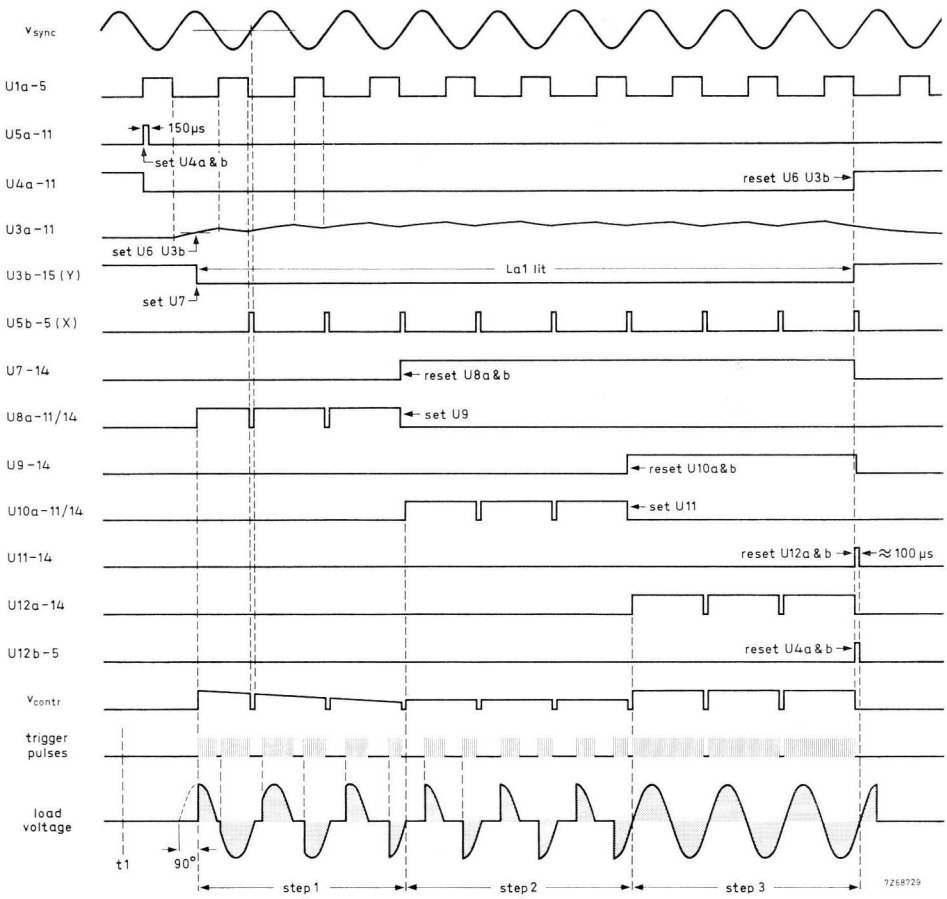


Fig.4-147 Wave pattern of three-step welding controller (switch S_1 of Fig.4-146 closing at time t_1). Each of welding steps 1 to 3 is assumed to have a duration of only three mains periods.

Controller. Fig.4-146 illustrates the controller and Fig.4-147 its waveforms. Setting S_1 to position "start" causes U_{5a} to emit a single pulse which sets flip-flop $U_{4a,b}$. After a fixed interval, flip-flop U_6 U_{3b} is set (time delay determined by both the width of the synchronization pulses emanating from U_{1a} and the value of C_4). Because the welding periods start coincidently with the setting of U_6 U_{3b}, the initial phase angle can be changed by varying C_4. Lamp L_{a1} is lit during the welding periods.

When U_6 U_{3b} is set, its Y-output goes LOW. This starts the timer circuit, and D_3 C_6, D_7 C_{12} ensure that the timers work in succession, timer 2 being set after the delay time of timer 1, and timer 3 being set after the delay time of timer 2. Thus, steps 1, 2 and 3 appear successively at the control output, the common point of decoupling diodes D_{13} D_{14} D_{16} (see v_{contr} waveform in Fig.4-147).

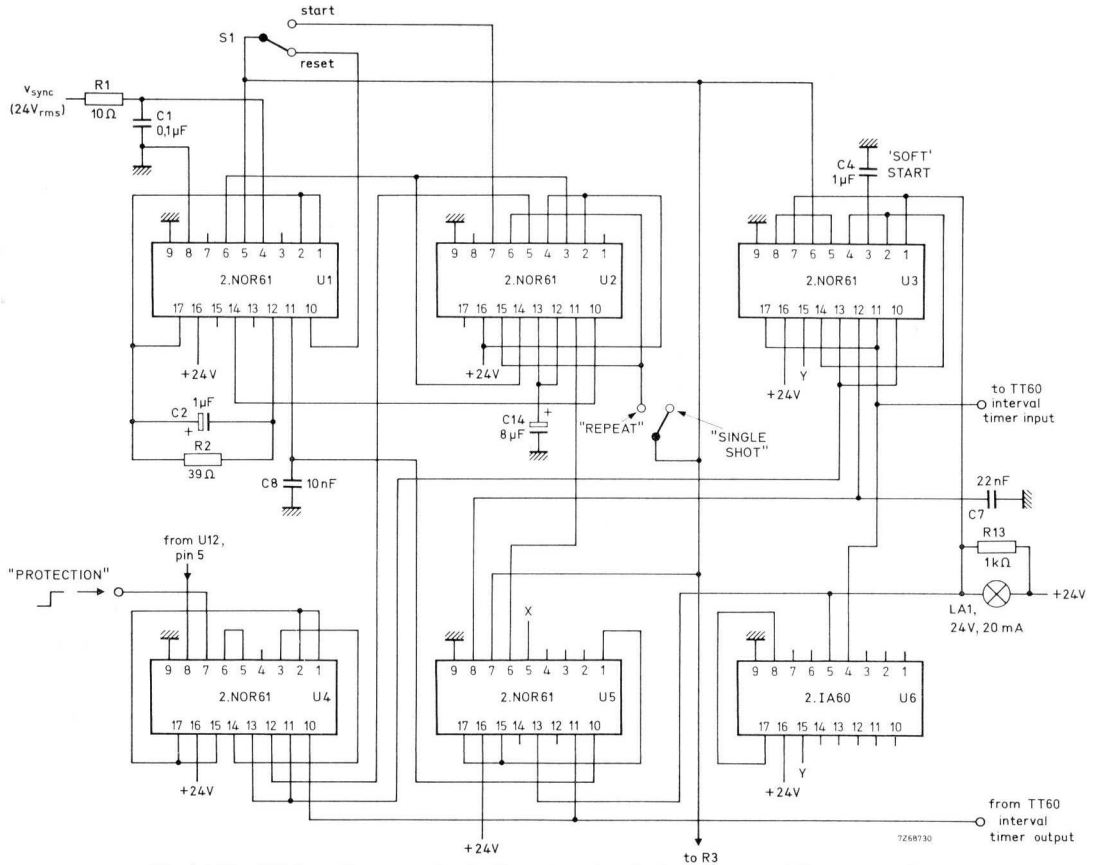


Fig.4-148 Wiring diagram (excluding timers) of three-step welding controller.

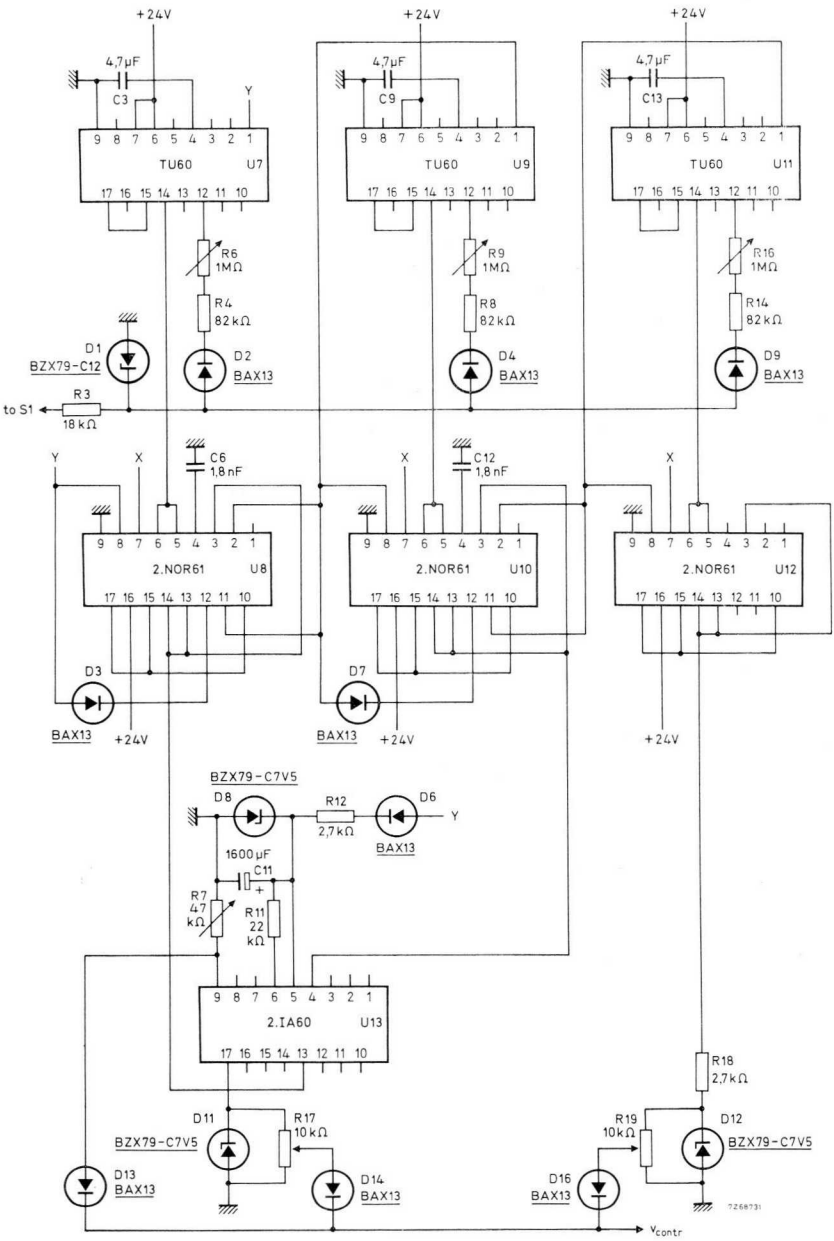


Fig.4-149 Wiring diagram of timers.

The ramp of the welding power occurring during step 1 (Table 4-14) is adjusted with R_7, which controls the discharge rate of C_{11}. The welding power (during steps 2 and 3) is adjusted with R_{17} and R_{19}, which sets the HIGH level of v_{contr}.

The purpose of the priming gate (U_{2b}) has been explained in the previous section.

Timing capacitors C_3, C_9 and C_{13} are charged by the synchronization pulses (U_{1a} output) supplied via D_2 R_4 R_6, D_4 R_8 R_9 and D_9 R_{14} R_{16}. As a result, the timers are not triggered during the positive half cycles (compare the waveforms of v_{sync} and U_{1a}-5), full mains cycles of load current will occur and the welding transformer does not saturate.

Figs.4-148 and 4-149 are the wiring lay-outs of the controller.

Phase shift circuit. The phase shift circuit is shown in Fig.4-150, and the operation of the sawtooth generator is outlined in Section 1.2.1. The input waveform *B* of the Schmitt trigger is the result of the sawtooth voltage *A* and the input signal v_{contr}; at level V_1, the Schmitt trigger trips on (point *P*), its output goes HIGH (waveform *D*), and trigger pulses start to appear. The Schmitt trigger is synchronously reset by the pulses at the collector of reset stage TR_4 (waveform *C*). Changing the HIGH level of v_{contr} shifts the switching point *P* and varies the trigger angle. Phase control is linear for a trigger angle of approximately 20° to 160°.

Fig.4-151 is the wiring diagram. The trigger pulse oscillator (U_{53}) is connected for a 15 Ω load, to obtain a powerful gate drive.

Power circuit. The circuit of Fig.4-153 includes protection of the power control devices against dv/dt and transients. Table 4-15 shows the values of the transient suppression components. The power control devices are selected according to the welding power required (Section 4.8.1) and they are driven by a high-power trigger pulse source (Fig.4-151).

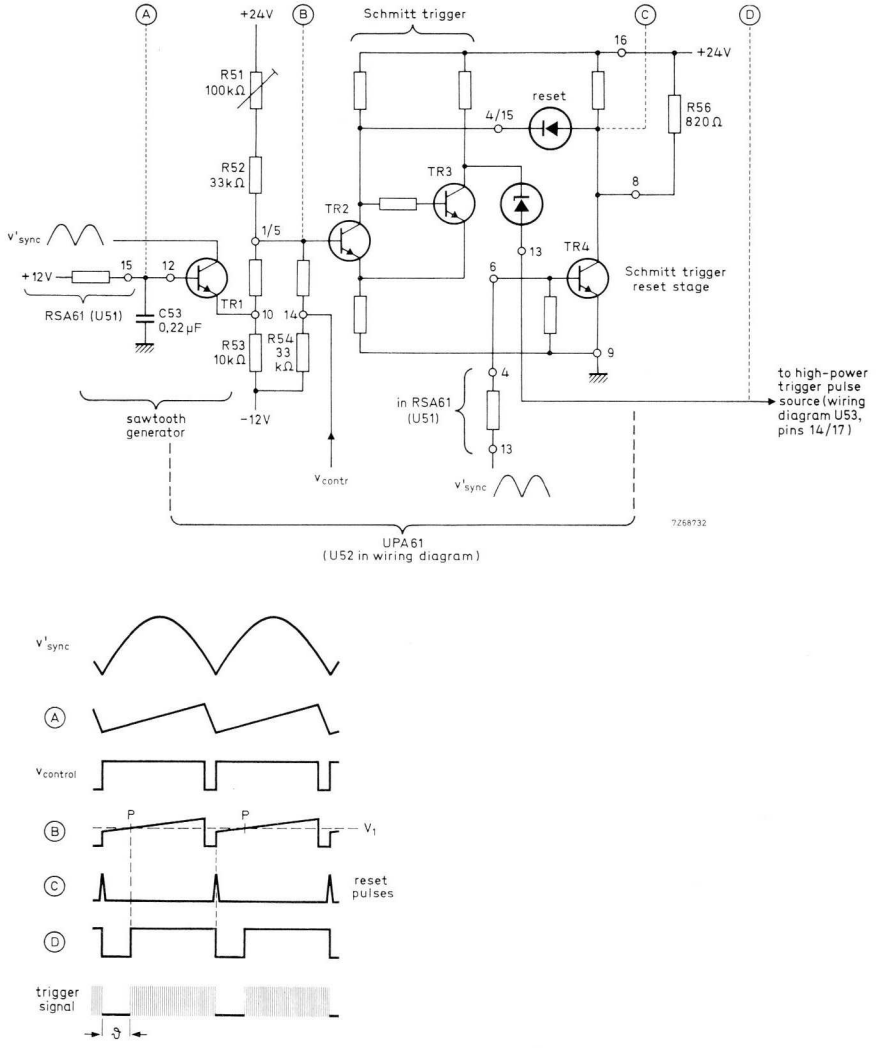


Fig.4-150 Detailed circuit of phase shift unit with waveforms; v_{contr} comes from the timers in Fig.4-146, and the wiring diagram is shown in Fig.4-151.

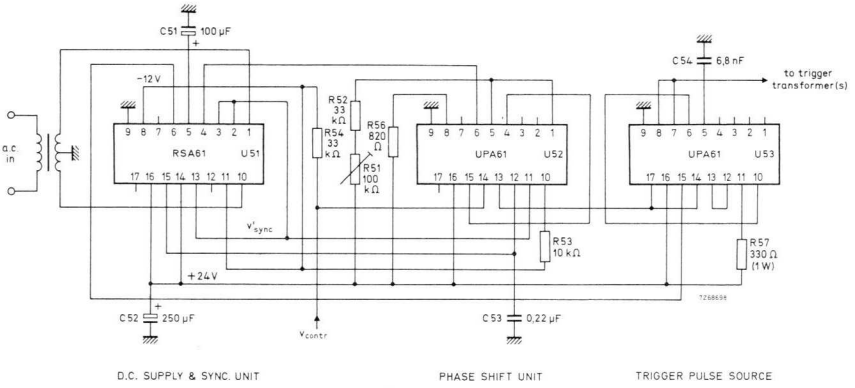


Fig.4-151 Wiring diagram of phase shift unit (v_{contr} comes from the timers, wiring diagram Fig.4-149).

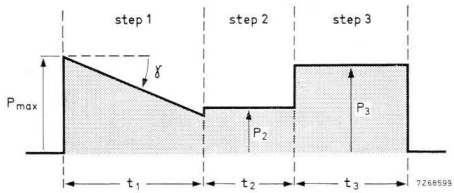


Fig.4-152 Time function of welding power.

Adjustment:

1. *Lengths t_1, t_2 and t_3 of steps 1, 2 and 3 in Fig.4-152 are adjustable between 0,9 s and 9 s by setting R_6, R_9 and R_{16}, respectively in Fig.4-149.*
2. *Slope γ of the power function occurring during step 1 (Fig.4-152) is adjustable by varying R_7 in Fig.4-149.*
3. *Levels P_2 and P_3 of the welding power during steps 2 and 3 (Fig.4-152) are adjustable between zero and maximum power by changing the setting of R_{17} and R_{19}, respectively, in Fig.4-149.*
4. *Adjust R_{51} in Fig.4-151, so that the trigger pulse oscillator is at the verge of oscillation with the welding controller in standby ($v_{contr} \approx 0{,}5$ V); this is checked by connecting an oscilloscope to pin 7 of U_{53}. After this adjustment, about 7,5 V is required at the control input to obtain 170° conduction angle.*
5. *If required, change the value of C_7 in Fig.4-148, so that v_{contr} goes HIGH coincidently with the full-cycle zero cross-over points of the mains voltage (compare the v_{sync}- and v_{contr}-waveforms in Fig.4-147). If C_7 is too large, zero trigger angle cannot be obtained.*
6. *If transformer inrush currents occur (observe with an oscilloscope) the value of C_4 in Fig.4-148 must be changed. No inrush condition arises for the welding periods starting at a phase angle roughly equal to that of the load. For C_4 equal to 1 µF, as specified, the phase angle is about 90°.*

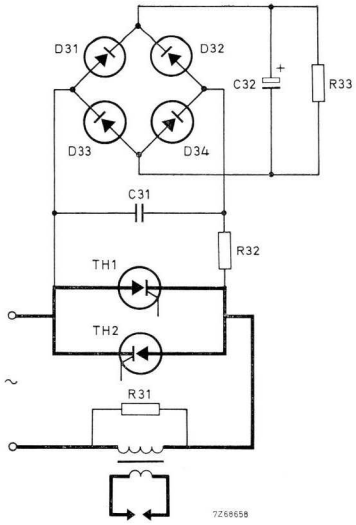


Fig.4-153 Power circuit (ref. Table 4-15)

Table 4-15. Components of Fig.4-153.

mains voltage	220 V to 240 V	380 V to 420 V	500 V to 550 V
D_{31} to D_{34}	BYX22-1200	BYX22-1200	2 × BYX45-800R*
R_{31}	560 Ω, 100 W 2322 323 23561	1800 Ω, 100 W 2322 323 23182	2700 Ω, 100 W 2322 323 23272
R_{32}	12 Ω, 7 W 2322 330 31129	12 Ω, 7 W 2322 330 31129	12 Ω, 7 W 2322 330 31129
R_{33}	10 kΩ, 25 W 2322 321 28103	11 kΩ, 50 W 2 × 2322 321 28562 in series**	11 kΩ, 80 W 2 × 2322 321 26562 in series**
C_{31}	3 μF, 250 V a.c. 2222 241 04623	2,5 μF, 380 V a.c. 2222 240 11617	2 μF, 500 V a.c. 2222 240 19612
C_{32}	32 μF, 400 V d.c. 2222 080 16329	50 μF, 600 V d.c. 2 × 2222 080 14101 in series**	25 μF, 800 V d.c. 2 × 2222 080 16509 in series**

* Two-in series in each branch.
** Common point of resistors in series connected to that of capacitors in series.

4.9 Miscellaneous circuits

4.9.1 Rectangular-wave generator[21])

The rectangular-wave generator circuit of Fig.4-154 has the following features:

- the range of the pulse repetition frequency, adjusted with R_1, is 2000:1
- the duty cycle of output signal v_{pulse}, variable between 0 % and almost 100 %, is proportional to the control input V_{contr} (0 V to 8 V range)
- a complementary output, $\overline{v_{pulse}}$, is available.

This circuit is, therefore, very useful for pulse generation systems. Circuit operation has been detailed in Section 1.2.2.

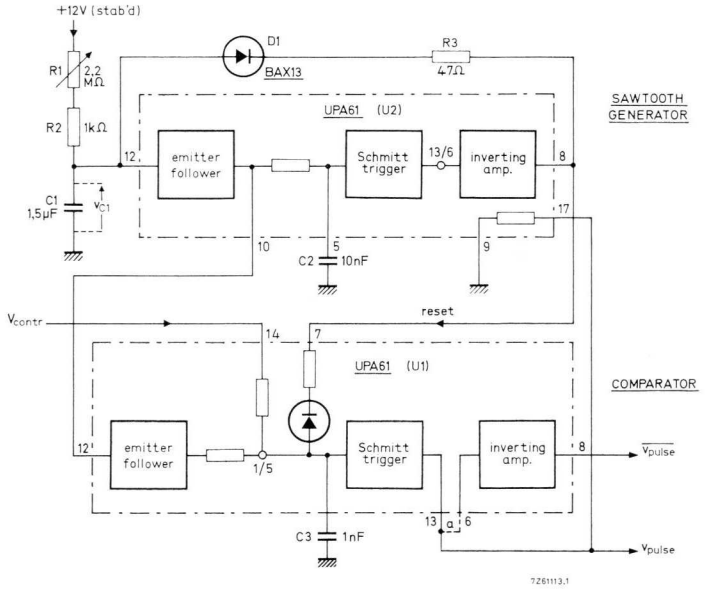


Fig.4-154 Circuit diagram of rectangular-wave generator.

[21]) AN No. 130, ordering code 9399 260 63001 – Rectangular-pulse Generator.

Timing circuit R_1 R_2 C_1 should be supplied from a stabilized d.c. source, so that mains fluctuations will not affect the pulse frequency.

At 24 V $\pm$ 25% d.c. supply, the v_{pulse}-output can drive up to four 2.NOR60-, 4.NOR60- or 2.NOR61-gates, two inputs of each gate being paralleled. At 12 V $\pm$ 5%, a 2.NOR60- or 4.NOR60-gate (three paralleled inputs) or a 2.NOR61-gate (pin 1 or 10) can be driven. Complementary output $\overline{v_{pulse}}$ is obtained by joining pins 6 and 13 (load resistane 90 Ω min.).

Fig.4-155 shows a plot of the duty cycle δ of v_{pulse} versus V_{contr}. The maximum value of δ that can be obtained is about 90% at 1 kHz (higher at a lower frequency). The duty cycle of the complementary output $\overline{v_{pulse}}$ is expressed as 1-δ.

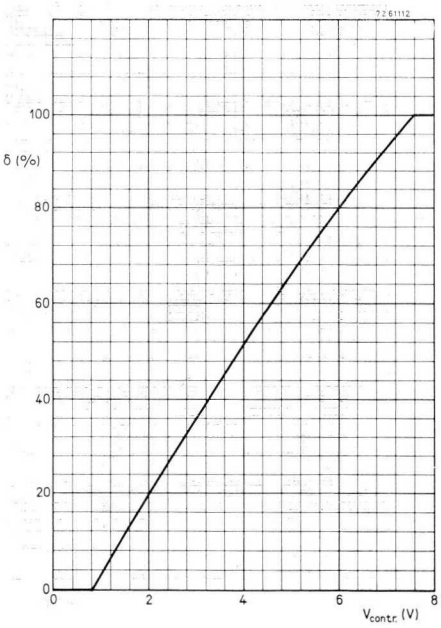


Fig.4-155 Duty cycle, δ, of v_{pulse} (Fig.4-154) vs. V_{contr} for 10 Hz repetition frequency.

Fig.4-156 shows the range of pulse repetition rate, which can be extended by switching the value of C_1.

The lay-out is shown in Fig.4-157. An increased output capability results, if pins 11 and 16 of both circuit blocks are connected to a +24 V supply; in that case, V_{contr} should be derived from the same d.c. source, so that d.c. supply fluctuations have little effect on the output duty cycle.

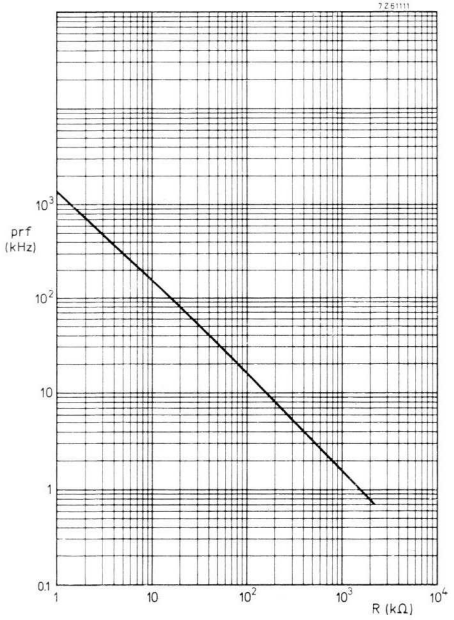


Fig.4-156 Pulse repetition frequency vs. capacitor charging resistor R ($R_1 + R_2$ in Fig.4-154) for C_1 equal to 1,5 μF.

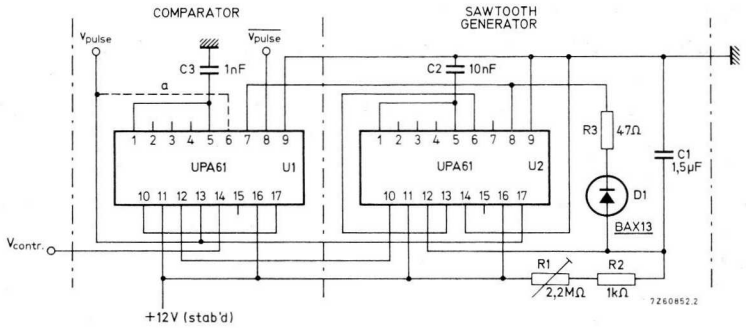


Fig.4-157 Wiring diagram of rectangular-wave generator.

4.9.2 Direct current transformer

As in the case of alternating current transformers, direct current transformers measure d.c. busbar currents whilst providing isolation between the power circuit and measuring circuit. Their principle of operation is well known[22]). This section discusses two circuit versions for feeding a direct current transformer, one being supplied from a negative d.c. source and providing a negative output, the other being fed from a positive d.c. source and yielding a positive output signal.

The circuits use the DCT61 (Section 2.9) which can withstand 5 kV test voltage. Sampling frequency is 5 kHz. Input response times are 1,4 ms (leading edge) and 0,5 ms (trailing edge). Output ripple is 10% and output impedance 1 kΩ; output load resistance should not be less than 10 kΩ. When using one primary turn (one lead passing through the DCT61-aperture) circuit performance is as given by the curves. A smaller current range is obtained by using more primary turns; for instance, 10 primary turns decrease the 0 to 120 A current range to a range of 0 to 12 A.

[22]) S.E. Tweedy, Electronic Engng. Feb.'48, p.38 – Magnetic Amplifiers.

Direct current transformer using negative supply source[23]). Fig.4-158 shows the circuit diagram together with the most important waveforms. The UPA61 functions as a high-power 5 kHz pulse source (Section 2.4.4) supplying negative pulses to the DCT61. The output pulses across R_2 R_3 D_3, whose amplitude is proportional to the d.c. input current I_{in}, are rectified by D_2 and the resultant signal is smoothed by C_2. Network R_3 D_3 is connected in series with R_2, to compensate for the forward voltage across D_2, this voltage drop becoming significant at a low input current. As a result, the circuit performs linearly even when the d.c. input current is very low. Performance is seen from Fig.4-159; clearly, deviation from linearity will occur at a high input current (exceeding 100 A) because the output signal is limited by the d.c. supply voltage. Fig.4-160 shows circuit response to a 50 Hz phase-controlled input current, and Fig.4-161 illustrates the circuit lay-out.

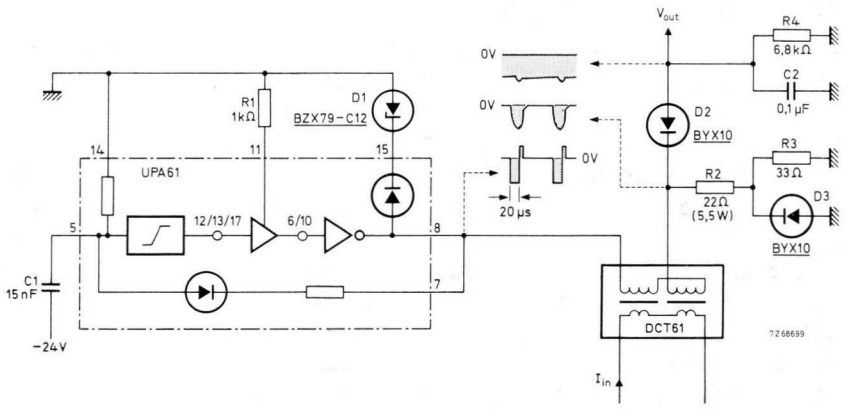


Fig.4-158 Direct current transformer using negative supply source.

[23]) AN No. 133, ordering code 9399 260 63301 – D.C. Current Transformer.

Fig.4-159 Performance of direct current transformer using negative supply source.

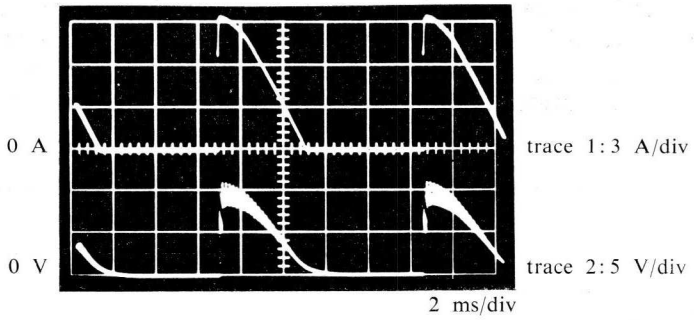


Fig.4-160 Circuit response to phase-controlled current. Trace 1: input current (90° trigger angle), Trace 2: output voltage.

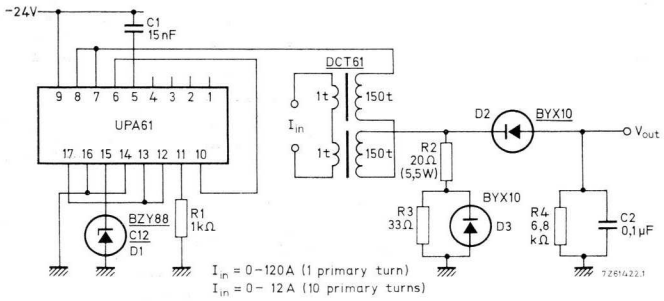


Fig.4-161 Wiring diagram of direct current transformer using negative supply source.

Direct current transformer using positive supply source. The circuit of Fig.4-162 functions in much the same way as that discussed previously (see the waveforms). It uses the 2.IA60 (connected as a Schmitt trigger) and the GLD60 grounded load driver. Fig.4-163 illustrates a circuit variant having a high sensitivity for low input currents. Fig.4-164 shows the performance of both circuits, and Fig.4-165 illustrates the wiring diagram.

The operation of the circuit variant is as follows (ref. Figs. 4-163 and 4-164). For low I_{in}-values, D_6 does not avalanche, and the increase of V_{out} with I_{in} is determined by the sum of R_6, R_8 and R_9. At a given value of I_{in}, D_6 avalanches, and any further increase of V_{out} depends on the much lower resistance of R_6. Consequently, the initial slope of the V_{out}-plot is very steep allowing the circuit to detect very small input currents. This is of importance in the twin bridge regenerative d.c. motor control system described in Section 4.7.4, where bridge

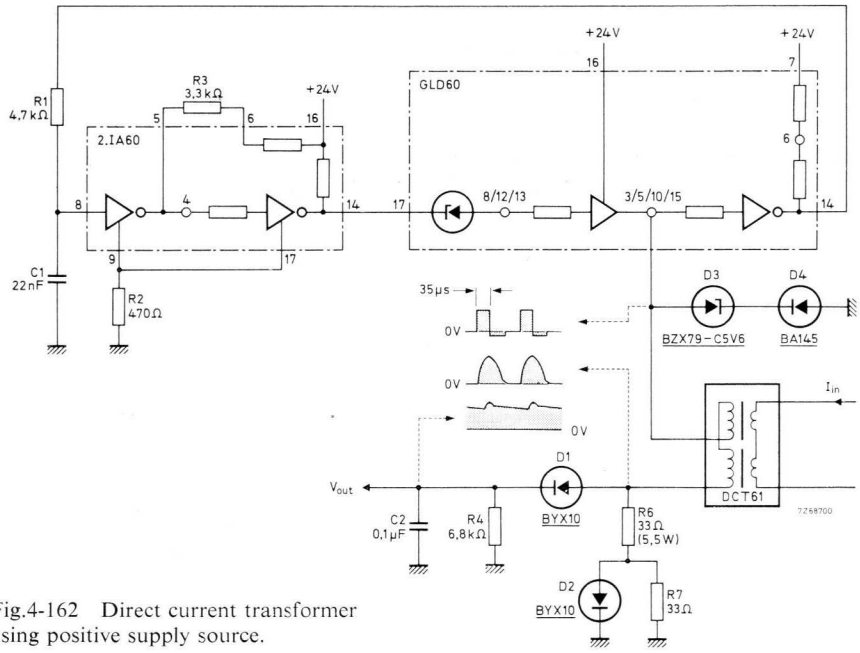


Fig.4-162 Direct current transformer using positive supply source.

switching should occur at zero armature current. The "height" of the bend in the plot of Fig.4-164 is about equal to the avalanche voltage of D_6.

Adjustment (Fig.4-163):

Set R_9 so that, without d.c. input current, the output voltage V_{out} is 0,1 V.

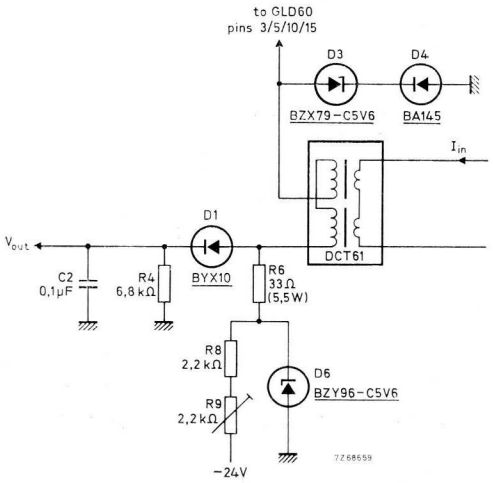


Fig.4-163 Circuit variant for detecting low direct currents.

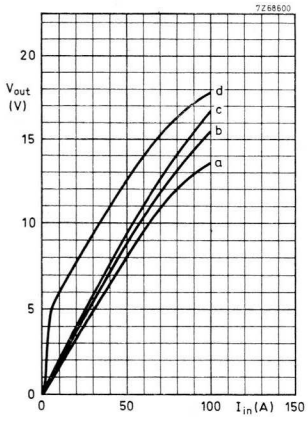


Fig.4-164 Performance of direct current transformer using positive supply source. Curve *a*: 20 V d.c. supply voltage, curve *b*: 24 V d.c. supply voltage, curve *c*: 28 V direct supply voltage, curve *d*: circuit variant according to Fig.4-163.

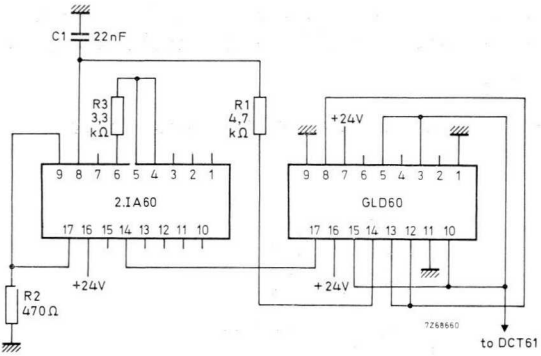


Fig.4-165 Wiring diagram of direct current transformer using positive supply source. The connection to pins 3/5/10/15 of GLD60 is shown in Fig.4-162 or 4-163.

4.9.3 D.C. VOLTAGE TRANSFORMER [24])

The d.c. voltage transformer described here contains a 20 kHz oscillator whose d.c. supply is the measured voltage. There is excellent linearity between the latter and the a.c. oscillator output. The measured voltage should be rectified, if necessary, so that it is always positive.

In the circuit of Fig.4-166, the 2.IA60 is connected as a Hartley oscillator operating at 20 kHz, and supplied from the measured voltage V_{in} through divider network R_1 to R_4. Voltage dependent resistor R_4 ensures good circuit performance over a large range of input voltage V_{in}. The oscillator input is effectively protected against reverse voltage by a safeguarding transistor whose base-emitter input is connected in anti-parallel with that of the oscillator transistor. The waveforms in Fig.4-166 illustrate circuit operation for a full-wave rectified input. The modulated 20 kHz output is rectified by the DOA61. (Because of D_1, the DOA61 output at pin 14 cannot become negative.) Network D_3 R_8 C_3 is a detector circuit, so that V_{out} is the envelope of the DOA61 output; this envelope is the replica of V_{in}.

Fig.4-167 shows circuit performance. Linearity is 1 % over a 20 V to 600 V input voltage range. The lay-out is shown in Fig.4-168. (Note the connection of the TT60.) The test voltage of the TT60 is 5 kV.

[24]) AN No. 136, ordering code 9399 260 63601 – D.C. Voltage Transformer.

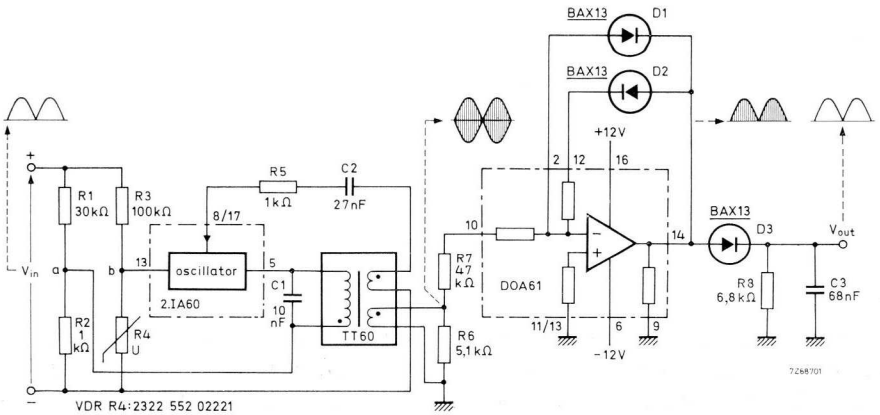


Fig.4-166 D.C. voltage transformer with waveforms (full-wave rectified input).

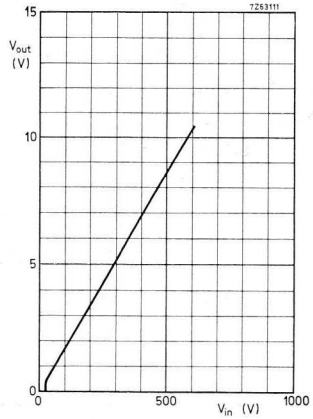


Fig.4-167 Performance of d.c. voltage transformer.

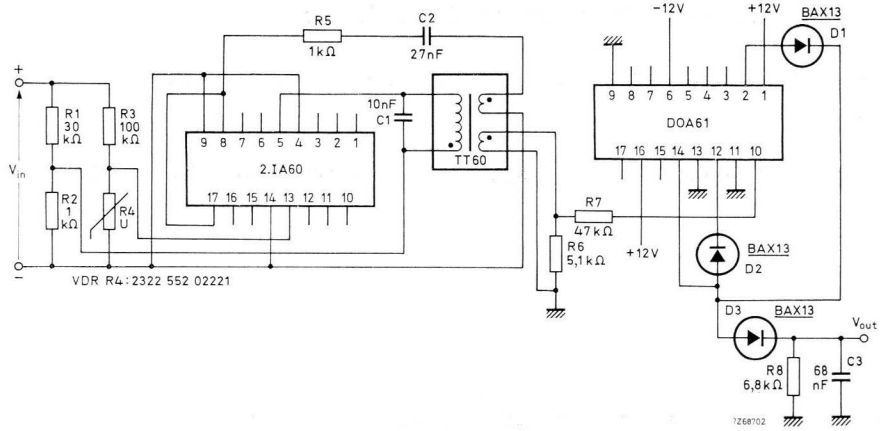


Fig.4-168 Wiring diagram of d.c. voltage transformer.

4.9.4 2 kHz SHIFT REGISTER[25])

The shift register described here needs only two external components per bit cell and four components for the drive circuit. Shift register input drive required is 2 D.U. (Section 2.2) and output capability is 8 D.U. The drive circuit needs 1 D.U. input drive (clock pulses) and is capable of driving up to 100 bit cells. The circuit is suitable for a frequency range from 0 Hz to over 2 kHz.

Shift register. Figs.4-169 and 4-170 show the two-phase shift register circuit and its waveforms; the circuit is based on the charge storage principle. Each bit cell consists of a 2.NOR61 NORbit and the NOR gates in the circuit block are connected to function as a bistable memory element. Input diodes D_{1a} D_{1b} improve noise immunity. Circuit operation is as follows.

Phase 1: During the interval between pulses, the "lock" input is HIGH, diode D_{2a} blocks, and the memory contents (Q-output) of the first bit cell is stored on C_{1a}. If Q is at "1", C_{1a} is charged via D_{3a}; if Q is at "0", C_{1a} discharges via D_{4a} ("shift" input LOW).

Phase 2: The next shift pulse causes the "shift" input to assume HIGH level. Diode D_{4a} blocks, so the data stored in C_{1a} is transferred to the memory element of the second bit cell upon cessation of the reset pulse. Diode D_{3a} prevents the capacitor discharging via the "lock" input.

Phase 1: The data shifted to the memory element of the second bit cell is stored on C_{1b}.

Phase 2: The data stored on C_{1b} sets the memory element of the third bit cell, etc.

[25]) AN No. 128, ordering code 9399 260 62801 – 2 kHz Shift Register.
AN No. 193, ordering code 9399 260 69301 – Silo Register.

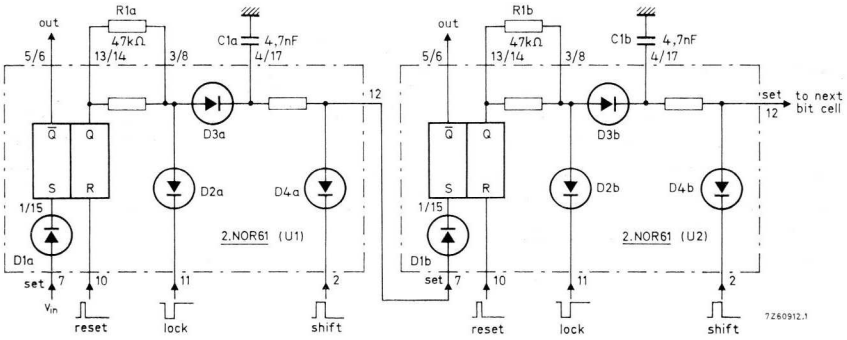


Fig.4-169 2 kHz shift register circuit diagram (two bit cells shown).

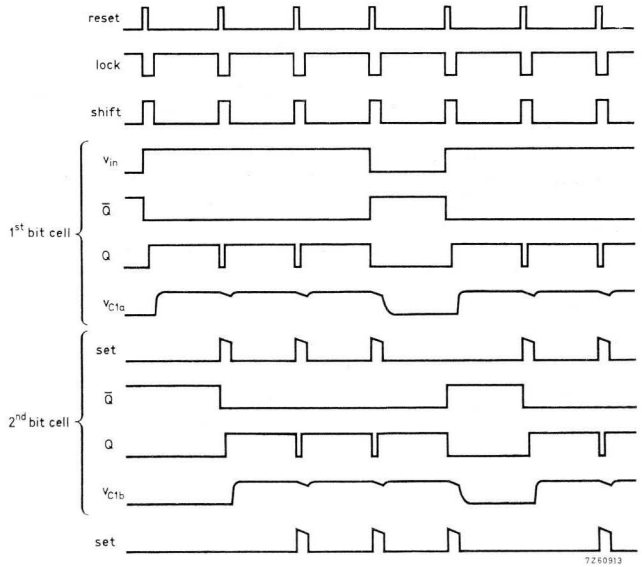


Fig.4-170 Shift register waveforms.

Drive circuit. The shift register drive circuit shown in Fig.4-171 should be clocked by positive pulses of at least 100 μs duration and 12 V amplitude. The waveforms are shown in Fig.4-172; low-speed clocking devices such as a mechanical switch do not upset circuit operation. Cascaded NOR gates *B* and *C* act as a bistable element that is set when amplifier *G* assumes HIGH level and is reset at the termination of a clock pulse when the output of amplifier *A* switches to HIGH level. The length of the lock and shift pulses is determined by C_{11} and that of the reset pulse depends on C_{12}.

Figs.4-173 and 4-174 show the lay-out of the shift register and its drive circuit.

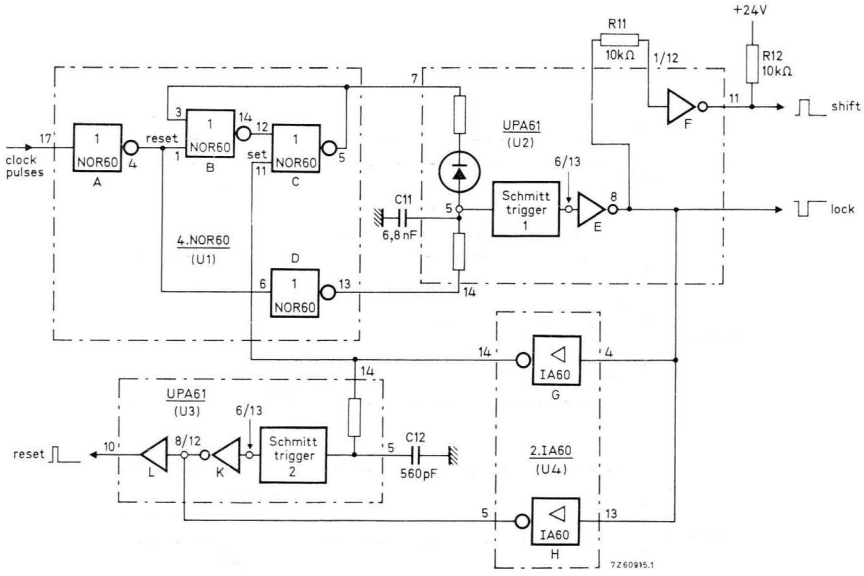


Fig.4-171 Drive circuit diagram.

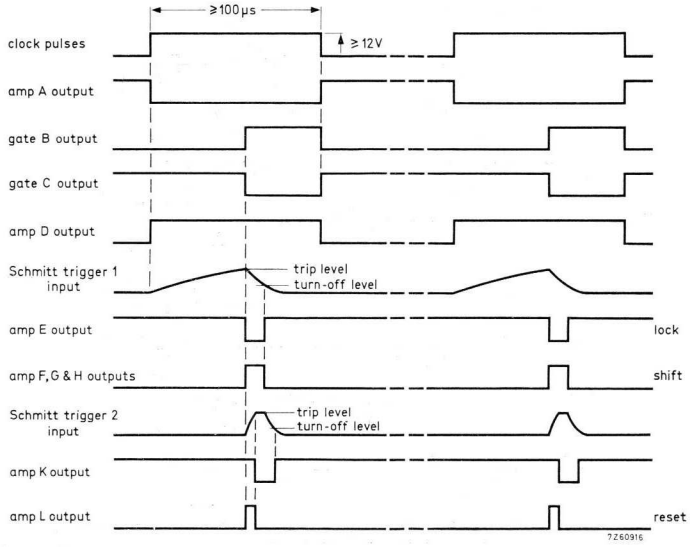


Fig.4-172 Drive circuit waveforms.

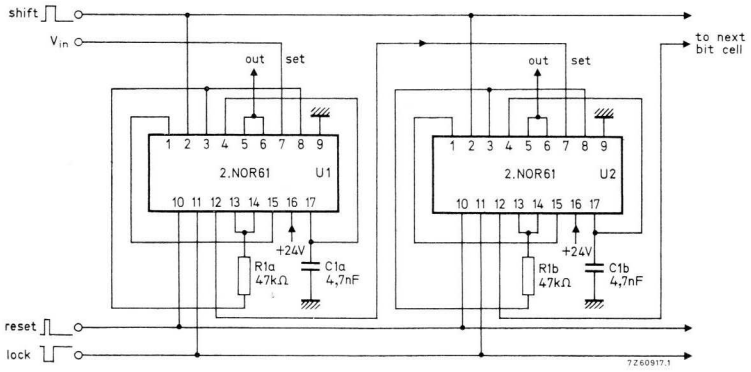


Fig.4-173 Shift register wiring diagram.

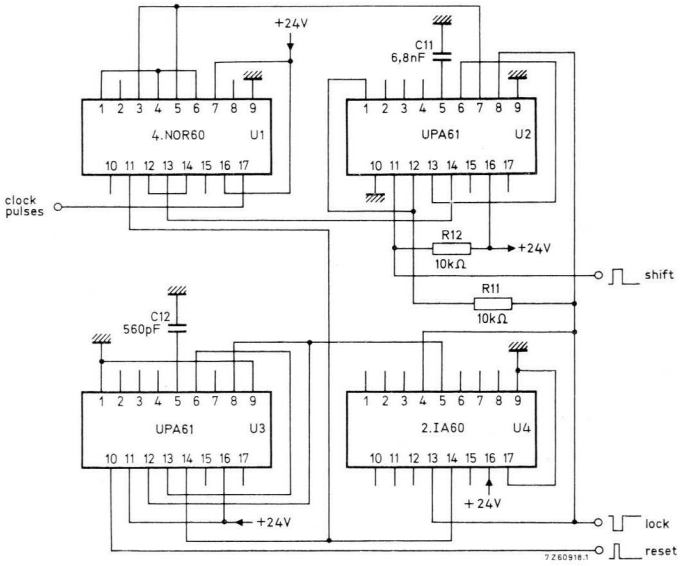


Fig.4-174 Drive circuit wiring diagram.

4.9.5 Scalers of two to eight[26])

Scalers, or dividers as they are often called, are indispensable in logic circuitry. The circuits described in this section employ the 2.NOR61 dual NOR gate as the bistable element (Section 2.8.7). The scaling factors are 2, 3, 4, 5, 6, 7 and 8. Higher scaling factors are obtained by cascading the circuits.

The normal technique for achieving scaling factors differing from a power of two is that a certain binary state is decoded to skip a number of steps. Because of the occurrence of a transitory state, a false pulse is produced. This shortcoming is avoided in the given circuits by the use of set and reset condition gates, which ensures that the condition dictated by the truth table is set *one step in advance*. Another advantage of the circuits is that few external components are needed, so that they can rapidly be assembled.

In all circuit diagrams, the outputs yielding the specified scaling factor are indicated by encircled lettering. Maximum operating frequency is 10 kHz.

Scaler of two. Fig.4-175 shows the 2.NOR61 connected as a bistable element, or scaler of two.

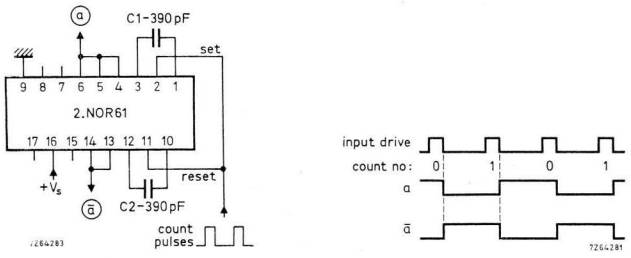


Fig.4-175 Scaler of two.

[26]) AI No. 462, ordering code 9399 264 46201 – Scalers of 2 to 8.

Scaler of three. The circuit of Fig.4-176 is a ring counter consisting of three single-transistor stages.

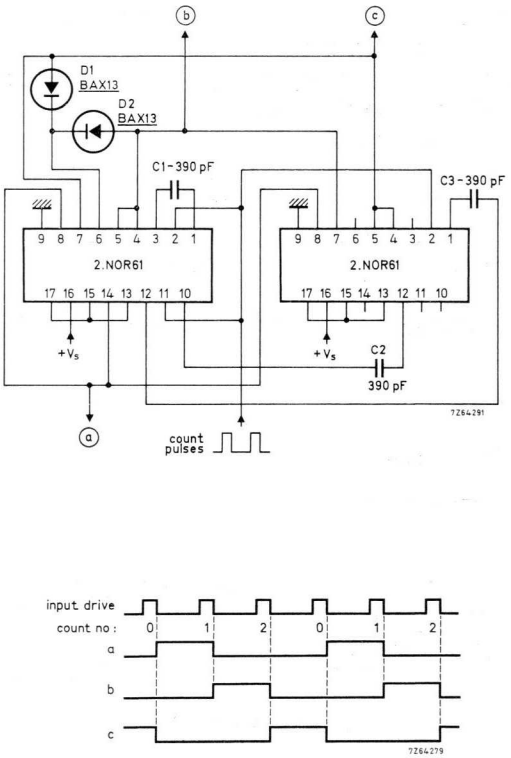
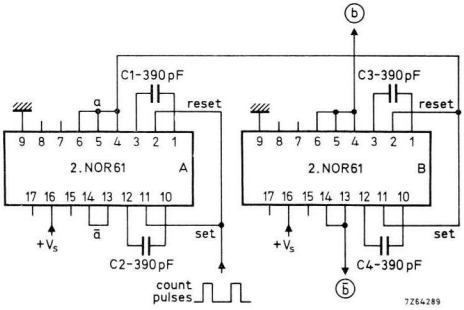


Fig.4-176 Scaler of three (ring counter).

Scaler of four. The circuit of Fig.4-177 is a ripple-through counter containing two of the basic bistable elements.



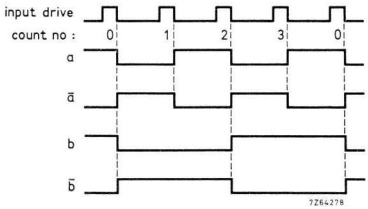


Fig.4-177 Scaler of four.

Scaler of five. A scaler of five can be built according to Fig.4-178. Only five out of the eight possible states are used. So, there are three illegitimate states, namely 101 (outputs *c*, *b* and *a* respectively), 110 and 111. However, after only one count pulse, the circuit reverts to a legitimate state because of the built-in set/reset conditions; the changes in response to the count input are: 101 – 010, 110 – 010, 111 – 000.

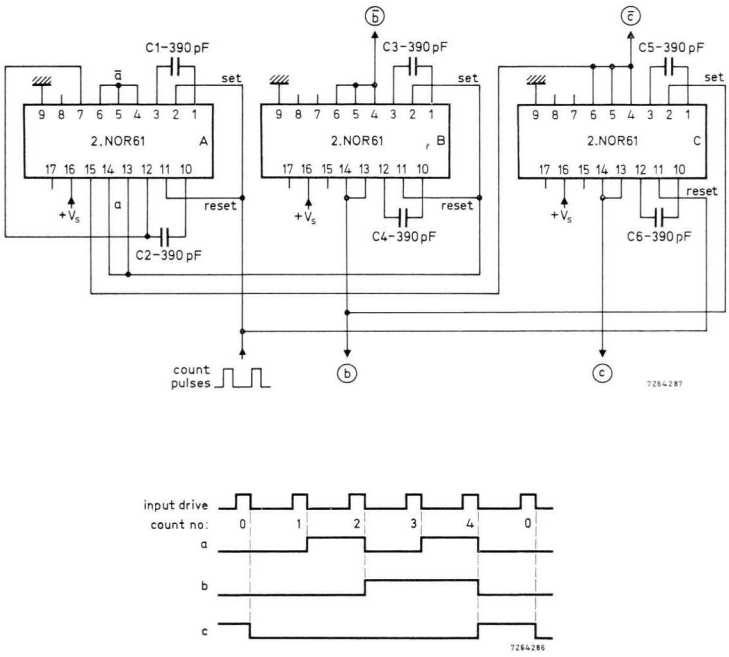


Fig.4-178 Scaler of five.

Scaler of six. The circuit of Fig.4-179 is ideal for a.c. motor speed control (by varying the count rate), as it produces an output pulse pattern comprising three square waves displaced over 120 °. The 2.NOR60 is required to prevent, by d.c. reset, infinite cycling between the two illegitimate states 010 and 101. Assuming state 010 to occur, the circuit proceeds to 101 in response to the count input. Because of d.c. reset, the scaler changes this state spontaneously to 111, which is a legitimate state.

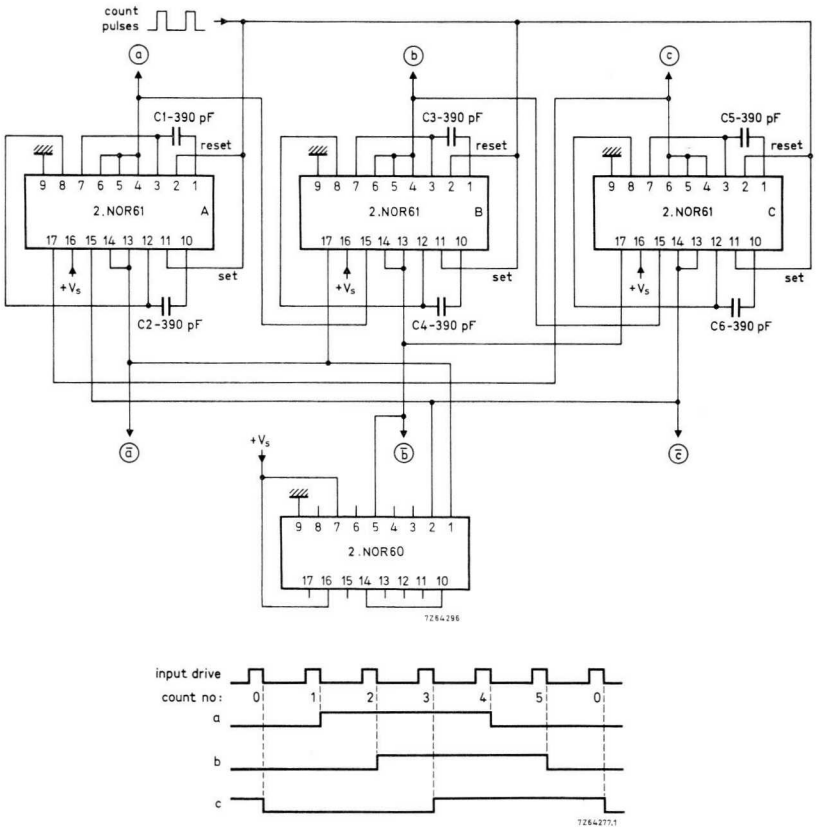
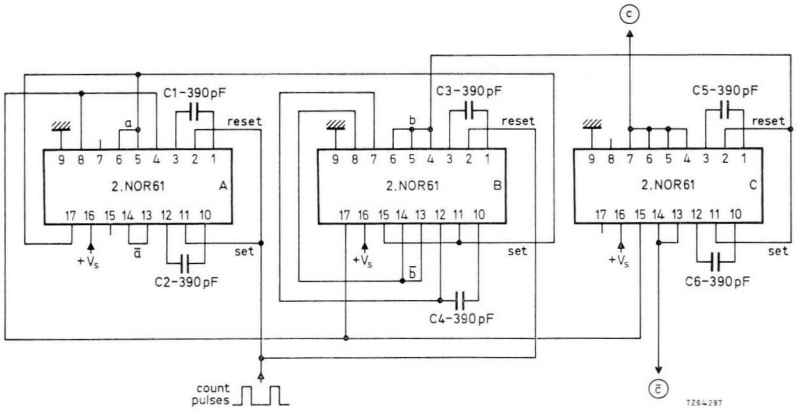


Fig.4-179 Scaler of six.

Scaler of seven. The scaler of seven (Fig.4-180) has one illegitimate state, namely 100. Owing to the incorporated set/reset conditions, this changes to 101 in response to the count input.



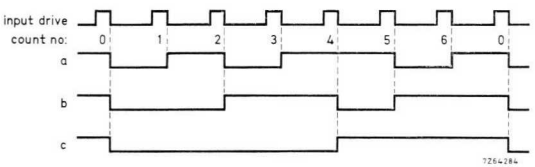
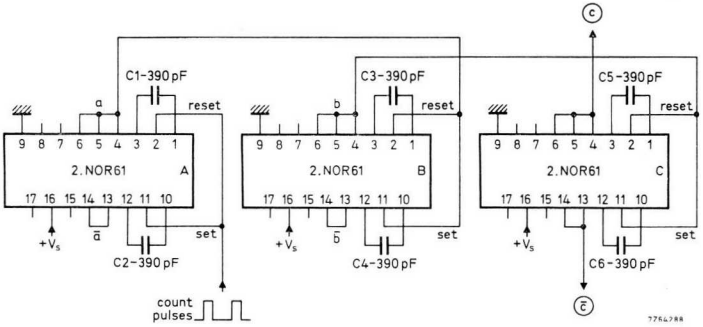


Fig.4-180 Scaler of seven.

Scaler of eight. Fig.4-181 shows the three-stage ripple-through binary counter, or scaler of eight.



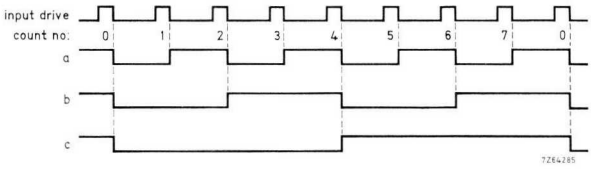


Fig.4-181 Scaler of eight.

5 Mounting accessories, chassis and input devices

This chapter discusses accessories, chassis, input devices (detectors), and d.c. supplies for NORbits*. For full specifications, consult the Data Handbook System, Components and Materials.

5.1 Mounting accessories

For the NORbits to be universally applicable, a number of mounting accessories is available. NORbits can be mounted according to any of the following methods:

- using a metal strip (Fig.5-1)
- using breadboard blocks BB60 (Section 5.1.1)
- using the universal mounting chassis UMC60 (Section 5.1.2)
- using a printed-wiring board (Section 5.1.3).

To allow fast preparation of system drawings and wiring lay-outs, stickers for drawing symbols and NORbit diagrams are available.

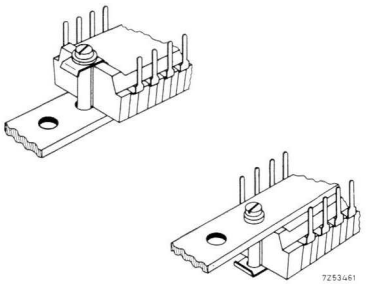


Fig.5-1 Strip-mounting of NORbits.

5.1.1 BREADBOARD BLOCK BB60

The breadboard block BB60, cat. no. 9390 198 00002, is ideal as a design aid, for experimenting or for teaching. Fig.5-2 gives the dimensions of the BB60. On one side, a size A NORbit block is soldered and, after the required number of BB60s has been dove-tailed together, connections are made by hook-up wiring plugged into silver-plated, cup-shaped contacts at the other side; for accommodating external components, there are two contacts for each NORbit

* 60- and 61-series circuit blocks.

terminal. To simplify terminal location, stickers (delivered with the breadboard blocks) are stuck on to the blank area at the component side of the BB60. A large breadboard containing extensive logic circuitry can be rapidly and easily assembled in the described manner; see Fig.5-3. Six BB60s can be housed in one UMC60 universal mounting chassis.

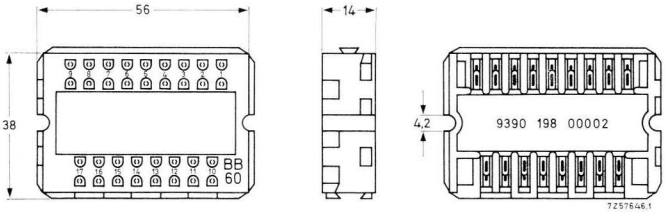


Fig.5-2 BB60 dimensions. Left: wiring side; right: NORbit side.

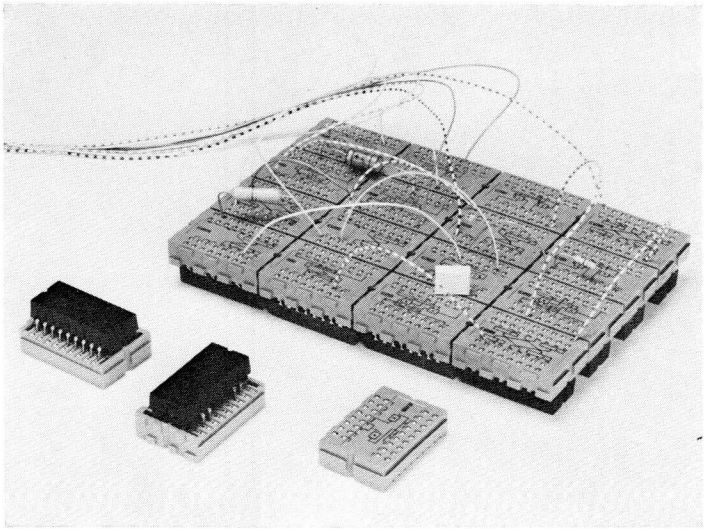


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Fig.5-3 Using the BB60.

5.1.2 Universal mounting chassis UMC60

The UMC60 universal mounting chassis, cat. no. 4322 026 38330 is comprised of a moulded polycarbonate body capable of housing up to six NORbits (Fig.5-4), the parts needed to clamp the NORbits into place and twenty 0,25 inch Faston tabs. The connections to the circuit blocks and the tabs can be made by soldering or wire wrapping.

The UMC60 is mounted as shown in Fig.5-5*a* to *e*.

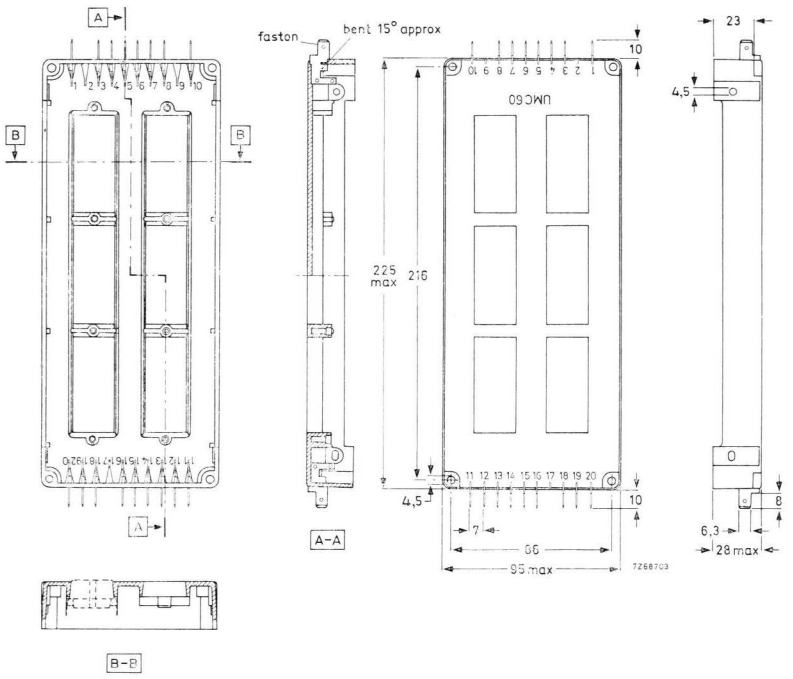

Fig.5-4 UMC60 dimensions.

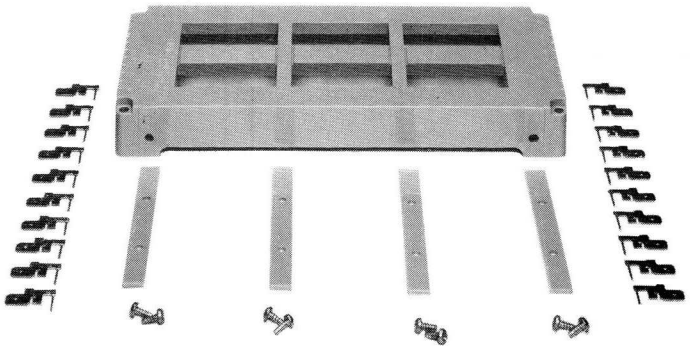

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Fig.5-5a UMC60 components (cat. no. 4322 026 38330).

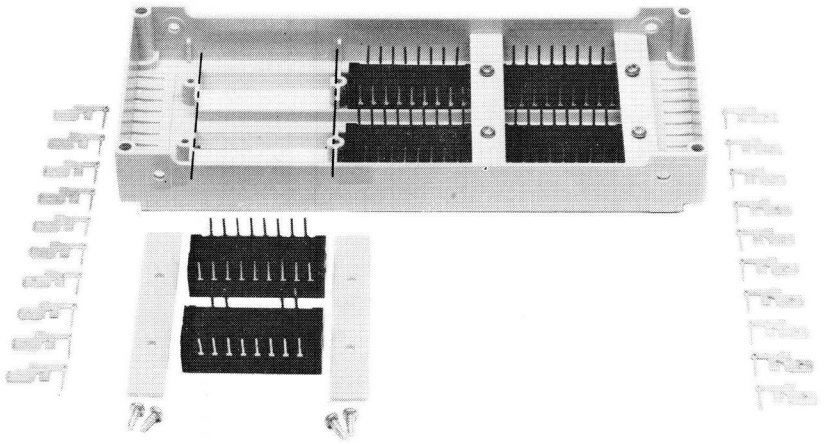

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Fig.5-5b Clamp NORbits in rectangular apertures with moulded polycarbonate strips and self-tapping screws. To fit the HPA60 (size B block), remove the material between apertures as indicated by the dotted lines.

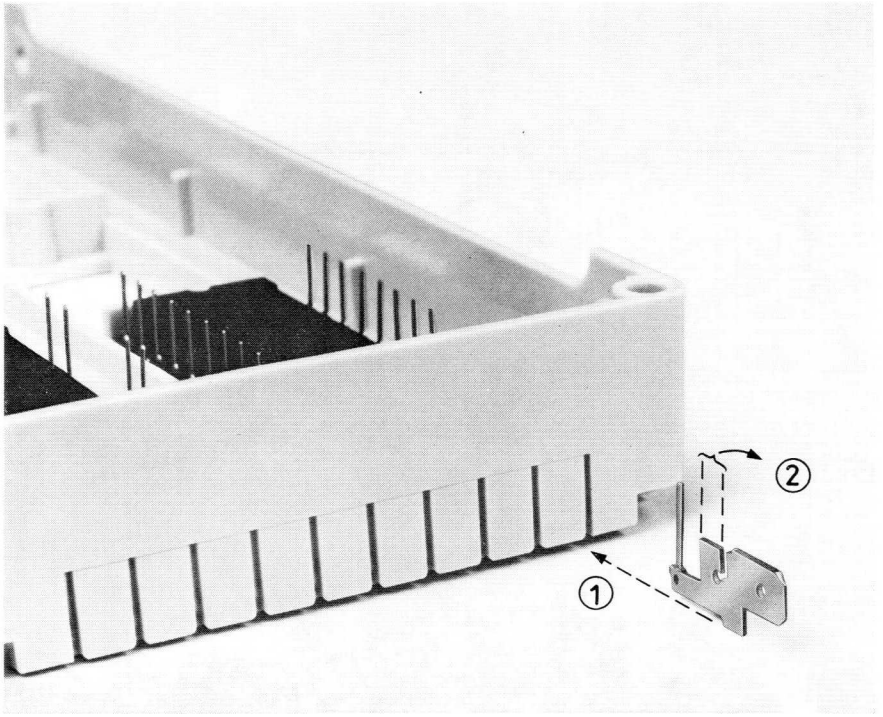

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Fig.5-5c (1) Insert Faston through slotted hole in chassis (2) then fix by bending slotted part 15° in indicated direction.

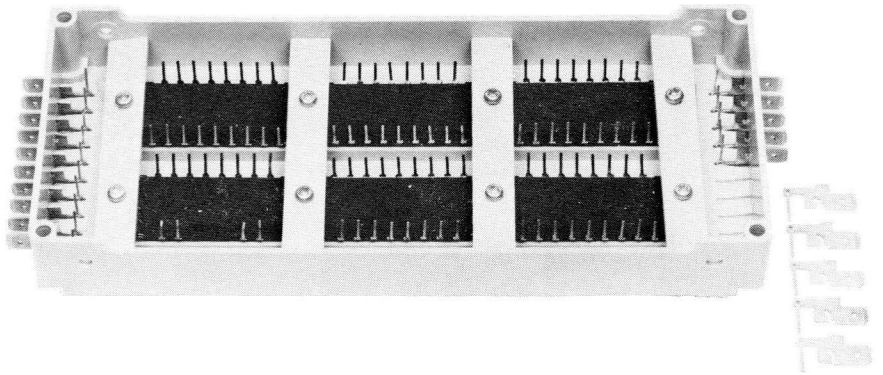

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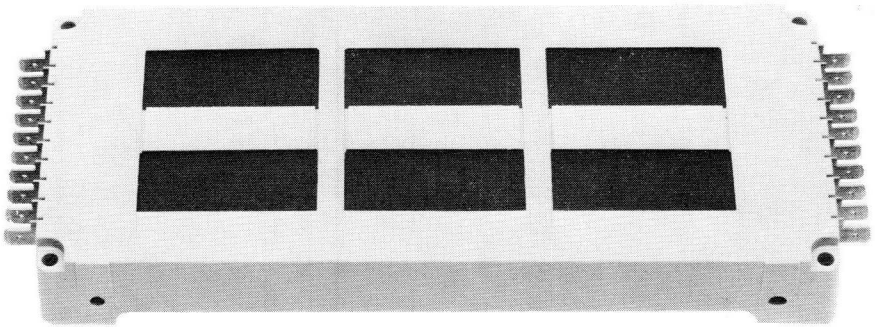
Fig.5-5d UMC60 with NORbits and some Fastons fitted.



720928-09-04

Fig.5-5e Assembled unit.

The circuit blocks can be clamped in the UMC60 (Fig.5-5*e*). Alternatively, they can be soldered on to the PWB63 printed-wiring board (Section 5.1.3) and the latter mounted in the UMC60 chassis (Fig.5-6). A third method is using the BB60 breadboard block (Fig.5-7).

Two or more UMC60 chassis can be bolted together side by side (Fig.5-8), or stacked (Fig.5-9); the hinged construction (Fig.5-10) allows easy inspection and maintenance.

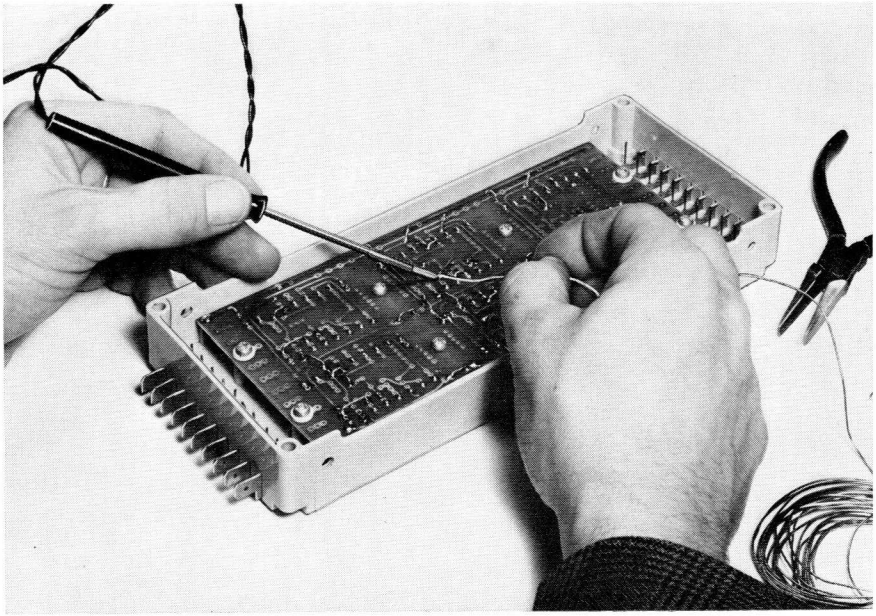


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Fig.5-6 Use of PWB63 printed-wiring board.

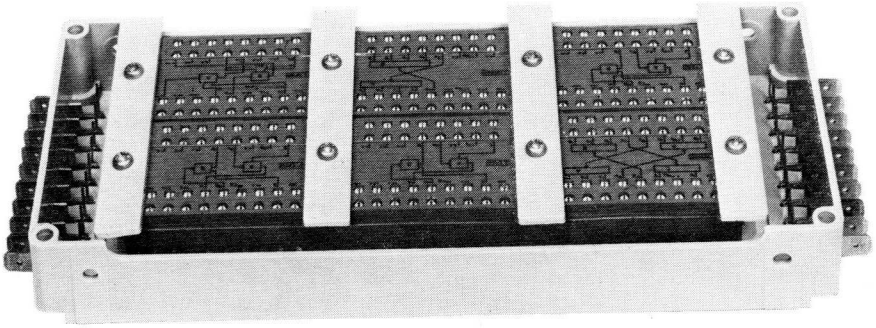

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Fig.5-7 Use of BB60 breadboard blocks.

Fig.5-8 UMC60s bolted together side by side.

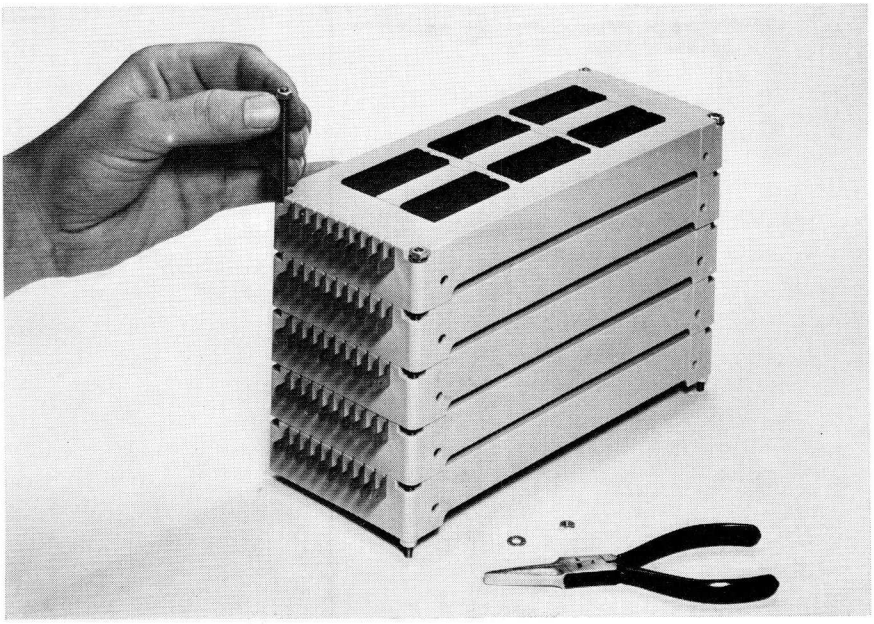

Fig.5-9 Stacked UMC60s.

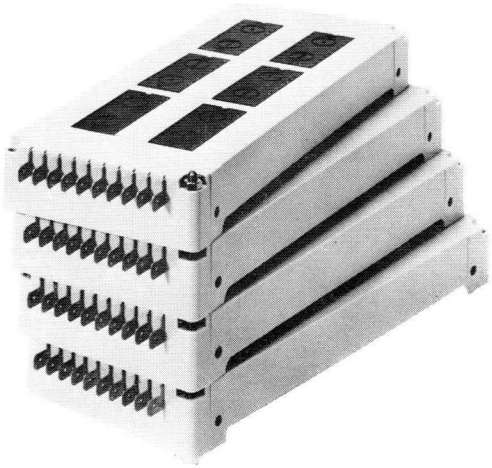

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Fig.5-10 Hinged UMC60s.

5.1.3 Printed-wiring boards

Printed-wiring boards are ideal for quantity production, all connections being made in "one go" by dip-soldering. Further, servicing is greatly simplified if each board performs a single function; it is then an easy matter to pinpoint a faulty board for replacement.

The board material may be either phenol paper (addition .../P to the type number) or glass epoxy. The latter is more expensive but it is the most suitable material in humid atmospheres because it has high insulation resistance.

Where several boards are stacked together, a chassis should be used (Section 5.2). Board/chassis/connector compatibility follows from Table 5-1; this table also specifies catalogue numbers.

Amongst the circuit boards discussed here, the GPB60, PWB60 and PWB61 are intended for general applications; the user would normally design his own printed-wiring lay-out for intricate circuitry.

Table 5-1. Board/chassis/connector compatibility.

board			chassis		connector		
type no.*	cat. No.	size A NORbits per board	cat. No.	boards per chassis	no. of contacts per connector	type No.	cat. No.
GBP60/P	4322 026 38610	10	4322 026 38240	21	2 × 23 0,2 inch pitch	FO45 or FO45+	2422 020 52591
GPB60	4322 026 38600						2422 035 52591
PWB60/P	4322 026 38800	10	4322 026 38230	21	2 × 22 0,156 inch pitch	FO47, FO50 or FO53+	2422 037 62212 2422 037 12212
PWB60	4322 026 38790						2422 039 12212
PWB61/P	4322 026 38820	10	4322 026 38240	21	2 × 23 0,2 inch pitch	FO45 or FO45+	2422 020 52591
PWB61	4322 026 38810						2422 035 52591
PWB62	4322 026 38780	4	4322 026 38250	20	2 × 32 0,1 inch pitch	connector delivered with board.	FO54
PWB63	4322 026 73750	6	4322 026 38330 (UMC60)	1	—	—	—

* Boards with type numbers ending in P are of phenol paper; all others consist of glass epoxy.
\+ Modified wrap (last turn of wrap consisting of insulated wire for greater mechanical strength).

Printed-wiring board (General Purpose Board) GPB60

Fig.5-11 illustrates the GPB60 printed-wiring board with extractor and locking mechanism. The latter locks the board in position after insertion in the chassis. For full occupation (ten NORbits) the circuit blocks must be located as shown, that is, the blocks together with any components should be mounted on the *track* side of the board and in such a way that pin 9 ("0 V" terminal) of a block is inserted into the innermost track ("0 V" track). Both inner tracks must be paralleled to reduce parasitic impedance.

The pads on the boards facilitate interconnection (Fig.5-13). The use of polarizing keys prevents boards being mounted in the wrong place.

Components are mounted in holes not occupied by the circuit blocks.

Printed-wiring boards PWB60 and PWB61

In contrast to the GPB60, the printed-wiring boards PWB60 and PWB61 are partly pre-wired, to reduce assembly time.

The PWB60 and PWB61 have the same wiring pattern but they have been designed for different connectors. Fig.5-12 shows the PWB61.

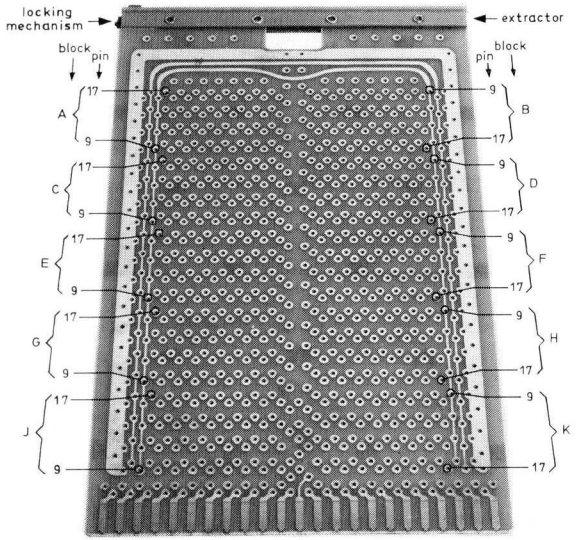
For full occupation (ten Norbits) the circuit blocks must be mounted according to Fig.5-12*a*.

One output of a 2.NOR60, 4.NOR60, 2.IA60 or 2.NOR61 is brought out by tracks connecting pad (pin) 5 of each position to an edge contact (contacts 4 to 8 and 18 to 22 in Fig.5-12*a*). If a UPA61 circuit block is used, the track to pad 5 should be cut, to prevent pick-up of interference by the sensitive Schmitt trigger input.

Double pads (Fig.5-12*a*) are provided at block positions A and B, which allows mounting of RC-networks for timers (TU60) if the latter are fitted in these positions.

Edge contacts 9 to 17 are connected through tracks to pads close to block positions A to D (Fig.5-12*a*), eliminating the need for making long connections from these positions to the board terminations.

Components are mounted in the holes between circuit blocks, supply being taken from the "+V" and "0 V" tracks. Block positions J and K have additional holes to accommodate components when these positions are not being used for circuit blocks. All components (and the blocks) should be mounted on the *track* side.



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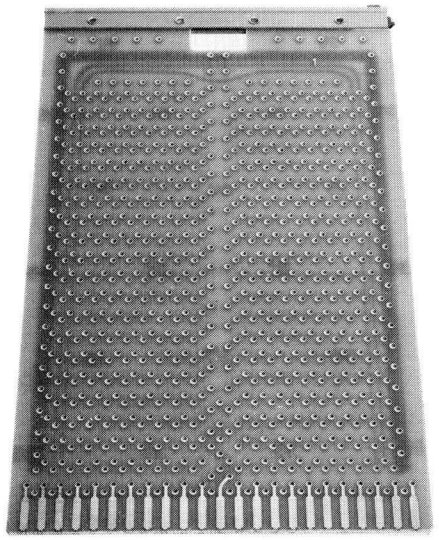
(a)



720907-05-05

(b)

Fig.5-11 GPB60: (a) track side (NORbit and component side), (b) pad side.

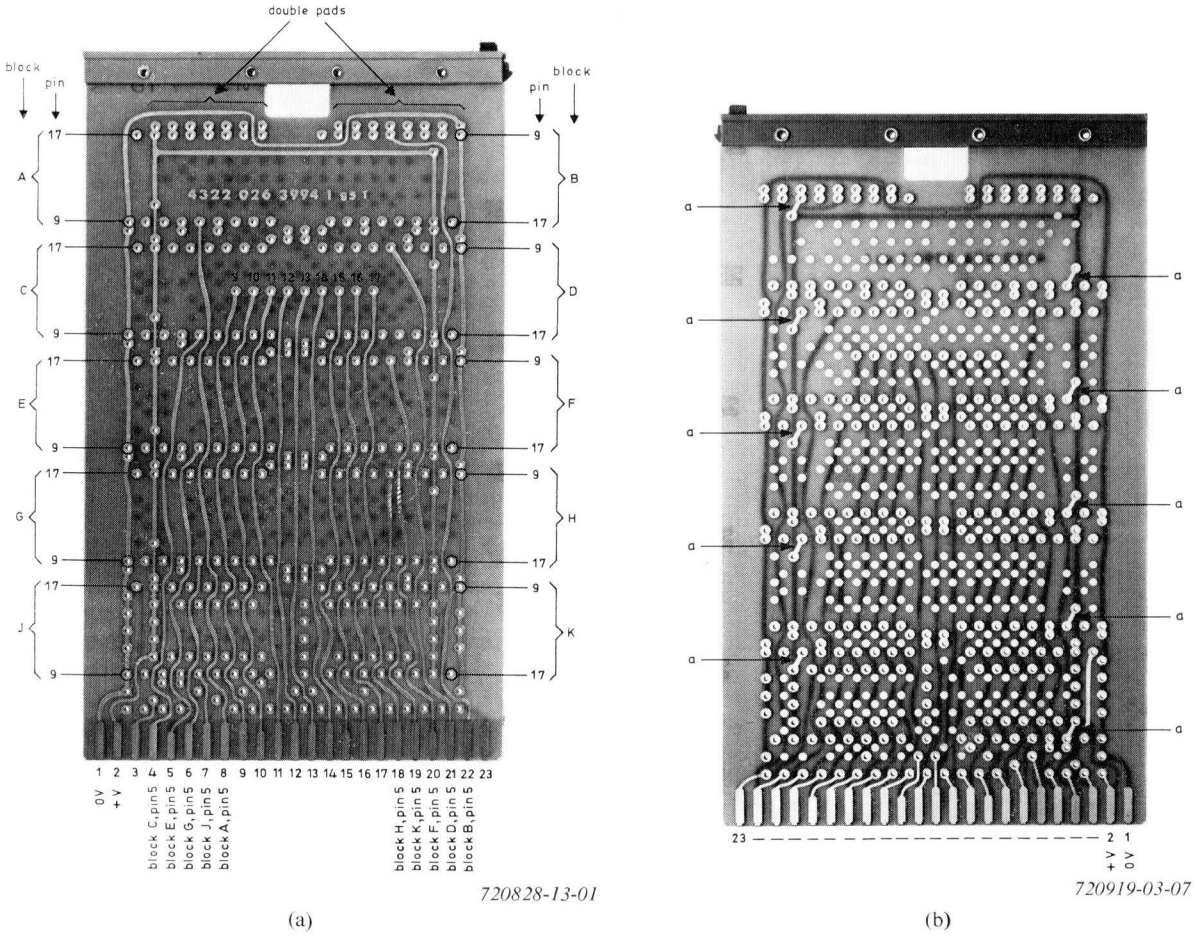


Fig.5-12 PWB61: (a) track side (NORbit and component side), (b) pad side.

As shown by connections *a* in Fig.5-12*b*, pad 7 of each block position is bridged to the "+V" track, so that both stages of a 2.NOR60 or all four stages of a 4.NOR60 receive d.c. supply voltage. The connection *a* should be cut when a 2.NOR60 is connected for wired-OR operation, or when 61-series NORbits are being used.

The pads ease interconnecting (Fig.5-13) which is carried out with 0,2 mm diameter bare copper wire. Insulation is used where pads or tracks must be crossed, resin-bonded fibre tubing (systoflex) being preferred to teflon tubing since the former can withstand greater mechanical stresses due to, for instance, sharp edges.

Polarizing keys prevent boards being inserted in the wrong place.

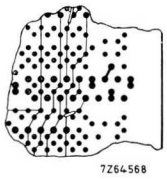


Fig.5-13 Interconnection via pads.

Miniature printed-wiring board PWB62

The PWB62 miniature printed-wiring board can accommodate four circuit blocks. All terminals of each block are brought out to the female connector ("terminal logic") and the connections between blocks are made on the pins of the mating connector, *not* on the board itself. In this way, wiring instructions are greatly simplified.

Fig.5-14 shows the outline of the PWB62 without connector. The encircled numbers (Fig.5-14*a*), refer to the pin numbering of the circuit blocks and indicate how the blocks (positions A to D) must be located. Connector pin numbering is shown by the numbers at the bottom. The PWB62 is delivered complete with male and female connectors type FO54, the female connector being already soldered in position: see Fig.5-15. As shown in the photograph of Fig.5-15*b*, the connector has bevelled edges so that the board cannot be mounted in the reversed position.

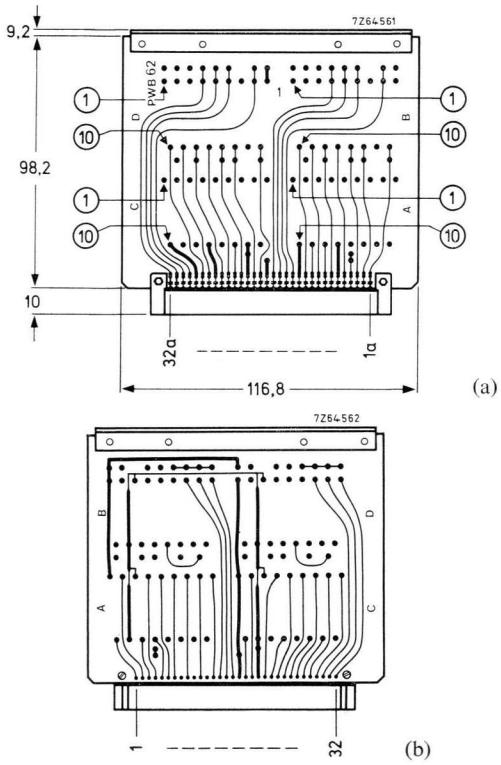


Fig.5-14 PWB62: (a) type number side (NORbit and component side), (b) non-type number side. Encircled numbers denote location of pins.

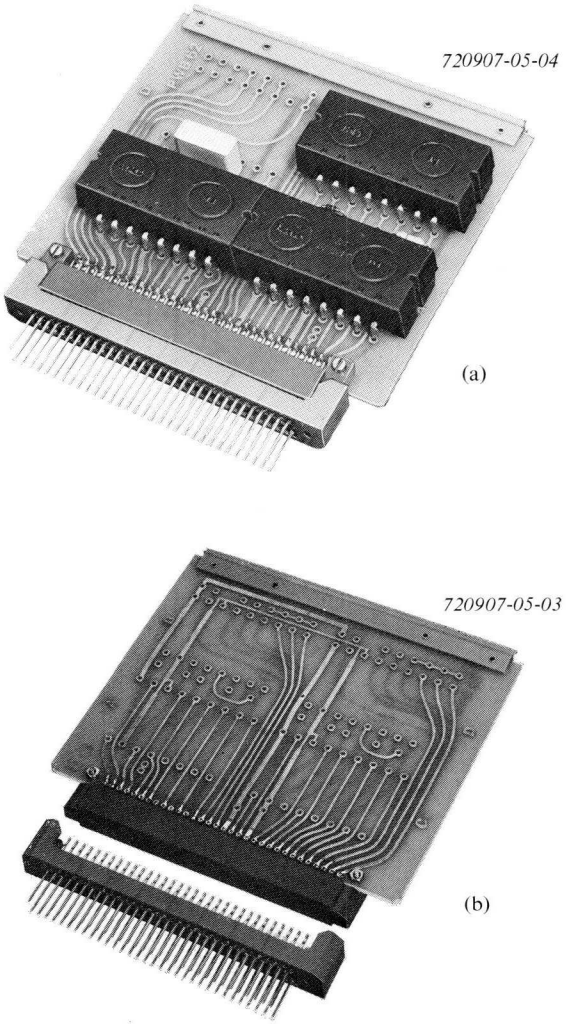


Fig.5-15 Showing both sides of assembled PWB62: (a) type number side, (b) non-type number side.

As an example of use, Fig.5-16 gives the completed PWB62 interconnection diagram for an alarm circuit. The vertical lines give the board connections (for instance, connector pin 13 on the non type-number side – ref. Fig.5-14 – connected to pin 1 of the circuit block in position A). The electronic circuit is drawn in the upper part of Fig.5-16, and the connections to be made between the pins of the male connector are shown by the horizontal lines (for instance, pin 10*a* on the type-number side to be interconnected with pin 5 on the non type-number side and pin 9*a* on the type-number side). The bottom of the interconnection diagram shows the outgoing connections.

An advantage of this system is that electronic circuitry and wiring lay-out are combined in one diagram, so that instructions are clear and only little time is required for preparation.

Connections are made by soldering or wire-wrapping; the latter technique can be used by unskilled labour to achieve higher reliability than obtainable with soldering (which requires semi-skilled labour).

Complete systems can be built from a few standard panels (PWB62 with circuit blocks), thus simplifying stock keeping and maintenance.

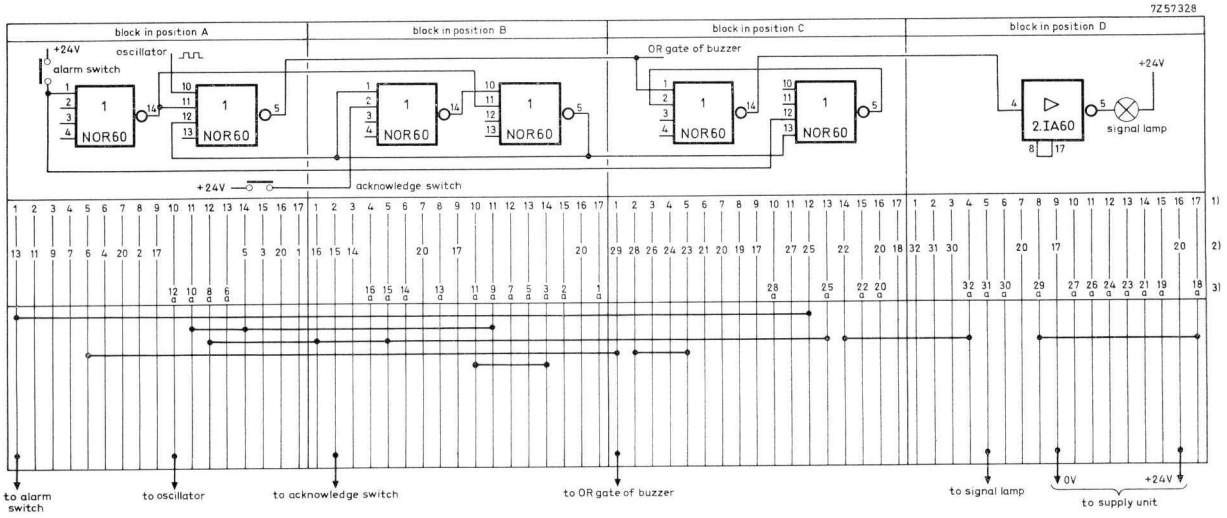


Fig.5-16 An example of a completed PWB62 interconnection diagram: (1) circuit block numbering, (2) numbering of pins connected to non type-number side of PWB62, (3) numbering of pins connected to type-number side of PWB62 (compare with Fig.5-14).

Printed-wiring board PWB63

The printed-wiring board PWB63, intended for mounting in the UMC60 (Section 5.1.2), is shown in Fig.5-17. It can carry six circuit blocks, positions A to F and simplifies mounting of components. The track pattern is such that interconnections are short (jumper connections). Interconnections and external components are located on the side shown in the figure; the circuit blocks are mounted on the other side.

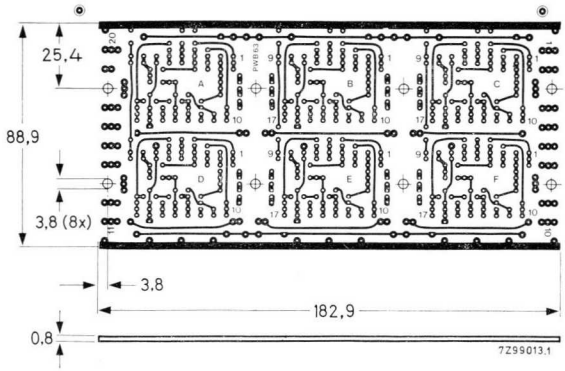


Fig.5-17 Track pattern and outline of PWB63. Pin numbers indicate positions of circuit blocks.

5.1.4 Stickers

Stickers are available to speed up the design of logic circuitry and wiring layouts. The stickers are supplied in sheets, each containing a set of drawing symbols or NORbit diagrams; these are printed on a self-adhesive, transparent base. Each sticker can be detached separately from the backing sheet, without cutting. The sheets are supplied in packets of fifty (ordering code 4322 026 71981 for the 61-series circuit blocks).

5.2 Chassis

The mounting chassis are intended for housing the printed-wiring boards with their components. Chassis/board/connector compatibility follows from Table 5-1. The boards are inserted in the chassis and mate with connectors at the rear for connection with other boards and external circuitry. All chassis are delivered in kit form with mounting instructions (connectors to be ordered separately); they suit the standard 19 inch rack.

5.2.1 Chassis 4322 026 38230 and 4322 026 38240

Chassis 4322 026 38230 is intended for FO47, FO50 or FO53 connectors, and chassis 4322 026 38240 for FO45 connectors. They accommodate a maximum of 21 printed-wiring boards. Fig.5-18 show an assembled chassis. Chassis construction is clear from Fig.5-19. Chassis material is anodized aluminium, weight is about 3 kg, and dimensions are 133 mm × 216 mm × 444 mm.

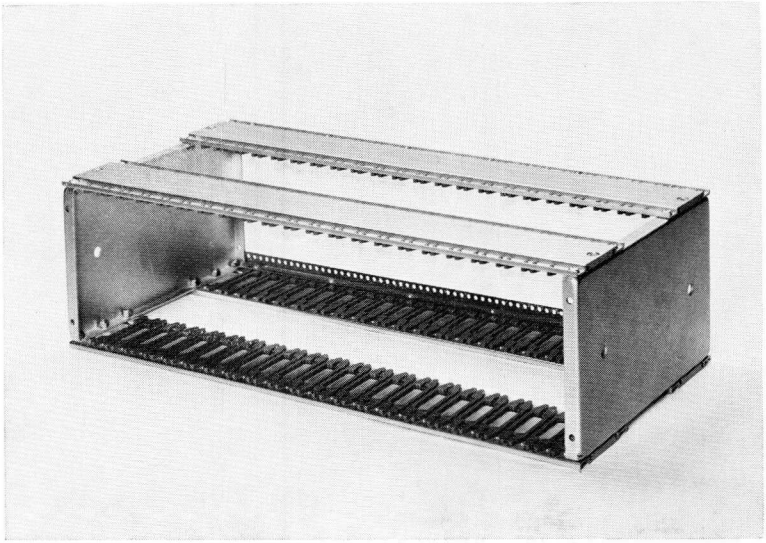


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Fig.5-18 Chassis 4322 026 38230 and 4322 026 38240.

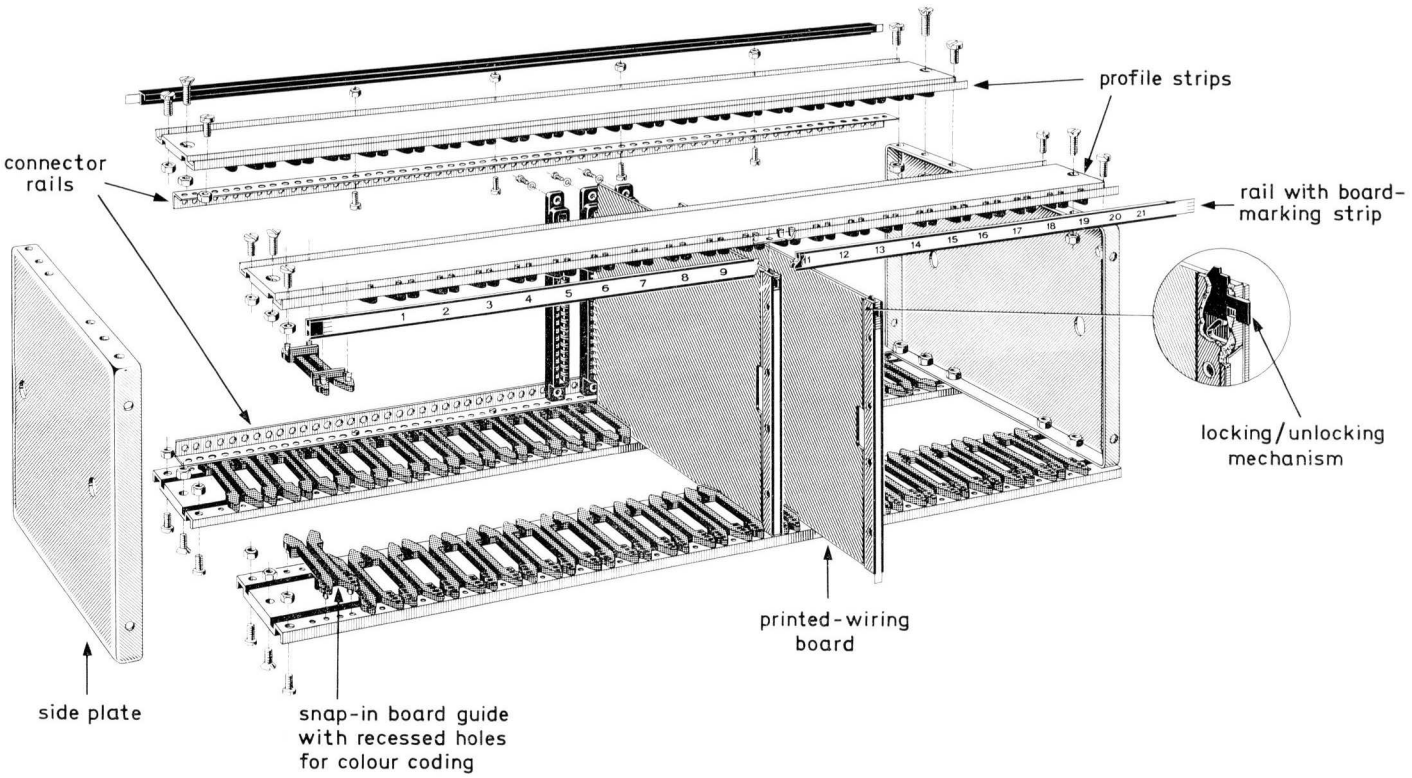
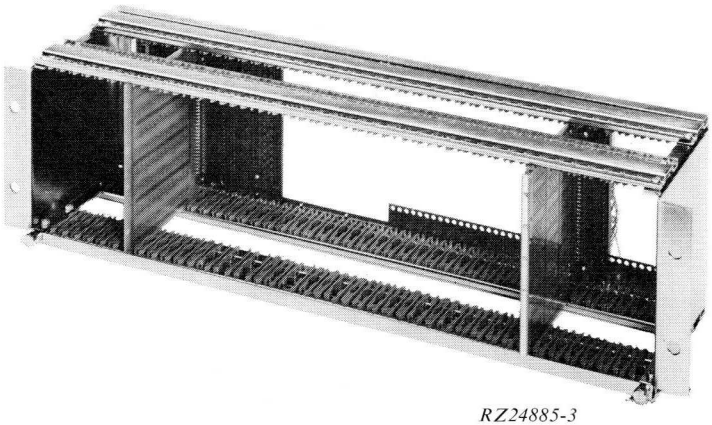


Fig.5-19 Exploded view of chassis 4322 026 38230 and 4322 026 38240.

5.2.2 Miniature chassis 4322 026 38250

The 4322 026 38250 miniature chassis accepts up to 20 printed-wiring boards PWB62. Fig.5-20 gives a general picture of the chassis and Fig.5-21 is an exploded view. Chassis material is nickel-chromium plated steel, weight is 2 kg approximately, and dimensions are 130 mm × 123 mm × 444 mm.



RZ24885-3

Fig.5-20 Miniature chassis 4322 026 38250.

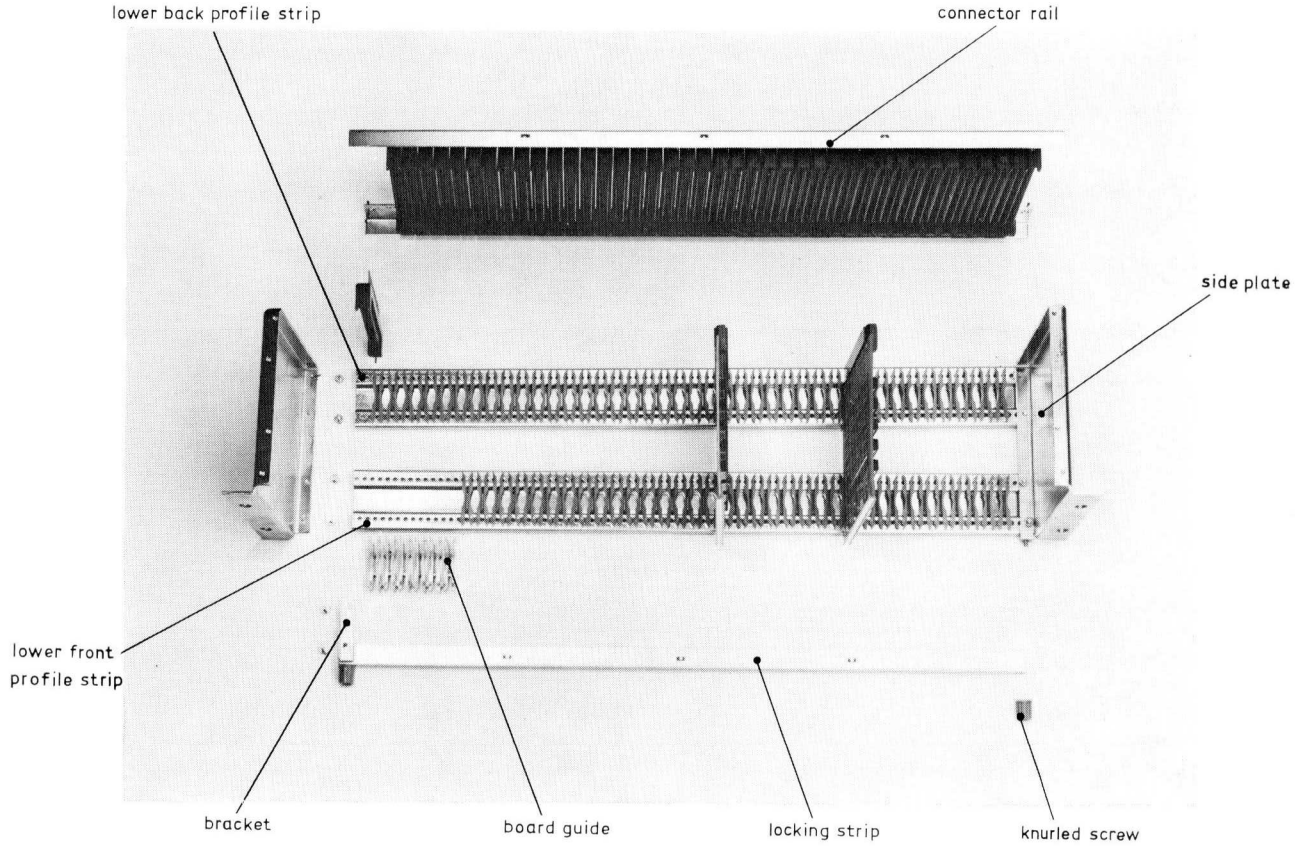


Fig.5-21 Exploded view of miniature chassis. *RZ23732-4*

5.3 Input devices

Input devices (or detectors) monitoring r.p.m., linear or angular displacement, etc., are indispensable for measuring or controlling mechanical motion. The input devices described here are capable of translating motion into an electrical signal suitable for handling by a logic system. Physical contact with the object or objects under measurement is avoided, so that wear is non-existent and reliability high.

As an introduction to these input devices, some information is given in Tables 5-2 and 5-3. Distinction is made between vane and proximity detectors, as seen from Table 5-2.

Other input devices are tachogenerators* and temperature sensors. For temperature sensing, NTC thermistors and diodes (forward voltage drop temperature dependent) can be used. A temperature sensor can be connected to a logic input to obtain on/off control, or to a linear input (for instance, that of a DOA61) to obtain time-proportional control. Tachogenerators are used for motor speed control.

Input devices are connected to the logic system via *screened* cables, thus avoiding pick-up of interference. The screen is grounded at the side of the logic system; here, the cables are terminated by RC filters to ensure a high signal/noise ratio, the RC product being made as large as possible without encroaching upon the required system speed.

* For instance, the 9904 121 000 ... series.

Table 5-2. Properties of input devices.

input device	maximum count rate	minimum object size detected	d.c. supply voltage	current consumption	applications
vane-switched oscillator VSO	1 kHz	8 mm*	12 V ± 10%	12 mA	– r.p.m. measurement. – angular position measurement.
miniature vane-switched oscillator MVSO	3 kHz	4 mm*	24 V ± 25% or 12 V ± 5%	20 mA + load current 12 mA + load current	– counting of small objects. – foil continuity checking. – programming.
electronic proximity detector EPD	1 kHz	* **	24 V+ 12 V ± 5%	16 mA	– detection of the presence or passage of metal objects.
miniature electronic proximity detector EPD60	1 kHz	* **	24 V ± 25% or 12 V ± 5%	15 mA	
light interruption probe LIP1	10 kHz	20 μm	12 V ± 5%	180 mA	– r.p.m. measurement. – position control. – counting of small objects.

* Object may consist of any metal.
** Size depends on distance from sensitive surface.
+ Via series resistor and 12 V voltage regulator diode.

Table 5-3. Drive capability of input devices.

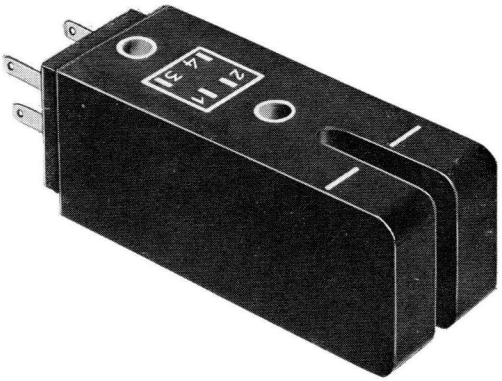
input device	no. of inputs of a NOR60 gate that must be paralleled	input drive of UPA61 Schmitt trigger++
vane-switched oscillator VSO	3*	via pin 5
miniature vane-switched oscillator MVSO	none**	via pin 5
electronic proximity detector EPD	2	via pin 14
miniature electronic proximity detector EPD60	none+	via pin 5 or 14
light interruption probe LIP1	4	via pin 5 and 1,2 kΩ series resistor

* Four inputs paralleled when using RC filter at gate input.
** MVSO and NOR60 gate supplied from a common d.c. source.
\+ Output capability 2 D.U. at 12 V and 3 D.U. at 24 V d.c. supply.
++ Section 2.4.

5.3.1 VANE-SWITCHED OSCILLATOR VSO

The VSO vane-switched oscillator (see Fig.5-22) detects small objects passing through its gap. If the metal object is a vane, the VSO works as a *static switch.*

As seen from the diagram in Fig.5-23, the VSO consists of an oscillator and a rectifier with an RC output filter. Oscillator coils L_1 L_2 are separated by the gap. If a metal object is placed between L_1 and L_2, feedback is reduced by eddy current losses in the metal. As a result, the oscillator output decreases or even drops to zero. The change in oscillator voltage is reflected in the d.c. output. Note that, because of the separate winding, L_3, the VSO output is isolated from the d.c. supply.



720809-21-01

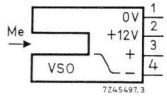


Fig.5-22 VSO (measuring 64 mm × 23 mm × 23 mm) and drawing symbol. Cable anchoring cover (supplied with VSO) not shown.

Fig.5-24 shows the termination of the VSO. For $R = 2200\,\Omega$ and $C = 0{,}47\,\mu F$, the maximum count rate is 100 Hz; the RC filter should be mounted *immediately* at the logic input.

Vane vibration (lengthwise vane displacement) can cause false pulses, giving rise to undesirable response of the logic system. In this event, the circuit of Fig.5-25 will be helpful[1]). The 2.IA60 works as a two-state device. It produces a clean output pulse because its hysteresis is 1 mm – see the performance graph of Fig.5-26. Hysteresis depends on R_4, and the switching level of the 2.IA60 is determined by R_1/R_2.

Fig.5-27 is an example of the use of the VSO in machine control.

[1]) AN No. 113, ordering code 9399 260 61301 – Increasing the VSO-displacement hysteresis.

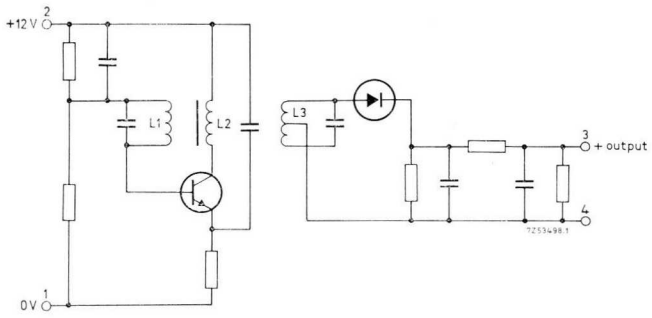


Fig.5-23 Circuit diagram of VSO.

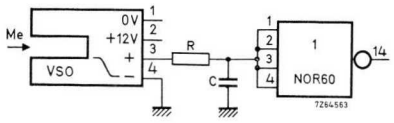


Fig.5-24 Termination of VSO.

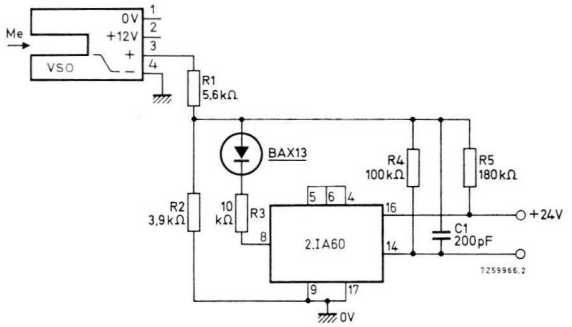


Fig.5-25 Use of 2.IA60 as a bistable device to eliminate the effect of vane vibration.

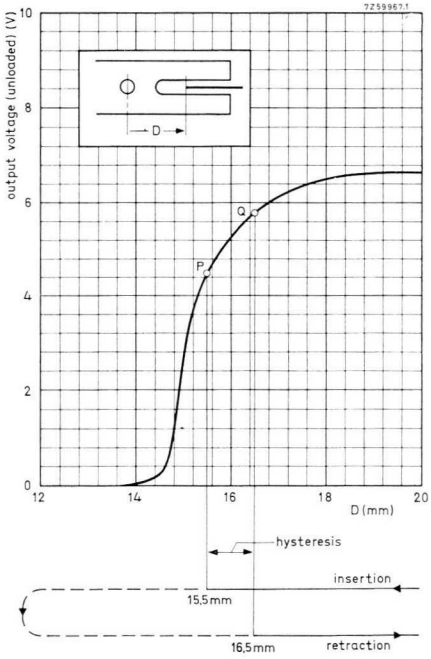
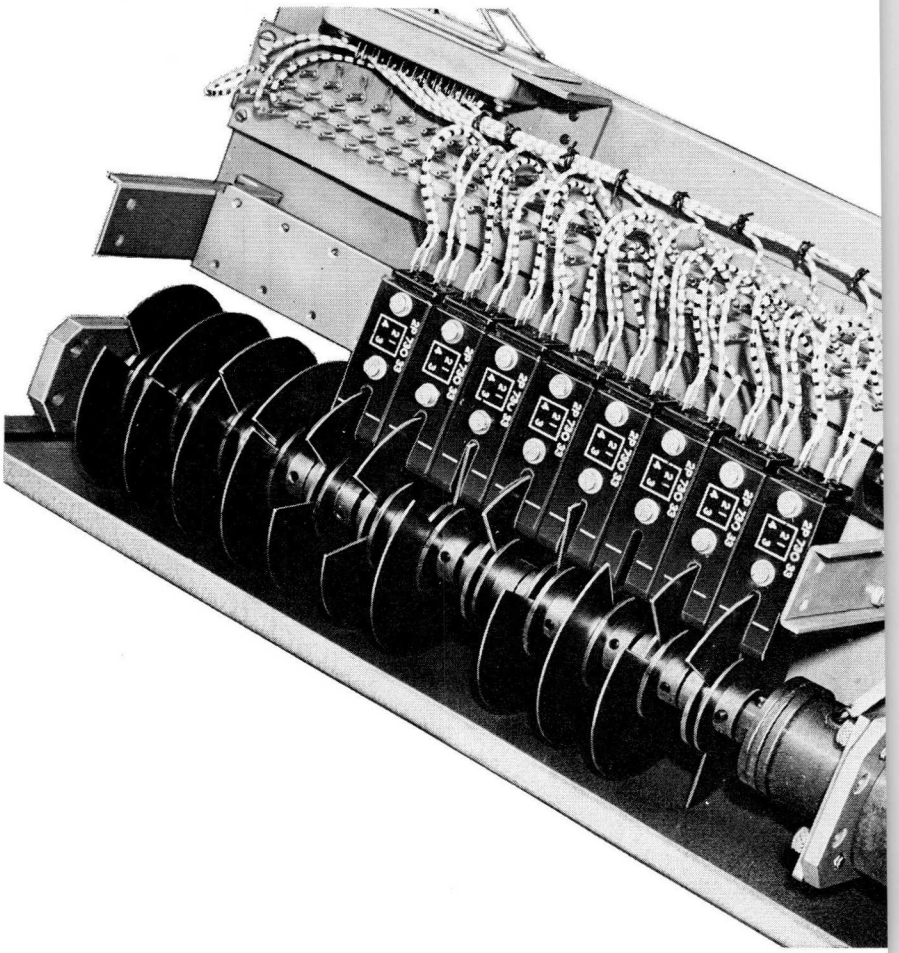


Fig.5-26 Typical VSO-output characteristic related to 2.IA60-output states.
——— = HIGH output; - - - - - - = LOW output.

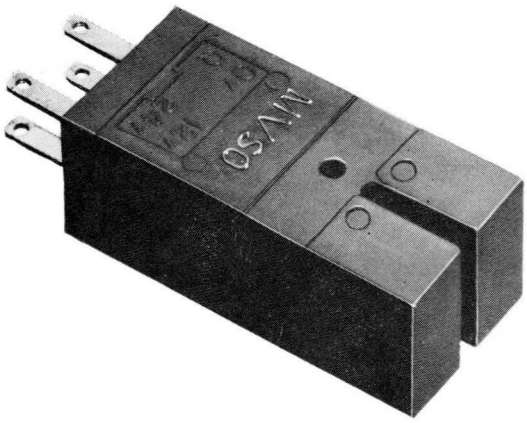


RK9230-4

Fig.5-27 Disc programmer for metal working machine using VSOs.

5.3.2 Miniature vane-switched oscillator MVSO

The MVSO vane-switched oscillator has the same working principle as the VSO, but it can detect smaller objects (minimum 4 mm size) and its maximum count rate is higher (3 kHz). Because of the addition of an amplifier, an increased output capability also results. Fig.5-28 illustrates the unit.



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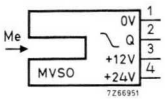
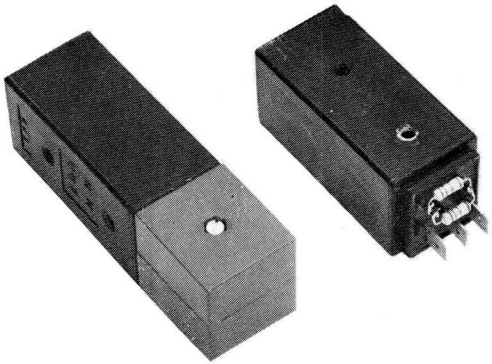


Fig.5-28 MVSO (measuring 41 mm × 19 mm × 15 mm) and drawing symbol.

5.3.3 Electronic proximity detector EPD

The EDP electronic proximity detector shown in Fig.5-29 decreases its output when a metal object is brought into its magnetic field. Fig.5-30 gives the EPD circuit diagram. With no metal object present, oscillator TR_1 L_1 L_2 produces



730730-02-10

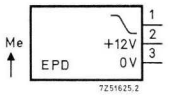


Fig.5-29 EPD (measuring 101,3 mm × 31 mm × 31 mm) and drawing symbol. Sensitive surface (opposite to terminal side) is 31 mm × 31 mm. Picture shows EPD with and without cable anchoring cover.

an a.c. voltage across L_3 which is rectified by TR_2. This transistor conducts, base current is extracted from TR_3, and the d.c. output is at almost +12 V. Inserting a metal object into the field of the sensing coil reduces the amplitude of oscillation, the collector current of TR_2 TR_3 decreases and the output of the EPD drops.

Fig.5-31 illustrates how the EPD should be terminated.

The performance of the EPD is seen from the graphs of Figs.5-32 and 5-33. Fig.5-32 gives the positions of a metal object in x, y co-ordinates for which the EPD output has dropped to 100 mV (x = distance of object from vertical line passing through centre of sensitive surface, y = distance of plane of object from that of sensitive surface). The plot of Fig.5-33 represents the output V_o of the EPD as a function of object distance y. It follows that the EPD performs excellently as a presence detector since its output drops from maximum to zero for less than 1 mm displacement.

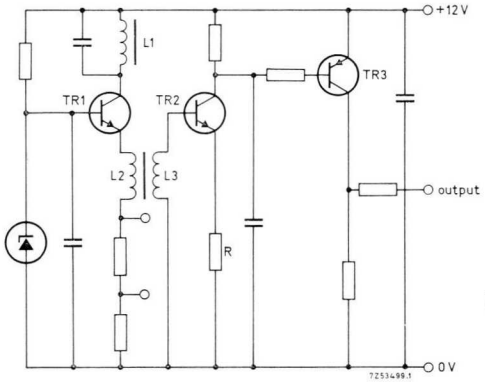


Fig.5-30 Circuit diagram of EPD.

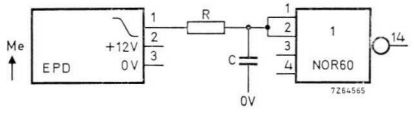


Fig.5-31 Termination of EPD.

R (Ω)	C (nF)	Max. count rate (Hz)
3300	470	66
3300	47	660
1000	100	1000

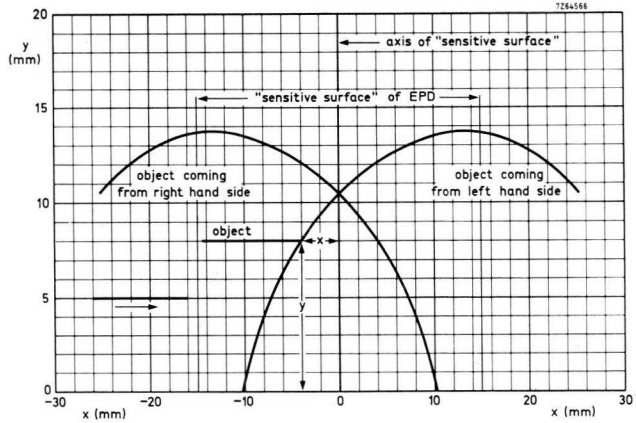


Fig.5-32 Response of EPD to 50 mm × 25 mm × 1 mm mild steel sheet moving parallel to sensitive surface with the 50 mm edge leading (direction of motion immaterial).

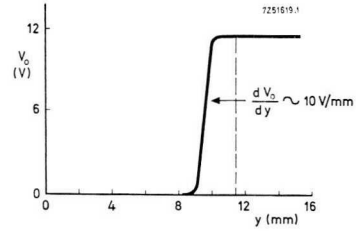
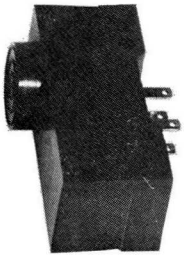


Fig.5-33 Detection of 50 mm × 25 mm × 1 mm mild steel sheet at y mm from sensitive surface.

5.3.4 Miniature electronic proximity detector EPD60

The miniature electronic proximity detector EPD60 (Fig.5-34) functions in much the same way as its larger counterpart, the EPD, but its output is *low* with *no* metal object present, and *high* when a metal object is *detected.* To allow detection to occur, the distance between the object and the sensing head must be no greater than 3 mm. The x, y plot of Fig.5-35 shows the response of the EPD60. The co-ordinates have the same meaning as those of Fig.5-32, the plot indicating the positions for which the output starts to rise. Detectors EPD60 can be stacked for compact building of programming units.



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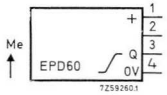


Fig.5-34 EDP60 (measuring 49,7 mm × 17,6 mm × 24,5 mm, excluding sensing head) and drawing symbol.

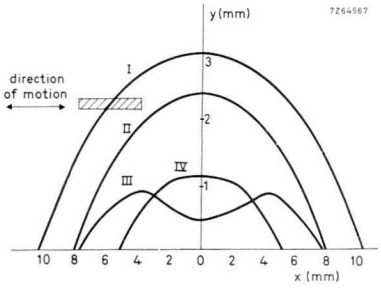
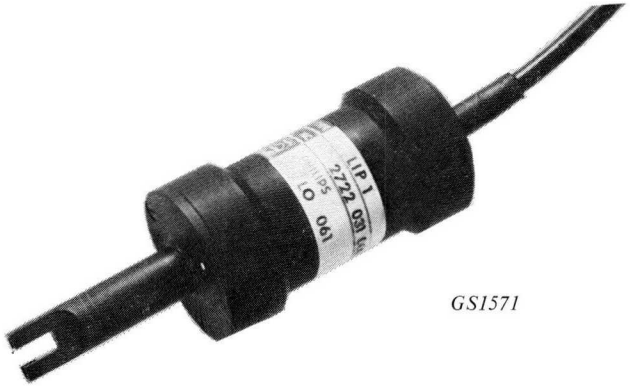


Fig.5-35 Response of EPD60 to disc moving parallel to sensor head (direction of motion immaterial): I mild steel 15 mm dia. 0,2 mm thick; II mild steel 10 mm dia. 0,2 mm thick; III copper 15 mm dia. 0,04 mm thick; IV copper 10 mm dia. 0,04 mm thick.

5.3.5 Light interruption probe LIP1

The light interruption probe LIP1 (Fig.5-36) has a novel optical system in which light emitted by a lamp in the LIP1 housing is passed through a light conductor and the gap, returned through another light conductor, then impinges on a photo-diode within the probe; as a result, the dimensions of the detection head are very small. The system has very high resolution in that it can detect an object of only 20 μm size intersecting the focal line; also, its count rate is high (10 kHz max.).



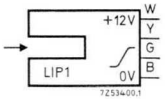


Fig.5-36 LIP1 (max. 32 mm dia.) and drawing symbol.

The diagram is as shown in Fig.5-37. With incident light, the resistance of the photo-diode is small, the transistor receives no base drive, and the output is low. Conversely, when the light is intercepted, the output of the LIP1 becomes high.

Fig.5-38 shows the termination of the LIP1.

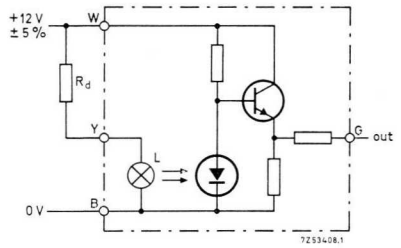


Fig.5-37 Circuit diagram of LIP1.

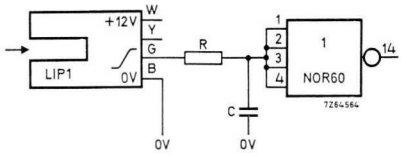
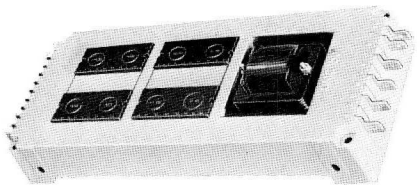


Fig.5-38 Termination of LIP1.

5.4 D.C. Supply units

5.4.1 Logic supply unit LSU60

The LSU60 is suitable for supplying small logic systems. It has 150 mA output current capability. Versions 4332 000 01000 and 4332 0000 01010 are available for 220 V and 110 V a.c. input, respectively. The LSU60 takes the area of a size B circuit block and, consequently, fits the UMC60 chassis: see Fig.5-39.



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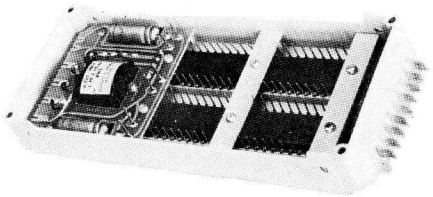
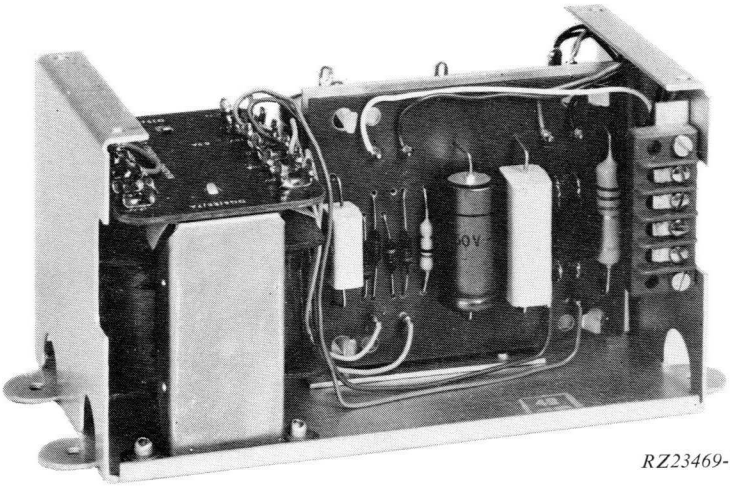


RZ27077-8

Fig.5-39 LSU60 mounted in UMC60 (top and bottom view).

5.4.2 Power supply units PSU60/61

Being capable of delivering 500 mA, the power supply units PSU60 and PSU61 are intended to supply more extensive logic circuitry. The PSU61 has an additional 100 V output for switch filters[2]) (25 mA output capability). Both units can be supplied from 100 V, 120 V, 220 V, 230 V, 240 V a.c. input. Fig.5-40 shows the appearance.



RZ23469-1

Fig.5-40 PSU60 (cover removed).

[2]) Application Book, ordering code 9399 263 01601 – Control System Design Manual for 60-series NORbits.

730726-04-04

One of the cold reduction mills at the Abbey Works of the Steel Company, Port Talbot, Wales, using NORbits to initiate an alarm should lubrication fail.

6 Wiring considerations

6.1 General recommendations[1])

The 61-series of circuit blocks has little sensitivity to interference, so that wiring will present few problems. When, however, interconnections are made injudiciously, difficulties may arise. The measures we give in this chapter will undoubtedly be helpful in circumventing such contingencies.

Disturbance of system operation may be caused by any of the following:

- interference from input devices
- interference induced in incoming lines
- interference from the mains supply
- interference by external fields
- interference generated internally.

Before treating the above subjects in detail, we will first make some general recommendations.

Use one Central Earth Point (CEP). All system components, cable screens, transformers inter-winding screens etc. should be earthed at one point by separate leads (Fig.6-1). There is then no risk that voltage drops across earth leads, caused by heavy output currents, would disturb highly sensitive system inputs. The earth leads should have sufficient thickness and be kept as short as possible, so that voltage drops due to large output currents are negligible. The cabinet must be earthed, to meet safety regulations; earthing is effected as shown in the diagram. It must be checked that the CEP is free from earth, with connection *a* in Fig.6-1 removed. If this is not the case, redundant earthing will result (see below). Under certain circumstances, improved interference suppression is obtained by connecting a 1 kΩ to 10 kΩ resistor (R_1 in Fig.6-1) between CEP and earth, or even when keeping the CEP floating.

Avoid earth loops. Earth loops are created by "redundant" earthing. These open loops are apt to pick up interference by magnetic induction. Fig.6-2 illustrates one particular case where connection of the cable screen to the housing of the sensor results in redundant earthing. The circulating current *i* generated by the magnetic field may cause unacceptable interference at sensitive system inputs.

[1]) AN No. 177, ordering code 9399 260 67701 – Digital Circuits, Design Recommendations.

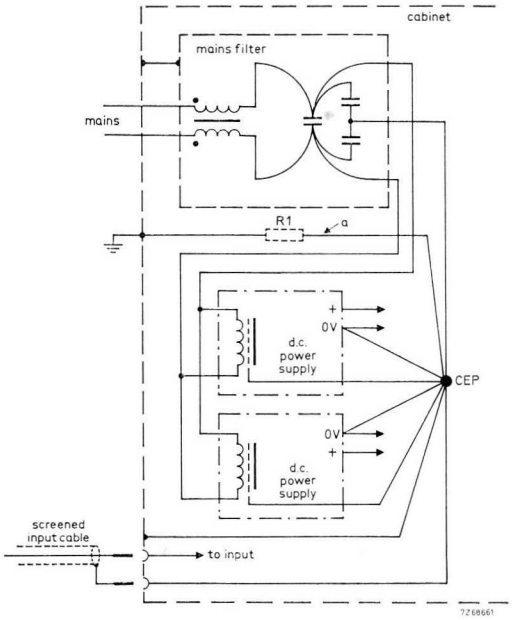


Fig.6-1 Earthing at a central point (CEP).

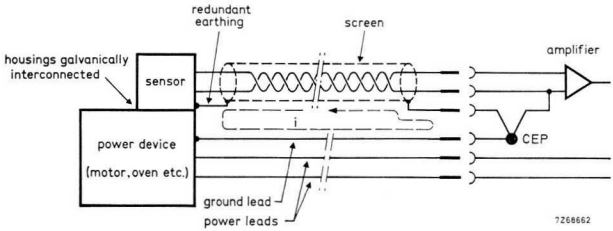


Fig.6-2 Example of redundant earthing.

6.2 Interference from input devices

Electronic input devices produce very little interference and create, therefore, no problems. The effect of contact bounce of mechanical switches is eliminated by using the 2.SF60 dual switch filter.

6.3 Interference induced in incoming lines

Electronic or magnetic fields can induce interference in incoming lines. The 2.SF60 switch filter is helpful in the case of a low-frequency signal (below say 100 Hz), but it attenuates high-frequency signals. In the latter case, screened cables with twisted wire pairs should be used. The earthed screen provides electrostatic shielding, and the twisted pair greatly reduces magnetic coupling. The screen of the cable must be connected to the CEP (Fig.6-2). If the cable enters the cabinet via a plug, the screen must be fed into the cabinet via one of the pins of the plug and *not* be earthed via the mass connection of the plug. Fig.6-3 shows the required arrangement for a d.c. motor plus tachogenerator as an example. Fig.6-4 is another example; to obtain effective interference suppression, the time constant of the *RC*-input filter is chosen to be so large that system speed requirements are just fulfilled.

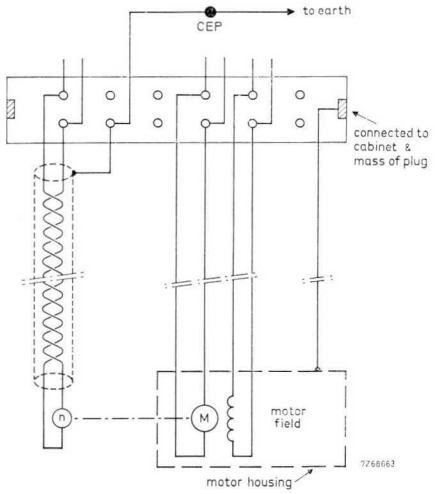


Fig.6-3 Earthing of cable screen.

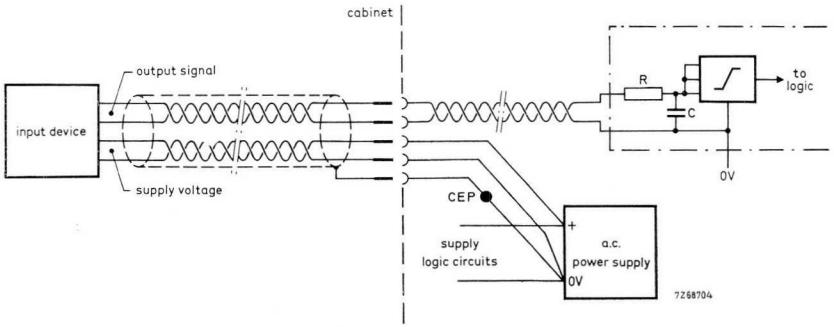


Fig.6-4 Connection of an input device and its d.c. supply.

6.4 Interference from the mains supply

The mains supply can be polluted by high-power switching (welders etc.), lightning discharges and the like. Mains interference suppression filters, such as the MF 0.5A and the MF 2A [2]), *mounted directly at the place where the a.c. lines enter the cabinet*, are very effective in obtaining a clean supply voltage.

The interconnection between the filter capacitors that are placed in series is directly connected to the CEP, the case making contact with the cabinet (Fig.6-1). If the case is connected to the interconnection point between the capacitors, it must be insulated from the cabinet and connected directly to the CEP. Mains switches, contactors, fuses, voltage indicators etc., not placed in the filtered part, should be housed in a *separate* compartment to obtain good screening from sensitive system inputs. Input transformers of d.c. supply units must have a screen between primary and secondary, the screen being connected to the CEP.

[2]) PN No. 51, ordering code 9399 260 85101 – Interference Suppression Filters.

Fig.6-5 illustrates how a synchronization circuit can be protected against interference. (The 2 × 17 V input is rectified by the RSA61 to obtain a synchronization signal for thyristor triggering – consult Section 1.2.1). Mains interference, occurring while the a.c. voltage passes through zero, tends to shift the zero cross-over points and disturb synchronization. The 0,1 μF capacitors across the transformer secondaries and the transformer leakage inductance form a low-pass filter suppressing interference. An inter-winding screen providing electrostatic shielding is recommended.

It is not wise to run low-voltage d.c. supply lines and mains supply lines together. Keep mains lines as short as possible and hold them far removed from low-level input leads.

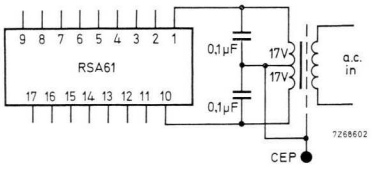


Fig.6-5 Protection of synchronization circuit.

6.5 Interference by external fields

The logic system should be installed in a metal cabinet which is properly earthed to provide screening against external electrical and magnetic fields. Never use the cabinet or its frame as an earth return conductor, because this would defeat the screening effect. It must be noted that high-frequency fields can penetrate through holes in the cabinet. A.C. supply lines should preferably be run in steel conduits or trunking to minimize the emission of disturbing a.c. fields. Operation near high-voltage installations requires careful observation of the measures suggested in this Chapter.

6.6 Interference generated internally

Interference, generated internally, is due to crosstalk, that is, signal transfer between adjacent wires. Crosstalk increases with:

- capacitance between wires
- magnetic coupling between wires
- impedance of shared wires.

As a general measure, it is recommended that RC input filters be used whose roll-off frequency conforms to system speed requirements (ref. Fig.6-4). Further, electrolytic capacitors (100 μF, or higher capacitance) directly across the + and 0 V supply terminals of high-power pulse oscillators reduce stray output currents, thus improving interference suppression.

Capacitive and magnetic coupling between wires. Point-to-point wiring has lower inter-wiring capacitance and inductance than wiring in cable harnesses (larger distance between wires) and gives, therefore, less crosstalk. If cable harnesses are wanted, do not combine high-level and low-level signal wires in one harness, unless screened and twisted wire pairs are used for these signals. *The screen should be connected to the CEP* (Fig.6-1). Twisted wires are *always* used for outgoing leads from supply units and for transmitting high-current signals from one to another part of a system. When wires are twisted, the magnetic fields generated by the current in both wires virtually cancel; this has the advantages of a small signal voltage loss (low overall inductance) and little electro-magnetic radiation.

Impedance of shared wires. A shared wire couples two circuits, for instance, an input and output circuit. The relatively large voltage drop caused by the output current across the shared-wire impedance can give rise to unacceptable crosstalk. For instance, a stretched wire of 0,8 mm diameter and 0,2 m length has about 0,3 μH inductance. This creates 1,5 V peak voltage drop at a current change of 5 A/μs, the latter being quite normal for the UPA61 operating as a high-power pulse oscillator! Wrap-around wiring is too thin (usually 0,2 mm diameter) for shared wiring and is not suitable either for carrying large output currents. A thicker wire gives a lower inductance. A few wiring examples are given here.

In the circuit of Fig.6-6*a*, the high capacitor discharge current i_{disch} of the UPA61-pulse oscillator causes a voltage drop v_n across the earth path *ab* which is shared with the highly sensitive input. Since v_n is in series with the low-level input signal v_i, appreciable interference is likely to occur. To avoid this, the improved circuit of Fig.6-6*b* uses separate earth leads. A common supply line may also cause problems, as is clear from the following example.

High-power pulse oscillators produce large output currents with steep edges. In Fig.6-7*a*, the pulsating output current i_o from output transistor TR_2 triggers TH_2. However, it produces a voltage drop v_n across the common supply wire which may be several metres long, depending on the distance between control and power circuitry. The voltage v_n is coupled to the primary winding of T_1 via parasitic capacitance C_p, causing i_n to flow. As a result, extremely narrow pulses appear at the gate of TH_1 and may cause spurious triggering when this thyristor is sensitive. The improved layout shown in Fig.6-7*b* prevents the risk of false triggering. The supply leads to the trigger transformers are separated, and thick wires are chosen for the common circuit paths. Cable screening and twisted wiring minimize radiation of the high-frequency trigger pulses. The 1000 μF decoupling capacitor is mounted as close as possible to the + and 0 V oscillator supply pins, to avoid stray output currents. The BY206 diodes prevent thyristor

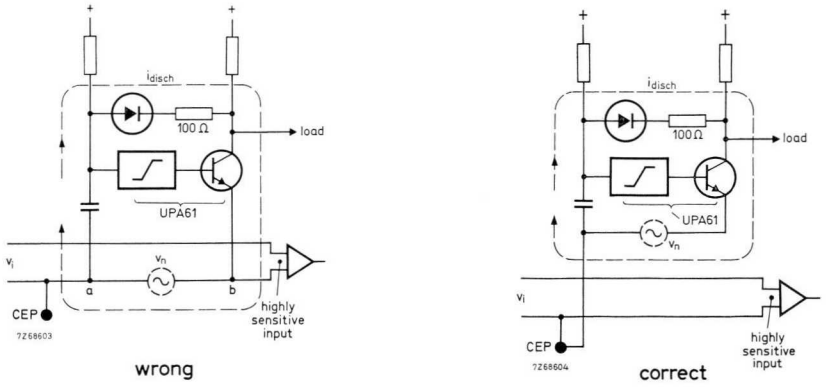
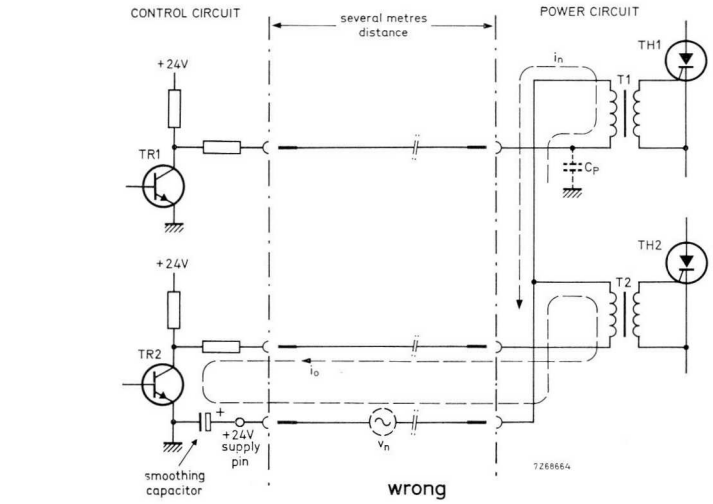
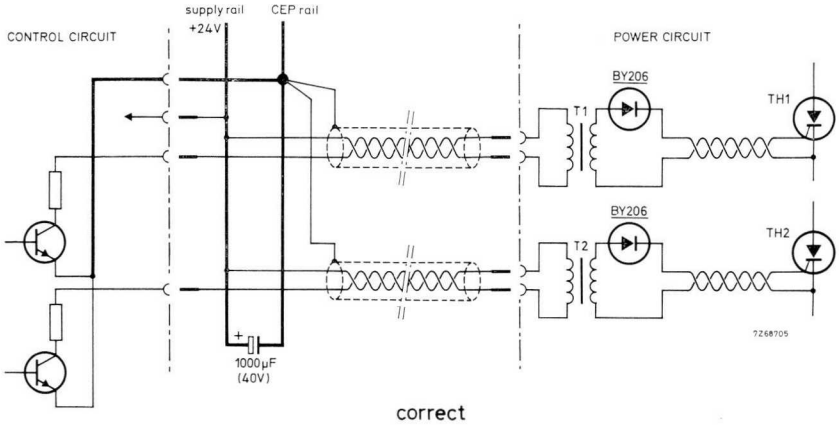


Fig.6-6 Earthing of pulse generator and sensitive input.



(a)



(b)

Fig.6-7 High-power circuitry using TT60 (T_1 and T_2). Note CEP in (b).

switching affecting the trigger circuits. Fig.6-8 illustrates how interfacing should occur. All wiring from the connector pins to those of the UPA61 should be kept *as short as possible*. The power circuit is that of a full-controlled three-phase bridge or a three-phase inverter (Section 4.6.3).

Fig.6-9 is a schematic representation of a trigger circuit with the TT61, mounted on a printed-wiring board. The common tracks shown heavy in the diagram (+ and 0 V potential) must have at least 0,2 mm^2 cross section and be kept as short as possible.

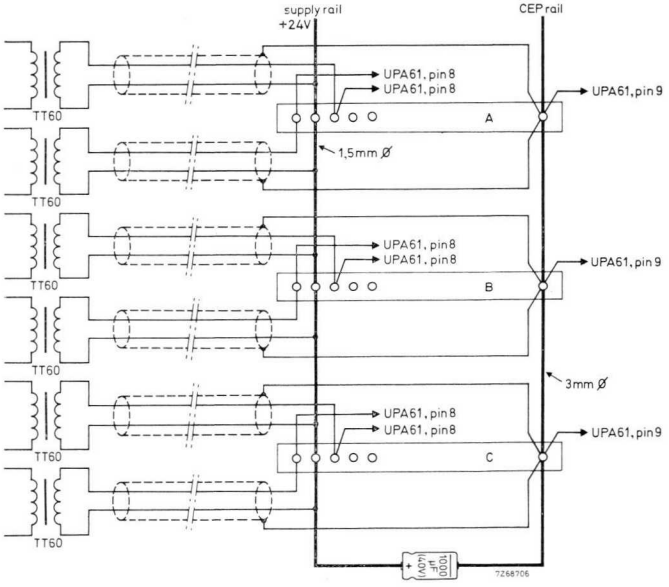


Fig.6-8 Interfacing between high-power trigger circuit and TT60 trigger transformers. *A*, *B*, *C* = edge connectors.

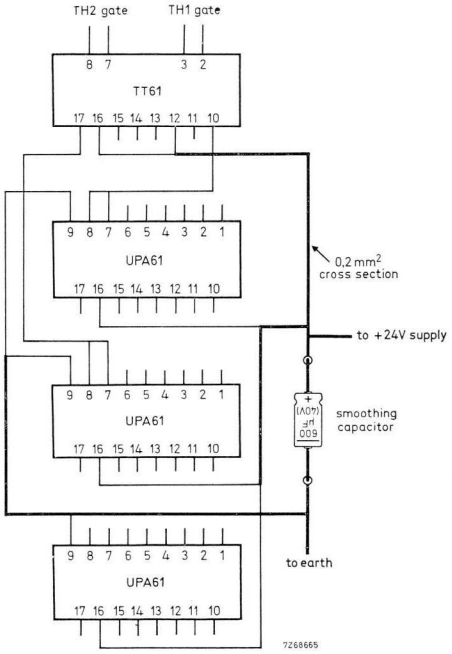


Fig.6-9 Schematic representation of printed wiring in trigger circuitry using TT61.

Appendix — Power stacks

A.1 Why power stacks?

Power stacks[1]) are pre-assembled, mains supplied rectifier or power control modules, built from standard components and comprising the power devices on their heatsinks, transient suppression RC-networks, interconnections and terminal blocks; further, free-wheeling diodes are included in the half-controlled bridge type modules. Trigger transformers for thyristor control are included, but trigger circuits should be provided separately. See our Data Handbook System for details.

A standard series of power stacks ("preferred types") is available covering a large output current range. In addition, stacks that comply with specific requirements can be ordered.

These power stacks offer important advantages, namely:

- output ratings are guaranteed
- construction of a complete rectifier or power control system is greatly simplified
- preferred types are available ex stock.

Power stacks come in the following standard circuit configurations for single-phase and three-phase use:

- diode bridge for rectification
- half-controlled bridge for non-regenerative power control
- full-controlled bridge for regenerative power control
- a.c. controller for a.c. power control.

Inverter and chopper stacks are also available.

As seen from Table A-1 the obtainable output power ranges from a few to many kilowatts; it can be increased significantly when forced cooling is used. Fig.A-1 illustrates a power stack.

[1]) Product Survey, ordering code 9399 213 06801 – Industrial Power Modules.

Table A-1. Output currents and output powers for preferred power stack types; a.c. input voltage 220 V for single-phase, and 380 V for three-phase.

configuration	obtainable output current*	obtainable output power*
single-phase diode bridge	20 A to 400 A	4 kVA to 77 kVA
single-phase half-controlled bridge	18 A to 240 A	3,5 kVA to 44 kVA
single-phase full-controlled bridge	13 A to 240 A	2,5 kVA to 44 kVA
single-phase a.c. controller	14 A to 270 A	3 kVA to 60 kVA
three-phase diode bridge	25 A to 550 A	13 kVA to 270 kVA
three-phase half-controlled bridge	20 A to 280 A	10 kVA to 140 kVA
three-phase full-controlled bridge	15 A to 330 A	6 kVA to 160 kVA
three-phase a.c. controller	14 A to 270 A	8 kVA to 170 kVA

* Free convection, $T_{amb} = 35\,^{\circ}C$.

The protection networks on the power stacks ensure suppression of commutation transients and will to some extent reduce mains-borne transients. To adequately safeguard against the latter, separate suppression networks should be used; these networks also prevent interference due to thyristor switching from entering into the mains; for further particulars, reference is made to earlier publications [2]).

[2]) AI No. 445, ordering code 9399 214 44501 – Transient Suppression Networks for Transformerless Controlled Rectifier Systems.
AN No. 146, ordering code 9399 250 64601 – Transient Suppression Networks for New Thyristor Range.

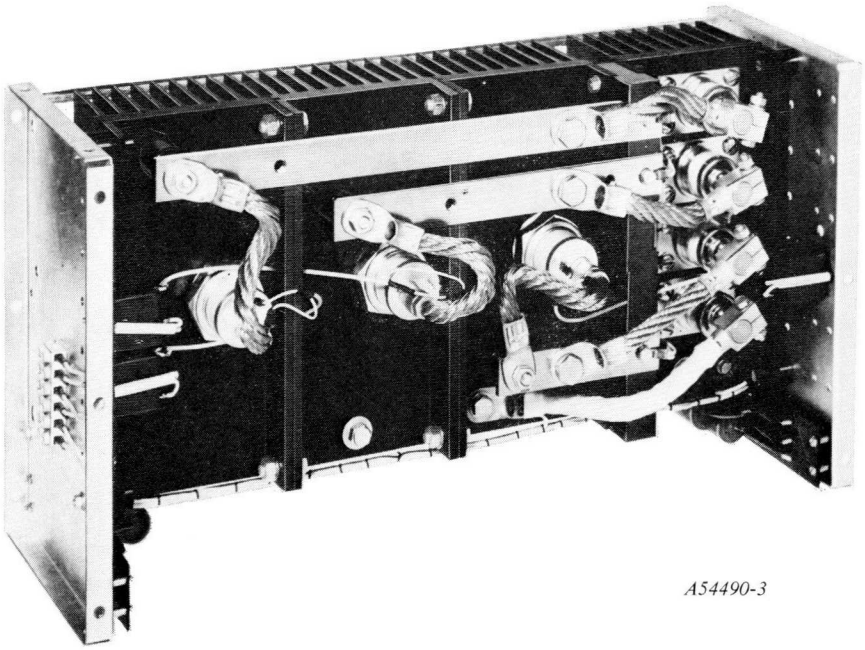


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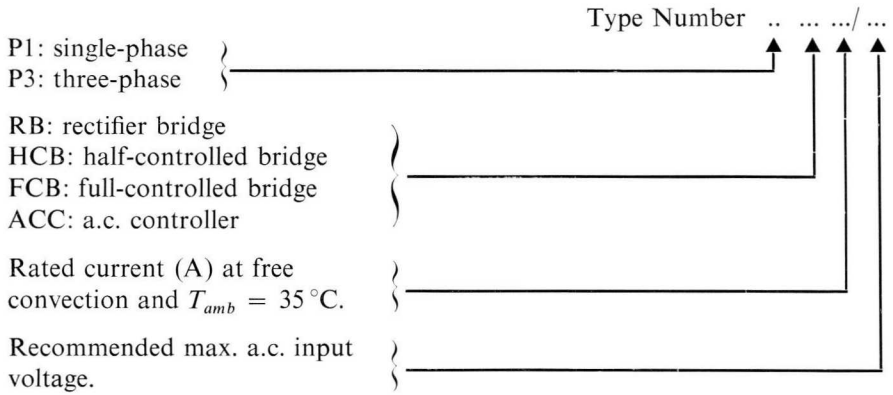
Fig.A-1 Three-phase half-controlled bridge, 400 V a.c. input, 550 A d.c. output current.

A.2 Construction

The power stacks consist of extruded aluminium heatsinks fitted between side plates. Only five different main components (heatsink lengths of 5 cm, 11 cm and 23 cm, and side plates of two different heights) and a few additional components are necessary to obtain the full range of power stacks.

Stack construction is such that there is about 5 cm clearance at the bottom when a stack is mounted on the base of a cabinet; if a clearance of, in general, 8 cm is left above the stack, sufficient cooling will be ensured.

Stack type number coding is as follows:



Power stack circuit configurations are given in Fig.A-2. For full information, including recommended fuses, the Data Handbook "Components and Materials" should be consulted.

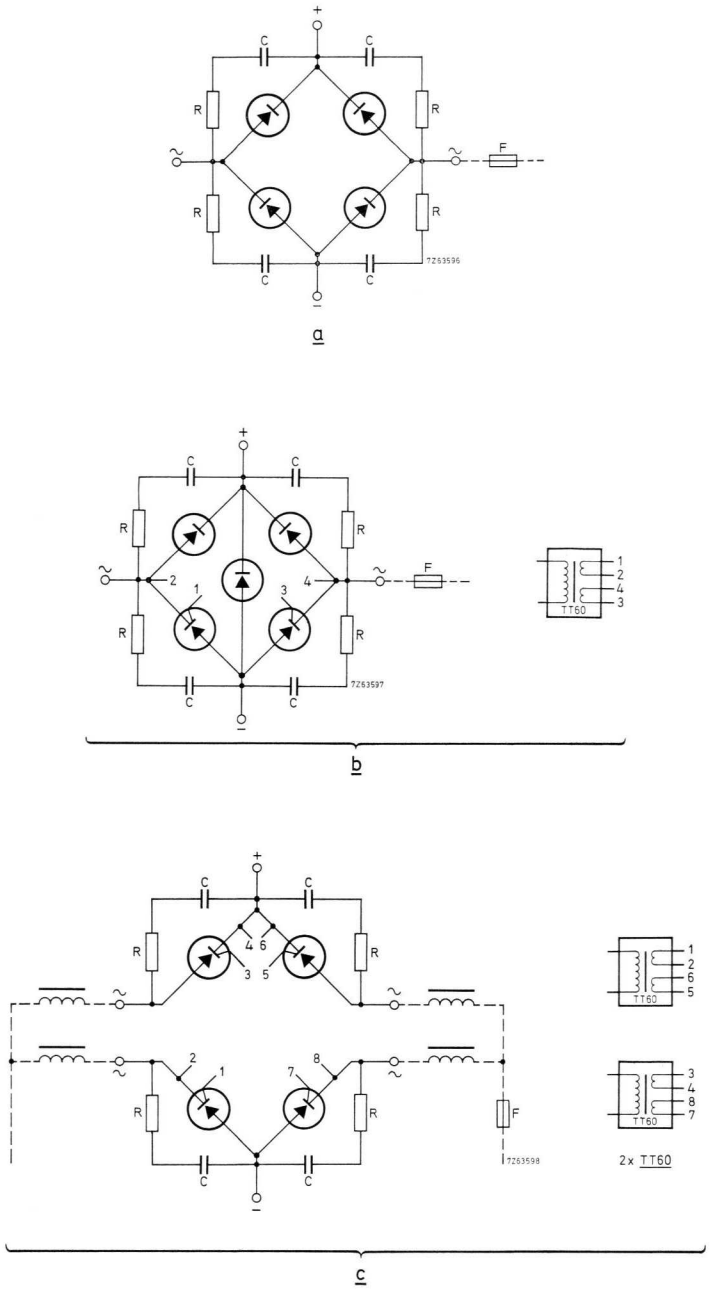


Fig.A-2 Power stack circuit configurations: *a.* single-phase diode bridge, *b.* single-phase half-controlled bridge, *c.* single-phase full-controlled bridge.

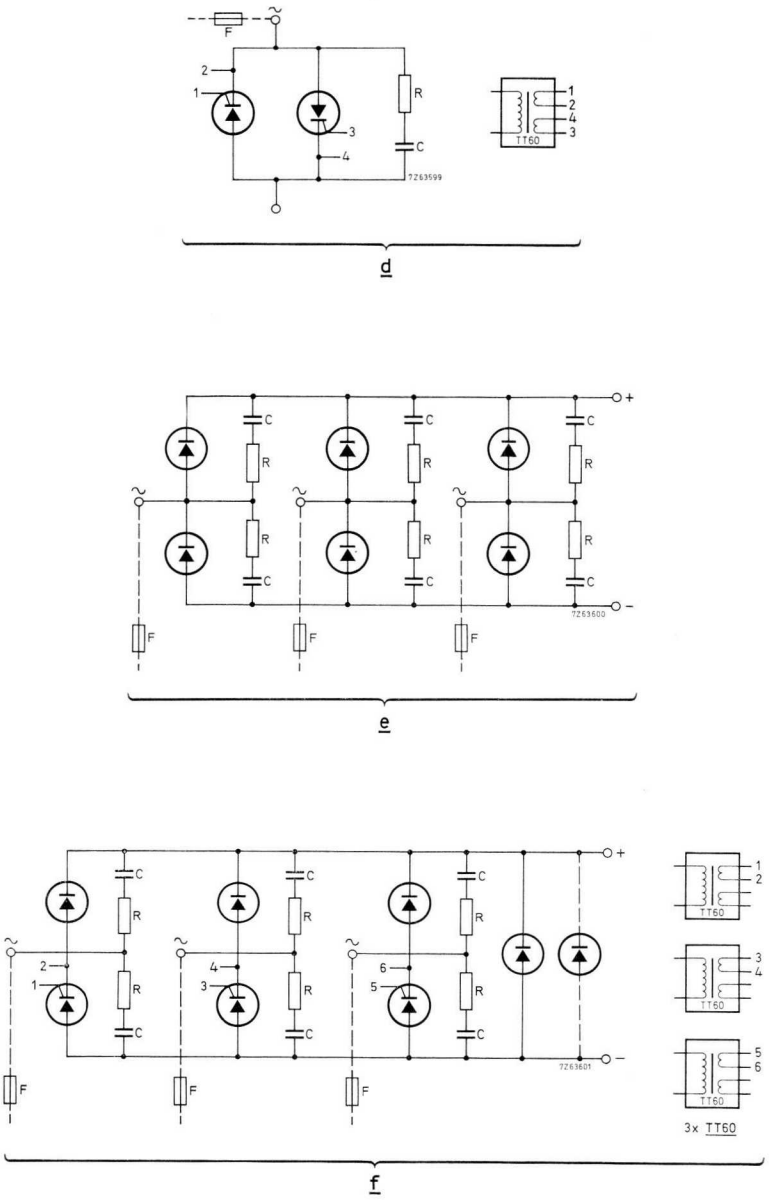


Fig.A-2 *(continued) d.* single-phase a.c. controller, *e.* three-phase diode bridge, *f.* three-phase half-controlled bridge.

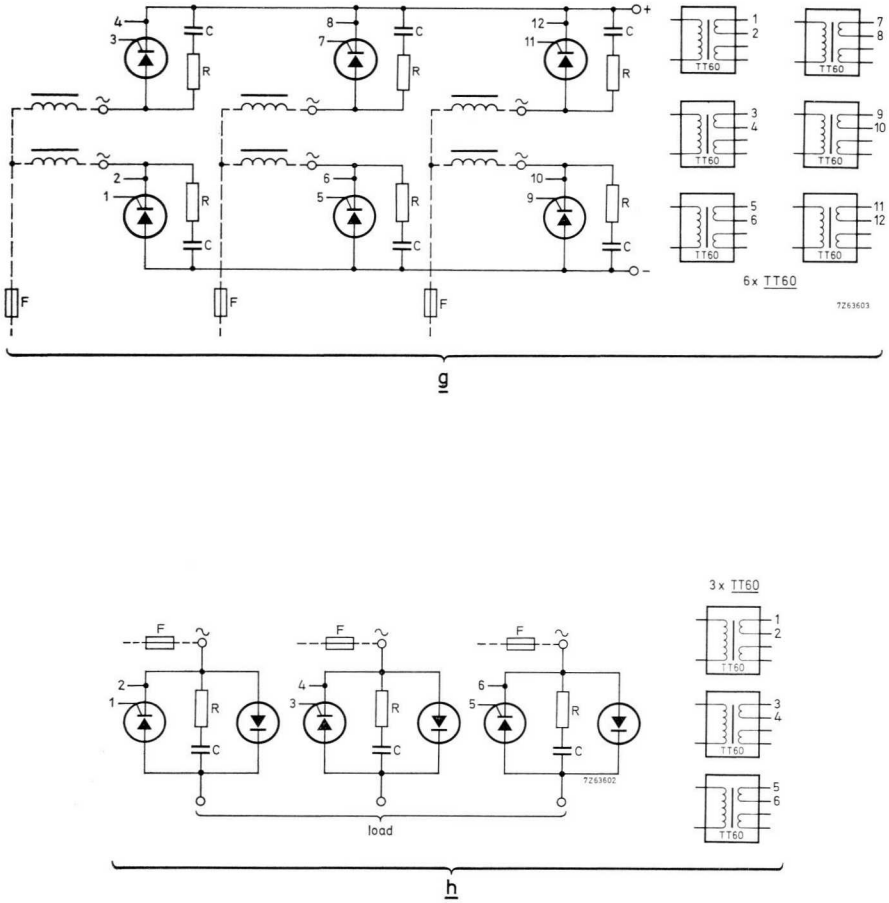
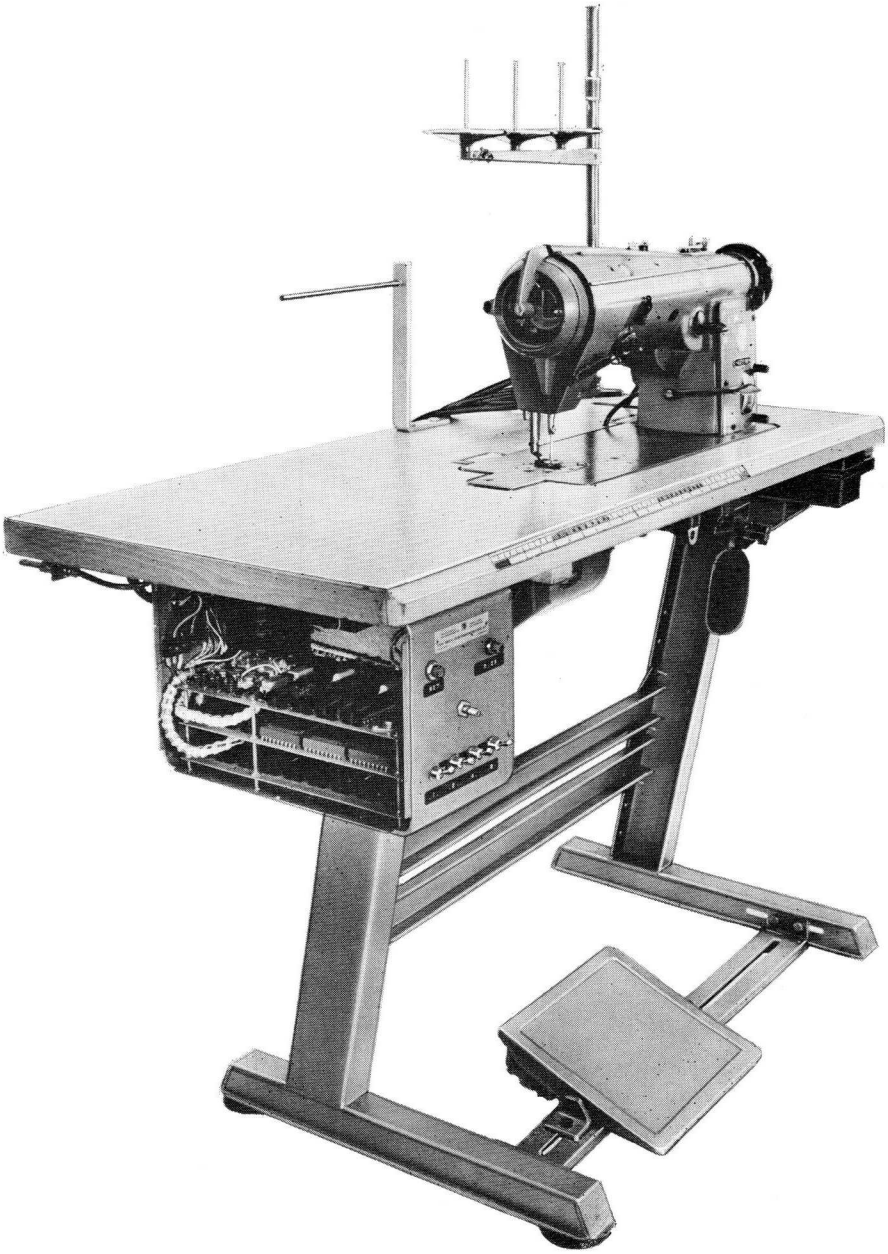


Fig.A-2 *(continued) g.* three-phase full-controlled bridge, *h.* three-phase half-controlled a.c. controller.



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Industrial sewing machine controlled by 61-series circuit modules.
Courtesy of Messrs. van Hout Electrotechniek B.V., Eindhoven, The Netherlands.

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