

PHILIPS

**DATA
HANDBOOK**



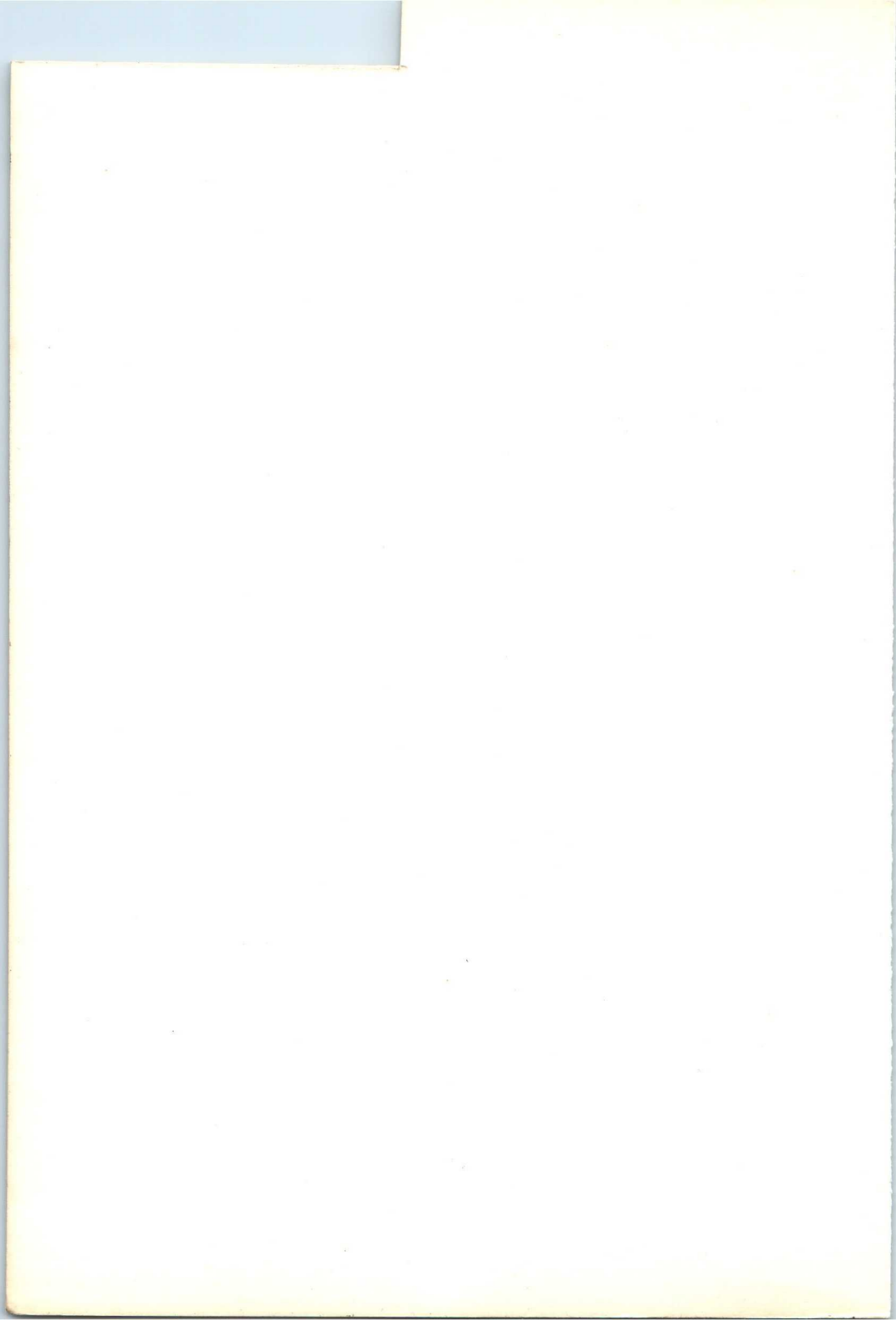
**ELECTRONIC COMPONENTS
AND MATERIALS**

**SEMICONDUCTORS
AND
INTEGRATED CIRCUITS**

PART 5 MARCH 1971

Digital Integrated Circuits

Linear Integrated Circuits



SEMICONDUCTORS AND INTEGRATED CIRCUITS

Part 5

March 1971

General

D T L

FC family

T T L

FJ family

MOS

FD family

Linear integrated circuits



DATA HANDBOOK SYSTEM

To provide you with a comprehensive source of information on electronic components, subassemblies and materials, our Data Handbook System is made up of three series of handbooks, each comprising several parts.

The three series, identified by the colours noted, are:

ELECTRON TUBES (9 parts) BLUE

SEMICONDUCTORS AND INTEGRATED CIRCUITS (5 parts) RED

COMPONENTS AND MATERIALS (5 parts) GREEN

The several parts contain all pertinent data available at the time of publication, and each is revised and reissued annually; the contents of each series are summarized on the following pages.

We have made every effort to ensure that each series is as accurate, comprehensive and up-to-date as possible, and we hope you will find it to be a valuable source of reference. Where ratings or specifications quoted differ from those published in the preceding edition they will be pointed out by arrows. You will understand that we can not guarantee that all products listed in any one edition of the handbook will remain available, or that their specifications will not be changed, before the next edition is published. If you need confirmation that the published data about any of our products are the latest available, may we ask that you contact our representative. He is at your service and will be glad to answer your inquiries.

ELECTRON TUBES (BLUE SERIES)

This series consists of the following parts, issued on the dates indicated.

| | |
|-----------------------------------------|-----------------------------------|
| Part 1 | January 1971 |
| Transmitting tubes (Tetrodes, Pentodes) | Associated accessories |
| Part 2 | February 1970 |
| Tubes for microwave equipment | |
| Part 3 | March 1970 |
| Special Quality tubes | Miscellaneous devices |
| Part 4 | April 1970 |
| Receiving tubes | |
| Part 5 | May 1970 |
| Cathode-ray tubes | Photoconductive devices |
| Photo tubes | Associated accessories |
| Camera tubes | |
| Part 6 | June 1970 |
| Photomultiplier tubes | Radiation counter tubes |
| Scintillators | Semiconductor radiation detectors |
| Photoscintillators | Neutron generator tubes |
| | Associated accessories |
| Part 7 | July 1970 |
| Voltage stabilizing and reference tubes | Thyratrons |
| Counter, selector, and indicator tubes | Ignitrons |
| Trigger tubes | Industrial rectifying tubes |
| Switching diodes | High-voltage rectifying tubes |
| Part 8 | August 1970 |
| T. V. Picture tubes | |
| Part 9 | January 1971 |
| Transmitting tubes (Triodes) | Associated accessories |
| Tubes for R. F. heating (Triodes) | |

January 1971

SEMICONDUCTORS AND INTEGRATED CIRCUITS (RED SERIES)

This series consists of the following parts, issued on the dates indicated.

Part 1 Diodes and Thyristors

September 1970

General
Signal diodes
Tunnel diodes
Variable capacitance diodes
Voltage regulator diodes

Rectifier diodes
Thyristors, diacs, triacs
Rectifier stacks
Accessories
Heatsinks

Part 2 Low frequency; Deflection

October 1970

General
Low frequency transistors (low power)
Low frequency power transistors

Deflection transistors
Accessories

Part 3 High frequency; Switching

November 1970

General
High frequency transistors

Switching transistors
Accessories

Part 4 Special types

December 1970

General
Transmitting transistors
Microwave devices
Field effect transistors
Dual transistors
Microminiature devices for
thick- and thin-film circuits

Beam lead devices for
thick- and thin-film circuits
Photo devices
Accessories

Part 5 Integrated Circuits

March 1971

General
Digital integrated circuits
DTL (FC family)
TTL (FJ family)
MOS (FD family)

Linear integrated circuits

COMPONENTS AND MATERIALS (GREEN SERIES)

This series consists of the following parts, issued on the dates indicated.

Part 1 Circuit Blocks, Input/Output Devices

September 1970

Circuit blocks 100 kHz Series
Circuit blocks 1-Series
Circuit blocks 10-Series
Circuit blocks 20-Series
Circuit blocks 40-Series
Counter modules 50-Series
Norbits 60-Series, 61-Series

Circuit blocks 90-Series
Circuit blocks for ferrite core
memory drive
Input/output devices

Part 2 Resistors, Capacitors

December 1970

Fixed resistors
Variable resistors
Non-linear resistors
Ceramic capacitors

Polyester, polycarbonate, polystyrene,
paper capacitors
Electrolytic capacitors
Variable capacitors

Part 3 Radio, Audio, Television

February 1971

FM tuners
Coils
Piezoelectric ceramic resonators
and filters
Loudspeakers
Audio and mains transformers

Television tuners
Components for black and white television
Components for colour television
Deflection assemblies for camera tubes

Part 4 Magnetic Materials, White Ceramics

March 1970

Ferrites for radio, audio
and television
Ferrocube potcores and square cores
Microchokes

Ferrocube transformer cores
Piezoxide
Permanent magnet materials

Part 5 Memory Products, Magnetic Heads, Quartz Crystals, Microwave Devices, Variable Transformers, Electro-mechanical Components

June 1970

Ferrite memory cores
Matrix planes, matrix stacks
Complete memories
Magnetic heads

Quartz crystal units, crystal filters
Isolators, circulators
Variable mains transformers
Electro-mechanical components

Technology relating to the products described in this publication is shared by the following companies.

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Electron Tubes Div.
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HICKSVILLE N.Y.
Sem. and Microcircuits Div.
Tel. 401-762-9000
SLATERSVILLE R.I. 02876
Electronic Components Div.
Tel. 516-234-7000
HAUPPAGE N.Y.

Uruguay

Luzilectron S.A.
Rondeau 1567, piso 5
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MONTEVIDEO

Venezuela

C.A. Philips Venezolana
Elcoma Department
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CARACAS



General

Preface

Type designation

Package outlines

Graphical symbols

Ratings

Letter symbols

1870
1871
1872
1873
1874
1875

PREFACE TO DATA OF INTEGRATED CIRCUITS

1. General

The published data comprise particulars needed by designers of equipment in which integrated circuits are to be incorporated, and criteria on which to base acceptance testing of such circuits. For ease of reference, the data on each circuit are grouped according to the several headings discussed below.

The limiting values quoted under the headings Characteristics and Package Outline may be taken as references for acceptance testing.

Values cited as typical are given for information only.

For an explanation of the type designation code, see the section Type Designation. For an explanation of the letter symbols used in designating terminals and performance of integrated circuits, and the electrical and logic quantities pertaining to them, see the section Letter Symbols.

2. Quick Reference Data

The main properties of the integrated circuit summarized for quick reference

3. Ratings

Ratings are limits beyond which the serviceability of the integrated circuit may be impaired. The ratings given here are in accordance with the Absolute Maximum System as defined in publication no. 134 of the International Electrical Commission; for further details see item 2 of the section Rating Systems.

If a circuit is used under the conditions set forth in the sections Characteristics and Additional System Design Data, its operation within the ratings is ensured.

4. Circuit diagram

Circuit diagrams and logic symbols are given to illustrate the circuit function. The diagrams show only essential elements, parasitic elements due to the method of manufacture normally being omitted. The manufacturer reserves the right to make minor changes to improve manufacturability.

5. System Design Data and Additional System Design Data

System Design Data normally derived from the Characteristics and based on worst-case assumptions as to temperature, loading and supply voltage, are quoted for the guidance of equipment designers. Supplementary information derived from measurements on large production samples may be given under Additional System Design Data.

PREFACE

6. Application information

Under this heading, practical circuit connections and the resulting performance are described. Care has been taken to ensure the accuracy and completeness of the information given, but no liability therefor is assumed, nor is licence under any patent implied.

7. Characteristics

Characteristics are measurable properties of the integrated circuit described. Under a specific set of test conditions compliance with limit values given under this heading establishes the specified performance of the circuit; this can be used as a criterion for acceptance testing.

Values cited as typical are given for information only and are not subject to any form of guarantee.

8. Logic symbols (digital circuits)

Graphical logic symbols accord with MIL standard 806B.

Supplementary drawings correlate logic functions with pin locations as a help to laying out printed circuit boards.

9. Outline drawing and pin 1 identification

Dimensional drawings indicate the pin numbering of circuit packages.

Dual in-line packages have a notch at one end to identify pin 1.

Take care not to mistake adventitious moulding marks for the pin 1 identification.

Flat packs identify pin 1 by a small projection on the pin itself and/or by a dot on the body of the package.

Metal can encapsulations identify pin 1 by a tab on the rim of the can.

PRO ELECTRON TYPE DESIGNATION CODE

The type number consists of three letters followed by three figures (sometimes followed by a version letter*)

For the purpose of type designation integrated circuits are divided in four groups:

- Digital family circuits
- Digital solitary circuits
- Analogue (including linear) circuits
- Mixed digital/analogue circuits

DIGITAL FAMILY TYPES

First two letters: family

Third letter: circuit function

First two figures: serial number

Third figure: operating ambient temperature range

DIGITAL SOLITARY TYPES

First letter: "S"

Second letter: extension of serial number

Third letter: circuit function

First two figures: serial number

Third figure: operating ambient temperature range

ANALOGUE (LINEAR) TYPES

First letter: "T"

Second and third letter: extension of serial number

First two figures: serial number

Third figure: operating ambient temperature range

MIXED DIGITAL/ANALOGUE TYPES

First letter: "U"

Second and third letter: extension of serial number

First two figures: serial number

Third figure: operating ambient temperature range

*The version letter denotes a variant with respect to electrical performance and/or encapsulation

FUNCTION

H = Combinatorial circuit

J = Bistable or multistable sequential circuit

K = Monostable sequential circuit

L = Level converter

N = Bimetastable or multimetastable sequential circuit

Q = Read/write memory circuit

R = Read-only memory circuit

S = Sense amplifier

Y = Miscellaneous

OPERATING AMBIENT TEMPERATURE RANGE

1 = 0 to + 70 °C or wider

2 = -55 to +125 °C or wider

3 = -10 to + 85 °C or wider

4 = +15 to + 55 °C or wider

5 = -25 to + 70 °C or wider

6 = -40 to + 85 °C or wider

0 = Open



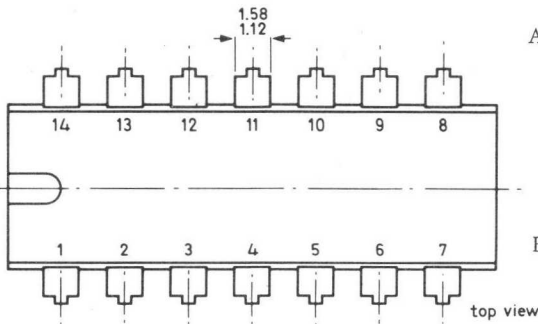
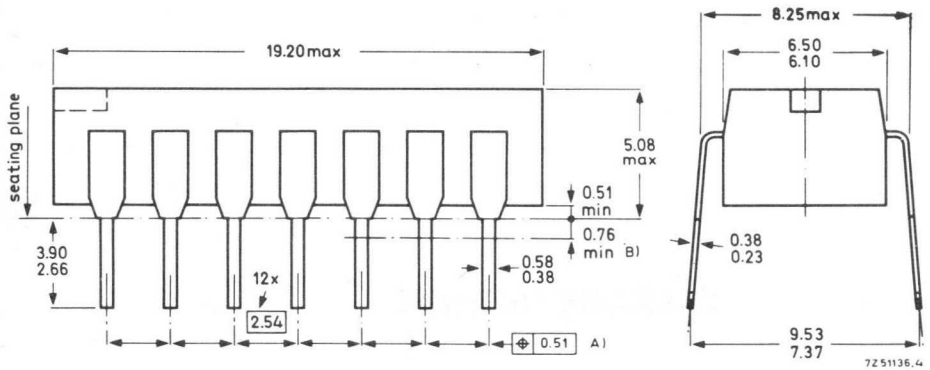
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PACKAGE OUTLINES

14 LEAD PLASTIC DUAL IN-LINE (type A)

Dimensions in mm



A) Centre-lines of all leads are within ± 0.254 mm of the nominal positions shown; in the worst case, the spacing between any two leads may deviate from nominal by ± 0.51 mm.

B) Lead spacing tolerances apply from seating plane to the line indicated.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300°C it must not be in contact for more than 10 seconds; if between 300°C and 400°C , for not more than 5 seconds.

2. By dip or wave

260°C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

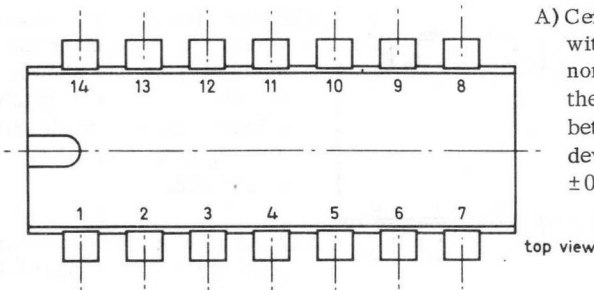
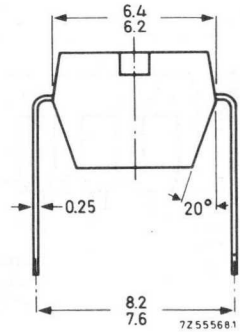
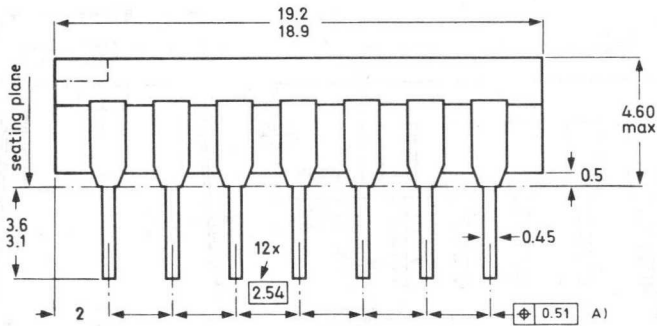
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

14 LEAD PLASTIC DUAL IN-LINE (type B)

Dimensions in mm



A) Centre-lines of all leads are within ± 0.254 mm of the nominal positions shown: in the worst case, the spacing between any two leads may deviate from nominal by ± 0.51 mm.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300°C it must not be in contact for more than 10 seconds; if between 300°C and 400°C , for more than 5 seconds.

2. By dip or wave

260°C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

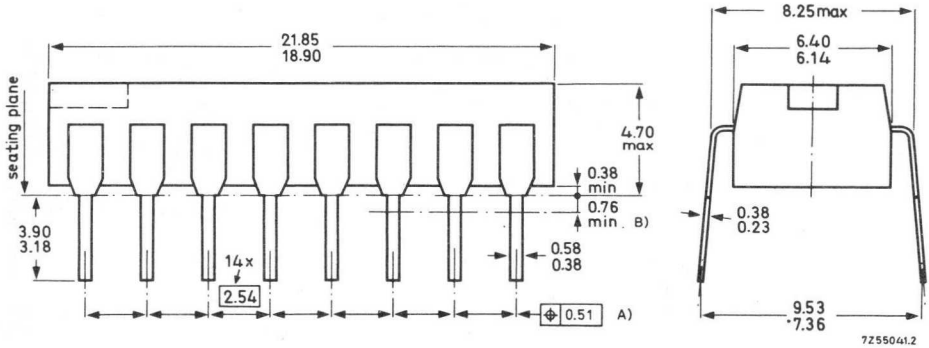
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

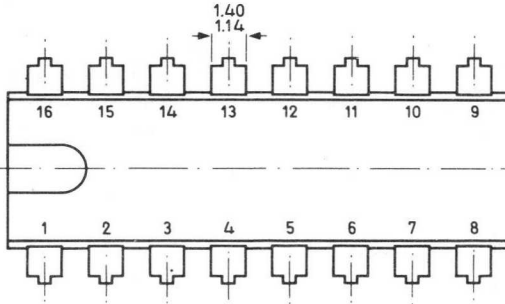
16 LEAD PLASTIC DUAL IN-LINE (type A)

Dimensions in mm



A) Centre-lines of all leads are within ± 0.254 mm of the nominal positions shown; in the worst case, the spacing between any two leads may deviate from nominal by ± 0.51 mm.

B) Lead spacing tolerances apply from seating plane to the line indicated.



top view

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300°C it must not be in contact for more than 10 seconds; if between 300°C and 400°C , for not more than 5 seconds.

2. By dip or wave

260°C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

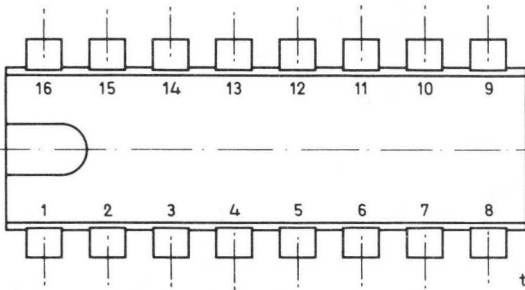
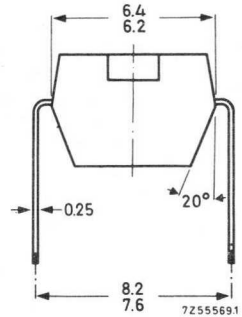
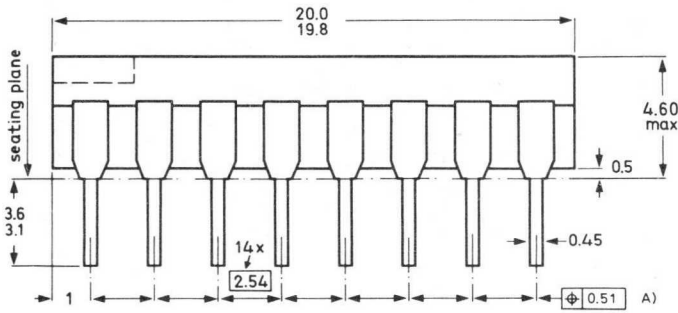
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16 LEAD PLASTIC DUAL IN-LINE (type B)

Dimensions in mm



A) Centre-lines of all leads are within ± 0.254 mm of the nominal positions shown; in the worst case, the spacing between any two leads may deviate from nominal by ± 0.51 mm.

top view

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300°C it must not be in contact for more than 10 seconds; if between 300°C and 400°C , for not more than 5 seconds.

2. By dip or wave

260°C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

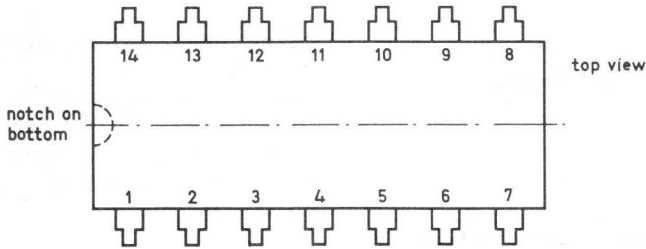
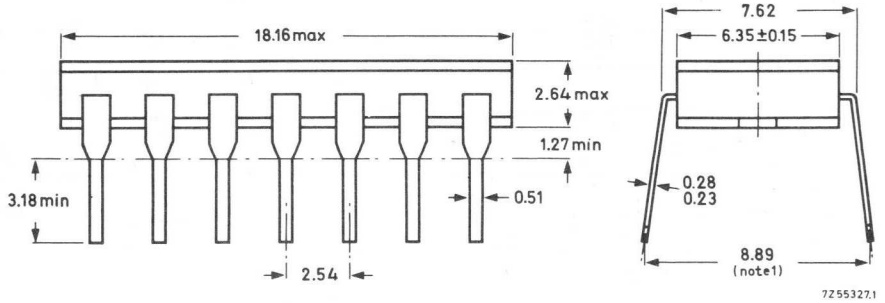
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

14 LEAD METAL-CERAMIC DUAL IN-LINE

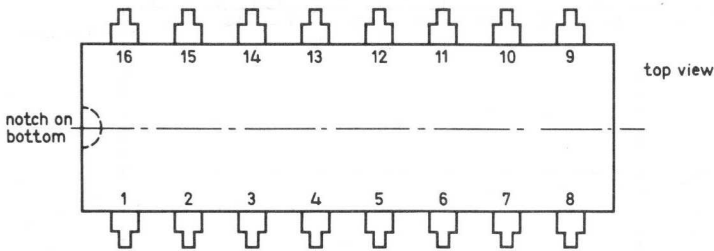
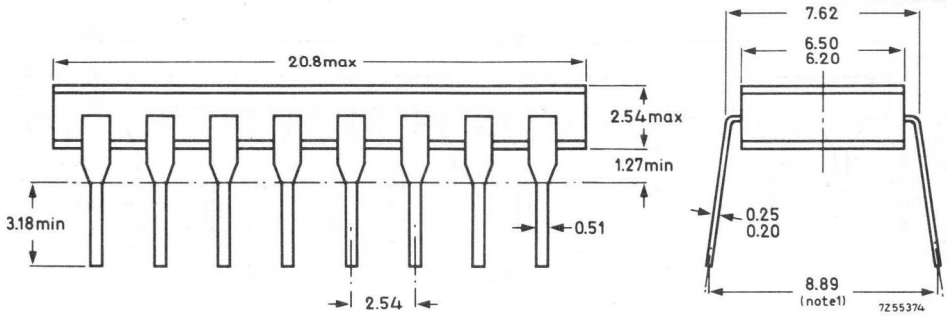
Dimensions in mm



1. Leads on opposite sides are designed to fit in holes 7.62 mm apart. They are given positive misalignment so that they grip after insertion.
2. Pin 1 is normally marked by a dot.

16 LEAD METAL-CERAMIC DUAL IN-LINE

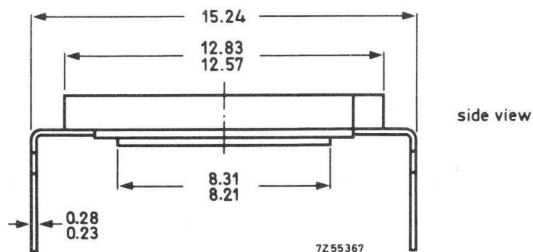
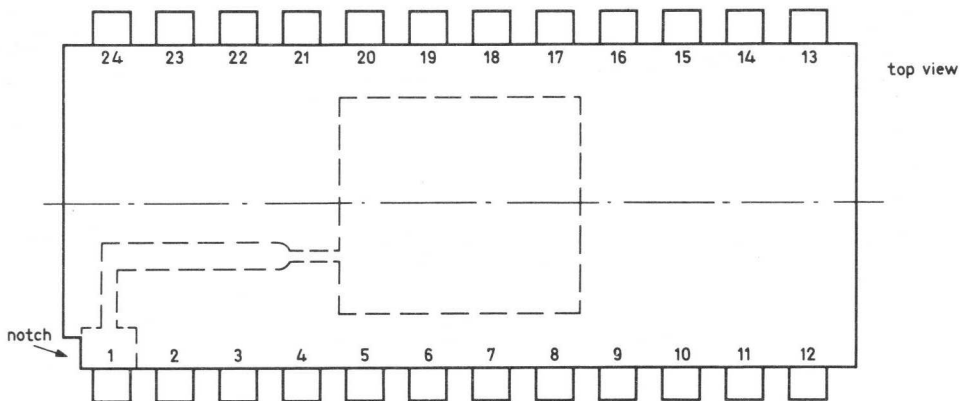
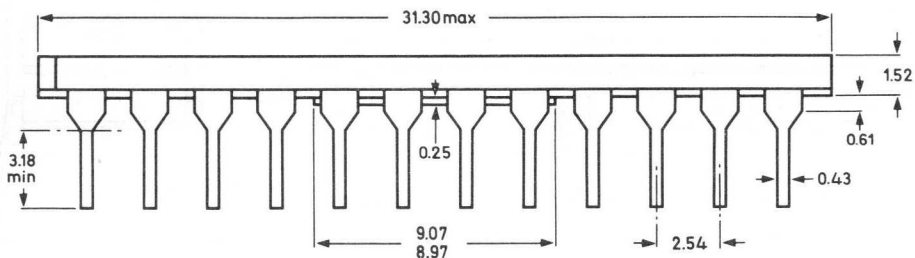
Dimensions in mm



1. Leads on opposite sides are designed to fit in holes 7.62 mm apart. They are given positive misalignment so that they grip after insertion.
2. Pin 1 is normally marked by a dot.

24 LEAD METAL-CERAMIC DUAL IN-LINE

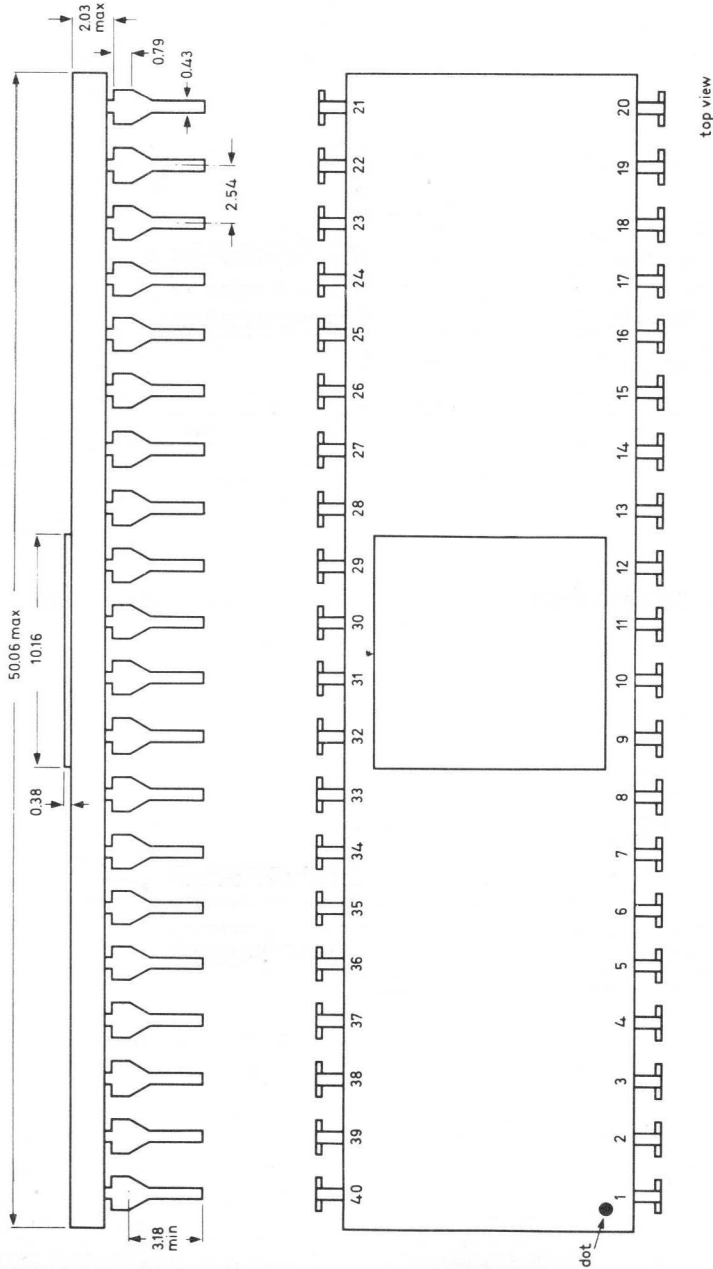
Dimensions in mm



Notes

1. Leads on opposite sides are designed to fit in holes 15.24 mm apart.
2. Pin 1 is marked by a notch and connected to the metal lid on the bottom of the package.

40 LEAD METAL-CERAMIC DUAL IN-LINE

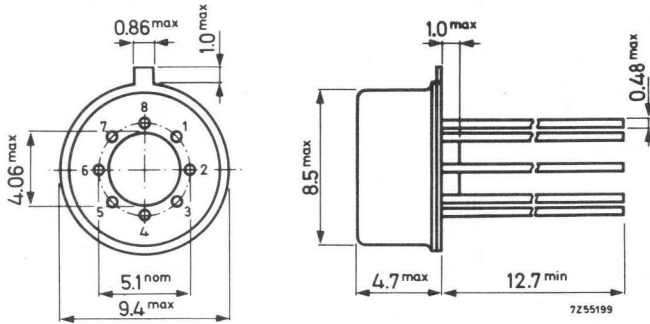


Notes

1. Leads on opposite sides are designed to fit in holes 15.24 mm apart.
2. Pin 1 is marked by a dot.
3. Dimensions in mm.

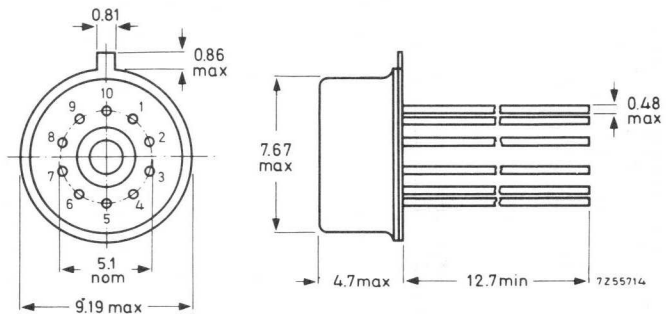
TO-99 METAL ENVELOPE

Dimensions in mm



TO-100 METAL ENVELOPE

Dimensions in mm



GATE SYMBOLS

Symbols taken from MIL-STD-806B published 26-2-1962 together with the explanation given in the MIL-STD are framed (the number in brackets refers to the section of the MIL-STD from which the extract has been made).

Other symbols and explanations are unframed.

A. LOGIC SYMBOLS (5 partial)*)

AND The symbol shown below represents the AND function (5.1).



OR The symbol shown below represents the OR function (5.2).



EXCLUSIVE-OR The symbol shown below represents the Exclusive-OR function (5.6).



STATE INDICATOR (Active) (5.3). The presence of the small circle symbol at the input(s) or output(s) of a function indicates:

- (a) Input Condition. The electrical condition at the input terminal(s) which control the active state of the respective function.
- (b) Output Condition. The electrical condition existing at the output terminal(s) of an activated function.



(5.3.1) A small circle(s) at the input(s) to any element (logical or non-logical) indicates that the relatively LOW (L) input signal activates the function. Conversely, the absence of a small circle indicates that the relatively HIGH (H) input signal activates the function.

(5.3.2) A small circle at the symbol output indicates that the output terminal of the activated function is relatively LOW (L), the absence indicates that the output terminal is relatively HIGH (H).

This small circle shall never be drawn by itself on a diagram.

On pages 4 and 5 the terms HIGH and LOW and the translation of logic notations "0" and "1" into HIGH and LOW will be elucidated.

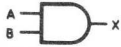
*) See appendix for drawing dimensions.

GRAPHICAL SYMBOLS

gates

EXAMPLES

AND (5.1.1)



| A | B | X |
|---|---|---|
| L | L | L |
| H | L | L |
| L | H | L |
| H | H | H |

The output is HIGH if and only if all inputs are HIGH.

(5.4)



| A | B | X |
|---|---|---|
| L | L | H |
| H | L | H |
| L | H | H |
| H | H | L |

The output is LOW if and only if all inputs are HIGH.

OR (5.2.1)



| A | B | X |
|---|---|---|
| L | L | L |
| H | L | H |
| L | H | H |
| H | H | H |

The output is HIGH if and only if any one or more of the inputs are HIGH.

(5.5)



| A | B | X |
|---|---|---|
| L | L | H |
| H | L | L |
| L | H | L |
| H | H | L |

The output is LOW if and only if any one or more of the inputs are HIGH.

EXCLUSIVE-OR (5.6.1)



| A | B | X |
|---|---|---|
| L | L | L |
| H | L | H |
| L | H | H |
| H | H | L |

The output is HIGH if and only if any one input is HIGH and all other inputs are LOW.



| A | B | X |
|---|---|---|
| L | L | H |
| H | L | L |
| L | H | L |
| H | H | H |

The output is LOW if and only if any one input is HIGH and all other inputs are LOW.

Table I, (5.7) of MIL-STD-806B, shows two-input AND and OR gate symbols with all the possible combinations of terminals with or without state indicator. It will be noted that the AND-gate symbol in the 1st column has the same function table as the OR-gate symbol in the 2nd column.

Table I

| AND | OR | Function Table | | |
|----------------|----------------|----------------|---|---|
| | | A | B | X |
| | | H | H | H |
| | | H | L | L |
| | | L | H | L |
| | | L | L | L |
| | | H | H | L |
| | | H | L | L |
| | | L | H | H |
| | | L | L | L |
| | | H | H | L |
| | | H | L | L |
| | | L | H | L |
| | | L | L | L |
| | See note 1 | H | H | L |
| | | H | L | L |
| | | L | H | L |
| | | L | L | H |
| | | H | H | H |
| | | H | L | H |
| | | L | H | H |
| | | L | L | L |
| | | H | H | H |
| | | H | L | H |
| | | L | H | L |
| | | L | L | H |
| See note 2 | | H | H | L |
| | | H | L | H |
| | | L | H | H |
| | | L | L | H |

Note 1. In literature often described as NOR.

Note 2. In literature often described as NAND.









Although the MIL-STD-806B does not use the expression NAND and NOR they are referred to because these terms are commonly used.

GRAPHICAL SYMBOLS

gates

Although MIL-STD-806B shows the EXCLUSIVE-OR symbol only without state indicator, for the sake of completeness Table II shows it with all the possible combinations of terminals with or without state indicator. It will be noted from the table that one function table (3rd column) is applicable to four symbols.

Table II

| Symbol | Symbol | Function Table | | | | | | | | | | | | | | | |
|-----------------------------------------------------------------------------------|-----------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
|  |  | <table border="1"> <thead> <tr> <th>A</th> <th>B</th> <th>X</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td>L</td> </tr> <tr> <td>H</td> <td>L</td> <td>H</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> </tr> <tr> <td>L</td> <td>L</td> <td>L</td> </tr> </tbody> </table> | A | B | X | H | H | L | H | L | H | L | H | H | L | L | L |
| A | B | X | | | | | | | | | | | | | | | |
| H | H | L | | | | | | | | | | | | | | | |
| H | L | H | | | | | | | | | | | | | | | |
| L | H | H | | | | | | | | | | | | | | | |
| L | L | L | | | | | | | | | | | | | | | |
|  |  | | | | | | | | | | | | | | | | |
|  |  | <table border="1"> <thead> <tr> <th>A</th> <th>B</th> <th>X</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td>H</td> </tr> <tr> <td>H</td> <td>L</td> <td>L</td> </tr> <tr> <td>L</td> <td>H</td> <td>L</td> </tr> <tr> <td>L</td> <td>L</td> <td>H</td> </tr> </tbody> </table> | A | B | X | H | H | H | H | L | L | L | H | L | L | L | H |
| A | B | X | | | | | | | | | | | | | | | |
| H | H | H | | | | | | | | | | | | | | | |
| H | L | L | | | | | | | | | | | | | | | |
| L | H | L | | | | | | | | | | | | | | | |
| L | L | H | | | | | | | | | | | | | | | |
|  |  | | | | | | | | | | | | | | | | |

See note 3

Note 3. In literature described as BINARY COMPARATOR

HIGH AND LOW

The terms relatively HIGH and relatively LOW are explained with reference to the following three examples

| | | |
|------------------|-------------------|-----------------|
| +5 volts = HIGH | | |
| +0.5 volts = LOW | +0.5 volts = HIGH | |
| | -5 volts = LOW | -5 volts = HIGH |
| | | -10 volts = LOW |

It can be seen that the more positive voltage is termed relatively HIGH and the less positive is termed relatively LOW. These terms are abbreviated to HIGH (H) and LOW (L) respectively and are used throughout MIL-STD-806B.

LOGICAL "1" AND "0"

In deviation from MIL-STD-806B Appendix B, which for the sake of fully general systems applicability (page 17, fig.5) refrains from establishing any fixed relations between "active-nonactive" and "logical 0-1", we have in the following rules chosen to relate "active" to "1" and "non-active" to "0", as being most suitable when regarding each gate function separately.


"0" at the input always symbolizes the non-activating signal or, at the output, the signal from a non-activated gate;


"1" at the input always symbolizes the activating signal or, at the output, the signal from an activated gate. (The expression activated does not mean that current must flow at the respective terminal(s) but refers to the influence of inputs upon the output(s) of the respective gates.)

The translation from the logic notation into the electrical levels HIGH and LOW is explained with the aid of two examples, one without state indicators and one with. In each case a two-input AND gate truth table is drawn up, and a function table corresponding to the symbol is given so that a direct comparison can be made.

| For inputs or outputs <u>without</u> state indicator | <u>with</u> state indicator |
|------------------------------------------------------|-----------------------------|
| Logic 1 = HIGH (H) | Logic 1 = LOW (L) |
| Logic 0 = LOW (L) | Logic 0 = HIGH (H) |

EXAMPLE

| Truth Table | | | Symbol | Function Table | | |
|-------------|---|--------|-------------------------------------------------------------------------------------|----------------|---|--------|
| Inputs | | Output | | Inputs | | Output |
| A | B | X | | | | |
| 0 | 0 | 0 |  | L | L | L |
| 1 | 0 | 0 | | H | L | L |
| 0 | 1 | 0 | | L | H | L |
| 1 | 1 | 1 | | H | H | H |

| Truth Table | | | Symbol | Function Table | | |
|-------------|---|--------|-------------------------------------------------------------------------------------|----------------|---|--------|
| Inputs | | Output | | Inputs | | Output |
| A | B | X | | | | |
| 0 | 0 | 0 |  | H | L | H |
| 1 | 0 | 0 | | L | L | H |
| 0 | 1 | 0 | | H | H | H |
| 1 | 1 | 1 | | L | H | L |

B. DRAWING PRACTICE

Any of the symbols from Tables I and II may be used in diagrams, bearing in mind the following general rule.

Every signal line shall preferably have at each end either a state indicator circle, or no state indicator circle.

An example showing how compliance with this rule can be achieved is given in the following sketch.

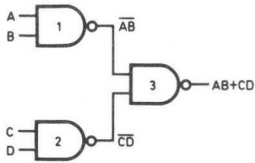


fig. 1

should be drawn as

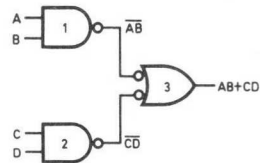


fig. 2

A further advantage of drawing the symbol of gate 3 as in fig. 2 is that it is more apparent that it behaves as an OR function than when drawn as in fig. 1 (cf. table I).

When state indicators are not used no more than four input lines should be drawn at the input side of the symbol (see fig. 3).

When state indicators are used no more than three input lines should be drawn at the input side (see fig. 4).

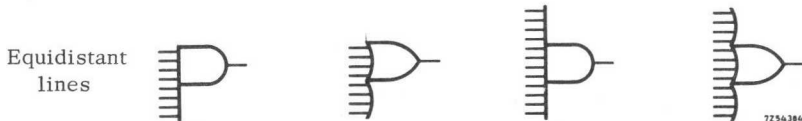
Following these rules will help to avoid unnecessary crowding of lines in the drawing. When more input lines are needed the input side of the symbol can be extended in any of the ways indicated in fig. 5.



fig. 3



fig. 4



Equidistant lines

fig. 5

EXTENDED INPUTS

If the number of inputs to an expandable gate is extended by means of an expander circuit, the output line(s) of the expander is (are) connected to the specific expansion input(s) of the gate as drawn below.

The expander symbol shall be drawn to the same dimensions as the gate symbol; however, two filled arrows shall be drawn on each connection line, one arrow close to the expander symbol and another close to the gate symbol.



f = gate

E = expander

A signal line provided with arrows need not imply the usual logic levels. Generally it should not be connected to "normal" inputs or outputs of gates.

C. OUTPUT COMBINATIONS (6.3)

Where functions have the capability of being combined according to the AND (or OR) function, simply by having the outputs connected, that capability shall be shown by enveloping the branched connection with a smaller sized AND or OR symbol.

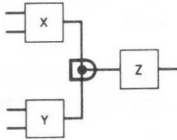


Note: These connections of outputs are often described in the literature as "WIRED-OR".

GRAPHICAL SYMBOLS

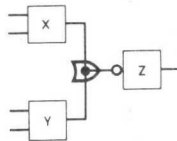
gates

EXAMPLES



The function Z is activated on its input by a HIGH level (because a state indicator is not applied there) if and only if both outputs of functions X and Y are HIGH.

The branched connection shall therefore be enveloped by a small-sized AND symbol.



The function Z is activated on its input by a LOW level (because a state indicator is applied there) if and only if one or both outputs of the functions X and Y are LOW.

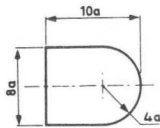
The branched connection shall therefore be enveloped by a small-sized OR symbol.

It should be noted that it would seem necessary to use state indicators on all terminals of the Dot "OR" symbol for correct interpretation of the circuit. However it is not usual to use state indicators on Dot symbols.

APPENDIX

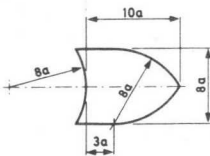
DRAWING DIMENSIONS

Ratio of dimensions of symbols may be derived from the drawings shown.

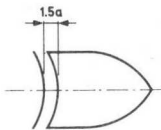


AND

Symbols enveloping a branched connection shall have half the dimensions of the fundamental symbols.



OR



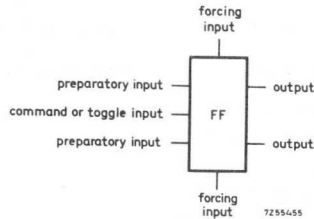
EXCLUSIVE -OR



STATE INDICATOR

FLIP-FLOP SYMBOLS

1. GENERAL SYMBOL



2. DEFINITIONS

Active or "1" state of an input signal.

That state (either a level or a transition from one level to the other) which causes, directly or indirectly, a change of the output state. Conversely, the inactive or "0" state of an input signal is that state which does not cause an output change.

Output state.

There may be one output terminal (Q) or two (Q₁ and Q₂). If there are two, the "output state" refers to the states of the signals at Q₁ and Q₂; since these are normally complementary, the state at Q₁ is usually considered to represent the output state.

Preparatory input terminal (e.g. J, K, D)

An input terminal to which application of an active signal does not directly cause a change of the output state but prepares the circuit for such a change.

Command input terminal (T)

An input terminal to which application of an active signal causes the output to assume the state corresponding to the preparatory inputs. It is also known as the "clock input terminal".

Toggle input terminal (T)

An input terminal at which an active transition from one level to the other directly causes a change of the output state.

Forcing input terminal (S₁ = "direct set", S₂ = "direct reset")

An input terminal at which application of an active signal directly causes the output to assume a specific state, irrespective of the states of other input terminals.

GRAPHICAL SYMBOLS

flip-flops

3. LOCATION OF TERMINALS AND USE OF POLARITY STATE INDICATOR, SHOWN BY EXAMPLES

Legend:

H = HIGH level

L = LOW level

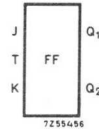
L→H = transition from LOW level to HIGH level

H→L = transition from HIGH level to LOW level

X = state (level or transition) has no influence

? = indeterminate, unless exact timing of relevant input signals (e.g. S₁ and S₂) is known.

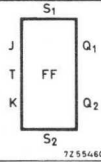
3.1. JK flip-flop without forcing inputs



An active ("1") signal at J, together with an inactive ("0") signal at K and an active signal transition at T, causes the "1" state at Q₁ and the "0" state at Q₂.

| Symbol | Function table | | | Q ₁ | Q ₂ |
|--------|----------------|---|-----|----------------|----------------|
| | J | K | T | | |
| | H | L | L→H | H | L |
| | L | H | L→H | L | H |
| | H | H | L→H | reversed | |
| | L | L | L→H | no change | |
| | X | X | H→L | no change | |
| | H | L | H→L | H | L |
| | L | H | H→L | L | H |
| | H | H | H→L | reversed | |
| | L | L | H→L | no change | |
| | X | X | L→H | no change | |
| | L | H | H→L | H | L |
| | H | L | H→L | L | H |
| | L | L | H→L | reversed | |
| | H | H | H→L | no change | |
| | X | X | L→H | no change | |

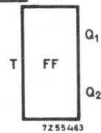
3.2. JK flip-flop with forcing inputs



Irrespective of the states at J, K and T: an active ("1") signal at S_1 , together with an inactive ("0") signal at S_2 , causes Q_1 to assume the "1" and Q_2 the "0" state

| Symbol | Function table | | | | | |
|--------|----------------|---|-----|-------|-------|-------------|
| | J | K | T | S_1 | S_2 | Q_1 Q_2 |
| | X | X | X | H | L | H L |
| | X | X | X | L | H | L H |
| | X | X | X | H | H | ? ? |
| | H | L | L→H | L | L | H L |
| | L | H | L→H | L | L | L H |
| | H | H | L→H | L | L | reversed |
| | L | L | L→H | L | L | no change |
| | X | X | H→L | L | L | no change |
| | X | X | X | L | H | H L |
| | X | X | X | H | L | L H |
| | X | X | X | L | L | ? ? |
| | H | L | H→L | H | H | H L |
| | L | H | H→L | H | H | L H |
| | H | H | H→L | H | H | reversed |
| | L | L | H→L | H | H | no change |
| | X | X | L→H | H | H | no change |

3.3. T flip-flop ("Toggle")



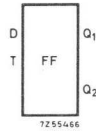
An active ("1") signal transition at T causes the complementary states at Q_1 and Q_2 to reverse.

| Symbol | Function table | |
|--------|----------------|-----------------------|
| | T | Q_1 Q_2 |
| | L→H H→L | reversed no change |
| | H→L L→H | reversed no change |

GRAPHICAL SYMBOLS

flip-flops

3.4. Edge-triggered D flip-flop

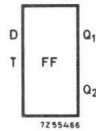


An active ("1") signal transition at T causes Q_1 to assume the same state as D. I.e., if D is in the "1" state during the active transition at T, Q_1 also assumes the "1" state; if D is "0", Q_1 also becomes "0". The output state will remain unchanged until the next active transition at T occurs.

| Symbol | Function table | | | Q_1 Q_2 |
|--------|----------------|-------|------------|-------------|
| | D | T | | |
| | | level | transition | |
| | H | | L→H | H L |
| L | | L→H | L H | |
| X | X | | no change | |
| X | | H→L | no change | |
| | H | | H→L | H L |
| L | | H→L | L H | |
| X | X | | no change | |
| X | | L→H | no change | |
| | L | | H→L | H L |
| H | | H→L | L H | |
| X | X | | no change | |
| X | | L→H | no change | |

3.5. Level-operated ("gated") D flip-flop, or "Bistable latch".

(Graphical symbol equal to 3.4.)



As long as the signal at T is at its active ("1") level, the signal at Q₁ follows the signal at D. When the signal at T changes to its inactive ("0") level, the signal at Q₁ latches (Subsequent changes in D cause no change in Q₁). Q₁ unlatches when the signal at T returns to its active level.

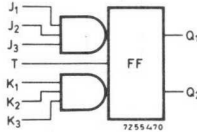
| Symbol | Function table | | | |
|--------|----------------|-------|-----------------------|-------------------------------|
| | D | T | | Q ₁ Q ₂ |
| | | level | subsequent transition | |
| | H | H | | H L |
| | H | H | H→L | H L |
| | L | H | | L H |
| | L | H | H→L | L H |
| | X | L | | no change |
| | H | L | | H L |
| | H | L | L→H | H L |
| | L | L | | L H |
| | L | L | L→H | L H |
| | X | H | | no change |
| | L | L | | H L |
| | L | L | L→H | H L |
| | H | L | | L H |
| | H | L | L→H | L H |
| | X | H | | no change |

GRAPHICAL SYMBOLS

flip-flops

4. MULTIPLE INPUTS

Where inputs are functionally combined by an input gate, the connecting line between the gate symbol and the flip-flop symbol may conveniently be omitted, as shown in the drawing.

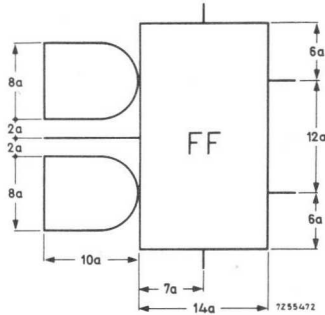


5. TIME DELAY CIRCUIT

The following time delay symbol (MIL-STD-806 B, 5.15) is used in some logic flip-flop block diagrams:



6. DRAWING DIMENSIONS (to MIL-STD-806 B)



The ratio of dimensions is given in the drawing above.

For dimensions of gates and state-indicators see "Appendix", page 8.

RATING SYSTEMS

ACCORDING TO I.E.C. PUBLICATION 134

1. DEFINITIONS OF TERMS USED

- 1.1 Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note: This definition excludes inductors, capacitors, resistors and similar components.

- 1.2 Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

- 1.3 Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

- 1.4 Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note: Limiting conditions may be either maxima or minima.

- 1.5 Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note: The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

2. ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

p. t. o.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

3. DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

4. DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

NOTE

It is common use to apply the Absolute Maximum System in semiconductor published data.

LETTER SYMBOLS FOR DIGITAL INTEGRATED CIRCUITS

(Additional symbols for MOS circuits on page 4)

1. General

The voltages and currents are related to the terminals to which they are applied or at which they appear. Each terminal is indicated by a letter relating to the function of the device or the function of the pertinent signal.

In order to avoid confusion by any ambiguity in logical conventions, signal levels are indicated by H (= HIGH, for the more positive potential) and L (= LOW, for the less positive potential). Where circuit functions or logical equations are involved, the logical convention is mentioned specifically (for positive logic: H = 1, and for negative logic: H = 0).

2. Terminal designations

- D = D input of D type latch flip-flops
- E = expander input (if necessary, this letter may be followed by an index, e.g. E₁ or E₂ or by one of the input letters, such as EG = gate expander input)
- G = gate input
- J, K = J, K input of JK flip-flops
- N = negative supply
- P = positive supply
- Q = output
- S = direct SET input
- T = trigger (or toggle) input
- ∅ = common supply return and voltage reference

3. Subscript sequence for voltages and currents

First subscript : terminal designation letter.

Second subscript: H (for HIGH) or L (for LOW), if applicable.

Third subscript : min or max, if applicable.

Examples: V_P, I_{QL}, V_{QHmin}, I_{PH} (in the latter case H denotes that the output level is HIGH).

4. Polarity of current and voltage

A current is defined as positive when its conventional direction of flow is into the device.

Unless otherwise specified, a voltage is measured with respect to the reference terminal (∅). Its polarity is defined as positive when the potential is higher than that of the reference terminal.

5. Time designations

If required for reasons of unambiguity, the related terminals may be included in the designations given below (e.g. t_{fQ1}).

t_f = fall time (transition from HIGH to LOW, see Fig. 1)

t_H = signal HIGH duration (Fig. 1)

t_L = signal LOW duration (Fig. 1)

t_{pd} = average propagation delay time, defined as $\frac{t_{pdr} + t_{pdf}}{2}$

t_{pdf} = fall propagation delay time (output voltage falling, see Fig. 2)

t_{pdr} = rise propagation delay time (output voltage rising, see Fig. 2)

t_r = rise time (transition from LOW to HIGH, see Fig. 1)

t_{sc} = duration of short circuit (from relevant terminal to common return terminal)

V_{pd} = reference voltage level for propagation delay measurement

Fig. 1.

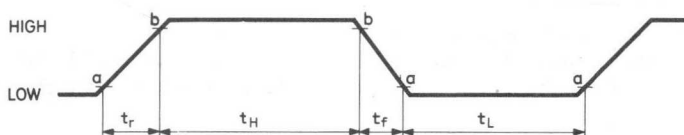
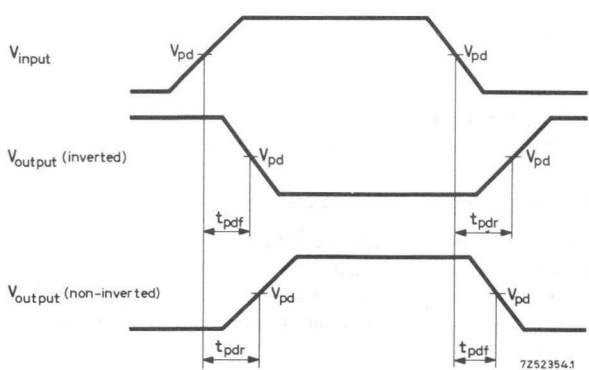


Fig. 2.



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6. Other designations

- i. c. = internally connected
Terminals with this indication should be left open. Otherwise correct working cannot be ensured; the device may even be damaged
- n. c. = not connected internally
It is recommended not to use these terminals for any connection
- I_p = supply current
The logic state of the device indicated by H or L is normally referred to the output level, unless otherwise specified
- I_{pmax} = supply current
Maximum d. c. value under defined conditions
- M = d. c. noise margin
- M_L = d. c. noise margin, signal level LOW
(defined as: $M_L = V_{GLmax} - V_{QLmax}$ under defined loading, temperature and supply voltage conditions)
- M_H = d. c. noise margin, signal level HIGH
(calculated from: $M_H = V_{QHmin} - V_{GHmin}$ under defined loading, temperature and supply voltage conditions)
- N_a = available d. c. fan-out (defined as: $N_a = \frac{I_{QLmax}}{-I_{GLmax}}$ under defined temperature and supply voltage conditions)
- $P_H; P_L$ = power consumption, defined as the product of the supply current(s) and of the corresponding supply voltage(s). The logical state of the device, indicated by a letter index H or L, is normally referred to the output level, unless otherwise specified
- P_{av} = average power consumption at 50% duty cycle, unless otherwise specified. It is defined as: $P_{av} = V_p \cdot \frac{I_{PH} + I_{PL}}{2}$
- P_{tot} = power dissipation, defined as the total power dissipated by the device. It is the sum of the products of all currents and voltages at each of the input, output and supply terminals, their polarities being taken into account. The logical state of the device indicated by a letter index H or L is normally referred to the output level, unless otherwise specified
- T_{amb} = operating ambient temperature, i. e. the temperature of the free air in which the normally operating device is placed without external heat conduction, unless otherwise specified
- T_{stg} = storage temperature, i. e. the temperature of the ambient medium in which the non-operating device is stored

LETTER SYMBOLS

digital circuits

V_{GLmax} = input voltage LOW at terminal G. With the specified level applied to the input of an inverting gate the output level will not be lower than the specified value V_{QHmin} at given I_{QH} .

V_{GHmin} = input voltage HIGH at terminal G. With the specified level applied to the input of an inverting gate the output level will not exceed the specified value V_{QLmax} at given I_{QL} .

ΔV_Q = change of output voltage caused by a specified change of output current

ADDITIONAL SYMBOLS FOR MOS CIRCUITS

2a. Terminal designations

- I = shift register input
- A = address input or decode matrix input
- ϕ = clock input
- WC = write control input
- D = data input
- CD = chip disable input
- Q = output
- C = chip inhibit input
- P_O = common supply return and voltage reference
- $P_1, P_2, \text{etc.}$ = supply input

3a. Subscript sequence for voltages

First (with or without second) subscript: terminal designation
Second or third subscript: H (HIGH) or L (LOW) if applicable

5a. Time designations

Details are described in the data sheets

6a. Other designations

- M_L = d.c. noise margin LOW ($M_L = V_{input L max} - V_{output L max}$)
- M_H = d.c. noise margin HIGH ($M_H = V_{output H min} - V_{input H min}$)
- R_{QH} = output resistance HIGH
- R_{QL} = output resistance LOW
- P_{av} = average power consumption

LETTER SYMBOLS FOR LINEAR INTEGRATED CIRCUITS

General

The voltages and currents are normally related to the terminals to which they are applied or at which they appear. Each terminal is indicated by a number. In appropriate cases voltages, currents etc. pertinent to one or more of the circuit elements (transistors, diodes) are given in which case symbols are based on the recommendations as published in I.E.C. Publication 148.

Quantity symbols

1. Instantaneous values of current, voltage and power, which vary with time are represented by the appropriate lower case letter.

Examples: i , v , p

2. Maximum (peak), average, d.c. and root-mean-square values are represented by the appropriate upper case letter.

Examples: I , V , P

Polarity of current and voltage

A current is defined to be positive when its conventional direction of flow is into the device.

A voltage is measured with respect to the reference terminal, which is indicated by the subscripts. Its polarity is defined to be positive when the potential is higher than that of the reference terminal.

Subscripts

For currents the number behind the quantity symbol indicates the terminal carrying the current.

Examples: I_2 , i_{14}

For voltages normally two number subscripts are used, connected by a hyphen. The first number indicates the terminal at which the voltage is measured and the second subscript the reference terminal.

Where there is no possibility of confusion the second subscript may be omitted.

Examples: V_{2-12} , v_{14-2} , V_5 , v_8

LETTER SYMBOLS

linear circuits

To distinguish between maximum (peak), average, d.c. and root-mean-square values the following subscripts are added:

For maximum (peak) values : M or m
For average values : AV or av
For root-mean-square values: (RMS) or (rms)
For d.c. values : no additional subscripts

The upper case subscripts indicate total values.

The lower case subscripts indicate values of varying components:

Examples: I_2 , I_{2AV} , $I_{2(rms)}$, $I_{2(RMS)}$

If in appropriate cases quantity symbols are pertinent to single elements of a circuit (transistors or diodes), the normal subscripts for semiconductor devices can be used.

Examples: V_{CBO} , V_{be} , V_{CES} , I_C
 V_{DSS} , V_{GS} , I_D

List of subscripts:

E, e = Emitter terminal
B, b = Base terminal for bipolar transistors,
Substrate for MOS devices
C, c = Collector terminal
D, d = Drain terminal
G, g = Gate terminal
S, s = Source terminal for MOS devices
Substrate for bipolar transistor circuits
(BR) = Break-down
M, m = Maximum (peak) value
AV, av = Average value
(RMS), (rms) = R.M.S. value

Electrical Parameter Symbols

1. The values of four pole matrix parameters or other resistances, impedances, admittances, etc., inherent in the device, are represented by the lower case symbol with appropriate subscript.

Examples: h_i , z_f , y_o , k_r

Subscripts for Parameter Symbols

1. The static values of parameters are indicated by upper case subscripts.

Examples: h_{FE} , h_I

2. The small signal values of parameters are indicated by lower case subscripts.

Examples: h_i , z_o

3. The first subscript, in matrix notation identifies the element of the four pole matrix.

- i (for 11) = input
- o (for 22) = output
- f (for 21) = forward transfer
- r (for 12) = reverse transfer

$$\text{Examples: } V_1 = h_i I_1 + h_r V_2$$

$$I_2 = h_f I_1 + h_o V_2$$

The voltage and current symbols in matrix notation are indicated by a single digit subscript.

The subscript 1 = input; the subscript 2 = output.

The voltages and currents in these equations may be complex quantities.

4. A second subscript is used only for separate circuit elements (e.g. transistors) to identify the circuit configuration:

- e = common emitter
- b = common base
- c = common collector

5. If it is necessary to distinguish between real and imaginary parts of the four pole parameters, the following notation may be used:

- $R_e (h_i)$ etc. ... for the real part
- $I_m (h_i)$ etc. ... for the imaginary part

LIST OF LETTER SYMBOLS IN ALPHABETICAL ORDER

| Letter symbol | Definition |
|--------------------------------------|--------------------------------------------------------------|
| B | Bandwidth |
| b_i, b_o | Input, respectively output susceptance |
| C_i, C_o | Input, respectively output capacitance |
| CMRR | Common-mode rejection ratio |
| d | Distortion |
| F | Noise figure |
| f | Frequency |
| f_c | Cut-off frequency |
| f_o | Centre frequency, intermediate frequency |
| f_m | Modulation frequency |
| f_T | Transition frequency |
| g_i, g_o | Input, respectively output conductance |
| G_p | Power gain |
| G_{tr} | Transducer gain |
| G_v | Voltage gain |
| $h_F, h_{FB}, h_{FC}, h_{FE}$ | DC current gain (output voltage held constant) |
| $h_f, h_{fb}, h_{fc}, h_{fe}$ | Small signal current gain (output short-circuited to a.c.) |
| $I_3, I_B, I_C, I_E, I_D, I_Q, I_S$ | Total d.c. current |
| $i_3, i_B, i_C, i_E, i_D, i_G, i_S$ | Instantaneous total value of the current |
| $I_{3AV}, I_{BAV}, I_{CAV}, I_{EAV}$ | Total average current |
| $I_{3M}, I_{BM}, I_{CM}, I_{EM}$ | Maximum (peak) value of the total current |
| $I_{3m}, I_{bm}, I_{cm}, I_{em}$ | Maximum (peak) value of the varying component of the current |
| I_{CBO} | Collector cut-off current (open emitter) |
| I_{CS} | Collector-substrate leakage current |
| I_{DSS} | Drain cut-off current (source short-circuited to gate) |

LETTER SYMBOLS

linear circuits

| Letter symbol | Definition |
|---------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| I_{EBO} | Emitter cut-off current |
| I_I, I_i | Input current of a specified circuit |
| I_{io} | Input offset current |
| I_O, I_o | Output current of a specified circuit |
| I_{OM} | Peak value of output current |
| $I_{o(p-p)}$ | Peak to peak value of output current |
| I_{tot} | Total supply current |
| K_f | Small signal voltage gain |
| K_O | Output impedance (see K parameters) |
| K_R | Reverse current transfer ratio |
| M | Modulation depth |
| P_i, P_o | Input, respectively output power of a specified circuit |
| P_{tot} | Total power dissipation in the device |
| R_i, R_o | Input, respectively output resistance of a specified circuit |
| R_L | Load resistance |
| R_S | Source resistance |
| R_{th} | Thermal resistance |
| SVRR | Supply voltage rejection ratio |
| T_{amb} | Ambient temperature |
| T_{case} | Case temperature |
| T_{stg} | Storage temperature |
| $V_3, V_{3-4}, V_{BE}, V_{CB}$ | Total value of the voltage (d.c.) |
| $v_3, v_{3-4}, v_{BE}, v_{CB}$ | Instantaneous value of the total voltage |
| V_{BEsat}, V_{CEsat} | Saturation voltage at specified bottoming conditions |
| $V_{(BR)CBO}, V_{(BR)CEO},$ $V_{(BR)EBO}$ | Breakdown voltage between the terminal of the first subscript and the reference terminal (second subscript) when the third terminal is open circuited |
| $V_{(BR)CS}$ | Collector to substrate breakdown voltage |
| $V_{CBO}, V_{CEO}, V_{EBO}, V_{CS},$ V_{1-3} | Voltage of the terminal indicated with respect to the reference terminal (second subscript) |

LETTER SYMBOLS

linear circuits

| Letter symbol | Definition |
|----------------------------------------------|----------------------------------------------------------------|
| V_i, V_o | Input, respectively output voltage of a specified circuit |
| V_{io} | Input offset voltage |
| $V_{i \text{ lim}}$ | Input voltage at which limiting starts |
| V_N | Negative supply voltage |
| V_P | Positive supply voltage |
| V_n | Noise voltage |
| Y_i, Y_f, Y_o, Y_r | Input, transfer, output and feedback admittance |
| Z_i, Z_o | Input, respectively output impedance |
| η | Efficiency |
| $\varphi_i, \varphi_f, \varphi_o, \varphi_r$ | Phase angle of input, transfer, output and feedback admittance |

DTL

FC family



1000
1000
1000
1000
1000

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

NAND GATES

| | non- R_C | R_C |
|------------------------------|------------|--------|
| Single 8-input NAND gate | FCH101 | FCH111 |
| Dual 4-input NAND gate | FCH121 | FCH131 |
| Triple 3-3-2-input NAND gate | FCH141 | FCH161 |
| Triple 3-input NAND gate | FCH151 | FCH171 |
| Quadruple 2-input NAND gate | FCH181 | FCH191 |
| Sextuple inverter | FCH201 | FCH211 |

QUICK REFERENCE DATA

| | | |
|--------------------------------------------------------------------------------------------|-----------------------------|-----------------|
| Supply voltage | V_P | $6.0 \pm 5\% V$ |
| Operating ambient temperature range | T_{amb} | 0 to +75 °C |
| Average propagation delay time N = 6, $C_W = 60 \text{ pF}$, $T_{amb} = 25 \text{ °C}$ | t_{pd} | typ. 30 ns |
| Available d.c. fan out $T_{amb} = 0 \text{ to } +75 \text{ °C}$ | N_a | ≥ 8 |
| D.C. noise margin $T_{amb} = 25 \text{ °C}$ | M_L | typ. 1.2 V |
| Power consumption per gate 50% duty cycle, $T_{amb} = 25 \text{ °C}$ | non- R_C gate P_{av} | typ. 7 mW |
| | R_C gate P_{av} | typ. 11 mW |

The FC family includes twelve NAND packages offering a wide selection of circuit configurations. It includes gate types with as well as without a collector resistor, ensuring optimum equipment design.

The fan-in of the circuits can easily be expanded by means of a diode array.

The outputs of these gates may be interconnected to perform the AND-OR-NOT function.

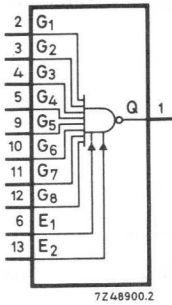
PACKAGE OUTLINE: 14 lead plastic dual in-line (type A). (See General Section)

FCH101 to 211

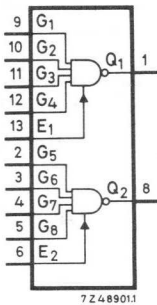
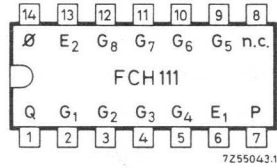
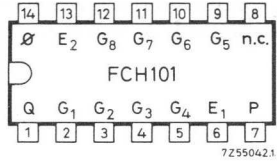
NAND gates

FC family

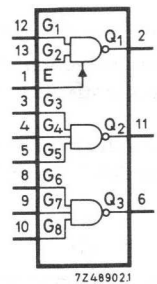
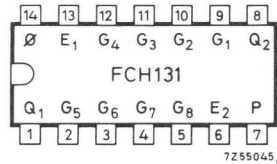
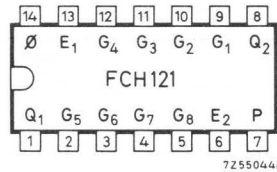
standard temperature range



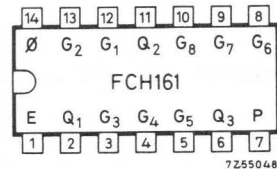
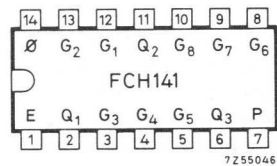
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FCH111 (R_C)

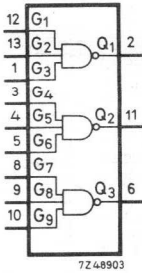


FCH121 (non- R_C)
FCH131 (R_C)

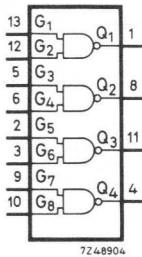
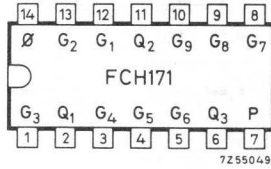
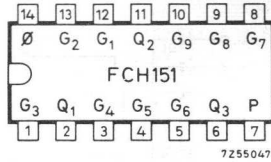


FCH141 (non- R_C)
FCH161 (R_C)

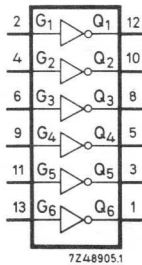
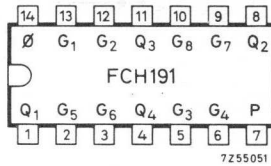
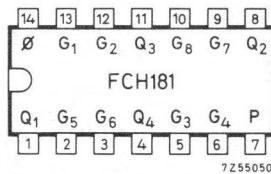




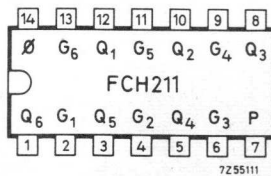
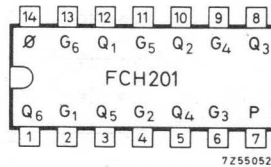
FCH151 (non- R_C)
FCH171 (R_C)



FCH181 (non- R_C)
FCH191 (R_C)



FCH201 (non- R_C)
FCH211 (R_C)



FCH101 to 211

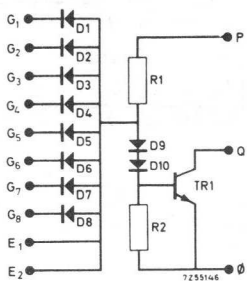
NAND gates

FC family

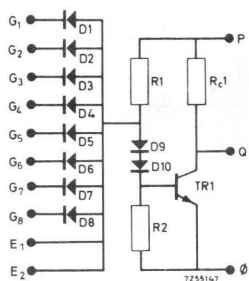
standard temperature range

CIRCUIT DIAGRAMS

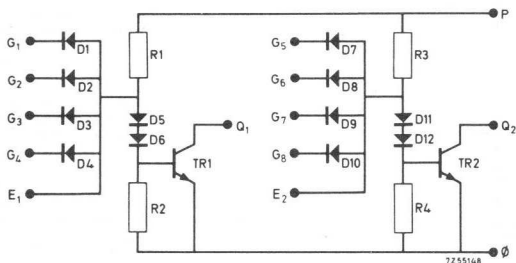
FCH101



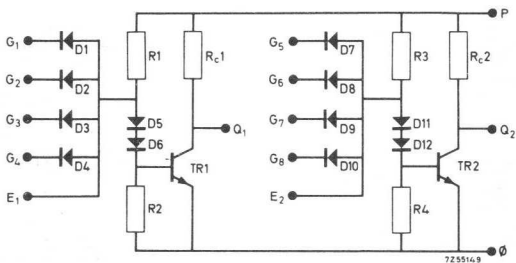
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FCH121

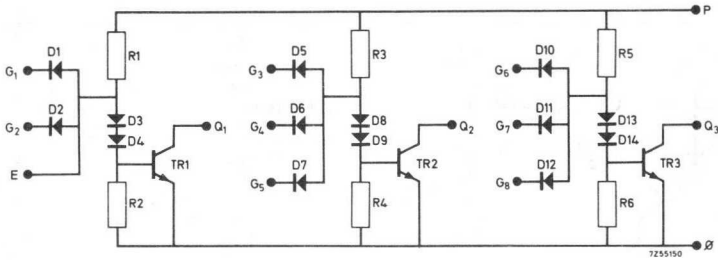


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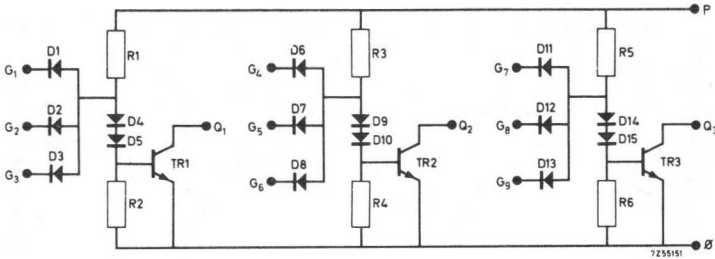


CIRCUIT DIAGRAMS (continued)

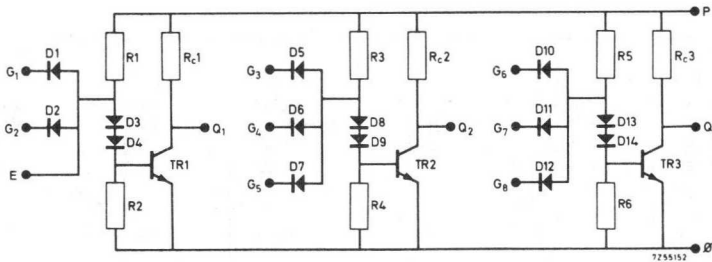
FCH141



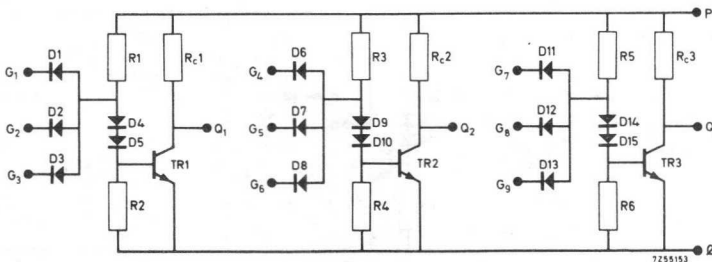
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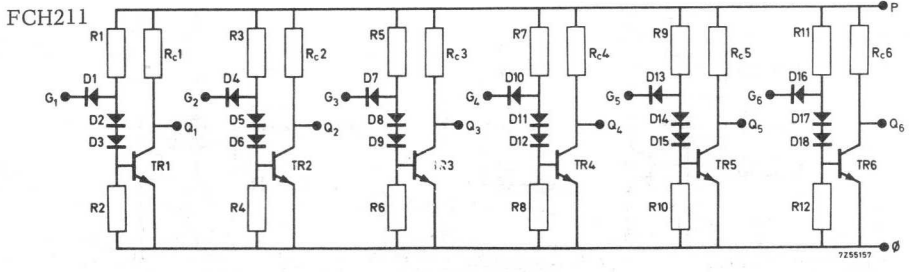
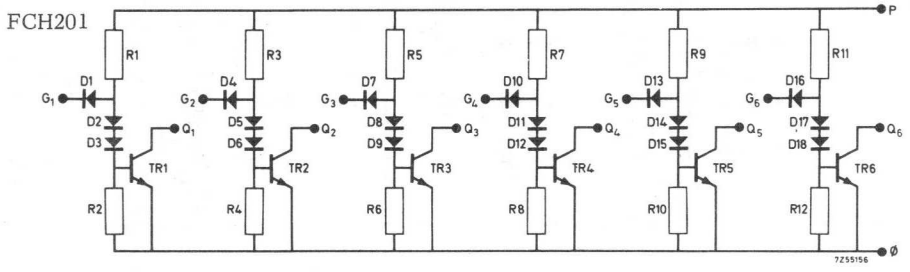
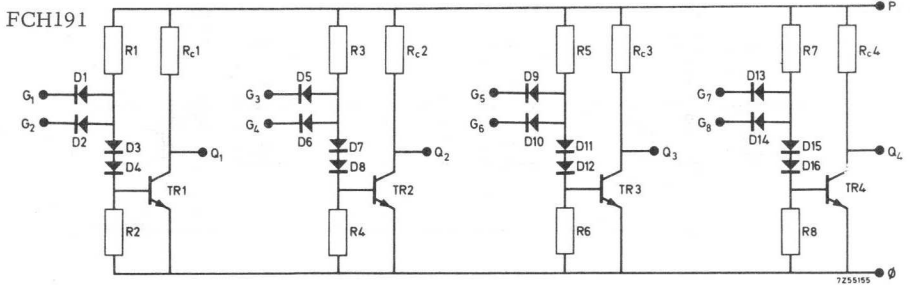
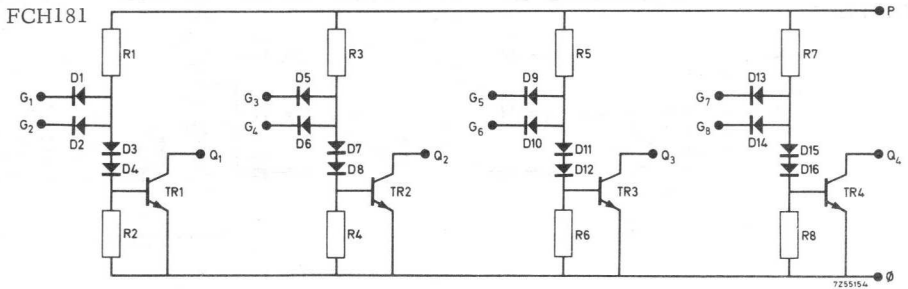
FCH161



FCH171



CIRCUIT DIAGRAMS (continued)



LOGIC FUNCTION

1. Individual gate operation

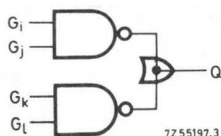


$Q = \overline{G_i \cdot G_j}$ for positive logic

Function table

| G_i | G_j | Q |
|-------|-------|---|
| L | X | H |
| X | L | H |
| H | H | L |

2. Commoned gate operation



Function table

| G_i | G_j | G_k | G_l | Q |
|-------|-------|-------|-------|---|
| L | X | L | X | H |
| L | X | X | L | H |
| X | L | L | X | H |
| X | L | X | L | H |
| H | H | X | X | L |
| X | X | H | H | L |

$Q = \overline{(\overline{G_i \cdot G_j}) \cdot (\overline{G_k \cdot G_l})} = \overline{G_i \cdot G_j} + \overline{G_k \cdot G_l}$ for positive logic

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS (Limiting values) ¹⁾

| | | | |
|-------------------------------------------|-------------|------|----------------|
| Supply voltage | V_P | max. | 8.0 V |
| Output voltage | V_Q | max. | 8.0 V |
| Input voltage | V_G | max. | 8.0 V |
| Output current ²⁾ | $-I_Q$ | max. | 20 mA |
| Input current ³⁾ | $-I_G$ | max. | 20 mA |
| Voltage difference between any two inputs | | max. | 8.0 V |
| Expander input voltages | | | |
| with respect to supply | $V_P - V_E$ | max. | 8.0 V |
| with respect to other inputs | $V_G - V_E$ | max. | 8.0 V |
| Expander input current | I_E | max. | 5.0 mA |
| Storage temperature | T_{stg} | | -55 to +125 °C |
| Operating ambient temperature | T_{amb} | | 0 to +75 °C |

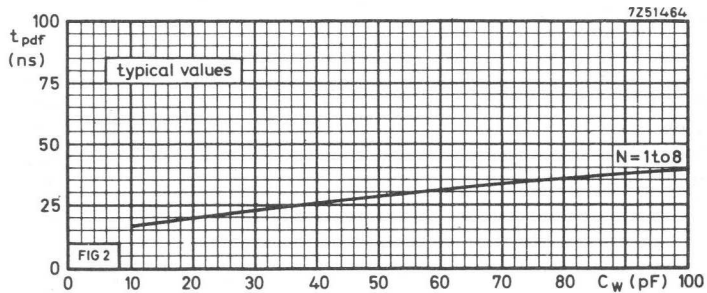
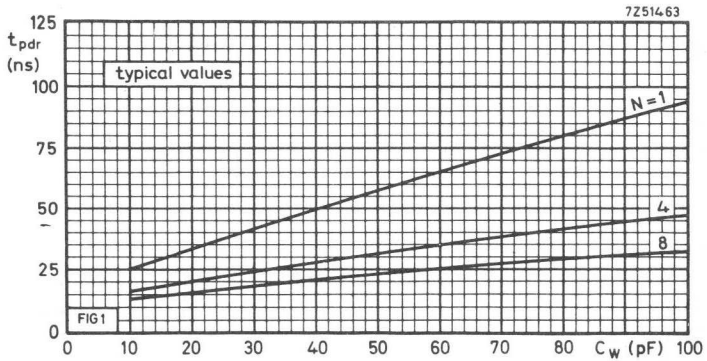
1) Limiting values according to the Absolute Maximum System as defined in IEC publication 134.

2) For negative output voltage.

3) At this limit, input voltage type.: -1.5 V.

SYSTEM DESIGN DATA (both non- R_C and R_C)

| | | | |
|----------------------------------------|------------|-----------|--------------|
| Uniform system temperature | | T_{amb} | 0 to +75 °C |
| Uniform system supply voltage | | V_P | 5.7 to 6.3 V |
| Available d.c. fan out | | N_a | ≥ 8 |
| D.C. noise margin | | M_L | min. 0.4 V |
| | | M_H | min. 1.8 V |
| Average propagation delay time | | t_{pd} | max. 75 ns |
| Equivalent input capacitance | | C_G | typ. 4 pF |
| Equivalent output capacitance | | C_Q | typ. 10 pF |
| Supply current per gate | non- R_C | I_{Pav} | typ. 1.20 mA |
| (duty cycle 50%) | R_C | I_{Pav} | typ. 1.75 mA |
| Power dissipation at $T_{amb} = 75$ °C | non- R_C | P_{tot} | max. 17.5 mW |
| (each gate) | R_C | P_{tot} | max. 22 mW |



CHARACTERISTICS of non- R_C gates

| | | T_{amb} (°C) | | | Conditions and references | |
|-----------------------------|--------------|----------------|------|------|---------------------------|--------------------------------------------------|
| | | 0 | +25 | +75 | V_P (V) | |
| <u>STATIC DATA</u> | | | | | | |
| Output voltage LOW | V_{QLmax} | 0.4 | 0.4 | 0.4 | V | 5.7 and 6.3 |
| at: | | | | | | |
| Output current LOW | I_{QLmax} | 16.0 | 15.1 | 14.2 | mA | 5.7 |
| | | 18.0 | 17.0 | 16.0 | mA | 6.3 |
| and at: | | | | | | 5.7 |
| Input voltage HIGH | V_{GHmin} | 2.3 | 2.2 | 2.1 | V | and 6.3 |
| Input current LOW | $-I_{GLmax}$ | 1.75 | 1.65 | 1.55 | mA | } $V_G = 0.4$ V; other inputs floating |
| | | 2.0 | 1.9 | 1.8 | mA | |
| Input current HIGH | I_{GHmax} | 1.0 | 1.0 | 25 | μ A | 5.7 } $V_G = 5.3$ V other inputs 0 V |
| Output current HIGH | I_{QHmax} | 70 | 70 | 70 | μ A | 5.7 and 6.3 } $V_Q = 5.3$ V |
| at: | | | | | | |
| Input voltage LOW | V_{GLmax} | 1.0 | 1.0 | 0.8 | V | 5.7 and 6.3 |
| Supply current 1) | I_{Pmax} | 2.0 | 1.9 | 1.8 | mA | 6.3 } G inputs LOW |
| <u>DYNAMIC DATA</u> | | | | | | |
| Rise propagation delay time | t_{pdrmax} | - | 85 | - | ns | 6.0 } $V_{pd} = 1.5$ V $N = 1; C_L = 40$ pF |
| | t_{pdrmax} | - | 70 | - | ns | 6.0 } $V_{pd} = 1.5$ V $N = 6; C_L = 60$ pF ← |
| Fall propagation delay time | t_{pdfmax} | - | 65 | - | ns | 6.0 } $V_{pd} = 1.5$ V $N = 1; C_L = 40$ pF |
| | t_{pdfmax} | - | 85 | - | ns | 6.0 } $V_{pd} = 1.5$ V $N = 6; C_L = 60$ pF ← |

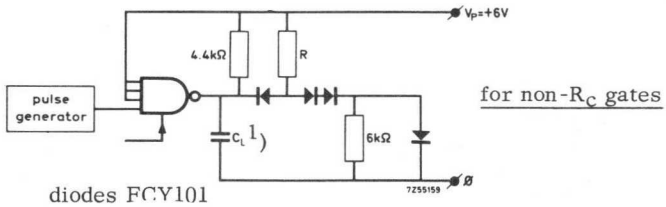
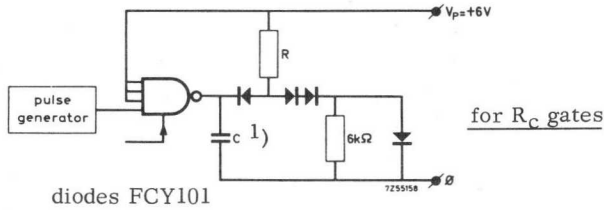
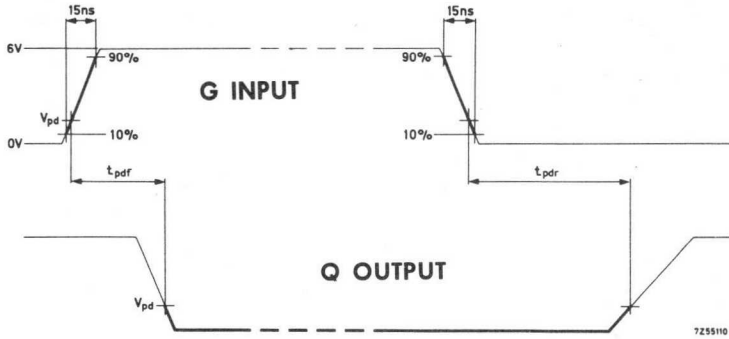
1) per gate

CHARACTERISTICS of R_C -gates

| | | T_{amb} ($^{\circ}C$) | | | Conditions and references | |
|------------------------------------------|---------------|---------------------------|------|------|---------------------------|---------------------------------------------------------------------------|
| | | 0 | +25 | +75 | V_p (V) | |
| <u>STATIC DATA</u> | | | | | | |
| Output voltage LOW | V_{QLmax} | 0.4 | 0.4 | 0.4 | V | 5.7 and 6.3 |
| at: | | | | | | |
| Output current LOW | I_{QLmax} | 14.0 | 13.2 | 12.4 | mA | 5.7 and 6.3 |
| and at: | | | | | | |
| Input voltage HIGH | V_{GHmin} | 2.3 | 2.2 | 2.1 | V | 5.7 and 6.3 |
| Output voltage HIGH | V_{QHmin} | 5.3 | 5.3 | 5.3 | V | 5.7 $I_Q = 0$ 5.7 $I_Q = -200 \mu A$ |
| at: | | | | | | |
| Input voltage LOW | V_{GLmax} | 1.0 | 1.0 | 0.8 | V | 5.7 and 6.3 |
| Input current LOW | $-I_{GLmax}$ | 1.75 | 1.65 | 1.55 | mA | 5.7 } $V_G = 0.4 V$; other 6.3 } inputs floating |
| Input current HIGH | I_{GHmax} | 1.0 | 1.0 | 25 | μA | 5.7 $V_G = 5.3 V$ other inputs 0 V |
| Output current LOW (AND-OR-NOT function) | $-I_{QLLmax}$ | 2.2 | 2.1 | 2.0 | mA | 6.3 $V_G = V_{QLmax}$ Output forced LOW externally to $V_Q = 0.4 V$ |
| Supply current | I_{Pmax} | 4.2 | 3.8 | 3.6 | mA | 6.3 G inputs HIGH |
| <u>DYNAMIC DATA</u> | | | | | | |
| Rise propagation delay time | t_{pdrmax} | - | 85 | - | ns | 6.0 $V_{pd} = 1.5 V$ $N = 1; C_L = 40 pF$ |
| | t_{pdrmax} | - | 70 | - | ns | 6.0 $V_{pd} = 1.5 V$ $N = 6; C_L = 60 pF$ |
| Fall propagation delay time | t_{pdfmax} | - | 65 | - | ns | 6.0 $V_{pd} = 1.5 V$ $N = 1; C_L = 40 pF$ |
| | t_{pdfmax} | - | 85 | - | ns | 6.0 $V_{pd} = 1.5 V$ $N = 6; C_L = 60 pF$ |

CHARACTERISTICS (continued)

DYNAMIC DATA



Waveforms and loading circuits, illustrating measurement of t_{pdr} and t_{pdf} .

Equivalent load for $N = 1$ and $C_L = 40$ pF when $R = 4$ k Ω

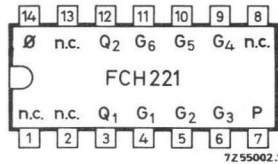
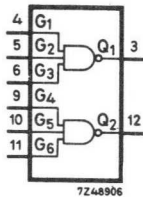
$N = 6$ and $C_L = 60$ pF when $R = 670$ Ω

¹⁾ Including probe and jig capacitance.

100
100
100
100
100

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

DUAL 3-INPUT LINE DRIVER NAND GATE



QUICK REFERENCE DATA

| | | | |
|-------------------------------------------------------------------------------------------|-----------|---------------|----|
| Supply voltage | V_P | $6.0 \pm 5\%$ | V |
| Operating ambient temperature range | T_{amb} | 0 to +75 | °C |
| Average propagation delay time $N = 15, C_w = 250 \text{ pF}, T_{amb} = 25 \text{ °C}$ | t_{pd} | typ. 35 | ns |
| Available d.c. fan-out $T_{amb} = 0 \text{ to } +75 \text{ °C}$ | N_a | \geq | 14 |
| D.C. noise margin $T_{amb} = 25 \text{ °C}$ | M_L | typ. 1.2 | V |
| Power consumption per gate 50% duty cycle, $T_{amb} = 25 \text{ °C}$ | P_{av} | typ. 11 | mW |

The FCH221 comprises two independent NAND gates incorporating bi-directional output circuitry for achieving high fan-out and for driving large capacitive loads. Typical applications are in parallel setting of registers, shift pulse driving and driving of long lines.

PACKAGE OUTLINE : 14 lead plastic dual in-line (type A). (See General Section)

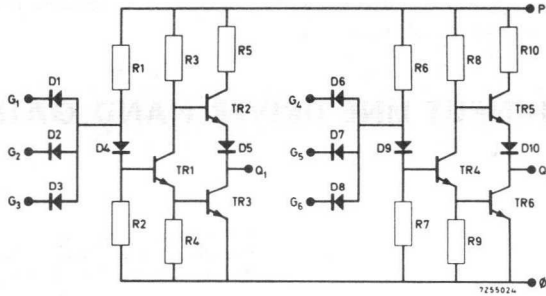
FCH221

dual line driver

FC family

standard temperature range

CIRCUIT DIAGRAM



LOGIC FUNCTION

| | | | |
|----------------|----------------|----------------|----------------|
| G ₁ | G ₂ | G ₃ | Q ₁ |
| G ₄ | G ₅ | G ₆ | Q ₂ |
| L | X | X | H |
| X | L | X | H |
| X | X | L | H |
| H | H | H | L |

$$\left. \begin{aligned} Q_1 &= \overline{G_1 \cdot G_2 \cdot G_3} \\ Q_2 &= \overline{G_4 \cdot G_5 \cdot G_6} \end{aligned} \right\} \text{ for positive logic}$$

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

RATINGS (Limiting values) ¹⁾

| | | | |
|------------------------------------------------------------------------|------------------|------|----------------|
| Supply voltage | V _P | max. | 8.0 V |
| Output voltage | V _Q | max. | 8.0 V |
| Input voltage | V _G | max. | 8.0 V |
| Output current ²⁾ | -I _Q | max. | 20 mA |
| Input current ³⁾ | -I _G | max. | 20 mA |
| Voltage difference between any two inputs | | max. | 8.0 V |
| Storage temperature | T _{stg} | | -55 to +125 °C |
| Operating ambient temperature | T _{amb} | | 0 to +75 °C |
| Output short-circuit duration; duty cycle 10% (either output, or both) | t _{Qsc} | max. | 60 ms |

¹⁾ Limiting values according to the Absolute Maximum System as defined in IEC publication 134.

²⁾ For negative output voltage in LOW state

³⁾ At this limit input voltage typ.: -1.5V.

SYSTEM DESIGN DATA

| | | |
|------------------------------------------------------|----------------|--------------------------|
| Uniform system temperature | T_{amb} | 0 to +75 °C |
| Uniform system supply voltage | V_P | 5.7 to 6.3 V |
| Available d. c. fan out | N_a | \geq 14 |
| D. C. noise margin | M_L M_H | min. 0.4 V min. 1.1 V |
| Average propagation delay time | t_{pd} | max. 113 ns |
| Equivalent input capacitance | C_G | typ. 7 pF |
| Supply current (duty cycle 50%) ¹⁾ | I_{Pav} | typ. 3.6 mA |
| Power dissipation at $T_{amb} = 75$ °C ¹⁾ | P_{tot} | max. 65 mW |



¹⁾ Both gates together; outputs not short-circuited.

FCH221

dual line driver

FC family

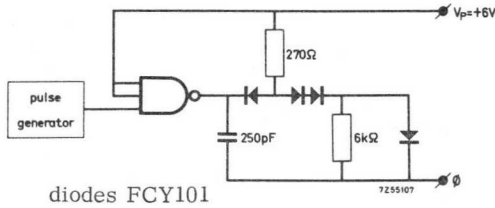
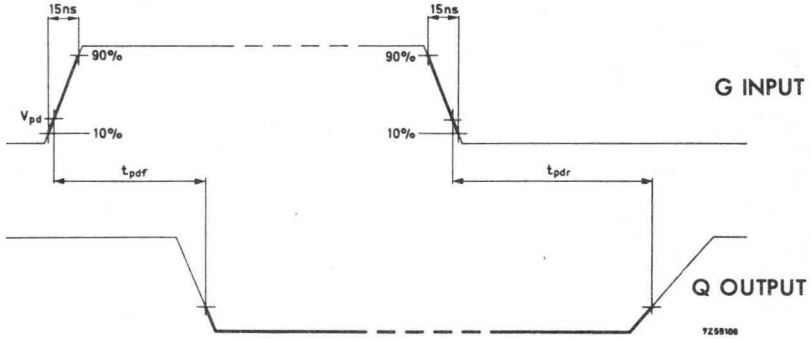
standard temperature range

CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and references | |
|--------------------------------------|----------------------|-----------------------|------|------|---------------------------|-----------------------------------------------------------------|
| | | 0 | +25 | +75 | V _P (V) | |
| <u>STATIC DATA</u> | | | | | | |
| Output voltage LOW | V _{QLmax} | 0.4 | 0.4 | 0.4 | V | 5.7 and 6.3 |
| at: | | | | | | |
| Output current LOW | I _{QLmax} | 25 | 27 | 26 | mA | 5.7 6.3 |
| and at: | | | | | | |
| Input voltage HIGH | V _{GHmin} | 2.3 | 2.2 | 2.1 | V | 5.7 and 6.3 |
| Output voltage HIGH | V _{QHmin} | 3.4 | 3.6 | 3.9 | V | 5.7 I _Q = -30 μA |
| at: | | 2.2 | 2.5 | 2.9 | V | 5.7 I _Q = -5 mA |
| Input voltage LOW | V _{GLmax} | 1.0 | 1.0 | 0.8 | V | 5.7 and 6.3 |
| Input current LOW | -I _{GLmax} | 1.75 | 1.65 | 1.55 | mA | 5.7 } V _G = 0.4 V; other |
| | | 2.0 | 1.9 | 1.8 | mA | 6.3 } inputs floating |
| Input current HIGH | I _{GHmax} | 1.0 | 1.0 | 25 | μA | 5.7 V _G = V _{QHmin} other inputs 0 V |
| Output short circuit current | -I _{Qsc} | 16.5 | 19.5 | 18.0 | mA | 5.7 V _G = V _{GLmax} V _Q = 0 V |
| Supply current (both gates together) | I _{Pmax} | - | 7.5 | - | mA | 6.3 G inputs HIGH |
| <u>DYNAMIC DATA</u> | | | | | | |
| Rise propagation delay time | t _{pdr} max | 130 | 105 | 130 | ns | 6.0 V _{pd} = 1.5 V N = 15; C _L = 250 pF |
| Fall propagation delay time | t _{pdf} max | 95 | 80 | 95 | ns | 6.0 V _{pd} = 1.5 V N = 15; C _L = 250 pF |

CHARACTERISTICS (continued)

DYNAMIC DATA



Equivalent load for $N = 15$ and $C_L^1) = 250$ pF

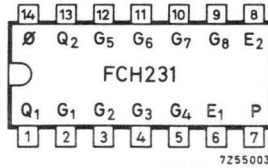
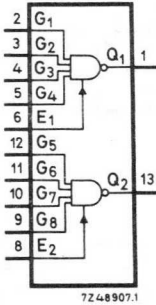
Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf} .

¹⁾ Including probe and jig capacitance.

1000
1000
1000
1000
1000

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

DUAL 4-INPUT LINE DRIVER NAND GATE



QUICK REFERENCE DATA

| | | | |
|-----------------------------------------------------------------------------|-----------|---------------|----|
| Supply voltage | V_P | $6.0 \pm 5\%$ | V |
| Operating ambient temperature range | T_{amb} | 0 to +75 | °C |
| Average propagation delay time N = 20, $C_w = 250$ pF, $T_{amb} = 25$ °C | t_{pd} | typ. 35 | ns |
| Available d.c. fan-out $T_{amb} = 0$ to +75 °C | N_a | \geq | 20 |
| D.C. noise margin $T_{amb} = 25$ °C | M_L | typ. 1.2 | V |
| Power consumption per gate 50% duty cycle, $T_{amb} = 25$ °C | P_{av} | typ. 11 | mW |

The FCH231 comprises two independent NAND gates incorporating bi-directional output circuitry for achieving very high fan-out and for driving large capacitive loads. Typical applications are in parallel setting of registers, shift pulse driving and driving of long lines.

PACKAGE OUTLINE 14 lead plastic dual in-line (type A).(See General Section)

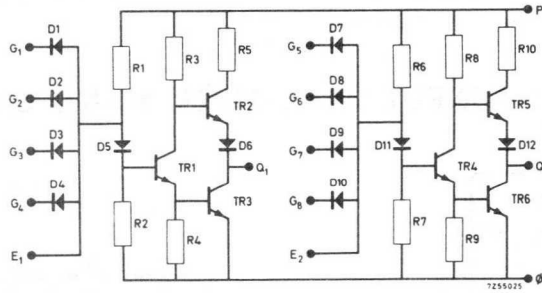
FCH231

dual line driver

FC family

standard temperature range

CIRCUIT DIAGRAM



LOGIC FUNCTION

| G ₁ | G ₂ | G ₃ | G ₄ | Q ₁ |
|----------------|----------------|----------------|----------------|----------------|
| G ₅ | G ₆ | G ₇ | G ₈ | Q ₂ |
| L | X | X | X | H |
| X | L | X | X | H |
| X | X | L | X | H |
| X | X | X | L | H |
| H | H | H | H | L |

$$Q_1 = \overline{G_1 \cdot G_2 \cdot G_3 \cdot G_4 \cdot E_1}^* \quad \left. \begin{array}{l} \text{for positive} \\ \text{logic} \end{array} \right\}$$

$$Q_2 = \overline{G_5 \cdot G_6 \cdot G_7 \cdot G_8 \cdot E_2}^*$$

* When provided with diode

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

RATINGS (Limiting values) ¹⁾

| | | | | |
|---------------------------------------------------------------------------|-------------|------|-------------|----|
| Supply voltage | V_P | max. | 8.0 | V |
| Output voltage | V_Q | max. | 8.0 | V |
| Input voltage | V_G | max. | 8.0 | V |
| Output current ²⁾ | $-I_Q$ | max. | 20 | mA |
| Input current ³⁾ | $-I_G$ | max. | 20 | mA |
| Voltage difference between any two inputs | | max. | 8.0 | V |
| Expander input voltages | | | | |
| with respect to supply | $V_P - V_E$ | max. | 8.0 | V |
| with respect to other inputs | $V_G - V_E$ | max. | 8.0 | V |
| Expander input current | I_E | max. | 5.0 | mA |
| Storage temperature | T_{stg} | | -55 to +125 | °C |
| Operating ambient temperature | T_{amb} | | 0 to +75 | °C |
| Output short-circuit duration; duty cycle 10% (either output, or both) | t_{Qsc} | max. | 60 | ms |

SYSTEM DESIGN DATA

| | | | | |
|------------------------------------------------------|-----------|--------|------------|----|
| Uniform system temperature | T_{amb} | | 0 to +75 | °C |
| Uniform system supply voltage | V_P | | 5.7 to 6.3 | V |
| Available d.c. fan out | N_a | \geq | 20 | |
| D.C. noise margin | M_L | min. | 0.4 | V |
| | M_H | min. | 1.2 | V |
| Average propagation delay time | t_{pd} | max. | 113 | ns |
| Equivalent input capacitance | C_G | typ. | 7 | pF |
| Supply current (duty cycle 50%) ⁴⁾ | I_{Pav} | typ. | 3.6 | mA |
| Power dissipation at $T_{amb} = 75$ °C ⁴⁾ | P_{tot} | max. | 73 | mW |

¹⁾ Limiting values according to the Absolute Maximum System as defined in IEC publication 134.

²⁾ For negative output voltage in LOW state.

³⁾ At this limit, input voltage typ. : -1.5V.

⁴⁾ Both gates together; outputs not short-circuited.

CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and references | |
|--------------------------------------|----------------------|-----------------------|------|------|---------------------------|-------------|
| | | 0 | +25 | +75 | V _P (V) | |
| <u>STATIC DATA</u> | | | | | | |
| Output voltage LOW | V _{QLmax} | 0.4 | 0.4 | 0.4 | V | 5.7 and 6.3 |
| at: | | | | | | |
| Output current LOW | I _{QLmax} | 35 | 33 | 31 | mA | 5.7 |
| | | 40 | 38 | 36 | mA | 6.3 |
| and at: | | | | | | |
| Input voltage HIGH | V _{GHmin} | 2.3 | 2.2 | 2.1 | V | 5.7 and 6.3 |
| Output voltage HIGH | V _{QHmin} | 3.5 | 3.7 | 4.0 | V | 5.7 |
| | | 2.6 | 2.8 | 2.9 | V | 5.7 |
| at: | | | | | | |
| Input voltage LOW | V _{GLmax} | 1.0 | 1.0 | 0.8 | V | 5.7 and 6.3 |
| Input current LOW | -I _{GLmax} | 1.75 | 1.65 | 1.55 | mA | 5.7 |
| | | 2.0 | 1.9 | 1.8 | mA | 6.3 |
| Input current HIGH | I _{GHmax} | 1.0 | 1.0 | 25 | μA | 5.7 |
| Output short circuit current | -I _{Qscmin} | 16.5 | 19.5 | 18.0 | mA | 5.7 |
| Supply current (both gates together) | I _{Pmax} | - | 7.5 | - | mA | 6.3 |
| <u>DYNAMIC DATA</u> | | | | | | |
| Rise propagation delay time | t _{pdrmax} | 80 | 85 | 120 | ns | 6.0 |
| Fall propagation delay time | t _{pdfmax} | 55 | 50 | 55 | ns | 6.0 |

I_Q = -30 μA
I_Q = -5 mA

V_G = 0.4 V; other inputs floating

V_G = V_{QHmin}
other inputs 0 V

V_G = V_{GLmax}
V_Q = 0 V

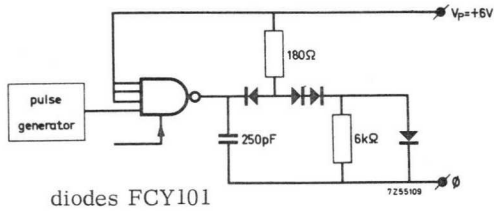
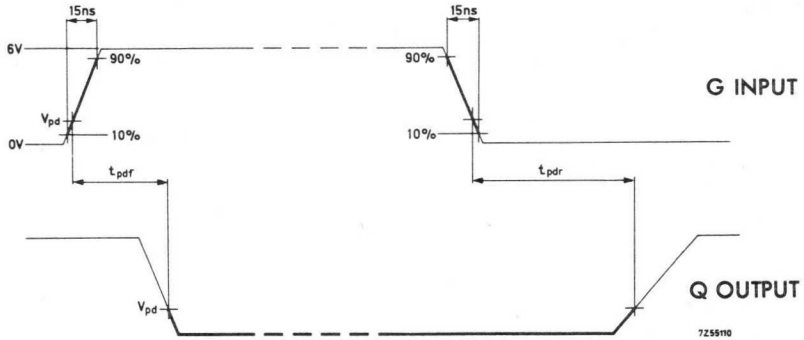
G inputs HIGH

V_{pd} = 1.5 V
N = 20; C_L = 250 pF

V_{pd} = 1.5 V
N = 20; C_L = 250 pF

CHARACTERISTICS (continued)

DYNAMIC DATA



Equivalent load for $N = 20$ and $C_L^1) = 250 \text{ pF}$

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

¹⁾ Including probe and jig capacitance.

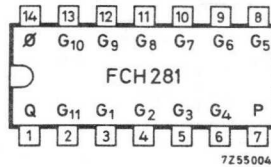
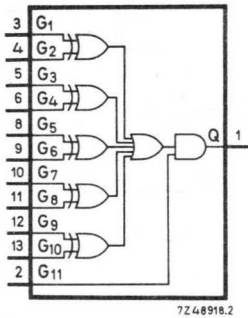
FC 11351

FC 11351

FC 11351

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

SINGLE 5-BIT COMPARATOR



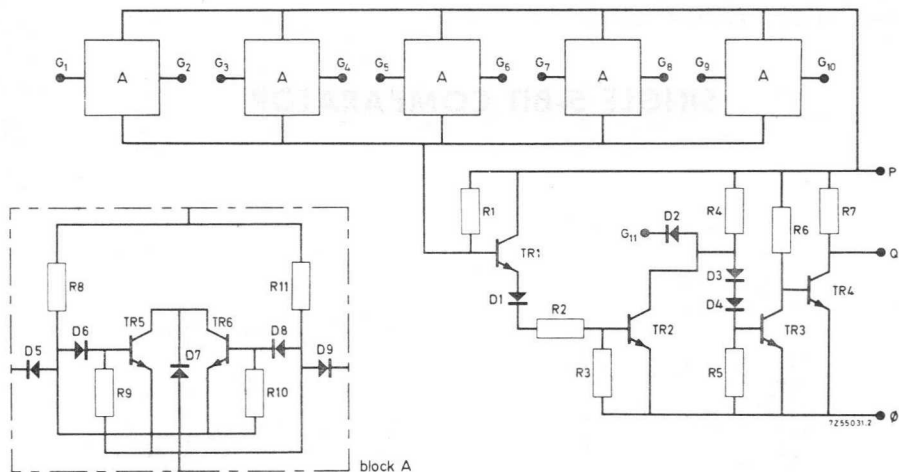
QUICK REFERENCE DATA

| | | |
|---------------------------------------------------------------------------|-----------|-----------------|
| Supply voltage | V_P | $6.0 \pm 5\%$ V |
| Operating ambient temperature range | T_{amb} | 0 to +75 °C |
| Average propagation delay time N = 6, $C_w = 60$ pF, $T_{amb} = 25$ °C | t_{pd} | typ. 150 ns |
| Available d.c. fan-out $T_{amb} = 0$ to +75 °C | N_a | ≥ 8 |
| D.C. noise margin $T_{amb} = 25$ °C | M_L | typ. 1.2 V |
| Power consumption 50% duty cycle, $T_{amb} = 25$ °C | P_{av} | typ. 50 mW |

The FCH281 comprises five exclusive-OR functions, an OR gate, and an AND gate. If on one or more pairs (G₁-G₂, --- G₉-G₁₀) one input is LOW and the other HIGH then the output will be HIGH provided G₁₁ is HIGH. Otherwise the output will be LOW.

PACKAGE OUTLINE : 14 lead plastic dual in -line (type A). (See General Section)

CIRCUIT DIAGRAM



FUNCTION TABLE

| G ₁ G ₂ | G ₃ G ₄ | G ₅ G ₆ | G ₇ G ₈ | G ₉ G ₁₀ | G ₁₁ | Q |
|-------------------------------|-------------------------------|-------------------------------|-------------------------------|--------------------------------|-----------------|---|
| Equal | Equal | Equal | Equal | Equal | H | L |
| Unequal | X | X | X | X | H | H |
| X | Unequal | X | X | X | H | H |
| X | X | Unequal | X | X | H | H |
| X | X | X | Unequal | X | H | H |
| X | X | X | X | Unequal | H | H |
| X | X | X | X | X | L | L |

| G ₁ | G ₂ | |
|----------------|----------------|---------|
| L | L | Equal |
| L | H | Unequal |
| H | L | Unequal |
| H | H | Equal |

H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)
 X = state is immaterial

LOGIC FUNCTION (continued)

$$Q = \left[(\overline{G_1} \cdot \overline{G_2} + G_1 \cdot G_2) + (\overline{G_3} \cdot \overline{G_4} + G_3 \cdot G_4) + (\overline{G_5} \cdot \overline{G_6} + G_5 \cdot G_6) + (\overline{G_7} \cdot \overline{G_8} + G_7 \cdot G_8) + (\overline{G_9} \cdot \overline{G_{10}} + G_9 \cdot G_{10}) \right] \cdot G_{11}$$

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

| | | | |
|-------------------------------------------|-----------|------|---------------------|
| Supply voltage | V_P | max. | 8.0 V |
| Output voltage | V_Q | max. | 8.0 V |
| Input voltage | V_G | max. | 8.0 V |
| Output current | $-I_Q$ | max. | 20 mA ¹⁾ |
| Input current | $-I_G$ | max. | 20 mA ²⁾ |
| Voltage difference between any two inputs | | max. | 8.0 V |
| Storage temperature | T_{stg} | | -55 to +125 °C |
| Operating ambient temperature | T_{amb} | | 0 to +75 °C |

1) For negative output voltage.

2) At this limit input voltage typ. : -1.5 V.

FCH281

comparator

FC family

standard temperature range

SYSTEM DESIGN DATA

| | | |
|----------------------------------------|-----------|--------------|
| Uniform system temperature | T_{amb} | 0 to +75 °C |
| Uniform system supply voltage | V_P | 5.7 to 6.3 V |
| Available d.c. fan out | N_a | \geq 8 |
| D.C. noise margin | M_L | min. 0.4 V |
| | M_H | min. 1.5 V |
| Average propagation delay time | t_{pd} | max. 250 ns |
| Equivalent input capacitance | C_G | typ. 4 pF |
| Supply current (duty cycle 50%) | I_{Pav} | typ. 10 mA |
| Power dissipation at $T_{amb} = 75$ °C | P_{tot} | max. 90 mW |

CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and references | |
|---------------------------|-----------------------------|-----------------------|------|------|---------------------------|---------------------------------|
| | | | | | 0 | +25 |
| <u>STATIC DATA</u> | | | | | | |
| Output voltage LOW | V _{QLmax} | 0.4 | 0.4 | 0.4 | V | } see note 1 |
| at: Output current LOW | I _{QLmax} | 14.0 | 13.2 | 12.4 | mA | |
| | | 16.0 | 15.2 | 14.4 | mA | 5.7 6.3 |
| Output voltage HIGH | V _{QHmin} | 5.3 | 5.3 | 5.3 | V | 5.7 and 6.3 |
| | V _{QHmin} | 4.7 | 4.7 | 4.5 | V | 5.7 |
| | | | | | | I _Q = 0 (see note 1) |
| | | | | | | I _Q = -200 μA |
| Input voltage LOW | V _{GLmax} | 1.0 | 1.0 | 0.8 | V | 5.7 and 6.3 |
| Input voltage HIGH | V _{GHmin} | 3.0 | 2.8 | 2.5 | V | 5.7 and 6.3 |
| Input current LOW | -I _{G1 to 10 Lmax} | 1.75 | 1.65 | 1.55 | mA | 5.7 |
| | -I _{G1 to 10 Lmax} | 2.0 | 1.9 | 1.8 | mA | 6.3 |
| | -I _{G11 Lmax} | 1.2 | 1.1 | 1.05 | mA | 5.7 |
| | -I _{G11 Lmax} | 1.35 | 1.25 | 1.20 | mA | 6.3 |
| | | | | | | V _{G1 to 10} = 0.4 V |
| | | | | | | V _{G1 to 10} = 0.4 V |
| | | | | | | V _{G11} = 0.4 V |
| | | | | | | V _{G11} = 0.4 V |
| Input current HIGH | I _{GHmax} | 1.0 | 1.0 | 25 | μA | 5.7 |
| | | | | | | V _G = 5.3 V |
| | | | | | | other inputs 0 V |
| Supply current | I _{Pmax} | 15.3 | 14.5 | 13.5 | mA | 6.3 |
| | | | | | | G inputs LOW |

Note 1

For the proper combination of inputs to be HIGH or LOW see function table on page 2.

CHARACTERISTICS (continued)

| | | T _{amb} (°C) 0 +25 +75 | | Conditions and references | | | |
|----------------------------------------------------------------------------------|---------------------|------------------------------------|-----|---------------------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| | | | | V _P (V) | | Fig. | |
| <u>DYNAMIC DATA</u> | | | | | | | |
| <u>Propagation delay times from one G (G₁ to G₁₀) to Q</u> | | | | | | | |
| Rise propagation delay time | t _{pdrmax} | - | 200 | - ns | 6.0 | V _{pd} = 1.5 V; N = 6 C _L = 80 pF all other inputs (including G ₁₁) at V _G = 5.3 V | 1; 2 |
| Fall propagation delay time | t _{pdfmax} | - | 200 | - ns | 6.0 | | |
| Rise propagation delay time | t _{pdrmax} | - | 250 | - ns | 6.0 | V _{pd} = 1.5 V; N = 6 C _L = 80 pF all other inputs (excluding G ₁₁) at V _G = 0.4 V V _{G₁₁} = 5.3 V | 1; 3 |
| Fall propagation delay time | t _{pdfmax} | - | | | | | |
| <u>Propagation delay times from G₁₁ to Q</u> | | | | | | | |
| Rise propagation delay time | t _{pdrmax} | - | 100 | - ns | 6.0 | V _{pd} = 1.5 V; N = 6 C _L = 80 pF V _{G₁} = 0 V all other inputs at V _G = 6.0 V | 1; 3 |
| Fall propagation delay time | t _{pdfmax} | - | 120 | - ns | 6.0 | | |

CHARACTERISTICS (continued)

DYNAMIC DATA

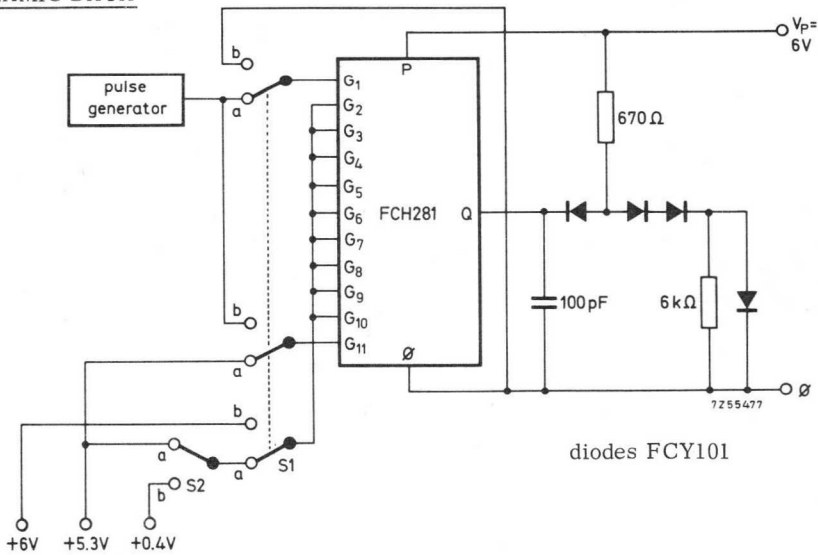


Fig. 1 Equivalent load for $N = 6$; C_L 1) = 80 pF

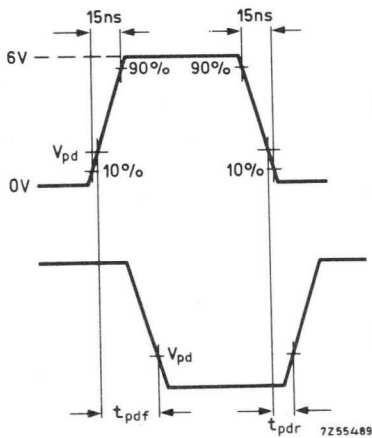


Fig. 2 Switch S1 in position a
Switch S2 in position a

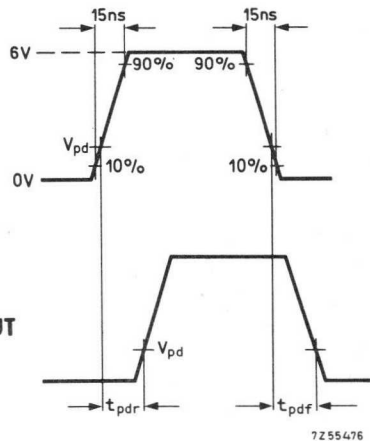


Fig. 3 Switch S1 in position a
Switch S2 in position b
or
Switch S1 in position b

Waveforms illustrating measurement of t_{pdr} and t_{pdf} . Switch S2 immaterial

1) Including probe and jig capacitance.

1880

1880

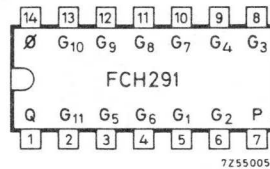
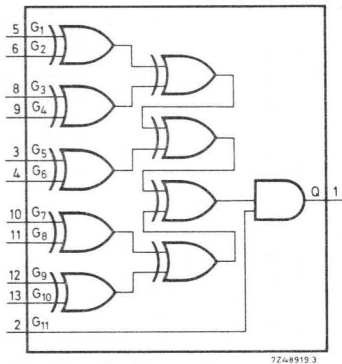
1880

1880

1880

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

SINGLE 10-BIT PARITY CHECKER



QUICK REFERENCE DATA

| | | | |
|---------------------------------------------------------------------------|-----------|---------------|----|
| Supply voltage | V_P | $6.0 \pm 5\%$ | V |
| Operating ambient temperature range | T_{amb} | 0 to +75 | °C |
| Average propagation delay time N = 6, $C_w = 60$ pF, $T_{amb} = 25$ °C | t_{pd} | typ. 150 | ns |
| Available d.c. fan-out $T_{amb} = 0$ to +75 °C | N_a | \geq | 7 |
| D.C. noise margin $T_{amb} = 25$ °C | M_L | typ. 1.2 | V |
| Power consumption 50% duty cycle, $T_{amb} = 25$ °C | P_{av} | typ. 110 | mW |

The FCH291 comprises nine exclusive-OR functions followed by an AND gate. If an odd number of inputs (G_1 to G_{10}) are HIGH the output will be HIGH, provided G_{11} is HIGH. If an even number of inputs (G_1 to G_{10}) are HIGH the output will be LOW, provided G_{11} is HIGH. If G_{11} is LOW the output will be LOW regardless the condition of other inputs.

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A). (See General Section)

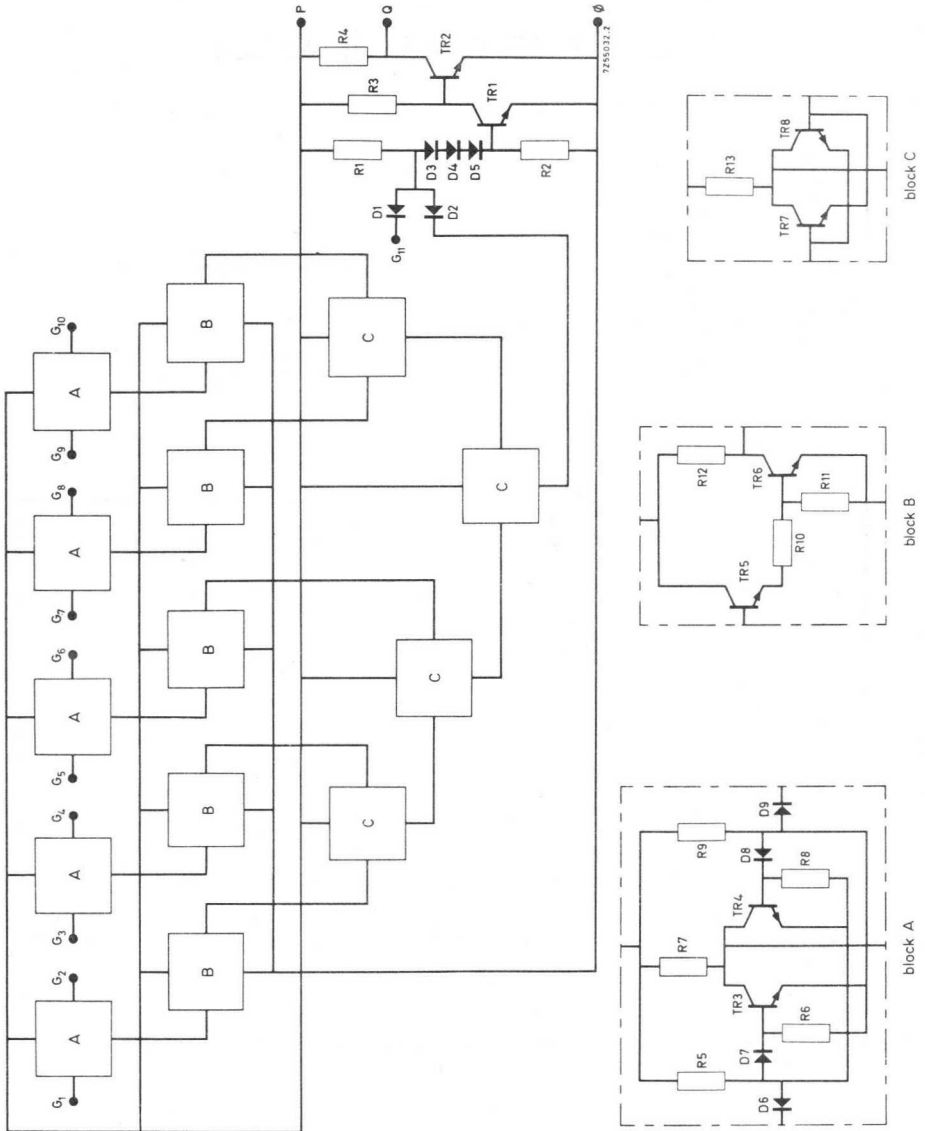
FCH291

parity checker

FC family

standard temperature range

CIRCUIT DIAGRAM



FUNCTION TABLE

| G ₁ | G ₂ | G ₃ | G ₄ | G ₅ | G ₆ | G ₇ | G ₈ | G ₉ | G ₁₀ | G ₁₁ | Q |
|----------------------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|-----------------|-----------------|---|
| Even number of inputs HIGH | | | | | | | | | | H | L |
| Odd number of inputs HIGH | | | | | | | | | | H | H |
| X | X | X | X | X | X | X | X | X | X | L | L |

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

| | | | |
|-------------------------------------------|-----------|------|---------------------|
| Supply voltage | V_P | max. | 8.0 V |
| Output voltage | V_Q | max. | 8.0 V |
| Input voltage | V_G | max. | 8.0 V |
| Output current | $-I_Q$ | max. | 20 mA ¹⁾ |
| Input current | $-I_G$ | max. | 20 mA ²⁾ |
| Voltage difference between any two inputs | | max. | 8.0 V |
| Storage temperature | T_{stg} | | -55 to +125 °C |
| Operating ambient temperature | T_{amb} | | 0 to +75 °C |

¹⁾ For negative output voltage.

²⁾ At this limit input voltage typ.: -1.5 V.

SYSTEM DESIGN DATA

| | | |
|-----------------------------------------|-----------|--------------|
| Uniform system temperature | T_{amb} | 0 to +75 °C |
| Uniform system supply voltage | V_P | 5.7 to 6.3 V |
| Available d.c. fan-out | N_a | ≥ 7 |
| D.C. noise margin | M_L | min. 0.4 V |
| | M_H | min. 0.8 V |
| Average propagation delay time | t_{pd} | max. 250 ns |
| Equivalent input capacitance | C_G | typ. 4 pF |
| Supply current (duty cycle 50%) | I_{Pav} | typ. 21 mA |
| Power dissipation at $T_{amb} = +75$ °C | P_{tot} | max. 190 mW |

CHARACTERISTICS

| | | T _{amb} (°C) 0 +25 +75 | | | Conditions and references | |
|---------------------------|-----------------------------|------------------------------------------|--------------|--------------|---------------------------|----------------------------------------------------------------------------|
| | | | | | V _P (V) | |
| <u>STATIC DATA</u> | | | | | | |
| Output voltage LOW | V _{QLmax} | 0.4 | 0.4 | 0.4 | V | 5.7 and 6.3 } see note 1 |
| at: Output current LOW | I _{QLmax} | 14.0 16.0 | 13.2 15.2 | 12.4 14.4 | mA mA | |
| Output voltage HIGH | V _{QHmin} | 5.3 | 5.3 | 5.3 | V | 5.7 and 6.3 } I _Q = 0 (see note 1) |
| | V _{QHmin} | 4.7 | 4.7 | 4.5 | V | 5.7 } I _Q = -200 μA |
| Input voltage LOW | V _{GLmax} | 1.0 | 1.0 | 0.8 | V | 5.7 and 6.3 |
| Input voltage HIGH | V _{GHmin} | 3.8 | 3.8 | 3.4 | V | 5.7 and 6.3 |
| Input current LOW | -I _{G1 to 10 Lmax} | 1.75 2.0 | 1.65 1.9 | 1.55 1.8 | mA mA | 5.7 } V _{G1 to 10} = 0.4 V 6.3 } V _{G1 to 10} = 0.4 V |
| | -I _{G11max} | 1.9 2.1 | 1.8 2.0 | 1.7 1.9 | mA mA | 5.7 } V _{G11} = 0.4 V 6.3 } V _{G11} = 0.4 V |
| Input current HIGH | I _{GHmax} | 1.0 | 1.0 | 25 | μA | 5.7 } V _G = 5.3 V other inputs 0 V |
| Supply current | I _{Pmax} | 32.0 | 30.5 | 28.0 | mA | 6.3 } G inputs LOW |

Note 1

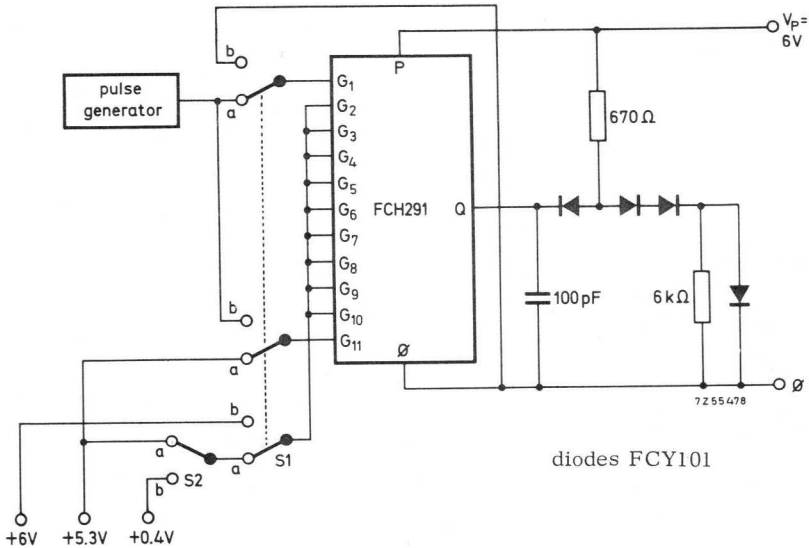
For the proper combination of inputs to be HIGH or LOW see function table on page 2.

CHARACTERISTICS (continued)

| | | T _{amb} (°C) | | | Conditions and references | | |
|----------------------------------------------------------------------------------|---------------------|-----------------------|-----|------|---------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| | | 0 | +25 | +75 | V _P (V) | | Fig. |
| <u>DYNAMIC DATA</u> | | | | | | | |
| <u>Propagation delay times from one G (G₁ to G₁₀) to Q</u> | | | | | | | |
| Rise propagation delay time | t _{pdrmax} | - | 200 | - ns | 6.0 | V _{pd} = 1.5 V; N = 6 C _L = 100 pF all other inputs (including G ₁₁) at V _G = 5.3 V | 1; 2 |
| Fall propagation delay time | t _{pdfmax} | - | 200 | - ns | 6.0 | | |
| Rise propagation delay time | t _{pdrmax} | - | 250 | - ns | 6.0 | V _{pd} = 1.5 V; N = 6 C _L = 100 pF all other inputs (excluding G ₁₁) at V _G = 0.4 V V _{G11} = 5.3 V | 1; 3 |
| Fall propagation delay time | t _{pdfmax} | - | | | | | |
| <u>Propagation delay times from G₁₁ to Q</u> | | | | | | | |
| Rise propagation delay time | t _{pdrmax} | - | 100 | - ns | 6.0 | V _{pd} = 1.5 V; N = 6 C _L = 100 pF V _{G1} = 0 V all other inputs at V _G = 6.0 V | 1; 3 |
| Fall propagation delay time | t _{pdfmax} | - | 120 | - ns | 6.0 | | |

CHARACTERISTICS (continued)

DYNAMIC DATA



diodes FCY101

Fig. 1 Equivalent load for $N = 6$; $C_L^1) = 100 \text{ pF}$

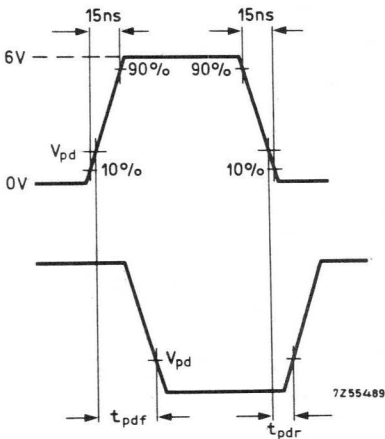


Fig. 2 Switch S2 in position a
Switch S1 in position a

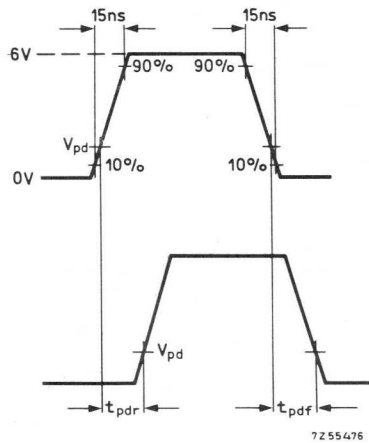


Fig. 3 Switch S1 in position a
Switch S2 in position b
or
Switch S1 in position b
Switch S2 immaterial

Waveforms illustrating measurement of t_{pdr} and t_{pdf} .
1) Including probe and jig capacitance.

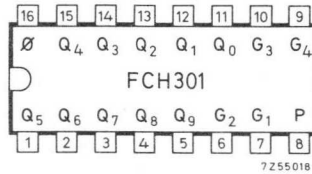
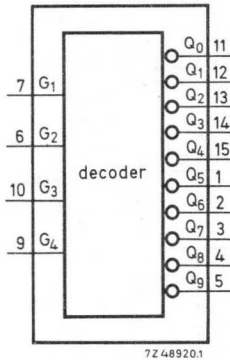
1917

June 24

1917
June 24
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June 24

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

SINGLE 4-BIT DECODER



PACKAGE OUTLINE

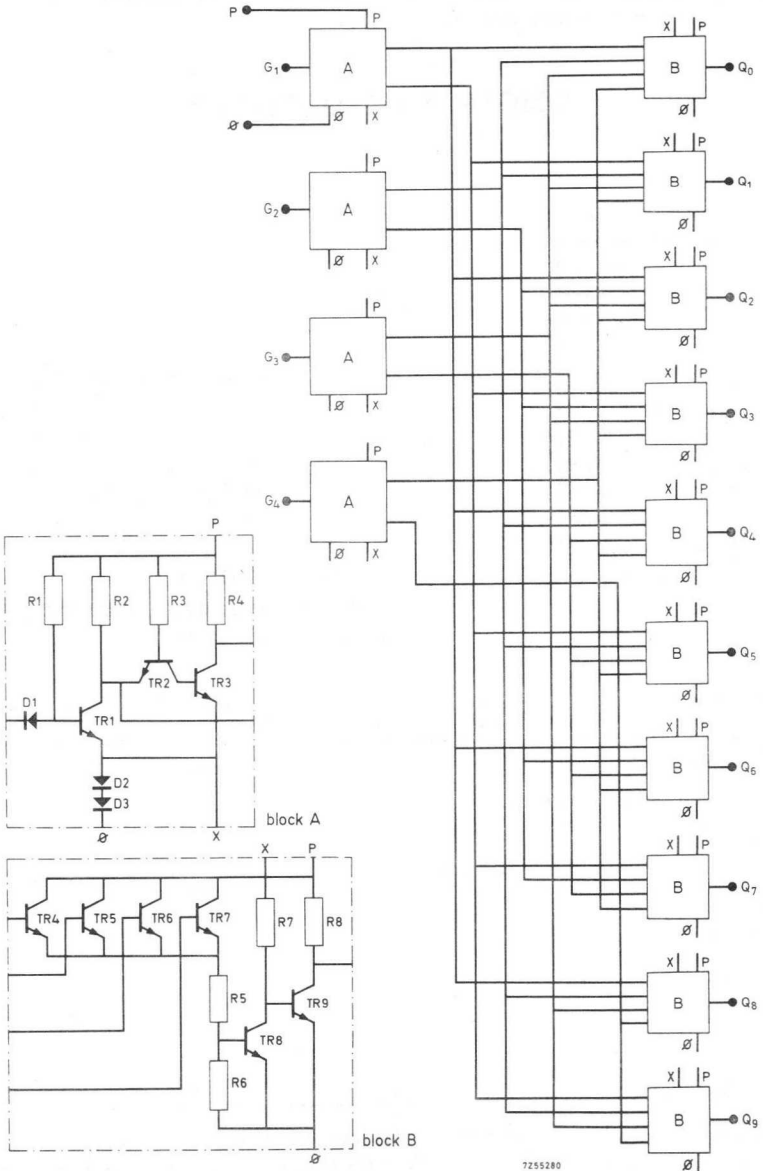
16 lead plastic dual in-line (type A)
 (See General Section)

QUICK REFERENCE DATA

| | | |
|---------------------------------------------------------------------------|-----------|-----------------|
| Supply voltage | V_P | $6.0 \pm 5\%$ V |
| Operating ambient temperature range | T_{amb} | 0 to +75 °C |
| Average propagation delay time N = 1, $C_w = 40$ pF, $T_{amb} = 25$ °C | t_{pd} | ≤ 100 ns |
| Available d.c. fan out $T_{amb} = 0$ to +75 °C | N_a | ≥ 9 |
| D.C. noise margin $T_{amb} = 25$ °C | M_L | ≥ 0.6 V |
| Power consumption 50% duty cycle, $T_{amb} = 25$ °C | P_{av} | typ. 250 mW |

The FCH301 is a fast binary (8-4-2-1) to decimal decoder formed by 18 gate functions. All outputs except the decoded one stay HIGH. If the input does not conform to the 8-4-2-1 code, all outputs remain HIGH.

CIRCUIT DIAGRAMS



FUNCTION TABLE

| G ₄ | G ₃ | G ₂ | G ₁ | Q ₀ | Q ₁ | Q ₂ | Q ₃ | Q ₄ | Q ₅ | Q ₆ | Q ₇ | Q ₈ | Q ₉ |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| L | L | L | L | L | H | H | H | H | H | H | H | H | H |
| L | L | L | H | H | L | H | H | H | H | H | H | H | H |
| L | L | H | L | H | H | L | H | H | H | H | H | H | H |
| L | L | H | H | H | H | H | L | H | H | H | H | H | H |
| L | H | L | L | H | H | H | H | L | H | H | H | H | H |
| L | H | L | H | H | H | H | H | H | L | H | H | H | H |
| L | H | H | L | H | H | H | H | H | H | L | H | H | H |
| L | H | H | H | H | H | H | H | H | H | H | L | H | H |
| H | L | L | L | H | H | H | H | H | H | H | H | L | H |
| H | L | L | H | H | H | H | H | H | H | H | H | H | L |
| H | L | H | L | H | H | H | H | H | H | H | H | H | H |
| H | L | H | H | H | H | H | H | H | H | H | H | H | H |
| H | H | L | L | H | H | H | H | H | H | H | H | H | H |
| H | H | L | H | H | H | H | H | H | H | H | H | H | H |
| H | H | H | L | H | H | H | H | H | H | H | H | H | H |
| H | H | H | H | H | H | H | H | H | H | H | H | H | H |

LOGIC FUNCTIONS

$$Q_0 = \overline{G_1} \cdot \overline{G_2} \cdot \overline{G_3} \cdot \overline{G_4}$$

$$Q_1 = \overline{G_1} \cdot \overline{G_2} \cdot \overline{G_3} \cdot G_4$$

$$Q_2 = \overline{G_1} \cdot G_2 \cdot \overline{G_3} \cdot \overline{G_4}$$

$$Q_3 = \overline{G_1} \cdot G_2 \cdot \overline{G_3} \cdot G_4$$

$$Q_4 = \overline{G_1} \cdot \overline{G_2} \cdot G_3 \cdot \overline{G_4}$$

$$Q_5 = G_1 \cdot \overline{G_2} \cdot \overline{G_3} \cdot \overline{G_4}$$

$$Q_6 = G_1 \cdot G_2 \cdot \overline{G_3} \cdot \overline{G_4}$$

$$Q_7 = G_1 \cdot G_2 \cdot G_3 \cdot \overline{G_4}$$

$$Q_8 = G_1 \cdot \overline{G_2} \cdot \overline{G_3} \cdot G_4$$

$$Q_9 = G_1 \cdot \overline{G_2} \cdot G_3 \cdot G_4$$

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage at T_{amb}: max. 40 °C

V_P max. 8.0 V

Output voltage

V_Q max. 8.0 V

Input voltage

V_G max. 8.0 V

Input current 1)

-I_G max. 20 mA

Voltage difference between any two inputs

max. 8.0 V

Storage temperature

T_{stg} -35 to +125 °C

Operating ambient temperature

T_{amb} 0 to +75 °C

1) At this limit, input voltage typ.: -1.5 V.

SYSTEM DESIGN DATA

| | | |
|--------------------------------|-----------|--------------|
| Operating ambient temperature | T_{amb} | 0 to +75 °C |
| Uniform system voltage | V_P | 5.7 to 6.3 V |
| Available d.c. fan out | N_a | 9 |
| D.C. noise margin | M_L | min. 0.4 V |
| | M_H | min. 2.9 V |
| Average propagation delay time | t_{pd} | 100 ns |
| Equivalent input capacitance | C_G | typ. 4 pF |
| Power dissipation | P_{tot} | max. 300 mW |

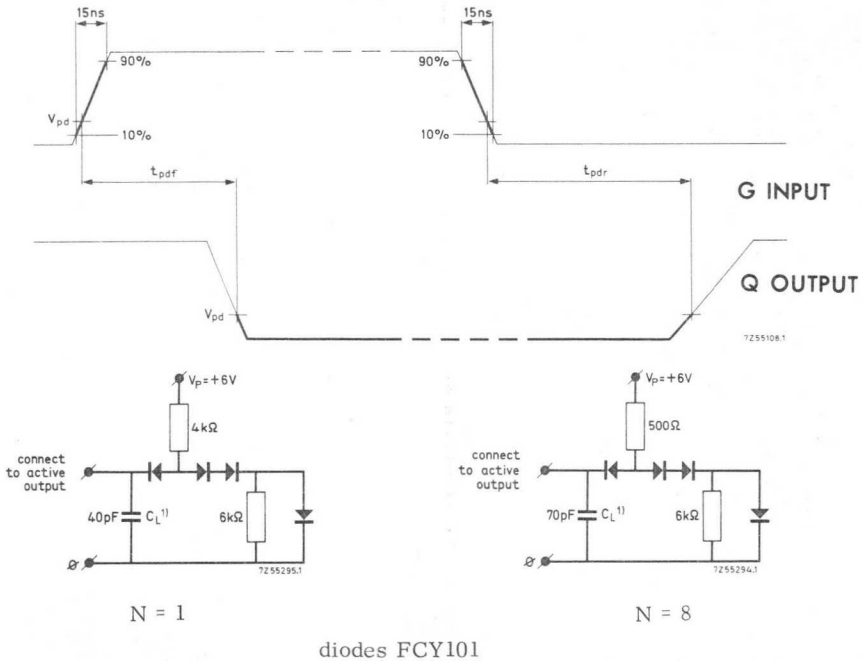
CHARACTERISTICS

| | | T_{amb} (°C) | | | Conditions and References | | |
|---------------------|--------------------|----------------------------|--------------|--------------|---------------------------|-----------------------------------|---------------------------------------------------------------------------|
| | | 0 | 25 | 75 | V_P (V) | | |
| <u>STATIC DATA</u> | Output voltage LOW | V_{QLmax} | 0.4 | 0.4 | 0.4 V | 5.7 and 6.3 5.7 6.3 | For the proper combination of inputs to be HIGH or LOW see Function Table |
| | at: | | | | | | |
| | Output current LOW | I_{QLmax} I_{QLmax} | 15.8 18.0 | 14.9 17.1 | 14.0 16.2 mA | | |
| Output voltage HIGH | V_{QHmin} | 5.2 | 5.2 | 5.2 V | 5.7 | $-I_Q = 0$ | |
| Input voltage LOW | V_{GLmax} | 1.0 | 1.0 | 0.8 V | 5.7 and 6.3 | | |
| Input voltage HIGH | V_{GHmin} | 2.6 | 2.5 | 2.4 V | 5.7 and 6.3 | | |
| Input current LOW | $-I_{GLmax}$ | 1.75 | 1.65 | 1.55 mA | 5.7 | $V_G = 0.4 V$ | |
| | $-I_{GLmax}$ | 2.0 | 1.9 | 1.8 mA | 6.3 | $V_G = 0.4 V$ | |
| Input current HIGH | I_{GHmax} | 1.0 | 1.0 | 25 μA | | $V_G = 6.3 V$ other inputs 0 V | |
| Supply current | I_{Pmax} | - | - | 48 mA | 6.3 | G inputs 0 V | |

CHARACTERISTICS (continued)

| | | T _{amb} (°C) | | | Conditions and References | |
|-----------------------------|----------------------|-----------------------|-----|----|---------------------------|------------------------------------------------------------|
| | | 0 | 25 | 75 | V _P (V) | |
| DYNAMIC DATA*) | | | | | | |
| Rise propagation delay time | t _{pdr} max | - | 110 | - | ns | { V _{pd} = 1.5 V N = 1; C _L = 40 pF |
| | t _{pdr} max | - | 30 | - | ns | { V _{pd} = 1.5 V N = 8; C _L = 70 pF |
| Fall propagation delay time | t _{pdf} max | - | 85 | - | ns | { V _{pd} = 1.5 V N = 1; C _L = 40 pF |
| | t _{pdf} max | - | 100 | - | ns | { V _{pd} = 1.5 V N = 8; C _L = 70 pF |

*) See figures below

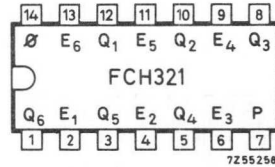
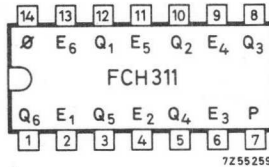
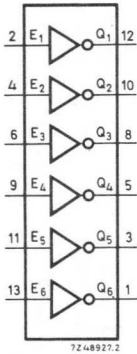


Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

1) Including probe and jig capacitance

100
100
100
100
100

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.



Sextuple inverter

| | |
|------------|--------|
| non- R_C | R_C |
| FCH311 | FCH321 |

QUICK REFERENCE DATA

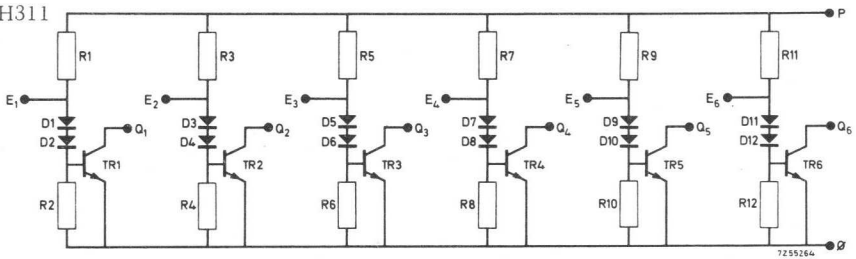
| | | | |
|-----------------------------------------------------------------------------------------|------------|---------------|------------|
| Supply voltage | V_P | $6.0 \pm 5\%$ | V |
| Operating ambient temperature range | T_{amb} | 0 to +75 | °C |
| Average propagation delay time $N = 6, C_w = 60 \text{ pF}, T_{amb} = 25 \text{ °C}$ | t_{pd} | typ. 30 | ns |
| Available d.c. fan out to FC gates $T_{amb} = 0 \text{ to } +75 \text{ °C}$ | N_a | \geq | 8 |
| Power consumption per inverter 50% duty cycle, $T_{amb} = 25 \text{ °C}$ | non- R_C | P_{av} | typ. 7 mW |
| | R_C | P_{av} | typ. 11 mW |

The fan-in of the circuits can easily be expanded by means of a diode array. The outputs of these inverters may be interconnected to perform the AND-OR-NOT function.

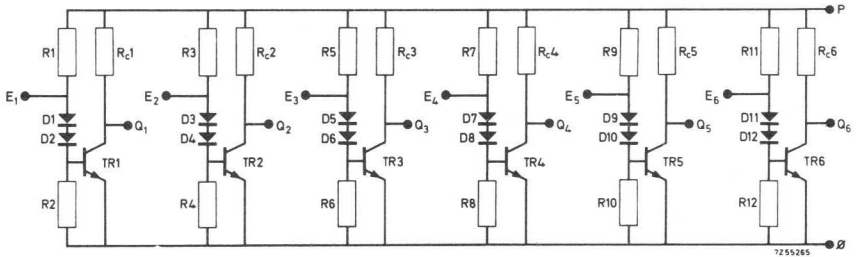
PACKAGE OUTLINES: 14 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAMS

FCH311

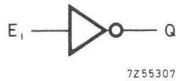


FCH321



LOGIC FUNCTION

1. Individual inverter operation



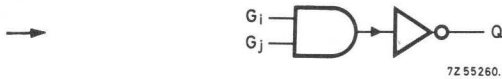
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$Q = \overline{E_i}$ for positive logic

Function table

| E_i | Q |
|-------|---|
| L | H |
| H | L |

2. Individual gate operation



7255260.2

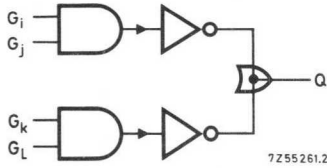
$Q = \overline{G_i \cdot G_j}$ for positive logic

Function table

| G_i | G_j | Q |
|-------|-------|---|
| L | X | H |
| X | L | H |
| H | H | L |

LOGIC FUNCTION (continued)

3. Commoned gate operation



Function table

| G_i | G_j | G_k | G_l | Q |
|-------|-------|-------|-------|---|
| L | X | L | X | H |
| L | X | X | L | H |
| X | L | L | X | H |
| X | L | X | L | H |
| H | H | X | X | L |
| X | X | H | H | L |

$$Q = (\overline{G_i \cdot G_j}) \cdot (\overline{G_k \cdot G_l}) = \overline{(G_i \cdot G_j) + (G_k \cdot G_l)} \text{ for positive logic}$$

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

The AND-function is obtained by connecting a diode array to the E input.

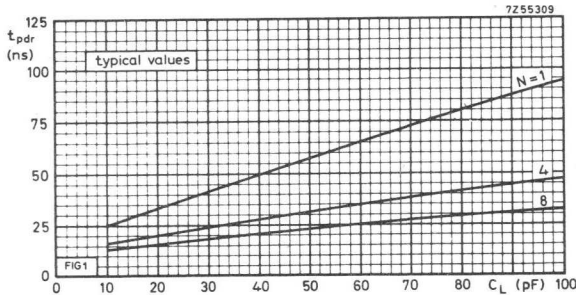
RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

| | | | |
|------------------------------------------------|-------------|------|----------------|
| Supply voltage | V_P | max. | 8.0 V |
| Output voltage (HIGH state) | V_Q | max. | 8.0 V |
| Output current ¹⁾ | $-I_Q$ | max. | 20 mA |
| Expander input voltages with respect to supply | $V_P - V_E$ | max. | 8.0 V |
| Expander input current | I_E | max. | 5.0 mA |
| Storage temperature | T_{stg} | | -55 to +125 °C |
| Operating ambient temperature | T_{amb} | | 0 to +75 °C |

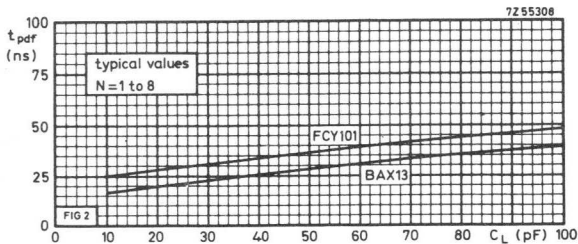
¹⁾ For negative output voltage.

SYSTEM DESIGN DATA (both non- R_C and R_C)

| | | |
|------------------------------------------------------------------------------------|------------------|------------------------|
| Uniform system temperature | T_{amb} | 0 to +75 °C |
| Uniform system supply voltage | V_p | 5.7 to 6.3 V |
| Available d.c. fan out to FC gates | N_a | ≥ 8 |
| Averaged propagation delay time with BAX13 diode | t_{pdf} | max. 75 ns |
| Increase of t_{pdf} with increasing expander capacitance for $C_w = 0$ to 100 pF | Δt_{pdf} | typ. 1.4 ns/pF |
| Equivalent output capacitance | C_Q | typ. 10 pF |
| Supply current (duty cycle 50%) | non- R_C | I_{Pav} typ. 7.2 mA |
| | R_C | I_{Pav} typ. 10.5 mA |
| Power dissipation at $T_{amb} = 75$ °C | non- R_C | P_{tot} max. 100 mW |
| | R_C | P_{tot} max. 171 mW |



t_{pdr} versus C_L for both BAX13 and FCY101 as input diode



t_{pdf} versus C_L for BAX13 and FCY101 as input diode

FC family

standard temperature range

FCH311 FCH321

inverters

CHARACTERISTICS of FCH311 (non R_C)

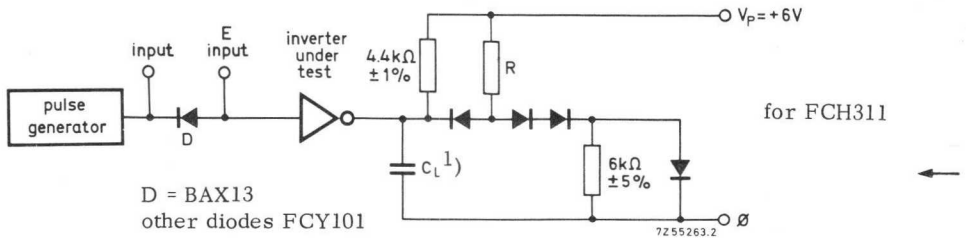
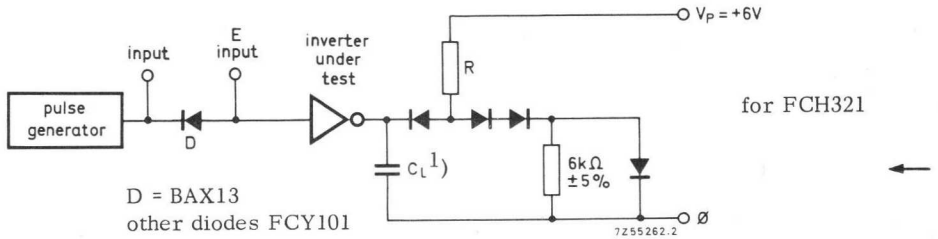
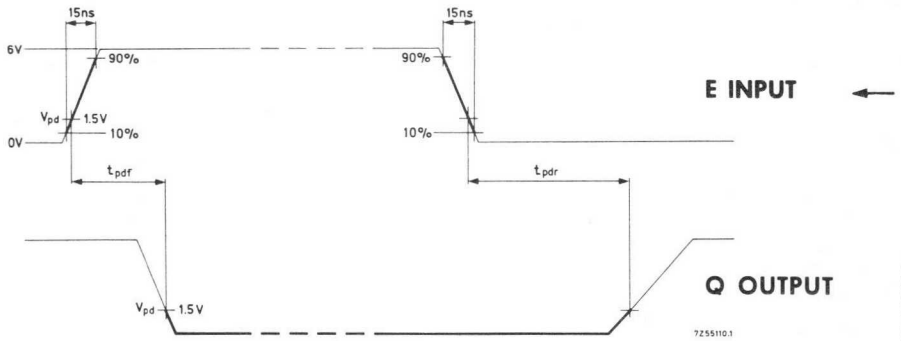
| | | T _{amb} (°C) | | | Conditions and references | |
|----------------------------------------|----------------------|-----------------------|------|------|---------------------------|--------------------------------------------------------------------|
| | | 0 | +25 | +75 | V _P (V) | |
| STATIC DATA | | | | | | |
| <u>Output voltage LOW</u> | V _{QLmax} | 0.4 | 0.4 | 0.4 | V | 5.7 and 6.3 |
| at: | | | | | | -I _E = 50 μA |
| <u>Output current LOW</u> | I _{QLmax} | 16.0 | 15.1 | 14.2 | mA | 5.7 and 6.3 |
| | | 18.0 | 17.0 | 16.0 | mA | |
| <u>Expander input voltage HIGH</u> | V _{EHmax} | 3.0 | 2.8 | 2.6 | V | 5.7 and 6.3 |
| | | | | | | { I _{QL} = I _{QL} max -I _E = 50 μA |
| <u>Input current LOW</u> | -I _{ELmax} | 1.75 | 1.65 | 1.55 | mA | 5.7 and 6.3 |
| at: | | 2.0 | 1.9 | 1.8 | mA | |
| <u>Expander input voltage LOW</u> | V _{EL} | 1.05 | 1.00 | 0.90 | V | |
| <u>Output current HIGH</u> | I _{QHmax} | 70 | 70 | 70 | μA | 5.7 and 6.3 |
| at: | | | | | | V _Q = 5.3 V |
| <u>Expander input voltage LOW</u> | V _{ELmax} | 1.8 | 1.7 | 1.4 | V | 5.7 and 6.3 |
| <u>Supply current</u> | I _{PHmax} | 12.0 | 11.4 | 10.8 | mA | 6.3 |
| at: | | | | | | |
| <u>Expander input voltage LOW</u> | V _{EL} | 1.05 | 1.00 | 0.90 | V | |
| <u>Supply current</u> | I _{PLmax} | 11.4 | 10.2 | 10.2 | mA | 6.3 |
| | | | | | | { Expander inputs floating |
| DYNAMIC DATA see also page 7 | | | | | | |
| <u>Rise propagation delay time</u> | t _{pdr} max | - | 85 | - | ns | 6.0 |
| | | | | | | R = 4 kΩ C _L = 40 pF |
| | t _{pdr} max | - | 70 | - | ns | 6.0 |
| | | | | | | R = 670 Ω C _L = 60 pF |
| <u>Fall propagation delay time</u> | t _{pdf} max | - | 65 | - | ns | 6.0 |
| | | | | | | R = 4 kΩ C _L = 40 pF |
| | t _{pdf} max | - | 85 | - | ns | 6.0 |
| | | | | | | R = 670 Ω C _L = 60 pF |

CHARACTERISTICS of FCH321 (R_C)

| | | T_{amb} (°C) | | | Conditions and references | |
|----------------------------------------------------------|----------------|----------------|--------------|--------------|---------------------------|-------------------------------------------------------------------------|
| | | 0 | +25 | +75 | V_P (V) | |
| STATIC DATA | | | | | | |
| Output voltage LOW at: Output current LOW | V_{QLmax} | 0.4 | 0.4 | 0.4 | 5.7 and 6.3 | $-I_E = 50 \mu A$ |
| | I_{QLmax} | 14.0 16.0 | 13.2 15.2 | 12.4 14.4 | 5.7 6.3 | |
| Expander input voltage HIGH | V_{EHmax} | 3.0 | 2.8 | 2.6 | 5.7 and 6.3 | $I_{QL} = I_{QL} \max$ $-I_E = 50 \mu A$ |
| Output voltage HIGH at: Expander input voltage LOW | V_{QHmin} | 5.3 4.1 | 5.3 4.1 | 5.3 3.9 | 5.7 5.7 | $I_Q = 0$ $I_Q = -200 \mu A$ |
| | V_{ELmax} | 1.8 | 1.7 | 1.4 | 5.7 and 6.3 | |
| Input current LOW at: Expander input voltage LOW | $-I_{ELmax}$ | 1.75 2.0 | 1.65 1.9 | 1.55 1.8 | 5.7 6.3 | |
| | V_{EL} | 1.05 | 1.00 | 0.90 | | |
| Output current LOW (AND-OR-NOT function) | $-I_{QLLmax}$ | 2.2 | 2.1 | 2.0 | 6.3 | Expander inputs LOW Output forced LOW externally to $V_Q = 0.4 V$ |
| Supply current | I_{PLmax} | 25.2 | 22.8 | 21.6 | 6.3 | Expander inputs floating |
| DYNAMIC DATA see also page 7 | | | | | | |
| Rise propagation delay time | $t_{pdr} \max$ | - | 85 | - | 6.0 | $R = 4 k\Omega$ $C_L = 40 pF$ |
| | $t_{pdr} \max$ | - | 70 | - | 6.0 | $R = 670 \Omega$ $C_L = 60 pF$ |
| Fall propagation delay time | $t_{pdf} \max$ | - | 65 | - | 6.0 | $R = 4 k\Omega$ $C_L = 40 pF$ |
| | $t_{pdf} \max$ | - | 85 | - | 6.0 | $R = 670 \Omega$ $C_L = 60 pF$ |

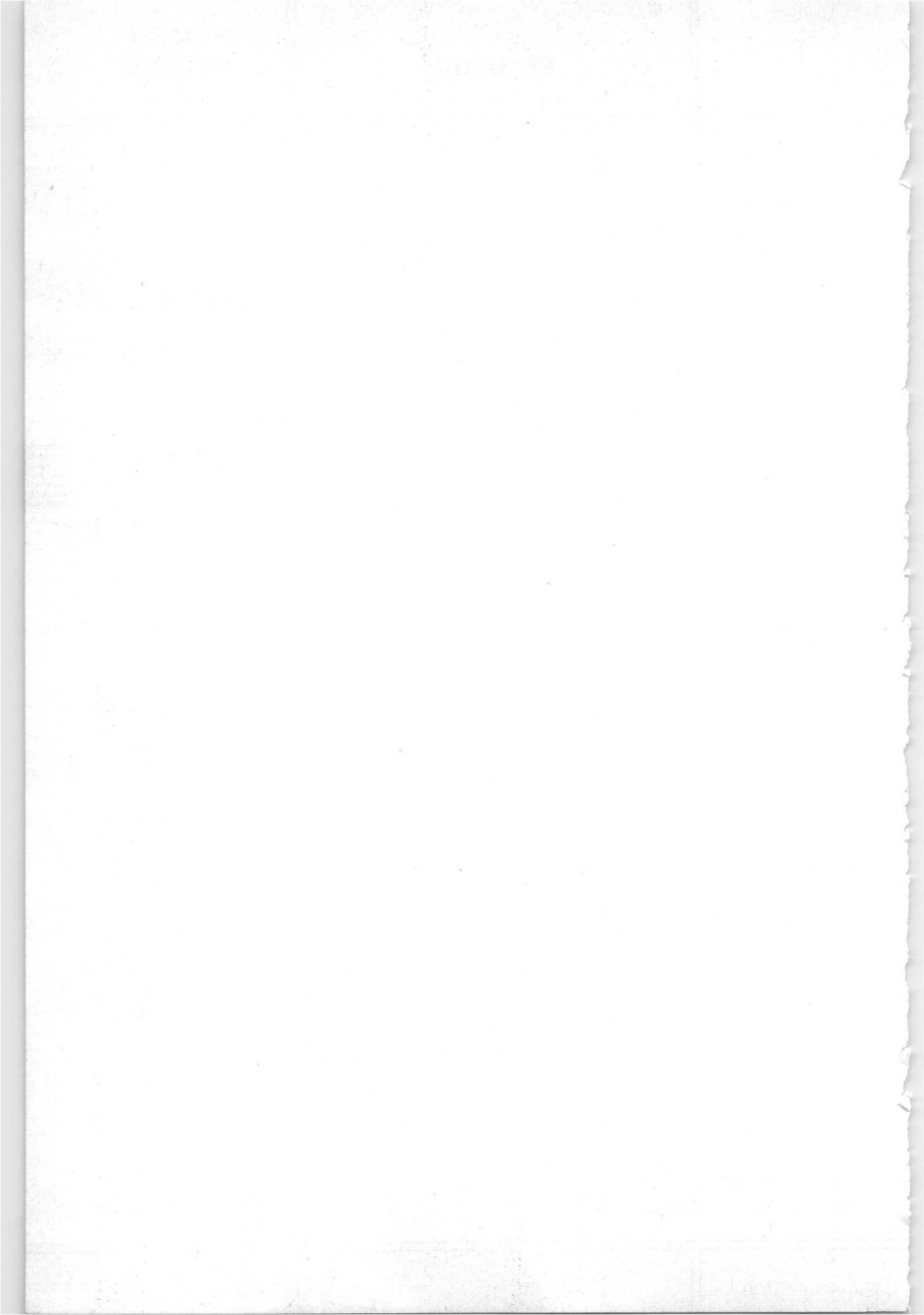
CHARACTERISTICS (continued)

DYNAMIC DATA



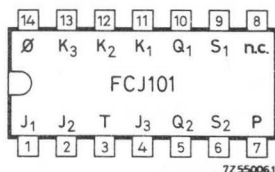
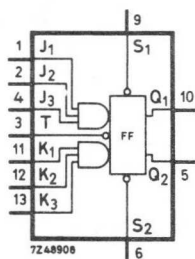
Waveforms and loading circuits, illustrating measurement of t_{pdr} and t_{pdf} .

1) Including probe and jig capacitance



The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

SINGLE JK FLIP-FLOP



QUICK REFERENCE DATA

| | | | |
|--------------------------------------------------------|-----------|---------------|-----|
| Supply voltage | V_P | $6.0 \pm 5\%$ | V |
| Operating ambient temperature range | T_{amb} | 0 to +75 | °C |
| Clock rate | f_c | typ. 10 | MHz |
| Available d.c. fan out $T_{amb} = 0$ to +75 °C | N_a | \geq | 8 |
| D.C. noise margin $T_{amb} = 25$ °C | M_L | typ. 1.2 | V |
| Power consumption 50% duty cycle, $T_{amb} = 25$ °C | P_{av} | typ. 36 | mW |

The FCJ101 performs the JK flip-flop operation. Three J and three K inputs permit an additional AND operation. Triggering occurs at the falling edge of a T signal. The direct-set inputs (overriding any other inputs) are active at the LOW level. The circuitry incorporates bi-directional outputs for driving capacitive loads. Typical applications are in high speed counters and shift registers.

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A). (See General Section)

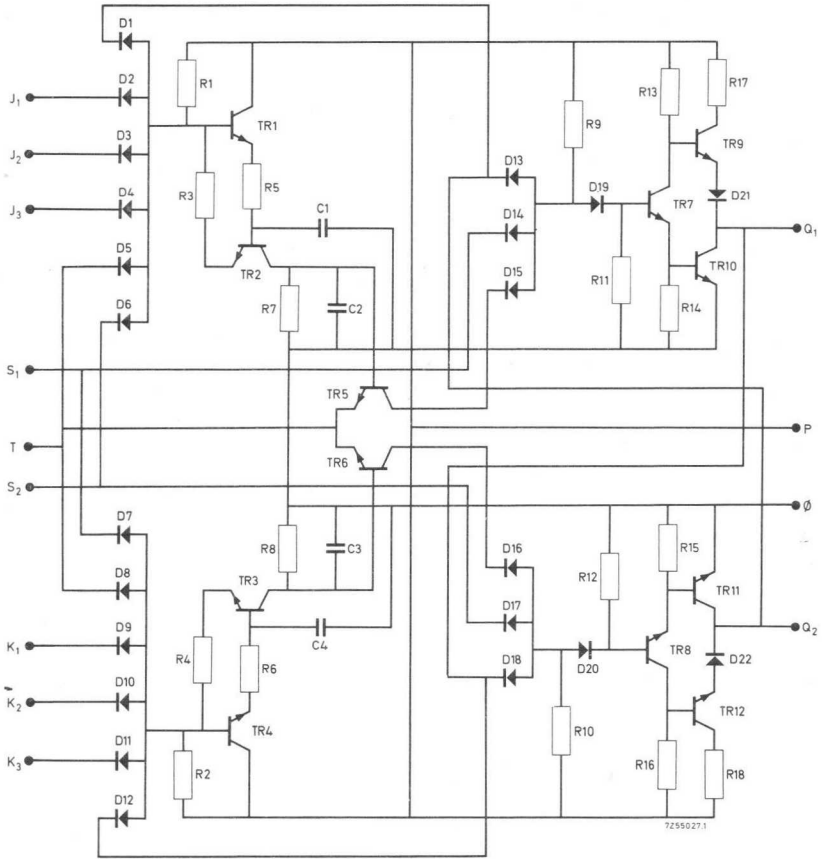
FCJ101

flip-flop

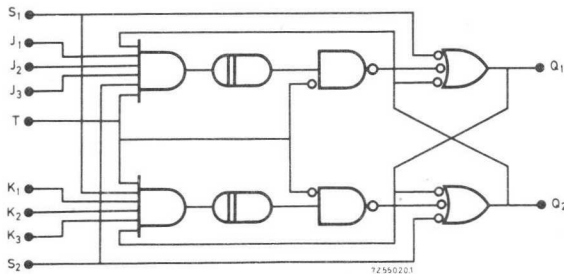
FC family

standard temperature range

CIRCUIT DIAGRAM



LOGIC DIAGRAM(to MIL standard 806B)



FUNCTION TABLES

1. Trigger action via T terminal

| T = HIGH | | T = LOW | |
|----------|---|----------------|----------------|
| J | K | Q ₁ | Q ₂ |
| H | H | reversed | |
| L | H | L | H |
| H | L | H | L |
| L | L | no change | |

The information on J and K is transferred into the flip-flop by T becoming HIGH. When T subsequently goes LOW the outputs will assume the levels shown in the table. Inputs S₁ and S₂ should be HIGH or floating.

$$\left. \begin{aligned} J &= J_1 \cdot J_2 \cdot J_3 \\ K &= K_1 \cdot K_2 \cdot K_3 \end{aligned} \right\} \text{ for positive logic}$$

2. Set or reset via S terminals

| S ₁ | S ₂ | Q ₁ | Q ₂ |
|----------------|----------------|----------------|----------------|
| H | L | L | H |
| L | H | H | L |
| L | L | H | H |
| H | H | no change | |

The set inputs override the other inputs and directly determine the outputs of the flip-flop.

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

RATINGS (Limiting values) ¹⁾

| | | | |
|-------------------------------------------|-----------------------------------------------------------------------|------|----------------|
| Supply voltage | V _P | max. | 8.0 V |
| Output voltage | V _Q | max. | 8.0 V |
| Input voltage | V _J , V _K , V _T , V _S | max. | 8.0 V |
| Output current ²⁾ | -I _Q | max. | 20 mA |
| Input current ³⁾ | -I _J , -I _K , -I _T , -I _S | max. | 20 mA |
| Voltage difference between any two inputs | | max. | 8.0 V |
| Storage temperature | T _{stg} | | -55 to +125 °C |
| Operating ambient temperature | T _{amb} | | 0 to +75 °C |

¹⁾ Limiting values according to the Absolute Maximum System as defined in IEC publication 134.

²⁾ For negative output voltage in LOW state.

³⁾ At this limit input voltage typ. : -1.5 V.

SYSTEM DESIGN DATA

| | | |
|-----------------------------------------------|-------------------|--------------------------|
| Uniform system temperature | T_{amb} | 0 to +75 °C |
| Uniform system supply voltage | V_P | 5.7 to 6.3 V |
| Available d. c. fan out | | |
| to J or K input | $N_{aJ} = N_{aK}$ | ≥ 8 |
| to S input | N_{aS} | ≥ 4 |
| to G input | N_{aG} | ≥ 8 |
| Available a. c. fan out | | |
| to T input | N_{aT} | ≥ 2 |
| D. C. noise margin | | |
| to T input | M_L M_H | min. 0.3 V min. 0.2 V |
| to J or K input | M_L M_H | min. 0.5 V min. 0.2 V |
| to S input | M_L M_H | min. 0.3 V min. 0.2 V |
| to G input | M_L M_H | min. 0.4 V min. 1.5 V |
| Average propagation delay time | t_{pd} | max. 85 ns |
| Maximum clock rate | f_c | ≥ 6 MHz |
| Equivalent input capacitances | | |
| for T input | C_T | typ. 30 pF |
| for J or K input | $C_J = C_K$ | typ. 20 pF |
| for S input | C_S | typ. 25 pF |
| Supply current (duty cycle 50%) | I_{pav} | typ. 6.0 mA |
| Power dissipation at $T_{amb} = 75\text{ °C}$ | P_{tot} | max. 56 mW |

CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and references | | |
|------------------------------------------|----------------------------------------------|-----------------------|------|------|---------------------------|--------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| | | | | | 0 | +25 | +75 |
| <u>STATIC DATA</u> | | | | | | | |
| Output voltage LOW | V _{QLmax} | 0.4 | 0.4 | 0.4 | V | 5.7 and 6.3 | |
| at: Output current LOW | I _{QLmax} | 14.0 | 16.5 | 12.4 | mA | 5.7 | |
| | | 16.0 | 19.0 | 14.4 | mA | 6.3 | |
| Output voltage HIGH | V _{QHmin} | 3.8 | 3.9 | 4.1 | V | 5.7 | |
| | | | | | | I _Q = -100 μA | |
| Output voltage HIGH (lowest permissible) | V _{QHPmin} | 3.6 | 3.3 | 3.0 | V | 5.7 | |
| at: Output current HIGH | -I _{QHmax} | 0.85 | 3.3 | 5.5 | mA | 5.7 | |
| Input current LOW | -I _{JLmax} , { | 1.75 | 1.65 | 1.55 | mA | 5.7 | V _J = V _K = 0.4 V; other inputs floating } V _T = 0.4 V; other inputs floating } V _S = 0.4 V; other inputs floating |
| | -I _{KLmax} { | 2.0 | 1.9 | 1.8 | mA | 6.3 | |
| | -I _{TLmax} | 3.5 | 3.3 | 3.1 | mA | 5.7 | |
| | -I _{SLmax} | 4.0 | 3.8 | 3.6 | mA | 6.3 | |
| Input current HIGH | -I _{JHmax} , -I _{KHmax} | 1 | 1 | 25 | μA | 5.7 | V _J = V _K = 5.3 V other inputs 0 V |
| | I _{THmax} | 2 | 2 | 50 | μA | 5.7 | V _T = 5.3 V other inputs 0 V |
| | I _{SHmax} | 2 | 2 | 50 | μA | 5.7 | V _S = 5.3 V other inputs 0 V |
| Supply current | I _{Pmax} | - | 9 | - | mA | 6.3 | T input LOW J, K, S inputs HIGH |



CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and references | | fig. |
|--------------------------------------------|----------------------------------------------------------------|-----------------------|-----|-----|---------------------------|--------------------------------------------------------------------------------------------------------------|------|
| | | | | | V _P (V) | | |
| <u>DYNAMIC DATA</u> | | | | | 5.7 and 6.3 | | |
| <u>Change of state</u> | | | | | | | |
| Input voltage HIGH | V _{THmin} V _{JHmin} V _{KHmin} | 3.6 | 3.3 | 3.0 | V | HIGH level at T and J and/or K to be present simultaneously | 1 |
| during: | | | | | | | |
| Input time HIGH | t _{THmin} | 50 | 50 | 50 | ns | | 1 |
| followed by: | | | | | | | |
| T-input slope | (-dt/dV) _{Tmax} (-dt/dV) _{Tmin} | 18 | 18 | 18 | ns/V | | 1 |
| to: | | | | | | | |
| T-input voltage LOW | V _{TLmax} | 0.7 | 0.7 | 0.7 | V | t _{TLmin} = t _{pdf} | 1 |
| <u>No change of state</u> | | | | | | | |
| JK-input voltage LOW | V _{JLmax} V _{KLmax} | 1.1 | 1.0 | 0.9 | V | J and K turning LOW after T and J and/or K having been HIGH simultaneously | 2 |
| during: | | | | | | | |
| JK-input time LOW | t _{JLmin} t _{KLmin} | 100 | 100 | 160 | ns | | 2 |
| <u>Clock skew protection</u> | | | | | | | |
| Hold time LOW | t _{holdLmax} | 15 | 15 | 15 | ns | | 2 |
| Hold time HIGH | t _{holdHmax} | 7 | 10 | 10 | ns | | 3 |
| <u>Set or Reset</u> | | | | | | | |
| S-input voltage LOW | V _{SLmax} | 1.0 | 0.9 | 0.7 | V | active t _{SLmin} = t _{pdf} | 4 |
| S-input voltage HIGH | V _{SHmin} | 3.6 | 3.3 | 3.0 | V | inactive | |
| <u>Propagation delay times from T to Q</u> | | | | | | | |
| Rise propagation delay time | t _{pdr max} | - | 70 | - | ns | 6.0 V _{pd} = 1.5 V N = 1; C _L = 60 pF | 5 |
| Fall propagation delay time | t _{pdf max} | - | 100 | - | ns | 6.0 V _{pd} = 1.5 V N = 8; C _L = 60 pF other output N = 1 C _L = 60 pF | 5 |

CHARACTERISTICS (continued)

DYNAMIC DATA

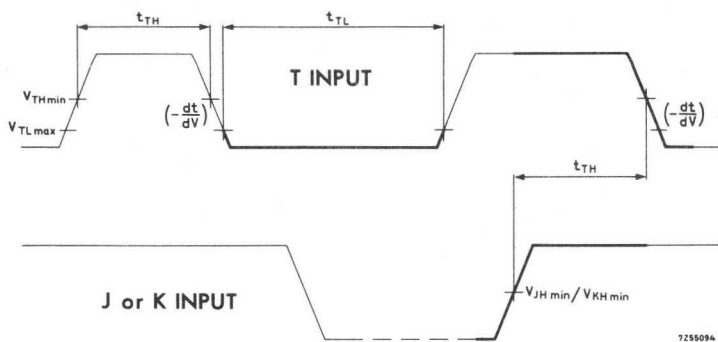


Fig.1. Waveforms illustrating conditions for change of state.

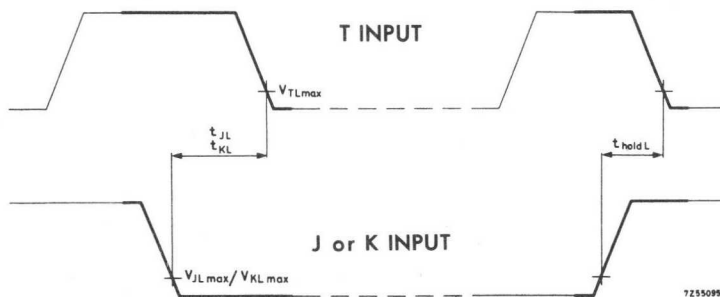


Fig.2. Waveforms illustrating conditions for no change of state.

For no change of state to result:

- a. the time between J or K reaching V_{JLmax} , V_{KLmax} (going LOW) and T reaching V_{TLmax} (going LOW) must be at least t_{JLmin} , t_{KLmin} .
- b. the time between J or K reaching V_{JLmax} , V_{KLmax} (going HIGH) and T reaching V_{TLmax} (going LOW) must be less than t_{holdL} .

CHARACTERISTICS (continued)

DYNAMIC DATA

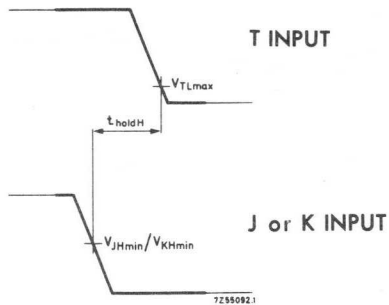


Fig.3. Waveforms illustrating conditions for change of state.
For a change of state still to result, the time between J or K reaching V_{JHmin} , V_{KHmin} (going LOW) and T reaching V_{TLmax} (going LOW) must be less than t_{holdH}

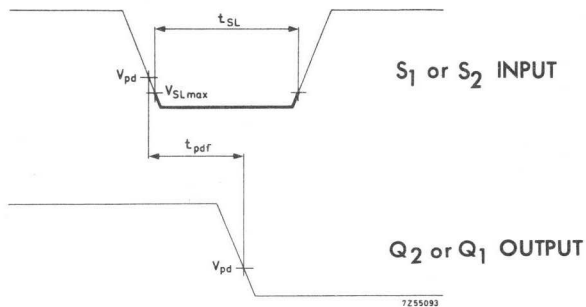
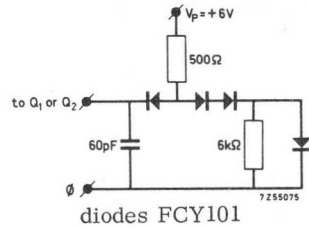
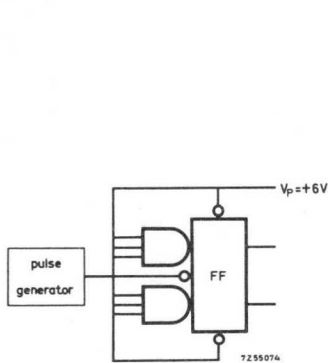
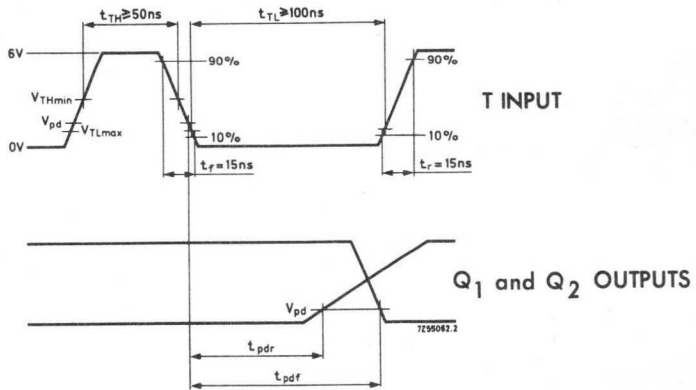


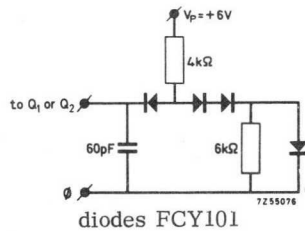
Fig.4. Waveforms illustrating conditions for set or reset.

CHARACTERISTICS (continued)

DYNAMIC DATA



Equivalent load for $N=8$ and $C_L^1) = 60$ pF



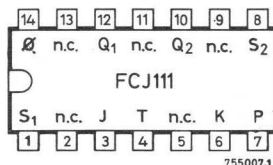
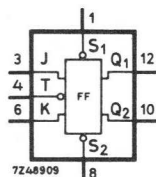
Equivalent load for $N=1$ and $C_L^1) = 60$ pF

Fig. 5. Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf} .

1) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

SINGLE JK MASTER-SLAVE FLIP-FLOP



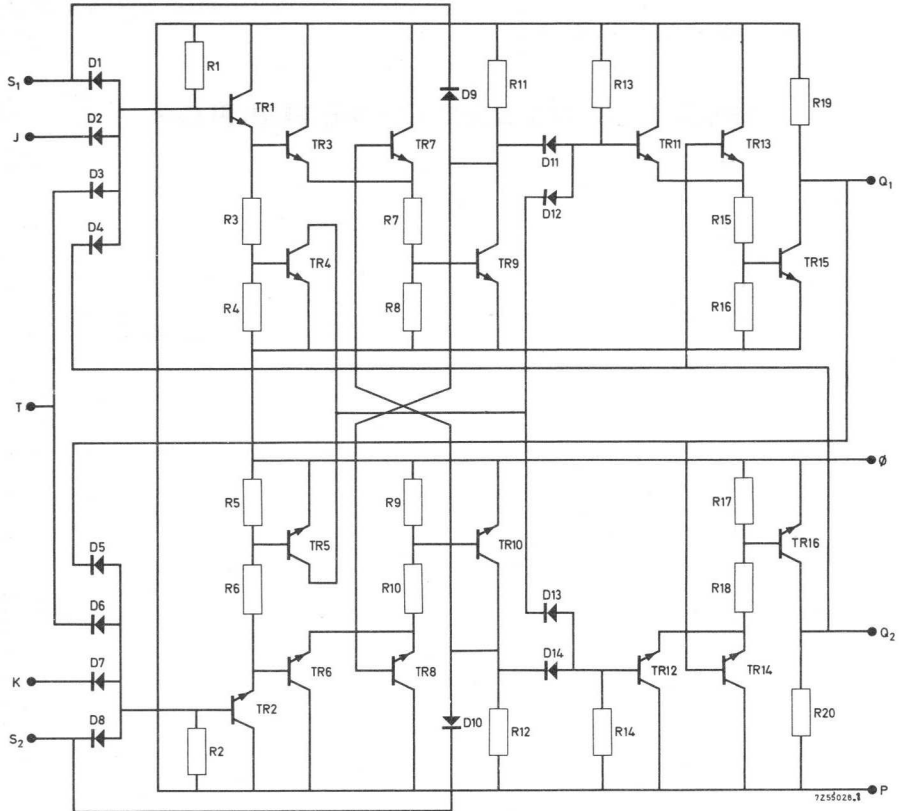
QUICK REFERENCE DATA

| | | | |
|--------------------------------------------------------|-----------|---------------|-----|
| Supply voltage | V_p | $6.0 \pm 5\%$ | V |
| Operating ambient temperature range | T_{amb} | 0 to +75 | °C |
| Clock rate | f_c | typ. 5 | MHz |
| Available d.c. fan-out $T_{amb} = 0$ to 75 °C | N_a | \geq | 8 |
| D.C. noise margin $T_{amb} = 25$ °C | M_L | typ. 1.2 | V |
| Power consumption 50% duty cycle, $T_{amb} = 25$ °C | P_{av} | typ. 67 | mW |

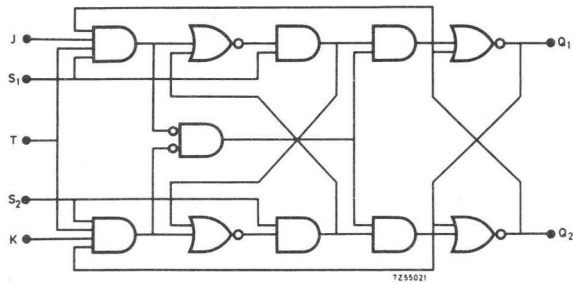
The FCJ111 is a direct-coupled JK flip-flop, operating on the master-slave principle. Operation depends on voltage levels only, i.e. rise and fall times of all input signals, including the trigger signal, are immaterial. The J, K and T inputs are logically equivalent, allowing the use of J and K for triggering. The direct set-inputs (overriding any other inputs) are active at the LOW level.

PACKAGE OUTLINE : 14 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM(to MIL standard 806B)



FUNCTION TABLES

1. Trigger action via T terminal (each flip-flop)

| T = HIGH | | T = LOW | |
|----------|---|----------------|----------------|
| J | K | Q ₁ | Q ₂ |
| H | H | reversed | |
| L | H | L | H |
| H | L | H | L |
| L | L | no change | |

The information on J and K is transferred into the master by T becoming HIGH. When T subsequently goes LOW the outputs will assume the levels shown in the table. Inputs S₁ or S₂ should be HIGH or floating.

2. Trigger action via J and K terminals

| J | K | Q ₁ | Q ₂ |
|-------|-------|----------------|----------------|
| H → L | X | H | L |
| X | H → L | L | H |
| H → L | H → L | reversed | |

If J or K go LOW with T HIGH, Q₁ and Q₂ assume the state shown. If both J and K go LOW with T HIGH, the outputs of Q₁ and Q₂ are reversed (exactly as if J and K remained HIGH and T were triggered). When triggering on J and K the T input requirements V_{TH} and V_{TL} (see CHARACTERISTICS) apply to J and K. S₁ and S₂ should be HIGH or floating.

3. Set or reset via S terminals

| S ₁ | S ₂ | Q ₁ | Q ₂ |
|----------------|----------------|----------------|----------------|
| H | L | L | H |
| L | H | H | L |
| L | L | indeterminate | |
| H | H | no change | |

The set inputs override the other inputs and directly determine the outputs of the flip-flop.

In the case of both set inputs going LOW the first to reach LOW will determine the output conditions.

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|-------------------------------------------|-----------------------------------------------------------------------|-------------|-------|
| Supply voltage | V _P | max. | 8.0 V |
| Output voltage | V _Q | max. | 8.0 V |
| Input voltage | V _J , V _K , V _T , V _S | max. | 8.0 V |
| Output current 1) | -I _Q | max. | 20 mA |
| Input current 2) | -I _J , -I _K , -I _T , -I _S | max. | 20 mA |
| Voltage difference between any two inputs | | max. | 8.0 V |
| Storage temperature | T _{stg} | -55 to +125 | °C |
| Operating ambient temperature | T _{amb} | 0 to +75 | °C |

1) For negative output voltage.

2) At this limit input voltage typ.: -1.5 V.

SYSTEM DESIGN DATA

| | | |
|----------------------------------------|-------------------|--------------------------|
| Uniform system temperature | T_{amb} | 0 to +75 °C |
| Uniform system supply voltage | V_P | 5.7 to 6.3 V |
| Available d.c. fan out | | |
| to T input | N_{aT} | ≥ 4 |
| to J or K input | $N_{aJ} = N_{aK}$ | ≥ 8 |
| to S input | N_{aS} | ≥ 5 |
| to G input | N_{aG} | ≥ 8 |
| D.C. noise margin | | |
| to T input | M_L M_H | min. 0.5 V min. 1.9 V |
| to J or K input | M_L M_H | min. 0.9 V min. 1.9 V |
| to S input | M_L M_H | min. 0.4 V min. 1.9 V |
| to G input | M_L M_H | min. 0.4 V min. 2.3 V |
| Average propagation delay time | t_{pd} | max. 150 ns |
| Maximum clock rate | f_c | ≥ 3 MHz |
| Equivalent input capacitances | | |
| for T input | C_T | typ. 8 pF |
| for J or K input | $C_J = C_K$ | typ. 4 pF |
| for S input | C_S | typ. 8 pF |
| Supply current (duty cycle 50%) | I_{pav} | typ. 11.2 mA |
| Power dissipation at $T_{amb} = 75 °C$ | P_{tot} | max. 110 mW |

CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and references | | |
|------------------------------------------|--------------------------------------------|-----------------------|------|------|---------------------------|--------------------|------------------------------------------------------------------------------------------------------------------------------------|
| | | 0 | +25 | +75 | V _P (V) | | |
| <u>STATIC DATA</u> | | | | | | | |
| Output voltage LOW | V _{QLmax} | 0.4 | 0.4 | 0.4 | V | 5.7 and 6.3 | |
| at: | | | | | | | |
| Output current LOW | I _{QLmax} | 14.0 | 13.2 | 12.4 | mA | 5.7 | |
| | | 16.0 | 15.2 | 14.4 | mA | 6.3 | |
| Output voltage HIGH | V _{QHmin} | 5.3 | 5.4 | 5.3 | V | 5.7 | |
| | | | | | | I _Q = 0 | |
| Output voltage HIGH (lowest permissible) | V _{QHPmin} | 3.9 | 3.5 | 2.8 | V | 5.7 | |
| at: | | | | | | | |
| Output current HIGH | -I _{QHmax} | 350 | 450 | 550 | μA | 5.7 | |
| Input current LOW | -I _{JLmax} , { | 1.75 | 1.65 | 1.55 | mA | 5.7 | } V _I = V _K = 0.4 V; } other inputs } floating } V _T = 0.4 V; other } inputs floating |
| | -I _{KLmax} { | 2.0 | 1.9 | 1.8 | mA | 6.3 | |
| | -I _{TLmax} | 3.5 | 3.3 | 3.1 | mA | 5.7 | |
| | | 4.0 | 3.8 | 3.6 | mA | 6.3 | |
| | -I _{SLmax} | 2.7 | 2.6 | 2.4 | mA | 5.7 | } V _S = 0.4 V; other } inputs floating |
| | | 3.0 | 2.9 | 2.7 | mA | 6.3 | |
| Input current HIGH | I _{JHmax} , I _{KHmax} | 1 | 1 | 25 | μA | 5.7 | V _J = V _K = 5.3 V other inputs 0 V |
| | I _{THmax} | 2 | 2 | 50 | μA | 5.7 | V _T = 5.3 V other inputs 0 V |
| | I _{SHmax} | 2 | 2 | 50 | μA | 5.7 | V _S = 5.3 V other inputs 0 V |
| Supply current | I _{Pmax} | - | 20 | - | mA | 6.3 | J, K, S, T inputs HIGH |

CHARACTERISTICS

| | | T _{amb} (°C) | Conditions and references | | |
|--------------------------------------------|----------------------------------------------------------------|-----------------------|---------------------------|-----------------------------------------------------------------------------------------------------------|------------------------------------------------------------|
| | | | V _P (V) | | fig. |
| <u>DYNAMIC DATA</u> | | | 5.7 and 6.3 | | |
| <u>Change of state</u> | | | | | |
| Input voltage HIGH | V _{THmin} V _{JHmin} V _{KHmin} | 3.1 2.9 2.5 V | } | HIGH level at T and J and/or K to be present simultaneously | 1 |
| during: T-input time HIGH | t _{THmin} | 100 100 100 ns | | | 1 |
| to: Input voltage LOW | V _{TLmax} | 1.3 1.1 0.9 V | | | t _{TLmin} = t _{pdr} |
| <u>No change of state</u> | | | | | |
| JK input voltage LOW | V _{JLmax} V _{KLmax} | 1.8 1.6 1.3 V | } | LOW level at J and K to be present prior to T turning HIGH and to remain present during T is HIGH | 2 |
| <u>Clock skew protection</u> | | | | | |
| Hold time | t _{holdmax} | 20 20 20 ns | | | 2 |
| <u>Set or Reset</u> | | | | | |
| S input voltage LOW | V _{SLmax} | 1.2 1.0 0.8 V | } | active t _{SLmin} = t _{pdr} inactive | 3 |
| S input voltage HIGH | V _{SHmin} | 3.1 2.9 2.5 V | | | |
| <u>DYNAMIC DATA</u> | | | | | |
| <u>Propagation delay times from T to Q</u> | | | | | |
| Rise propagation delay time | t _{pdr max} | - 200 - ns | } | V _{pd} = 1.5 V N = 1; C _L = 60 pF other output N = 8; C _L = 56 pF | 4 |
| Fall propagation delay time | t _{pdf max} | - 100 - ns | | | { V _{pd} = 1.5 V N = 8; C _L = 56 pF |

CHARACTERISTICS (continued)

DYNAMIC DATA

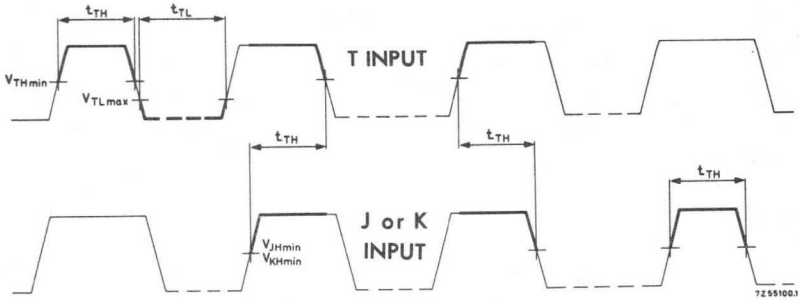


Fig. 1. Waveforms illustrating conditions for change of state.

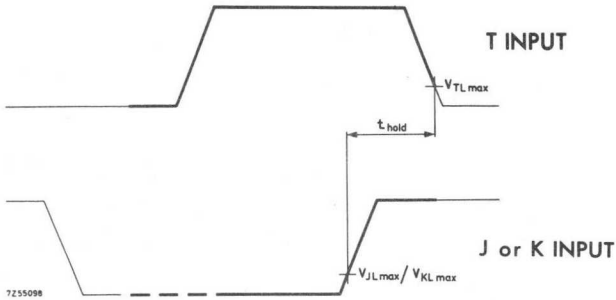


Fig. 2. Waveforms illustrating conditions for no change of state.

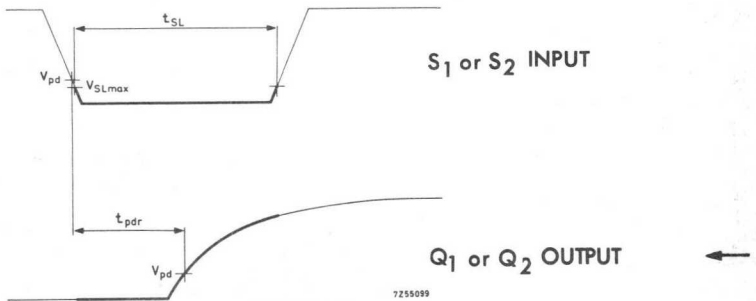
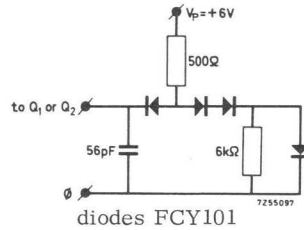
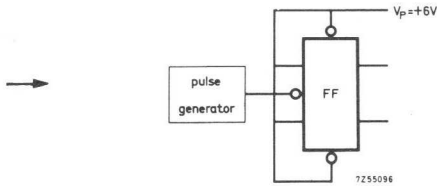
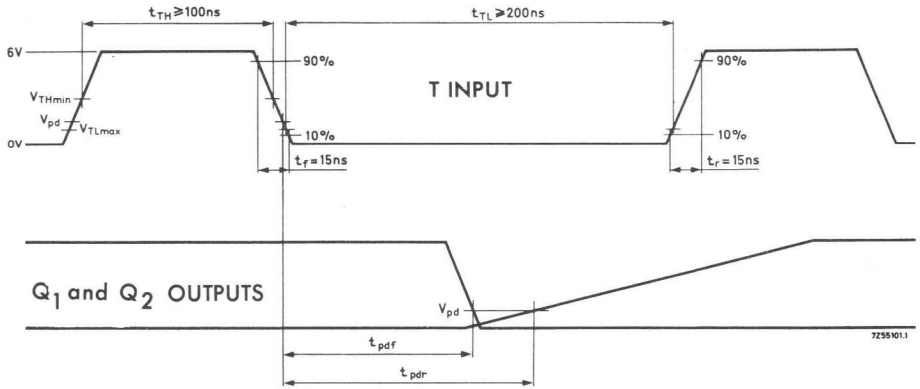


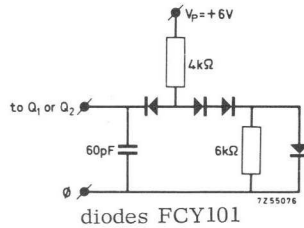
Fig. 3. Waveforms illustrating conditions for set or reset.

CHARACTERISTICS (continued)

DYNAMIC DATA



Equivalent load for $N = 8$ and $C_L^1) = 56\text{ pF}$



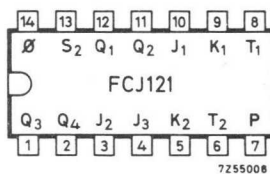
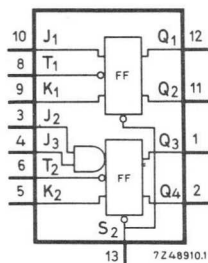
Equivalent load for $N = 1$ and $C_L^1) = 60\text{ pF}$

Fig. 4. Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf} .

1) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

DUAL JK MASTER-SLAVE FLIP-FLOP



QUICK REFERENCE DATA

| | | |
|-------------------------------------------------------------------------|-----------|-----------------|
| Supply voltage | V_p | $6.0 \pm 5\%$ V |
| Operating ambient temperature range | T_{amb} | 0 to +75 °C |
| Clock rate | f_c | typ. 7 MHz |
| Available d.c. fan out $T_{amb} = 0$ to +75 °C | N_a | ≥ 8 |
| D.C. noise margin $T_{amb} = 25$ °C | M_L | typ. 1.2 V |
| Power consumption 50% duty cycle, $T_{amb} = 25$ °C (each flip-flop) | P_{av} | typ. 50 mW |

The FCJ121 comprises two independent direct coupled JK flip-flops, operating on the master-slave principle. Operation depends on voltage levels only, i.e. rise and fall times of all input signals including trigger signals are immaterial. The common set-input (overriding any other inputs) is active at the LOW level. Typical applications are in medium speed counters.

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A). (See General Section)

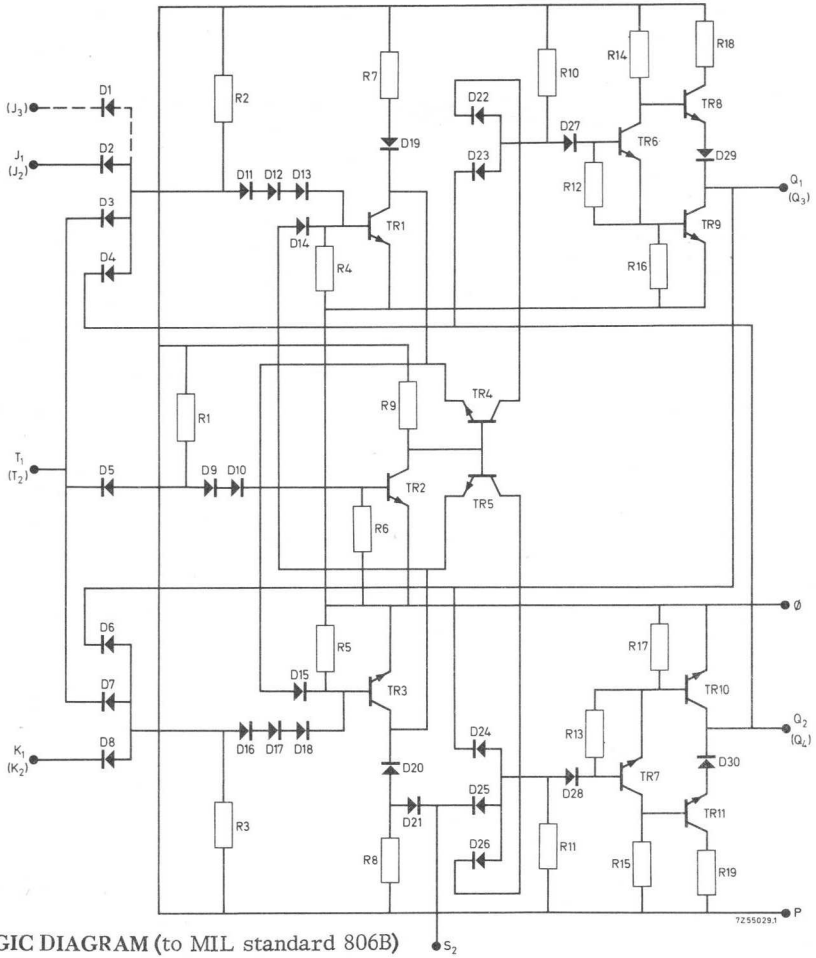
FCJ121

dual flip-flop

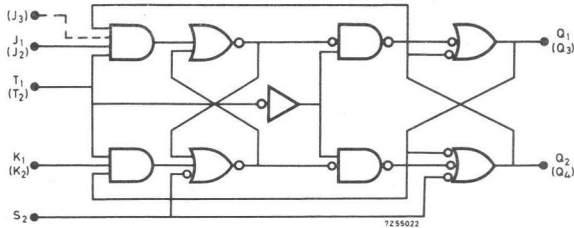
FC family

standard temperature range

CIRCUIT DIAGRAM



LOGIC DIAGRAM (to MIL standard 806B)



FUNCTION TABLES

1. Trigger action via T terminal (each flip-flop)

| T = HIGH | | T = LOW | |
|----------------|----------------|----------------|----------------|
| J ₁ | K ₁ | Q ₁ | Q ₂ |
| J ₂ | K ₂ | Q ₃ | Q ₄ |
| H | H | reversed | |
| L | H | L | H |
| H | L | H | L |
| L | L | no change | |

The information on J and K is transferred into the master by T becoming HIGH. When T subsequently goes LOW the outputs will assume the levels shown in the table. Input S₂ should be HIGH or floating.

For the flip-flop with two J-inputs: $J = J_2 \cdot J_3$ for positive logic

2. Set or Reset via S₂ terminal (both flip-flops)

| | | |
|----------------|----------------|----------------|
| S ₂ | Q ₁ | Q ₂ |
| S ₄ | Q ₃ | Q ₄ |
| L | L | H |
| H | no change | |

The set input overrides the other inputs and directly determines the outputs of both flip-flops.

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

RATINGS (Limiting values)¹⁾

| | | | |
|-------------------------------------------|-----------------------------------------------------------------------|------|----------------|
| Supply voltage | V _P | max. | 8.0 V |
| Output voltage | V _Q | max. | 8.0 V |
| Input voltage | V _J , V _K , V _T , V _S | max. | 8.0 V |
| Output current ²⁾ | -I _Q | max. | 20 mA |
| Input current ³⁾ | -I _J , -I _K , -I _T , -I _S | max. | 20 mA |
| Voltage difference between any two inputs | | max. | 8.0 V |
| Storage temperature | T _{stg} | | -55 to +125 °C |
| Operating ambient temperature | T _{amb} | | 0 to +75 °C |

¹⁾ Limiting values according to the Absolute Maximum System as defined in IEC publication 134.

²⁾ For negative output voltage in LOW state.

³⁾ At this limit input voltage typ. : -1.5 V

SYSTEM DESIGN DATA

| | | |
|------------------------------------------------------|-------------------|--------------------------|
| Uniform system temperature | T_{amb} | 0 to +75 °C |
| Uniform system supply voltage | V_F | 5.7 to 6.3 V |
| Available d. c. fan out | | |
| to T input | N_{aT} | ≥ 3 |
| to J or K input | $N_{aJ} = N_{aK}$ | ≥ 10 |
| to S input | N_{aS} | ≥ 2 |
| to G input | N_{aG} | ≥ 8 |
| D. C. noise margin | | |
| to T input | M_L M_H | min. 0.3 V min. 1.2 V |
| to J or K input | M_L M_H | min. 0.7 V min. 1.2 V |
| to S input | M_L M_H | min. 0.3 V min. 1.9 V |
| to G input | M_L M_H | min. 0.4 V min. 1.5 V |
| Average propagation delay time | t_{pd} | max. 105 ns |
| Maximum clock rate | f_c | ≥ 5 MHz |
| Equivalent input capacitances | | |
| for T input | C_T | typ. 12 pF |
| for J or K input | $C_J = C_K$ | typ. 4 pF |
| for S input | C_S | typ. 16 pF |
| Supply current (duty cycle 50%) ¹⁾ | I_{pav} | typ. 16.8 mA |
| Power dissipation at $T_{amb} = 75$ °C ¹⁾ | P_{tot} | max. 150 mW |

¹⁾ Both flip-flops together.

CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and references | |
|-------------------------------------------|-----------------------|------------------------------------|------|------|---------------------------|-------------|
| | | 0 | +25 | +75 | V _P (V) | |
| <u>STATIC DATA</u> | | | | | | |
| Output voltage LOW | V _{QL} | 0.4 | 0.4 | 0.4 | V | 5.7 and 6.3 |
| at: | | | | | | |
| Output current LOW | I _{QLmax} | 14.0 | 16.5 | 12.4 | mA | 5.7 |
| | | 16.0 | 19.0 | 14.4 | mA | 6.3 |
| Output voltage HIGH | V _{QHmin} | 3.8 | 3.9 | 4.1 | V | 5.7 |
| | | I _Q = -100 μA | | | | |
| Output voltage HIGH (lowest permissible) | V _{QHPmin} | 3.6 | 3.3 | 3.0 | V | 5.7 |
| at: | | | | | | |
| Output current HIGH | -I _{QHmax} | 0.85 | 3.3 | 5.5 | mA | 5.7 |
| Input current LOW | -I _{JLmax} , | 1.4 | 1.3 | 1.2 | mA | 5.7 |
| | -I _{KLmax} | 1.6 | 1.5 | 1.4 | mA | 6.3 |
| | -I _{TLmax} | 4.0 | 3.8 | 3.5 | mA | 5.7 |
| | | 4.5 | 4.2 | 3.9 | mA | 6.3 |
| | -I _{SLmax} | 5.7 | 5.5 | 5.2 | mA | 5.7 |
| | | 6.6 | 6.3 | 5.8 | mA | 6.3 |
| Input current HIGH | I _{JHmax} , | 1 | 1 | 25 | μA | 5.7 |
| | I _{KHmax} | | | | | 5.7 |
| | I _{THmax} | 3 | 3 | 75 | μA | 5.7 |
| | I _{SHmax} | 4 | 4 | 100 | μA | 5.7 |
| Supply current (both flip-flops together) | I _{Pmax} | - | 26.7 | - | mA | 6.3 |
| | | T input LOW J, K, S inputs HIGH | | | | |



CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and references | | |
|--------------------------------------------|----------------------------------------------------------------|-----------------------|-----|-----|---------------------------|---------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------|
| | | 0 | +25 | +75 | V _P (V) | fig. | |
| <u>DYNAMIC DATA</u> | | | | | 5.7 and 6.3 | | |
| <u>Change of state</u> | | | | | | | |
| Input voltage HIGH | V _{THmin} V _{JHmin} V _{KHmin} | 2.6 | 2.3 | 1.9 | V | HIGH level at T and J and/or K to be present simultaneously | 1 |
| during: Input time HIGH | t _{THmin} | 60 | 60 | 60 | ns | | 1 |
| to: T-input voltage LOW | V _{TLmax} | 1.0 | 1.0 | 0.7 | V | t _{TLmin} = t _{pdf} | 1 |
| <u>No change of state</u> | | | | | | | |
| J/K input voltage LOW | V _{JLmax} V _{KLmax} | 1.6 | 1.4 | 1.1 | V | LOW level at J and K to be present prior to T turning HIGH and to remain present during T is HIGH | 2 |
| <u>Clock skew protection</u> | | | | | | | |
| Hold time | t _{hold max} | 10 | 10 | 10 | ns | | 2 |
| <u>Reset</u> | | | | | | | |
| S input voltage LOW | V _{SLmax} | 1.0 | 1.0 | 0.7 | V | active t _{SLmin} = t _{pdf} inactive | 3 |
| S input voltage HIGH | V _{SHmin} | 1.9 | 1.8 | 1.6 | V | | |
| <u>DYNAMIC DATA</u> | | | | | | | |
| <u>Propagation delay times from T to Q</u> | | | | | | | |
| Rise propagation delay time | t _{pdr max} | - | 90 | - | ns | 6.0 { V _{pd} = 1.5 V N = 1; C _L = 60 pF | 4 |
| Fall propagation delay time | t _{pdf max} | - | 120 | - | ns | | 6.0 { V _{pd} = 1.5 V N = 8; C _L = 60 pF other output: N = 1; C _L = 60 pF |

CHARACTERISTICS(continued)

DYNAMIC DATA

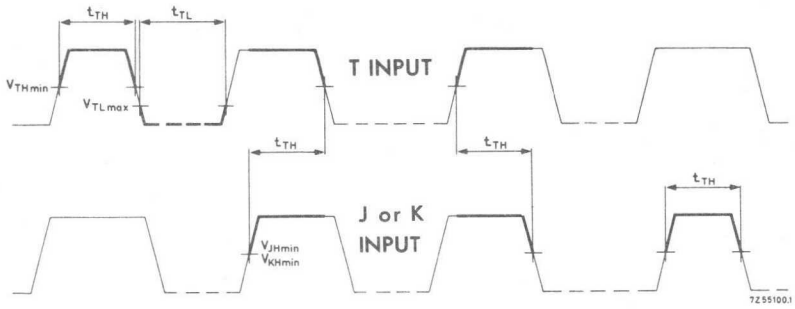


Fig. 1. Waveforms illustrating conditions for change of state.

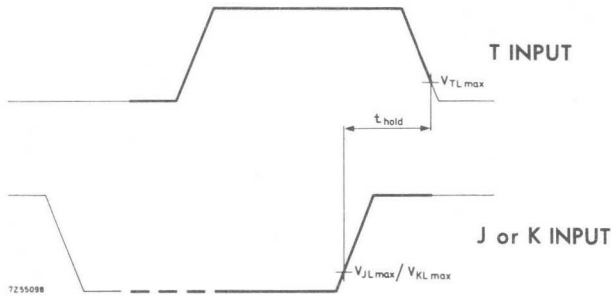


Fig. 2. Waveforms illustrating conditions for no change of state.

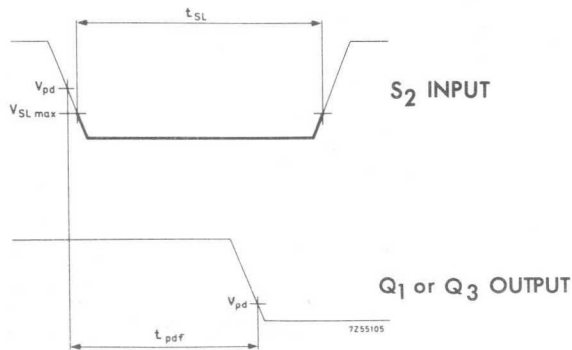
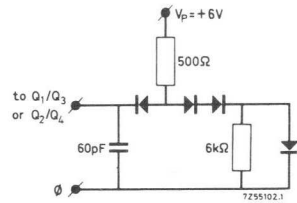
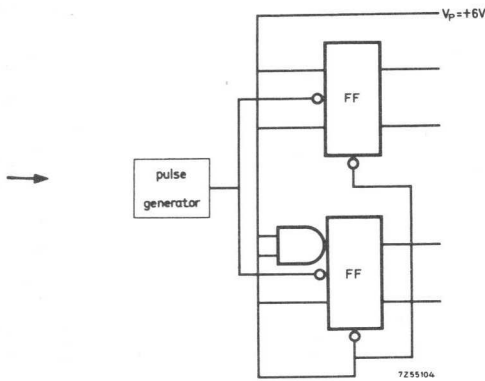
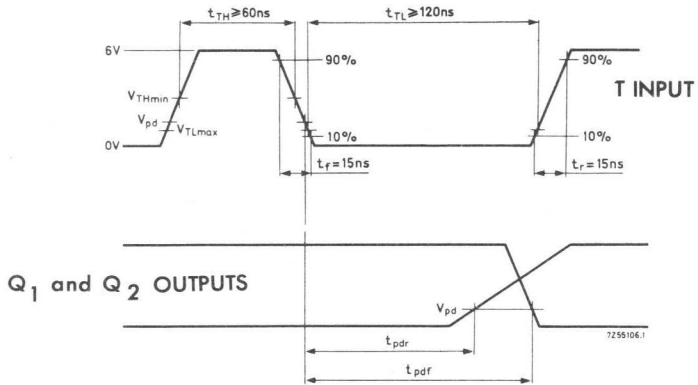


Fig. 3. Waveforms illustrating conditions for set or reset.

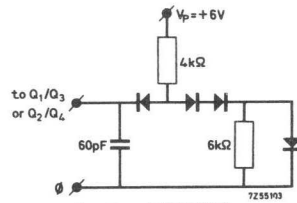
CHARACTERISTICS (continued)

DYNAMIC DATA



diodes FCY101

Equivalent load for $N = 8$ and $C_L^1) = 60 \text{ pF}$



diodes FCY101

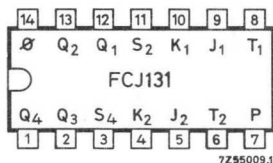
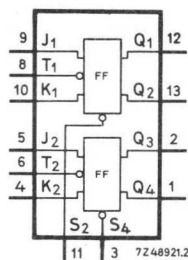
Equivalent load for $N = 1$ and $C_L^1) = 60 \text{ pF}$

Fig. 4. Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf}

1) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

DUAL JK MASTER-SLAVE FLIP FLOP



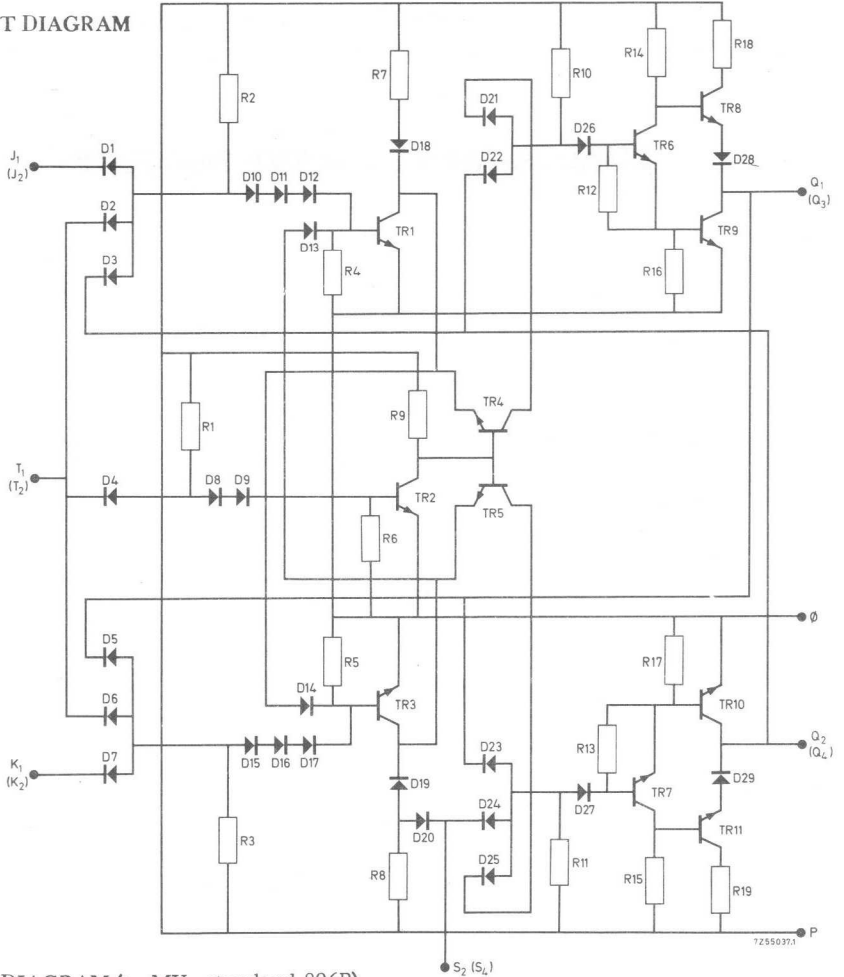
QUICK REFERENCE DATA

| | | | |
|--------------------------------------------------------|-----------|---------------|-----|
| Supply voltage | V_p | $6.0 \pm 5\%$ | V |
| Operating ambient temperature range | T_{amb} | 0 to +75 | °C |
| Clock rate | f_c | typ. 7 | MHz |
| Available d.c. fan out $T_{amb} = 25$ °C | N_a | \geq | 8 |
| D.C. noise margin $T_{amb} = 25$ °C | M_L | typ. 1.2 | V |
| Power consumption 50% duty cycle, $T_{amb} = 25$ °C | P_{av} | typ. 100 | mW |

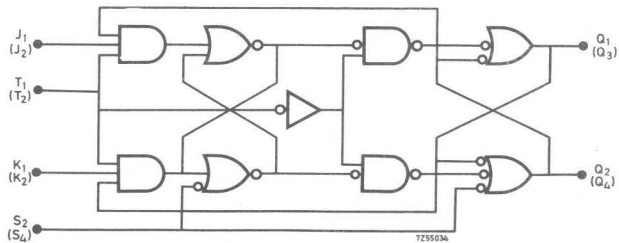
The FCJ131 comprises two independent direct coupled JK flip-flops, operating on the master-slave principle. Operation depends on voltage levels only, i.e. rise and fall times of all input signals, including the trigger signals, are immaterial. The separate set inputs (overriding any other inputs) are active at the LOW level. Typical applications include counters and shift registers.

PACKAGE OUTLINE 14 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM (to MIL standard 806B)



FUNCTION TABLES

1. Trigger action via T terminal (each flip-flop)

| T = HIGH | | T = LOW | |
|----------------|----------------|----------------|----------------|
| J ₁ | K ₁ | Q ₁ | Q ₂ |
| J ₂ | K ₂ | Q ₃ | Q ₄ |
| H | H | reversed | |
| L | H | L | H |
| H | L | H | L |
| L | L | no change | |

The information on J and K is transferred into the master by T becoming HIGH. When T subsequently goes LOW the outputs will assume the levels shown in the table. Inputs S₂ and S₄ should be HIGH or floating.

2. Set or reset via S terminals (each flip-flop)

| | | |
|----------------|----------------|----------------|
| S ₂ | Q ₁ | Q ₂ |
| S ₄ | Q ₃ | Q ₄ |
| L | L | H |
| H | no change | |

The set inputs override the other inputs and directly determine the outputs of the relevant flip-flop.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

| | | | |
|-------------------------------------------|-----------------------------------------------------------------------|------|----------------|
| Supply voltage | V _P | max. | 8.0 V |
| Output voltage | V _Q | max. | 8.0 V |
| Input voltage | V _J , V _K , V _T , V _S | max. | 8.0 V |
| Output current ¹⁾ | -I _Q | max. | 20 mA |
| Input current ²⁾ | -I _J , -I _K , -I _T , -I _S | max. | 20 mA |
| Voltage difference between any two inputs | | max. | 8.0 V |
| Storage temperature | T _{stg} | | -55 to +125 °C |
| Operating ambient temperature | T _{amb} | | 0 to +75 °C |

¹⁾ For negative output voltage in LOW state.

²⁾ At this limit input voltages typ. : -1.5V.

SYSTEM DESIGN DATA

| | | |
|------------------------------------------------------|-------------------|--------------------------|
| Uniform system temperature | T_{amb} | 0 to +75 °C |
| Uniform system supply voltage | V_P | 5.7 to 6.3 V |
| Available d. c. fan out | | |
| to T input | N_{aT} | ≥ 3 |
| to J or K input | $N_{aJ} = N_{aK}$ | ≥ 10 |
| to S input | N_{aS} | ≥ 4 |
| to G input | N_{aG} | ≥ 8 |
| D. C. noise margin | | |
| to T input | M_L M_H | min. 0.3 V min. 1.2 V |
| to J or K input | M_L M_H | min. 0.7 V min. 1.2 V |
| to S input | M_L M_H | min. 0.3 V min. 1.9 V |
| to G input | M_L M_H | min. 0.4 V min. 1.5 V |
| Average propagation delay time | t_{pd} | max. 105 ns |
| Maximum clock rate | f_c | ≥ 5 MHz |
| Equivalent input capacitances | | |
| for T input | C_T | typ. 12 pF |
| for J or K input | $C_J = C_K$ | typ. 4 pF |
| for S input | C_S | typ. 8 pF |
| Supply current (duty cycle 50%) ¹⁾ | I_{pav} | typ. 16.8 mA |
| Power dissipation at $T_{amb} = 75$ °C ¹⁾ | P_{tot} | max. 150 mW |

¹⁾ Both flip-flops together

CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and references | |
|-------------------------------------------|--------------------------------------------|-----------------------|--------------|--------------|---------------------------|-----------------------------------------------------------------|
| | | 0 | +25 | +75 | V _P (V) | |
| STATIC DATA | | | | | | |
| Output voltage LOW | V _{QLmax} | 0.4 | 0.4 | 0.4 | V | 5.7 and 6.3 |
| at: Output current LOW | I _{QLmax} | 14.0 16.0 | 16.5 19.0 | 12.4 14.4 | mA | 5.7 6.3 |
| Output voltage HIGH | V _{QHmin} | 3.8 | 3.9 | 4.1 | V | 5.7 I _Q = -100 μA |
| Output voltage HIGH (lowest permissible) | V _{QHPmin} | 3.6 | 3.3 | 3.0 | V | 5.7 |
| at: Output current HIGH | -I _{QHmax} | 0.85 | 3.3 | 5.5 | mA | 5.7 |
| Input current LOW | -I _{JLmax} | 1.4 1.6 | 1.3 1.5 | 1.2 1.4 | mA | 5.7 6.3 |
| | -I _{KLmax} | | | | | |
| | -I _{TLmax} | 4.0 | 3.8 | 3.5 | mA | 5.7 |
| | | 4.5 | 4.2 | 3.9 | mA | 6.3 |
| -I _{SLmax} | 2.9 3.3 | 2.8 3.2 | 2.6 2.9 | mA | 5.7 6.3 | |
| Input current HIGH | I _{JHmax} , I _{KHmax} | 1 | 1 | 25 | μA | 5.7 V _J = V _K = 5.3 V other inputs 0 V |
| | I _{THmax} | 3 | 3 | 75 | μA | 5.7 V _T = 5.3 V other inputs 0 V |
| | I _{SHmax} | 2 | 2 | 50 | μA | 5.7 V _S = 5.3 V other inputs 0 V |
| Supply current (both flip-flops together) | I _{Pmax} | - | 26.7 | - | mA | 6.3 T inputs LOW J, K, S inputs HIGH |

CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and references | | |
|--------------------------------------------|----------------------------------------------------------------|-----------------------|-----|-----|---------------------------|-----------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------|
| | | 0 | +25 | +75 | V _P (V) | fig. | |
| <u>DYNAMIC DATA</u> | | | | | 5.7 and 6.3 | | |
| <u>Change of state</u> | | | | | | | |
| Input voltage HIGH | V _{THmin} V _{JHmin} V _{KHmin} | 2.6 | 2.3 | 1.9 | V | } HIGH level at T and J and/or K to be present simultaneously | |
| during: Input time HIGH | t _{THmin} | 60 | 60 | 60 | ns | | 1 |
| to: T-input voltage LOW | V _{TLmax} | 1.0 | 1.0 | 0.7 | V | t _{TLmin} = t _{pdf} | 1 |
| <u>No change of state</u> | | | | | | | |
| J/K input voltage LOW | V _{JLmax} V _{KLmax} | 1.6 | 1.4 | 1.1 | V | } LOW level at J and K to be present prior to T turning HIGH and to remain present during T is HIGH | 2 |
| <u>Clock skew protection</u> | | | | | | | |
| Hold time | t _{hold max} | 10 | 10 | 10 | ns | | 2 |
| <u>Reset</u> | | | | | | | |
| S input voltage LOW | V _{SLmax} | 1.0 | 1.0 | 0.7 | V | } active t _{SLmin} = t _{pdf} inactive | 3 |
| S input voltage HIGH | V _{SHmin} | 1.9 | 1.8 | 1.6 | V | | |
| <u>DYNAMIC DATA</u> | | | | | | | |
| <u>Propagation delay times from T to Q</u> | | | | | | | |
| Rise propagation delay time | t _{pdr max} | - | 90 | - | ns | } V _{pd} = 1.5 V N = 1; C _L = 60 pF | 4 |
| Fall propagation delay time | t _{pdf max} | - | 120 | - | ns | | } V _{pd} = 1.5 V N = 8; C _L = 60 pF other output: N = 1; C _L = 60 pF |

CHARACTERISTICS (continued)

DYNAMIC DATA

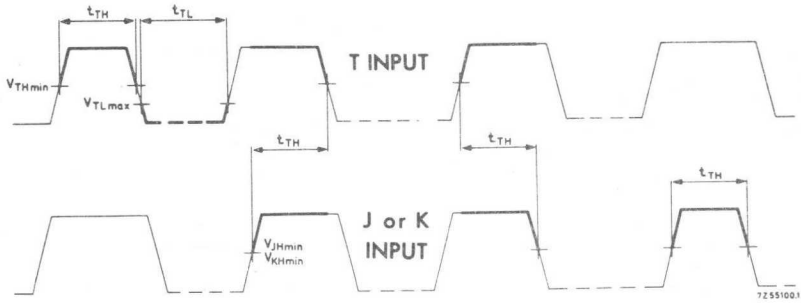


Fig. 1. Waveforms illustrating conditions for change of state.

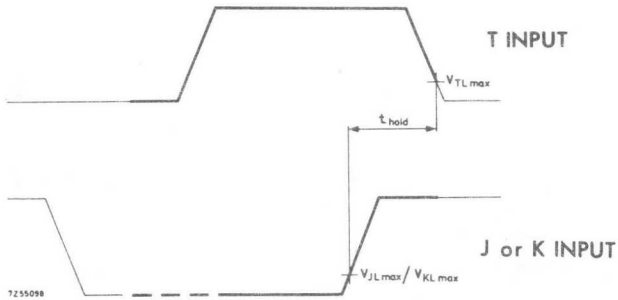


Fig. 2. Waveforms illustrating conditions for no change of state.

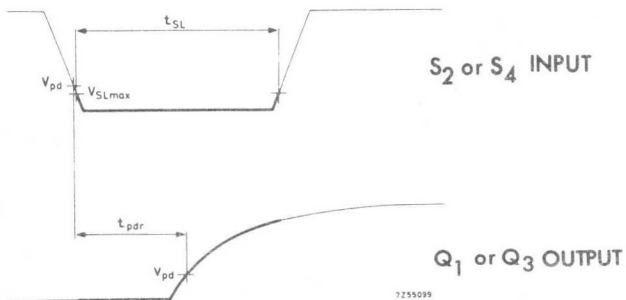
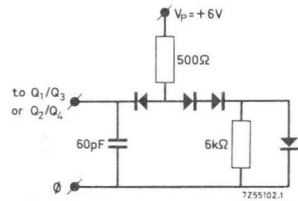
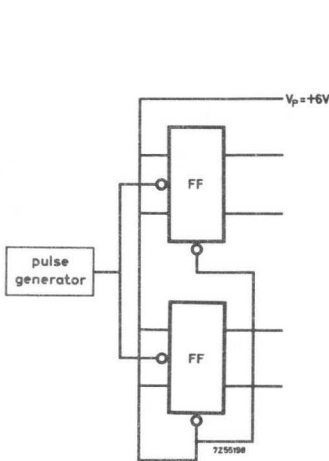
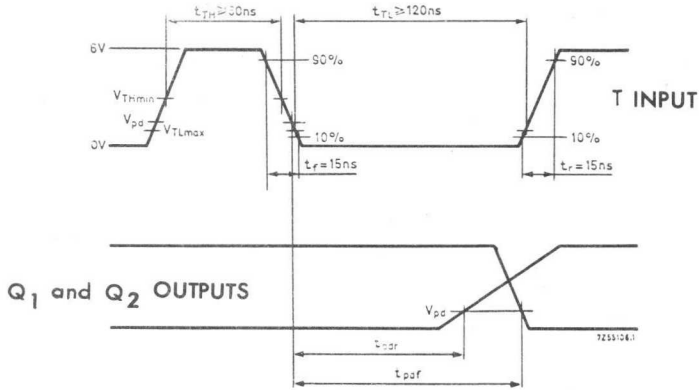


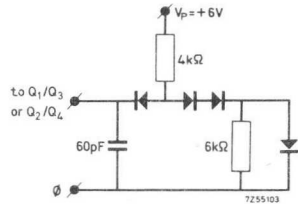
Fig. 3. Waveforms illustrating conditions for set or reset.

CHARACTERISTICS (continued)

DYNAMIC DATA



Diodes FCY101
Equivalent load for $N = 8$ and $C_L^1) = 60 \text{ pF}$

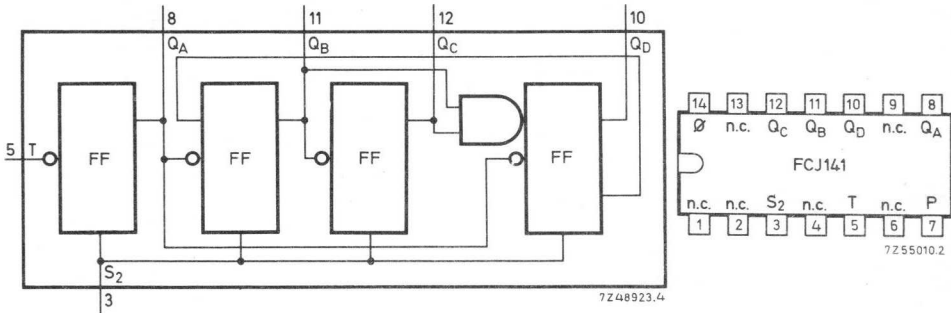


Diodes FCY101
Equivalent load for $N = 1$ and $C_L^1) = 60 \text{ pF}$

Fig. 4. Waveforms and loading circuits illustrating measurement of t_{pdR} and t_{pdf} .
1) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

SINGLE ASYNCHRONOUS 10-COUNTER



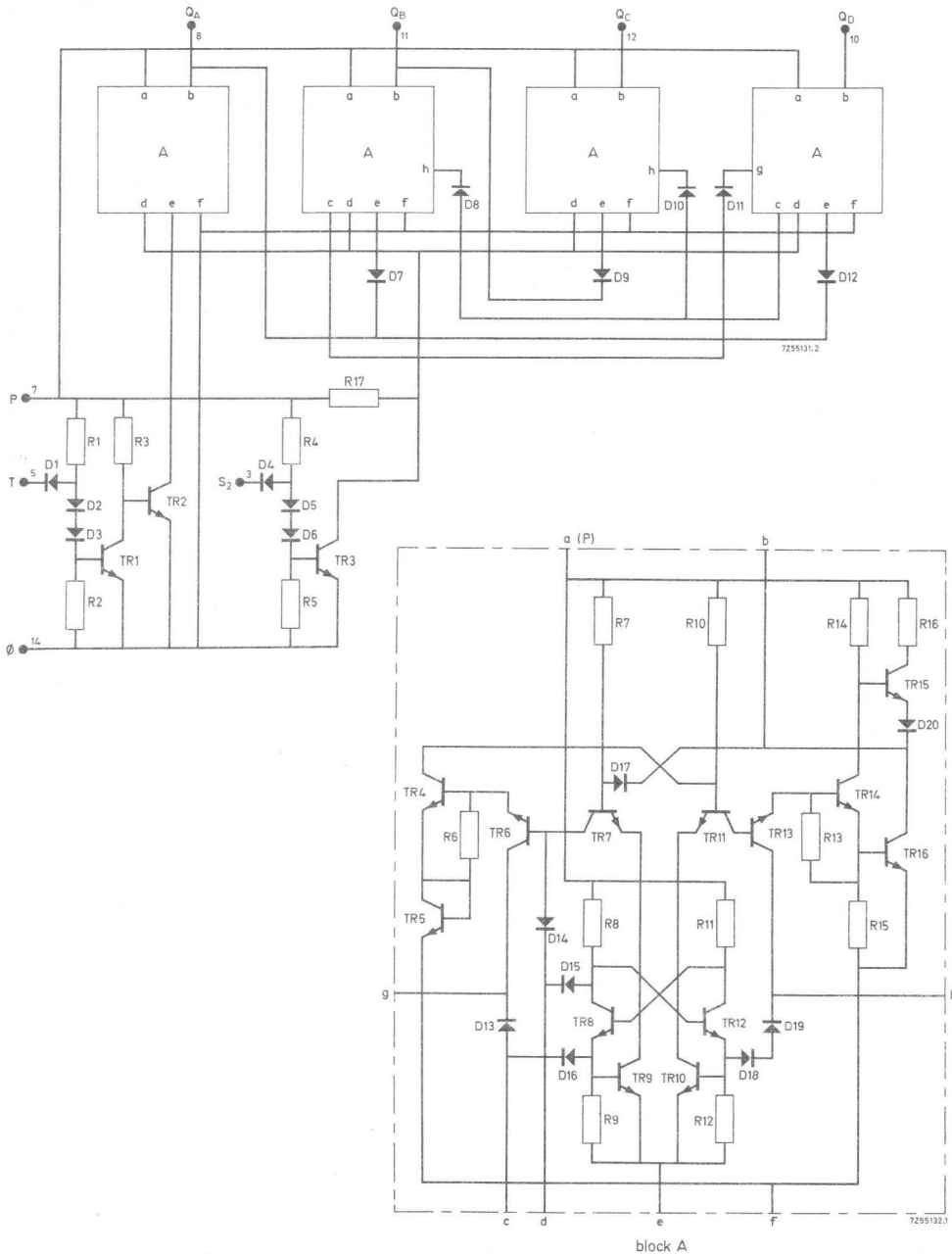
QUICK REFERENCE DATA

| | | |
|--------------------------------------------------------|-----------|-----------------|
| Supply voltage | V_P | $6.0 \pm 5\%$ V |
| Operating ambient temperature range | T_{amb} | 0 to +75 °C |
| Clock rate | f_c | typ. 7 MHz |
| Available d. c. fan out $T_{amb} = 25$ °C | N_a | ≥ 8 |
| D. C. noise margin $T_{amb} = 25$ °C | M_L | typ. 1.2 V |
| Power consumption 50% duty cycle, $T_{amb} = 25$ °C | P_{av} | typ. 180 mW |

The FCJ141 is four master-slave flip-flops interconnected to form an a-synchronous decade counter in the 8-4-2-1 code. The information is transferred to the master when the trigger signal is HIGH (the first flip-flop is triggered by the count input at T). When the trigger signal is LOW the information is transferred to the slaves and appears at the outputs. A common reset input S_2 directly resets the outputs and overrides the T input.

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAMS



FUNCTION TABLES

| Count | OUTPUT | | | |
|-------|--------|----|----|----|
| | QD | QC | QB | QA |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |

| S2 | QD | QC | QB | QA |
|----|-------|----|----|----|
| L | count | | | |
| H | L | L | L | L |

Input S when being at the HIGH state overrides the count input and directly resets all outputs in the LOW state

H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|-------------------------------------------|--------------|------|----------------|
| Supply voltage | V_P | max. | 8.0 V |
| Input voltage | $V_T; V_S$ | max. | 8.0 V |
| Output voltage | V_Q | max. | 8.0 V |
| Input current 1) | $-I_S; -I_T$ | max. | 20 mA |
| Output current 2) | $-I_Q$ | max. | 20 mA |
| Voltage difference between any two inputs | | max. | 8.0 V |
| Storage temperature | T_{stg} | | -35 to +125 °C |
| Operating ambient temperature | T_{amb} | | 0 to +75 °C |

1) At this limit, input voltage typ. -1.5 V.

2) For negative output voltage in LOW state.

SYSTEM DESIGN DATA

| | | | |
|----------------------------------------------|-----------|------------|-------------|
| Uniform system temperature | T_{amb} | 0 to +75 | $^{\circ}C$ |
| Uniform system supply voltage | V_P | 5.7 to 6.3 | V |
| Available d. c. fan out | N_a | \geq | 8 |
| D. C. noise margin | | | |
| to T input | M_L | min. 0.4 | V |
| | M_H | min. 1.6 | V |
| to S input | M_L | min. 0.4 | V |
| | M_H | min. 1.6 | V |
| Average propagation delay time | | | |
| T input to Q_3 output | t_{pd} | typ. 200 | ns |
| Clock rate | f_c | max. 3.5 | MHz |
| Equivalent input capacitances | | | |
| for T input | C_T | typ. 4 | pF |
| for S input | C_S | typ. 4 | pF |
| Supply current (duty cycle 50%) | I_{pav} | max. 46 | mA |
| Power dissipation at $T_{amb} = 75^{\circ}C$ | P_{tot} | max. 270 | mW |

CHARACTERISTICS

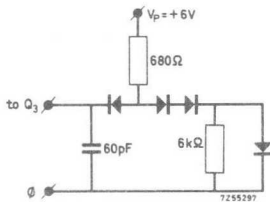
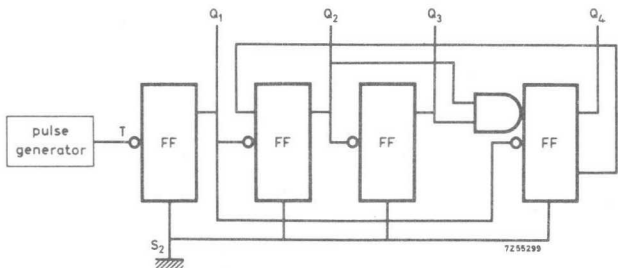
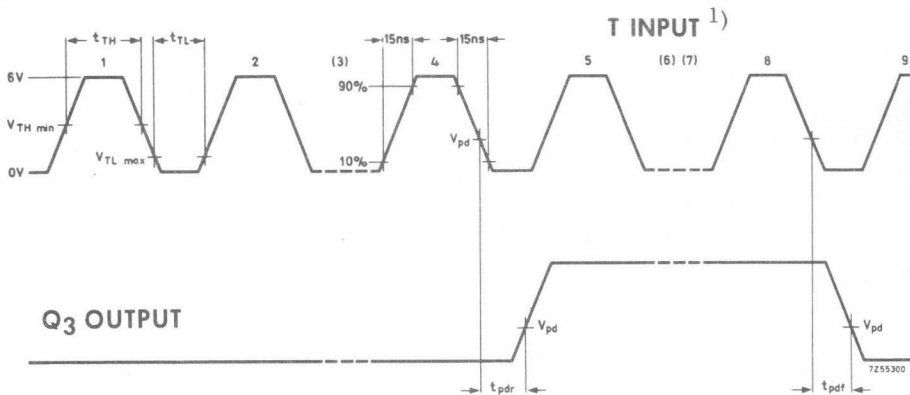
| | | T _{amb} (°C) | | | Conditions and references | |
|---------------------------------------------|-----------------------|-----------------------|------|------|---------------------------|-----------------------------------------------------|
| | | | | | | |
| <u>STATIC DATA</u> | | | | | | |
| Output voltage LOW | V _{QL} max. | 0.4 | 0.4 | 0.4 | V | 5.7 and 6.3 |
| at: | | | | | | |
| Output current LOW | I _{QLmax} | 14.0 | 13.2 | 12.4 | mA | 5.7 |
| | I _{QLmax} | 16.0 | 15.2 | 14.4 | mA | 6.3 |
| Output voltage HIGH | V _{QH} min. | 3.8 | 3.9 | 4.1 | V | 5.7 |
| at: | | | | | | |
| Output current HIGH | -I _{QH} | 100 | 100 | 100 | μA | 5.7 |
| Output voltage HIGH (lowest permissible) | V _{QHP} min. | 3.6 | 3.3 | 3.0 | V | 5.7 |
| at: | | | | | | |
| Output current HIGH | -I _{QHmax} | 0.85 | 3.3 | 5.5 | mA | 5.7 |
| Input current LOW | -I _{TL} max. | 1.75 | 1.65 | 1.55 | mA | 5.7 |
| | -I _{SL} max. | 1.75 | 1.65 | 1.55 | mA | 5.7 |
| | -I _{TL} max. | 2.0 | 1.9 | 1.8 | mA | 6.3 |
| | -I _{SL} max. | 2.0 | 1.9 | 1.8 | mA | 6.3 |
| | | | | | | V _T = V _S = 0.4 V |
| Input current HIGH | I _{TH} max. | 1.0 | 1.0 | 25.0 | μA | 5.7 |
| | I _{SH} max. | | | | | |
| | | | | | | V _T = V _S = 5.3 V |
| Supply current | I _{Pmax} | - | 45 | 40 | mA | 6.3 |
| | | | | | | { V _T = 0 V V _S = floating |

CHARACTERISTICS (continued)

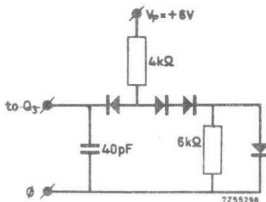
| <u>STATIC AND DYNAMIC DATA</u> | | T_{amb} (°C) | | | Conditions and references | |
|-------------------------------------------------------------------------------------------------------------------|---------------------------|----------------|-----|-----|---------------------------|-------------|
| | | 0 | 25 | 75 | V_p (V) | |
| <u>Reset input active</u> HIGH level at S to be present during | V_{SHmin} | 2.3 | 2.2 | 2.1 | V | 5.7 and 6.3 |
| | t_{SHmin} | 100 | 100 | 140 | ns | |
| <u>Reset input inactive</u> LOW level at S | V_{SLmax} | 1.0 | 1.0 | 0.8 | V | 5.7 and 6.3 |
| | | | | | | |
| <u>Change of state of the master of the lowest order flip-flop</u> HIGH level at T to be present during | V_{THmin} | 2.3 | 2.2 | 2.1 | V | 5.7 and 6.3 |
| | t_{THmin} | - | 100 | - | ns | |
| <u>Change of state of the slave of the lowest order flip-flop</u> | | | | | | |
| <u>Slope of falling edge at T</u> | $(-\frac{dt}{dV})_{Tmax}$ | 1 | 1 | 1 | $\mu s/V$ | |
| LOW level at T to be present during | V_{TLmax} | 1.0 | 1.0 | 0.8 | V | 5.7 and 6.3 |
| | t_{TLmin} | 100 | 100 | 140 | ns | |
| <u>Propagation delay times from T to Q3</u> | | | | | | |
| Propagation delay reference level | V_{pd} | | 1.5 | | V | |
| Rise propagation delay time | $t_{pdr max}$ | - | 200 | - | ns | 6.0 |
| Fall propagation delay time | $t_{pdf max}$ | - | 200 | - | ns | 6.0 |

CHARACTERISTICS (continued)

DYNAMIC DATA



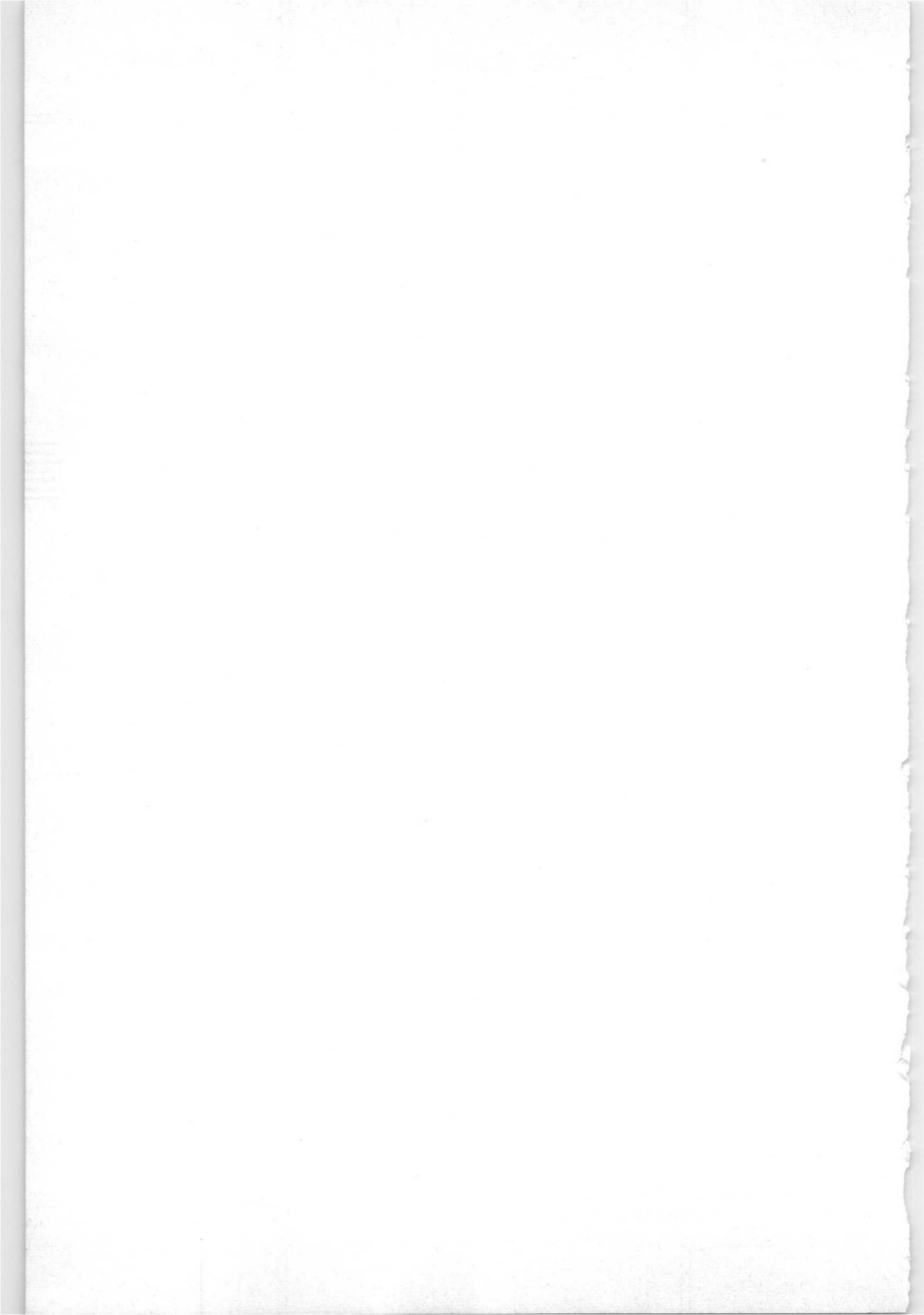
diodes FCY101
 $C_L^{(2)} = 60\text{ pF}$
Equivalent load for N = 6



diodes FCY101
 $C_L^{(2)} = 40\text{ pF}$
Equivalent load for N = 1

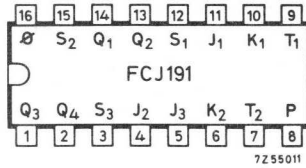
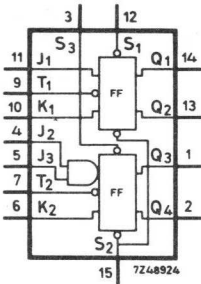
1) The falling edge of the T input signals is max. 1 $\mu\text{s}/V$

2) Including jig and probe capacitance



The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

DUAL JK MASTER-SLAVE FLIP-FLOP



QUICK REFERENCE DATA

| | | | |
|-------------------------------------|-----------|---------------|-----|
| Supply voltage | V_P | $6.0 \pm 5\%$ | V |
| Operating ambient temperature range | T_{amb} | 0 to +75 | °C |
| Clock rate | f_c | typ. 7 | MHz |
| Available d.c. fan-out | N_a | \geq | 8 |
| $T_{amb} = 0$ to +75 °C | | | |
| D.C. noise margin | M_L | typ. 1.2 | V |
| $T_{amb} = 25$ °C | | | |
| Power consumption | P_{av} | typ. 100 | mW |
| 50% duty cycle, $T_{amb} = 25$ °C | | | |

The FCJ191 comprises two independent direct coupled JK flip-flops, operating on the master-slave principle. Operation depends on voltage levels only, e.g. rise and fall times of all input signals including the trigger signal are immaterial. The set and reset inputs (overriding any other inputs) are active at the LOW level. Typical applications include counters and shift registers.

PACKAGE OUTLINE 16 lead plastic dual in-line (type A). (See General Section)

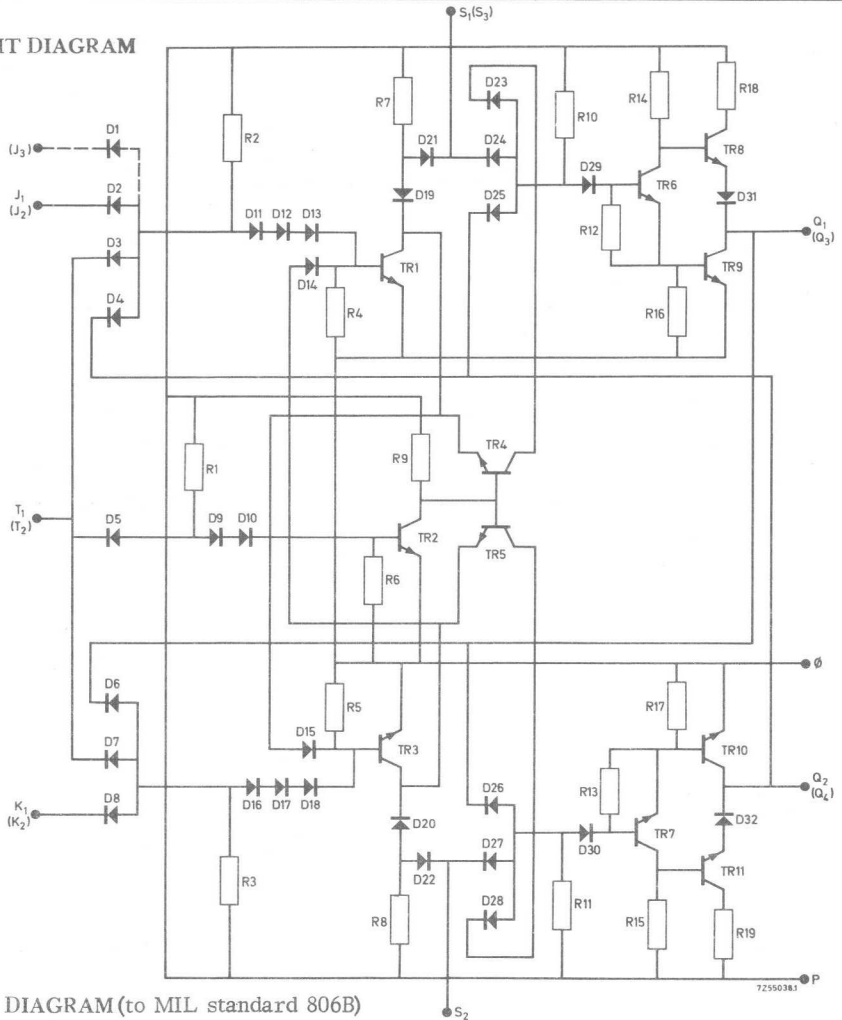
FCJ191

dual flip-flop

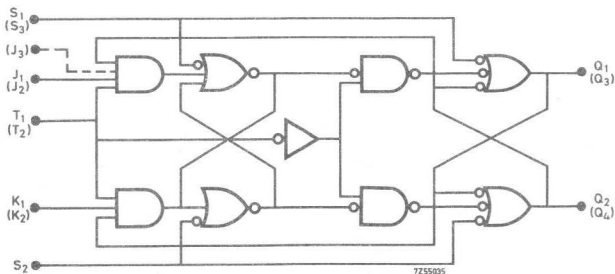
FC family

standard temperature range

CIRCUIT DIAGRAM



LOGIC DIAGRAM (to MIL standard 806B)



FUNCTION TABLES

1. Trigger action via T terminal (each flip-flop)

| T = HIGH | | T = LOW | |
|----------------|----------------|----------------|----------------|
| J ₁ | K ₁ | Q ₁ | Q ₂ |
| J | K ₂ | Q ₃ | Q ₄ |
| H | H | reversed | |
| L | H | L | H |
| H | L | H | L |
| L | L | no change | |

The information on J and K is transferred into the master by T becoming HIGH. When T subsequently goes LOW the outputs will assume the levels shown in the table. Inputs S₁, S₂ and S₃ should be HIGH or floating.

For the flip-flop with two J-inputs is $J = J_2 \cdot J_3$ for positive logic

2. Set or reset via S terminals

| | | | |
|----------------|----------------|----------------|----------------|
| S ₁ | S ₂ | Q ₁ | Q ₂ |
| S ₃ | S ₂ | Q ₃ | Q ₄ |
| H | L | L | H |
| L | H | H | L |
| L | L | H | H |
| H | H | no change | |

The set inputs override the other inputs and directly determine the outputs of the relevant flip-flop.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

| | | | |
|-------------------------------------------|--------------------------|------|----------------|
| Supply voltage | V_P | max. | 8.0 V |
| Output voltage | V_Q | max. | 8.0 V |
| Input voltage | V_J, V_K, V_T, V_S | max. | 8.0 V |
| Output current ¹⁾ | $-I_Q$ | max. | 20 mA |
| Input current ²⁾ | $-I_J, -I_K, -I_T, -I_S$ | max. | 20 mA |
| Voltage difference between any two inputs | | max. | 8.0 V |
| Storage temperature | T_{stg} | | -55 to +125 °C |
| Operating ambient temperature | T_{amb} | | 0 to +75 °C |

1) For negative output voltage in LOW state.

2) At this limit input voltage typ. : -1.5 V

SYSTEM DESIGN DATA

| | | |
|------------------------------------------------------|---------------------|--------------|
| Uniform system temperature | T_{amb} | 0 to +75 °C |
| Uniform system supply voltage | V_p | 5.7 to 6.3 V |
| Available d. c. fan out | | |
| to T input | N_{aT} | ≥ 3 |
| to J or K input | $N_{aJ} = N_{aK}$ | ≥ 10 |
| to S input | N_{aS2} | ≥ 2 |
| | $N_{aS1} = N_{aS3}$ | ≥ 4 |
| to G input | N_{aG} | ≥ 8 |
| D. C. noise margin | | |
| to T input | M_L | min. 0.3 V |
| | M_H | min. 1.2 V |
| to J or K input | M_L | min. 0.7 V |
| | M_H | min. 1.2 V |
| to S input | M_L | min. 0.3 V |
| | M_H | min. 1.9 V |
| to G input | M_L | min. 0.4 V |
| | M_H | min. 1.5 V |
| Average propagation delay time | t_{pd} | max. 105 ns |
| Maximum clock rate | f_c | ≥ 5 MHz |
| Equivalent input capacitances | | |
| for T input | C_T | typ. 12 pF |
| for J or K input | $C_J = C_K$ | typ. 4 pF |
| for S input | C_{S2} | typ. 16 pF |
| | $C_{S1} = C_{S3}$ | typ. 8 pF |
| Supply current (duty cycle 50%) ¹⁾ | I_{pav} | typ. 16.8 mA |
| Power dissipation at $T_{amb} = 75$ °C ¹⁾ | P_{tot} | max. 150 mW |

¹⁾ Both flip-flops together

CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and references | |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|--------------|---------------------------|-------------|
| | | 0 | +25 | +75 | V _P (V) | |
| <u>STATIC DATA</u> | | | | | | |
| Output voltage LOW | V _{QLmax} | 0.4 | 0.4 | 0.4 | V | 5.7 and 6.3 |
| at: Output current LOW | I _{QLmax} | 14.0 16.0 | 16.5 19.0 | 12.4 14.4 | mA mA | 5.7 6.3 |
| Output voltage HIGH | V _{QHmin} | 3.8 | 3.9 | 4.1 | V | 5.7 |
| I _Q = -100 μA | | | | | | |
| Output voltage HIGH (lowest permissible) | V _{QHPmin} | 3.6 | 3.3 | 3.0 | V | 5.7 |
| at: Output current HIGH | -I _{QHmax} | 0.85 | 3.3 | 5.5 | mA | 5.7 |
| Input current LOW | -I _{JLmax} , -I _{KLmax} | 1.4 1.6 | 1.3 1.5 | 1.2 1.4 | mA mA | 5.7 6.3 |
| | -I _{TLmax} | 4.0 4.5 | 3.8 4.2 | 3.5 3.9 | mA mA | 5.7 6.3 |
| | | -I _{S2Lmax} | 5.7 6.6 | 5.5 6.3 | 5.2 5.8 | mA mA |
| | -I _{S1Lmax} -I _{S3Lmax} | | 2.9 3.3 | 2.8 3.2 | 2.6 2.9 | mA mA |
| | | } V _J = V _K = 0.4 V; } other inputs floating } V _T = 0.4 V; other inputs floating } V _S = 0.4 V; other inputs floating } V _S = 0.4 V; other inputs floating | | | | |
| | Input current HIGH | I _{JHmax} , I _{KHmax} | 1 | 1 | 25 | μA |
| I _{THmax} | | 3 | 3 | 75 | μA | 5.7 |
| I _{S2Hmax} | | 4 | 4 | 100 | μA | 5.7 |
| I _{S1Hmax} I _{S3Hmax} | | 2 | 2 | 50 | μA | 5.7 |
| V _J = V _K = 5.3 V other inputs 0 V V _T = 5.3 V other inputs 0 V V _S = 5.3 V other inputs 0 V V _S = 5.3 V other inputs 0 V | | | | | | |
| Supply current (both flip-flops together) | I _{Pmax} | - | 26.7 | - | mA | 6.3 |
| T input LOW J, K, S inputs HIGH | | | | | | |

CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and references | |
|--------------------------------------------|----------------------------------------------------------------|-----------------------|-----|-----|---------------------------|---------------------------------------------------------------------------------------------------|
| | | 0 | +25 | +75 | V _P (V) | fig. |
| <u>DYNAMIC DATA</u> | | | | | 5.7 and 6.3 | |
| <u>Change of state</u> | | | | | | |
| Input voltage HIGH | V _{THmin} V _{JHmin} V _{KHmin} | 2.6 | 2.3 | 1.9 | V | HIGH level at T and J and/or K to be present simultaneously |
| during: Input time HIGH | t _{THmin} | 60 | 60 | 60 | ns | |
| to: T-input voltage LOW | V _{TLmax} | 1.0 | 1.0 | 0.7 | V | t _{TLmin} = t _{pdf} |
| <u>No change of state</u> | | | | | | |
| J/K input voltage LOW | V _{JLmax} V _{KLmax} | 1.6 | 1.4 | 1.1 | V | LOW level at J and K to be present prior to T turning HIGH and to remain present during T is HIGH |
| <u>Clock skew protection</u> | | | | | | |
| Hold time | t _{hold max} | 10 | 10 | 10 | ns | 2 |
| <u>Reset</u> | | | | | | |
| S input voltage LOW | V _{SLmax} | 1.0 | 1.0 | 0.7 | V | { active t _{SLmin} = t _{pdf} inactive |
| S input voltage HIGH | V _{SHmin} | 1.9 | 1.8 | 1.6 | V | |
| <u>DYNAMIC DATA</u> | | | | | | |
| <u>Propagation delay times from T to Q</u> | | | | | | |
| Rise propagation delay time | t _{pdr max} | - | 90 | - | ns | 6.0 { V _{pd} = 1.5 V N = 1; C _L = 60 pF |
| Fall propagation delay time | t _{pdf max} | - | 120 | - | ns | |

CHARACTERISTICS (continued)

DYNAMIC DATA

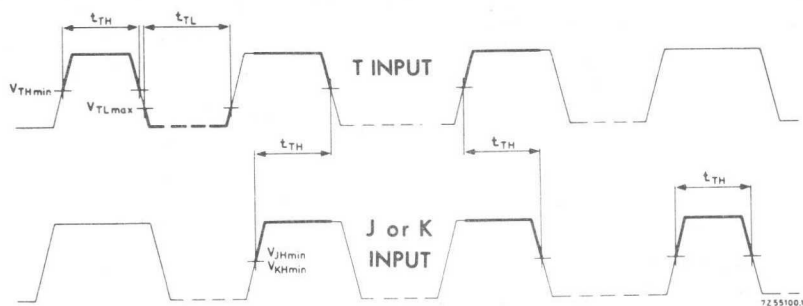


Fig. 1. Waveforms illustrating conditions for change of state.

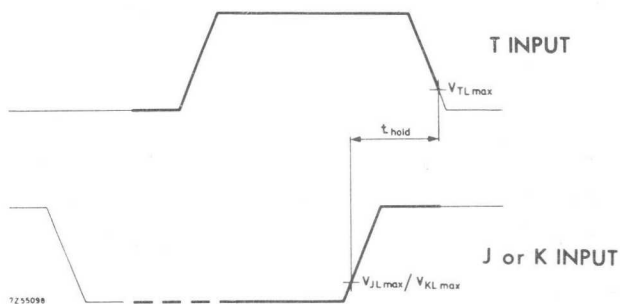


Fig. 2. Waveforms illustrating conditions for no change of state.

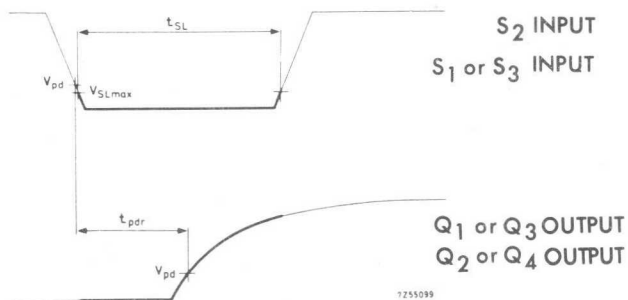
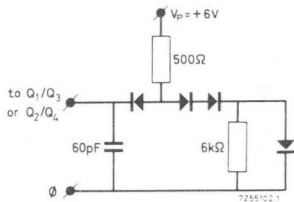
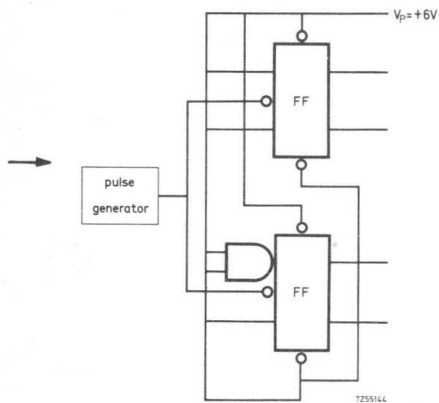
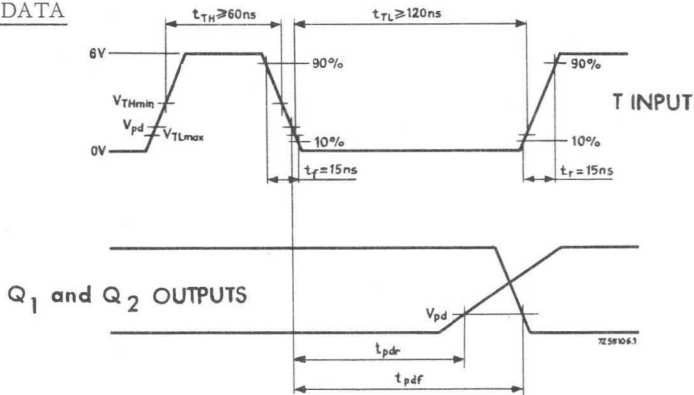


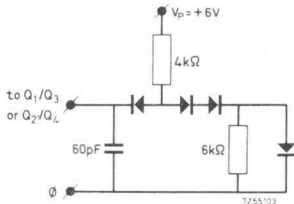
Fig. 3. Waveforms illustrating conditions for set or reset.

CHARACTERISTICS (continued)

DYNAMIC DATA



Diodes FCY101
Equivalent load for $N = 8$ and $C_L^1) = 60 \text{ pF}$

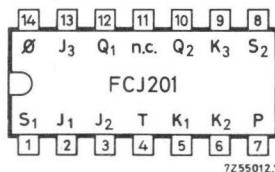
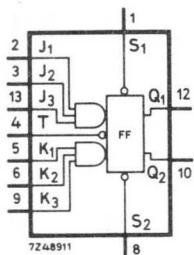


Diodes FCY101
Equivalent load for $N = 1$ and $C_L^1) = 60 \text{ pF}$

Fig. 4. Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf} .
1) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

SINGLE JK MASTER-SLAVE FLIP-FLOP



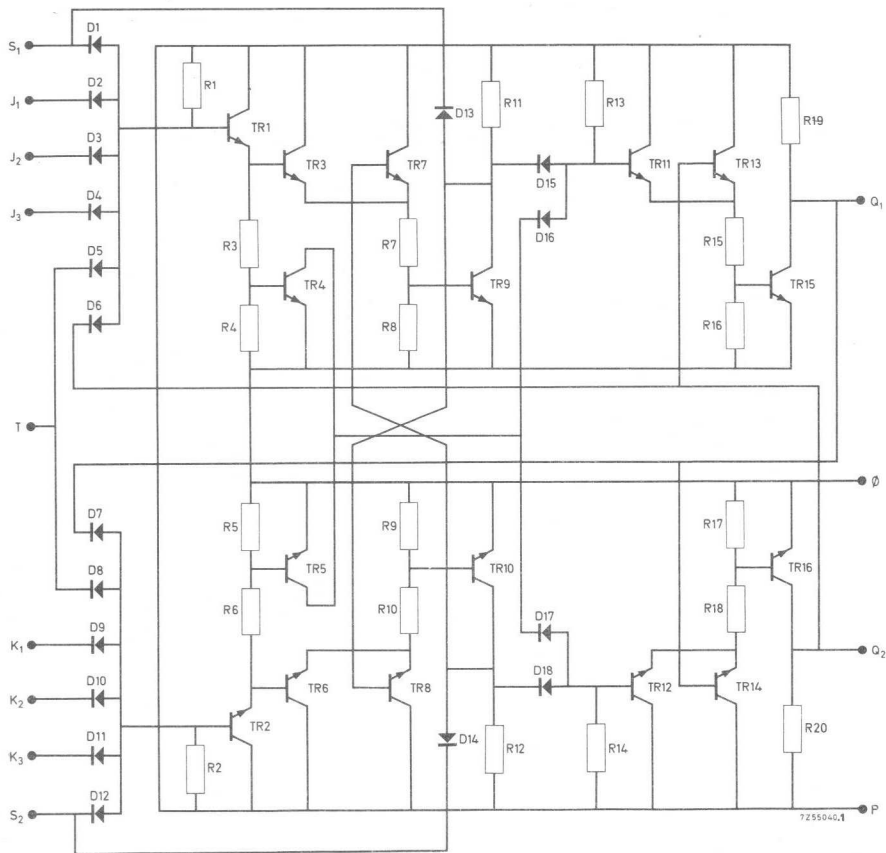
QUICK REFERENCE DATA

| | | | |
|-------------------------------------|-----------|---------------|-----|
| Supply voltage | V_P | $6.0 \pm 5\%$ | V |
| Operating ambient temperature range | T_{amb} | 0 to +75 | °C |
| Clock rate | f_c | typ. 5 | MHz |
| Available d.c. fan out | N_a | \geq | 8 |
| $T_{amb} = 0$ to +75 °C | | | |
| D.C. noise margin | M_L | typ. 1.2 | V |
| $T_{amb} = 25$ °C | | | |
| Power consumption | P_{av} | typ. 67 | mW |
| 50% duty cycle, $T_{amb} = 25$ °C | | | |

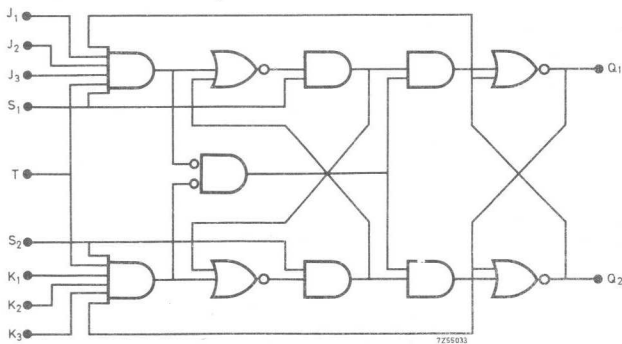
The FCJ201 is a direct-coupled JK flip-flop, operating on the master-slave principle. Operation depends on voltage levels only, i.e. rise and fall times of all input signals, including the trigger signal, are immaterial. The J, K and T inputs are logically equivalent, allowing the use of J and K for triggering. The direct set inputs (overriding any other inputs) are active at the LOW level.

PACKAGE OUTLINE : 14 lead plastic dual in-line (type A) .(See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM (to MIL standard 806B)



FUNCTION TABLES

1. Trigger action via T terminal (each flip-flop)

| T = HIGH | | T = LOW | |
|----------|---|----------------|----------------|
| J | K | Q ₁ | Q ₂ |
| H | H | reversed | |
| L | H | L | H |
| H | L | H | L |
| L | L | no change | |

The information on J and K is transferred into the master by T becoming HIGH. When T subsequently goes LOW the outputs will assume the levels shown in the table. Inputs S₁ and S₂ should be HIGH or floating.

$J = J_1 \cdot J_2 \cdot J_3; K = K_1 \cdot K_2 \cdot K_3$ (for positive logic)

2. Trigger action via J and K terminals

| J | K | Q ₁ | Q ₂ |
|-------|-------|----------------|----------------|
| H → L | X | H | L |
| X | H → L | L | H |
| H → L | H → L | reversed | |

If J or K go LOW with T HIGH, Q₁ and Q₂ assume the state shown. If both J and K go LOW with T HIGH, the outputs of Q₁ and Q₂ are reversed (exactly as if J and K remained HIGH and T were triggered). When triggering on J and K the T input requirements V_{TH} and V_{TL} (see CHARACTERISTICS) apply to J and K. S₁ and S₂ should be HIGH or floating.

$J = J_1 \cdot J_2 \cdot J_3; K = K_1 \cdot K_2 \cdot K_3$
(for positive logic)

3. Set or reset via S terminals

| S ₁ | S ₂ | Q ₁ | Q ₂ |
|----------------|----------------|----------------|----------------|
| H | L | L | H |
| L | H | H | L |
| L | L | indeterminate | |
| H | H | no change | |

The set inputs override the other inputs and directly determine the output of the flip-flop. In the case of both set inputs going LOW the first to reach LOW will determine the output conditions.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS (Limiting values)¹⁾

| | | | |
|-------------------------------------------|-----------------------------------------------------------------------|------|----------------|
| Supply voltage | V _p | max. | 8.0 V |
| Output voltage | V _Q | max. | 8.0 V |
| Input voltage | V _J , V _K , V _T , V _S | max. | 8.0 V |
| Output current ²⁾ | -I _Q | max. | 20 mA |
| Input current ³⁾ | -I _J , -I _K , -I _T , -I _S | max. | 20 mA |
| Voltage difference between any two inputs | | max. | 8.0 V |
| Storage temperature | T _{stg} | | -55 to +125 °C |
| Operating ambient temperature | T _{amb} | | 0 to +75 °C |

1) Limiting values according to the Absolute Maximum System as defined in IEC publication 134.

2) For negative output voltage.

3) At this limit input voltage type.: -1.5 V.

SYSTEM DESIGN DATA

| | | |
|----------------------------------------|-------------------|--------------------------|
| Uniform system temperature | T_{amb} | 0 to +75 °C |
| Uniform system supply voltage | V_p | 5.7 to 6.3 V |
| Available d. c. fan out | | |
| to T input | N_{aT} | ≥ 4 |
| to J or K input | $N_{aJ} = N_{aK}$ | ≥ 8 |
| to S input | N_{aS} | ≥ 5 |
| to G input | N_{aG} | ≥ 8 |
| D. C. noise margin | | |
| to T input | M_L M_H | min. 0.5 V min. 1.9 V |
| to J or K input | M_L M_H | min. 0.9 V min. 1.9 V |
| to S input | M_L M_H | min. 0.4 V min. 1.9 V |
| to G input | M_L M_H | min. 0.4 V min. 2.3 V |
| Average propagation delay time | t_{pd} | max. 150 ns |
| Maximum clock rate | f_c | ≥ 3 MHz |
| Equivalent input capacitances | | |
| for T input | C_T | typ. 8 pF |
| for J or K input | $C_J = C_K$ | typ. 4 pF |
| for S input | C_S | typ. 8 pF |
| Supply current (duty cycle 50%) | I_{Pav} | typ. 11.2 mA |
| Power dissipation at $T_{amb} = 75$ °C | P_{tot} | max. 110 mW |

CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and references | | |
|------------------------------------------|------------------------------------------------|-----------------------|------|------|---------------------------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| | | 0 | +25 | +75 | V _P (V) | | |
| <u>STATIC DATA</u> | | | | | | | |
| Output voltage LOW | V _{QLmax} | 0.4 | 0.4 | 0.4 | V | 5.7 and 6.3 | |
| at: | | | | | | | |
| Output current LOW | I _{QLmax} | 14.0 | 13.2 | 12.4 | mA | 5.7 | |
| | | 16.0 | 15.2 | 14.4 | mA | 6.3 | |
| Output voltage HIGH | V _{QHmin} | 5.3 | 5.4 | 5.3 | V | 5.7 | |
| | | I _Q = 0 | | | | | |
| Output voltage HIGH (lowest permissible) | V _{QHPmin} | 3.9 | 3.5 | 2.8 | V | 5.7 | |
| at: | | | | | | | |
| Output current HIGH | -I _{QHmax} | 350 | 450 | 550 | μA | 5.7 | |
| Input current LOW | -I _{JLmax} , -I _{KLmax} { | 1.75 | 1.65 | 1.55 | mA | 5.7 | } V _J = V _K = 0.4 V; } other inputs } floating } V _T = 0.4 V; other } inputs floating } V _S = 0.4 V; other } inputs floating |
| | | 2.0 | 1.9 | 1.8 | mA | 6.3 | |
| | -I _{TLmax} | 3.5 | 3.3 | 3.1 | mA | 5.7 | |
| | | 4.0 | 3.8 | 3.6 | mA | 6.3 | |
| -I _{SLmax} | 2.7 | 2.6 | 2.4 | mA | 5.7 | | |
| | 3.0 | 2.9 | 2.7 | mA | 6.3 | | |
| Input current HIGH | I _{JHmax} , I _{KHmax} | 1 | 1 | 25 | μA | 5.7 | V _J = V _K = 5.3 V other inputs 0 V |
| | I _{THmax} | 2 | 2 | 50 | μA | 5.7 | V _T = 5.3 V other inputs 0 V |
| | I _{SHmax} | 2 | 2 | 50 | μA | 5.7 | V _S = 5.3 V other inputs 0 V |
| Supply current | I _{Pmax} | - | 20 | - | mA | 6.3 | J, K, S, T inputs HIGH |

CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and references | | |
|--------------------------------------------|----------------------------------------------------------------|-----------------------|-----|-----|---------------------------|-----------------------------------------------------------------------------------------------------------|----------------------------------------------------------|
| | | | | | V _P (V) | | fig. |
| <u>DYNAMIC DATA</u> | | | | | 5.7 and 6.3 | | |
| <u>Change of state</u> | | | | | | | |
| Input voltage HIGH | V _{THmin} V _{JHmin} V _{KHmin} | 3.1 | 2.9 | 2.5 | V | HIGH level at T and J and/or K to be present simultaneously | 1 |
| during: T-input time HIGH | t _{THmin} | 100 | 100 | 100 | ns | | 1 |
| to: Input voltage LOW | V _{TLmax} | 1.3 | 1.1 | 0.9 | V | t _{TLmin} = t _{pdr} | 1 |
| <u>No change of state</u> | | | | | | | |
| JK input voltage LOW | V _{JLmax} V _{KLmax} | 1.8 | 1.6 | 1.3 | V | LOW level at J and K to be present prior to T turning HIGH and to remain present during T is HIGH | 2 |
| <u>Clock skew protection</u> | | | | | | | |
| Hold time | t _{holdmax} | 20 | 20 | 20 | ns | | 2 |
| <u>Set or Reset</u> | | | | | | | |
| S input voltage LOW | V _{SLmax} | 1.2 | 1.0 | 0.8 | V | active t _{SLmin} = t _{pdr} inactive | 3 |
| S input voltage HIGH | V _{SHmin} | 3.1 | 2.9 | 2.5 | V | | |
| <u>DYNAMIC DATA</u> | | | | | | | |
| <u>Propagation delay times from T to Q</u> | | | | | | | |
| Rise propagation delay time | t _{pdr max} | - | 200 | - | ns | V _{pd} = 1.5 V N = 1; C _L = 60 pF other output N = 8; C _L = 56 pF | 4 |
| Fall propagation delay time | t _{pdf max} | - | 100 | - | ns | | V _{pd} = 1.5 V N = 8; C _L = 56 pF |

CHARACTERISTICS (continued)

DYNAMIC DATA

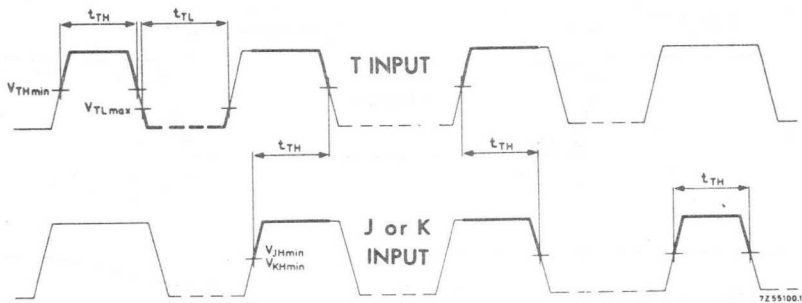


Fig. 1. Waveforms illustrating conditions for change of state.

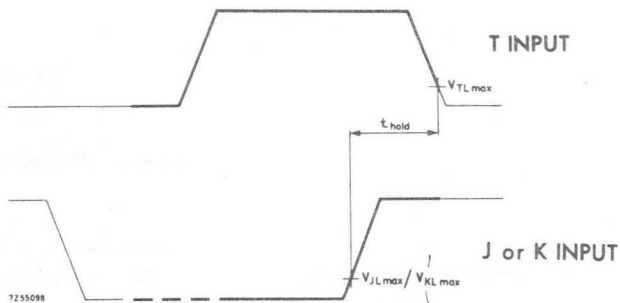


Fig. 2. Waveforms illustrating conditions for no change of state.

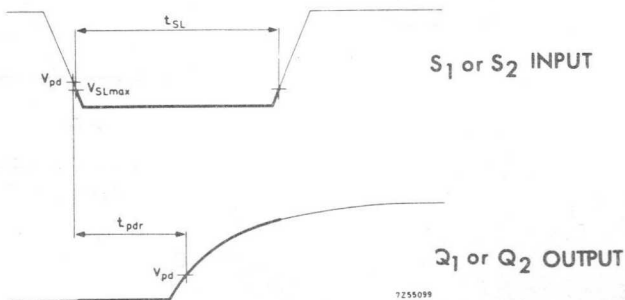
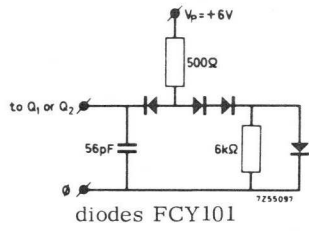
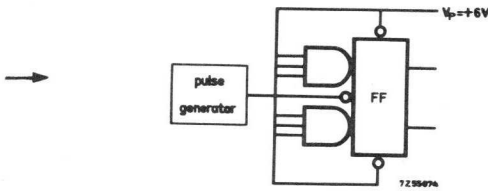
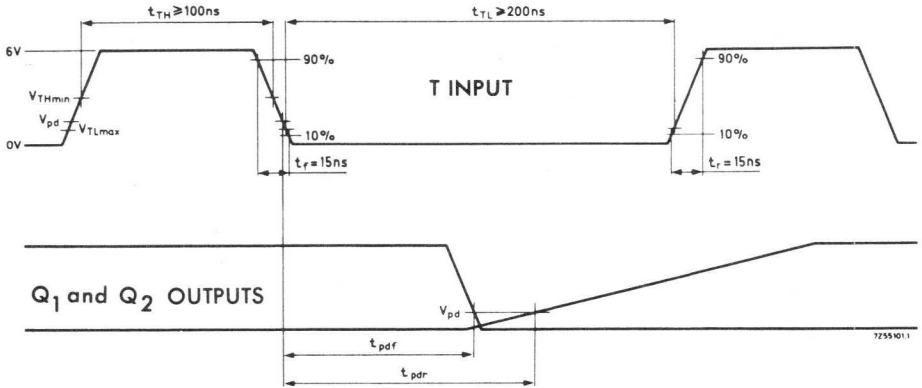


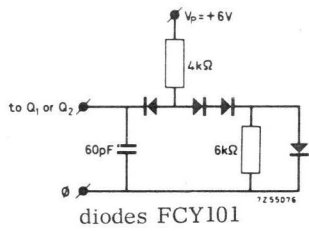
Fig. 3. Waveforms illustrating conditions for set or reset.

CHARACTERISTICS (continued)

DYNAMIC DATA



Equivalent load for $N=8$ and $C_L^1) = 56 \text{ pF}$

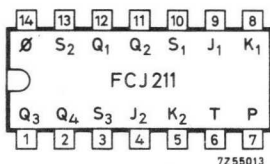
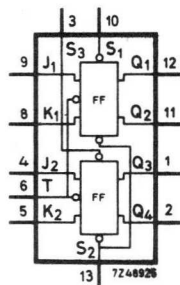


Equivalent load for $N=1$ and $C_L^1) = 60 \text{ pF}$

Fig. 4. Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf} .
1) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

DUAL JK MASTER SLAVE FLIP-FLOP



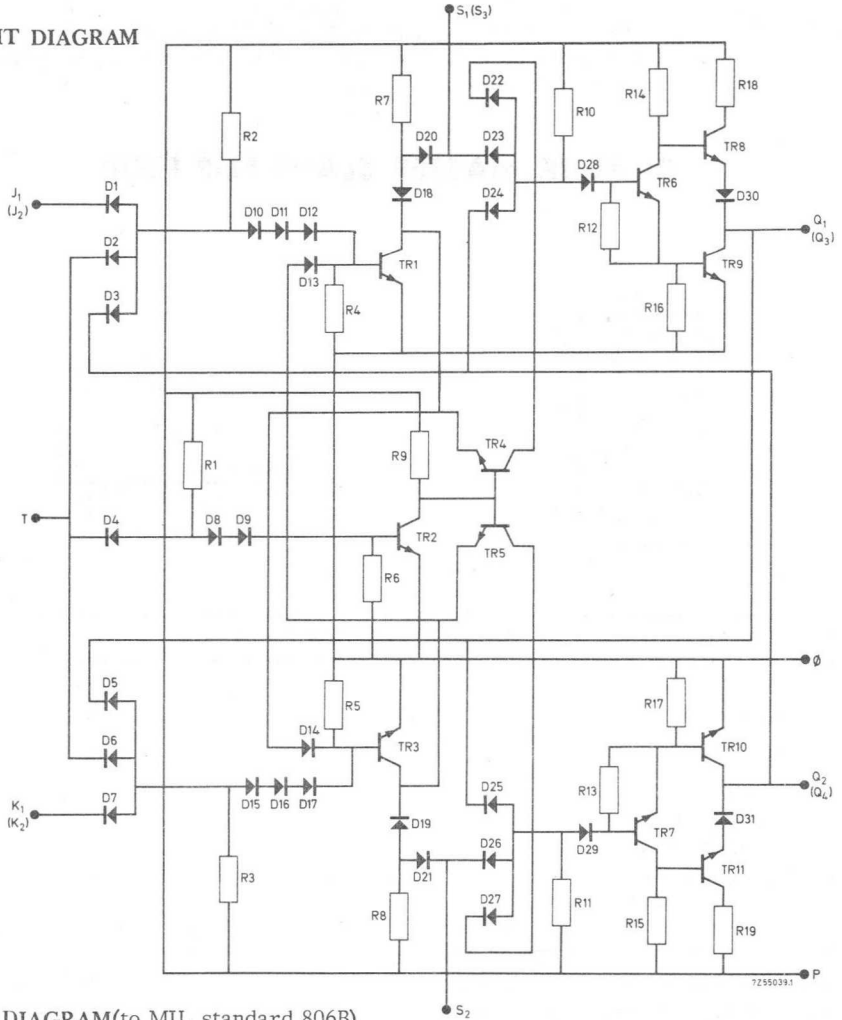
QUICK REFERENCE DATA

| | | |
|--------------------------------------------------------|-----------|-----------------|
| Supply voltage | V_P | $6.0 \pm 5\%$ V |
| Operating ambient temperature range | T_{amb} | 0 to +75 °C |
| Clock rate | f_C | typ. 7 MHz |
| Available d.c. fan-out $T_{amb} = 0$ to +75 °C | N_a | ≥ 8 |
| D.C. noise margin $T_{amb} = 25$ °C | M_L | typ. 1.2 V |
| Power consumption 50% duty cycle, $T_{amb} = 25$ °C | P_{av} | typ. 100 mW |

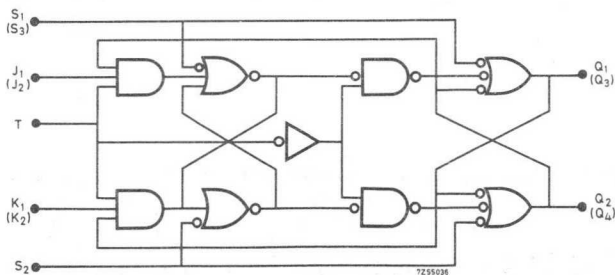
The FCJ211 comprises two independent direct-coupled JK flip-flops, operating on the master-slave principle. Operation depends on voltage levels only, i.e. rise and fall times of all input signals, including trigger signals, are immaterial. The set and reset inputs (overriding any other inputs) are active at the LOW level. Typical applications include synchronous counters and shift registers.

PACKAGE OUTLINE 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM (to MIL standard 806B)



FUNCTION TABLES

1. Trigger action via T terminal (each flip-flop)

| T = HIGH | | T = LOW | |
|----------------|----------------|----------------|----------------|
| J ₁ | K ₁ | Q ₁ | Q ₂ |
| J | K ₂ | Q ₃ | Q ₄ |
| H | H | reversed | |
| L | H | L | H |
| H | L | H | L |
| L | L | no change | |

The information on J and K is transferred into the master by T becoming HIGH. When T subsequently goes LOW the outputs will assume the levels shown in the table. Inputs S₁, S₂ and S₃ should be HIGH or floating.

2. Set or reset via S terminals

| S ₁ | S ₂ | Q ₁ | Q ₂ |
|----------------|----------------|----------------|----------------|
| S ₃ | S ₄ | Q ₃ | Q ₄ |
| H | L | L | H |
| L | H | H | L |
| L | L | H | H |
| H | H | no change | |

The set inputs override the other inputs and directly determine the outputs of the relevant flip-flop.

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System(IEC134)

| | | | |
|-------------------------------------------|-----------------------------------------------------------------------|-------------|-------|
| Supply voltage | V _P | max. | 8.0 V |
| Output voltage | V _Q | max. | 8.0 V |
| Input voltage | V _J , V _K , V _T , V _S | max. | 8.0 V |
| Output current 1) | -I _Q | max. | 20 mA |
| Input current 2) | -I _J , -I _K , -I _T , -I _S | max. | 20 mA |
| Voltage difference between any two inputs | | max. | 8.0 V |
| Storage temperature | T _{stg} | -55 to +125 | °C |
| Operating ambient temperature | T _{amb} | 0 to +75 | °C |

1) For negative output voltage in LOW state.

2) At this limit input voltage typ. -1.5 V.

SYSTEM DESIGN DATA

| | | |
|------------------------------------------------------|----------------------------------|--------------------------|
| Uniform system temperature | T_{amb} | 0 to +75 °C |
| Uniform system supply voltage | V_P | 5.7 to 6.3 V |
| Available d.c. fan out | | |
| to T input | N_{aT} | ≥ 1 |
| to J or K input | $N_{aJ} = N_{aK}$ | ≥ 10 |
| to S input | N_{aS2} $N_{aS1} = N_{aS3}$ | 2 4 |
| to G input | N_{aG} | ≥ 8 |
| D.C. noise margin | | |
| to T input | M_L M_H | min. 0.3 V min. 1.2 V |
| to J or K input | M_L M_H | min. 0.7 V min. 1.2 V |
| to S input | M_L M_H | min. 0.3 V min. 1.9 V |
| to G input | M_L M_H | min. 0.4 V min. 1.5 V |
| Average propagation delay time | t_{pd} | max. 105 ns |
| Maximum clock rate | f_c | ≥ 5 MHz |
| Equivalent input capacitances | | |
| for T input | C_T | typ. 24 pF |
| for J or K input | $C_J = C_K$ | typ. 4 pF |
| for S input | C_{S2} $C_{S1} = C_{S3}$ | typ. 16 pF typ. 8 pF |
| Supply current (duty cycle 50%) ¹⁾ | I_{Pav} | typ. 16.8 mA |
| Power dissipation at $T_{amb} = 75 °C$ ¹⁾ | P_{tot} | max. 150 mW |

¹⁾ Both flip-flops together

CHARACTERISTICS

| | | T_{amb} (°C) | | | Conditions and references | | |
|-------------------------------------------|----------------------------|----------------|--------------|--------------|---------------------------|------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| | | 0 | +25 | +75 | V_P (V) | | |
| <u>STATIC DATA</u> | | | | | | | |
| Output voltage LOW | V_{QLmax} | 0.4 | 0.4 | 0.4 | V | 5.7 and 6.3 | |
| at: Output current LOW | I_{QLmax} | 14.0 16.0 | 16.5 19.0 | 12.4 14.4 | mA mA | 5.7 6.3 | |
| Output voltage HIGH | V_{QHmin} | 3.8 | 3.9 | 4.1 | V | 5.7 $I_Q = -100 \mu A$ | |
| Output voltage HIGH (lowest permissible) | V_{QHPmin} | 3.6 | 3.3 | 3.0 | V | 5.7 | |
| at: Output current HIGH | $-I_{QHmax}$ | 0.85 | 3.3 | 5.5 | mA | 5.7 | |
| Input current LOW | $-I_{JLmax}, -I_{KLmax}$ | 1.4 | 1.3 | 1.2 | mA | 5.7 | $V_J = V_K = 0.4 V$; other inputs floating $V_T = 0.4 V$; other inputs floating $V_S = 0.4 V$; other inputs floating $V_S = 0.4 V$; other inputs floating |
| | | 1.6 | 1.5 | 1.4 | mA | 6.3 | |
| | $-I_{TLmax}$ | 8.0 | 7.6 | 7.0 | mA | 5.7 | |
| | | 9.0 | 8.4 | 7.8 | mA | 6.3 | |
| | $-I_{S2Lmax}$ | 5.7 | 5.5 | 5.2 | mA | 5.7 | |
| $-I_{S1Lmax}, -I_{S3Lmax}$ | 6.6 | 6.3 | 5.8 | mA | 6.3 | | |
| Input current HIGH | I_{JHmax}, I_{KHmax} | 1 | 1 | 25 | μA | 5.7 | $V_J = V_K = 5.3 V$ other inputs 0 V $V_T = 5.3 V$ other inputs 0 V $V_S = 5.3 V$ other inputs 0 V $V_S = 5.3 V$ other inputs 0 V |
| | | 6 | 6 | 150 | μA | 5.7 | |
| | I_{S2Hmax} | 4 | 4 | 100 | μA | 5.7 | |
| | $-I_{S1Hmax}, -I_{S3Hmax}$ | 2 | 2 | 50 | μA | 5.7 | |
| | | | | | | | |
| Supply current (both flip-flops together) | I_{Pmax} | - | 26.7 | - | mA | 6.3 | T input LOW J, K, S inputs HIGH |

CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and references | | |
|--------------------------------------------|----------------------------------------------------------------|-----------------------|-----|-----|---------------------------|-----------------------------------------------------------------------------------------------------|------------------------------------------------------------|
| | | 0 | +25 | +75 | V _P (V) | fig. | |
| <u>DYNAMIC DATA</u> | | | | | 5.7 and 6.3 | | |
| <u>Change of state</u> | | | | | | | |
| Input voltage HIGH | V _{THmin} V _{JHmin} V _{KHmin} | 2.6 | 2.3 | 1.9 | V | } HIGH level at T and J and/or K to be present simultaneously | |
| during: | | | | | | | |
| Input time HIGH | t _{THmin} | 60 | 60 | 60 | ns | 1 | |
| to: | | | | | | | |
| T-input voltage LOW | V _{TLmax} | 1.0 | 1.0 | 0.7 | V | t _{TLmin} = t _{pdf} | |
| <u>No change of state</u> | | | | | | | |
| J/K input voltage LOW | V _{JLmax} V _{KLmax} | 1.6 | 1.4 | 1.1 | V | } LOW level at J and K to be present prior to T turning HIGH and to remain present during T is HIGH | |
| | | | | | | | |
| <u>Clock skew protection</u> | | | | | | | |
| Hold time | t _{hold max} | 10 | 10 | 10 | ns | 2 | |
| <u>Reset</u> | | | | | | | |
| S input voltage LOW | V _{SLmax} | 1.0 | 1.0 | 0.7 | V | } active t _{SLmin} = t _{pdf} inactive | |
| S input voltage HIGH | V _{SHmin} | 1.9 | 1.8 | 1.6 | V | | |
| <u>DYNAMIC DATA</u> | | | | | | | |
| <u>Propagation delay times from T to Q</u> | | | | | | | |
| Rise propagation delay time | t _{pdr max} | - | 90 | - | ns | 6.0 | } V _{pd} = 1.5 V N = 1; C _L = 60 pF |
| Fall propagation delay time | t _{pdf max} | - | 120 | - | ns | 6.0 | |

CHARACTERISTICS (continued)

DYNAMIC DATA

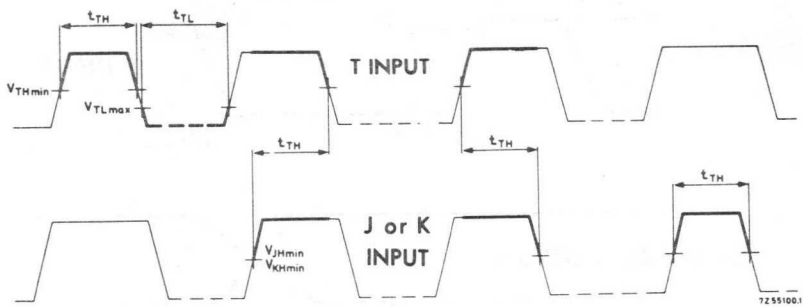


Fig. 1. Waveforms illustrating conditions for change of state.

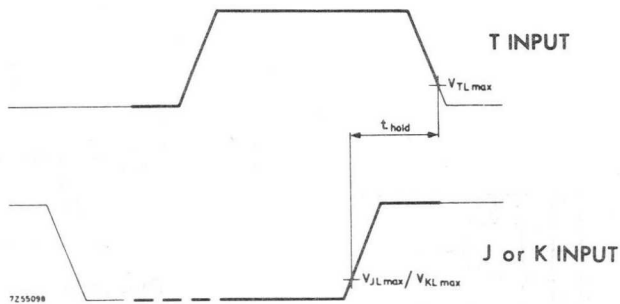


Fig. 2. Waveforms illustrating conditions for no change of state.

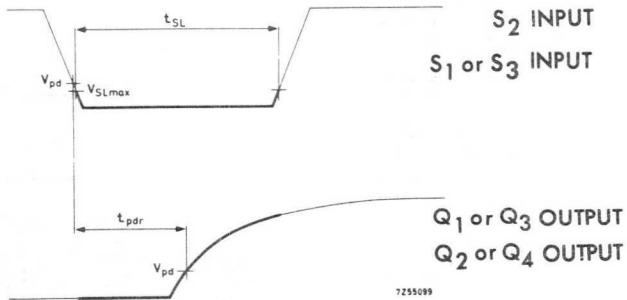
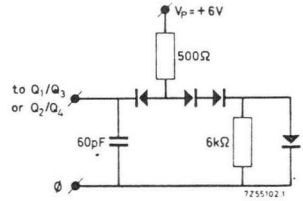
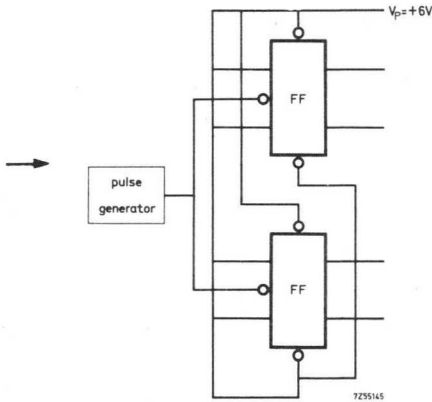
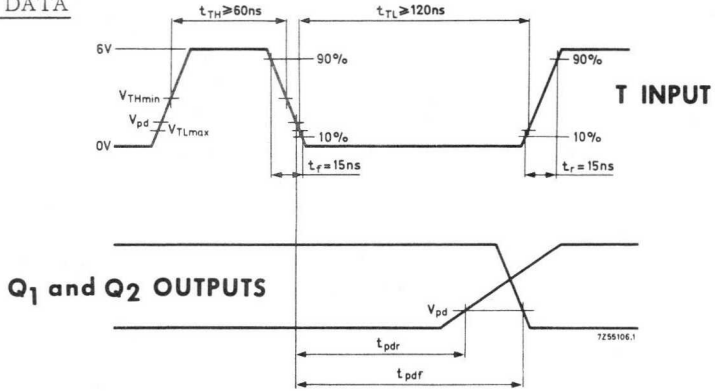


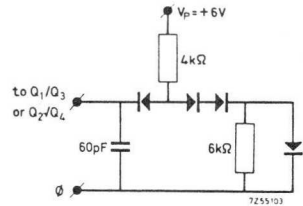
Fig. 3. Waveforms illustrating conditions for set or reset.

CHARACTERISTICS (continued)

DYNAMIC DATA



Diodes FCY101
Equivalent load for N = 8 and C_L^1) = 60 pF

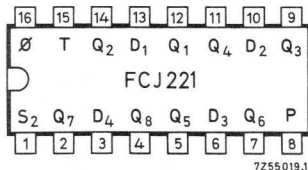
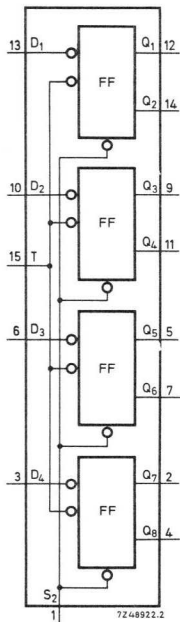


Diodes FCY101
Equivalent load for N = 1 and C_L^1) = 60 pF

Fig. 4. Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf}
1) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication and industrial control.

QUADRUPLE LATCH FLIP-FLOP



PACKAGE OUTLINE

16 lead plastic dual in-line (type A)
See General Section

QUICK REFERENCE DATA

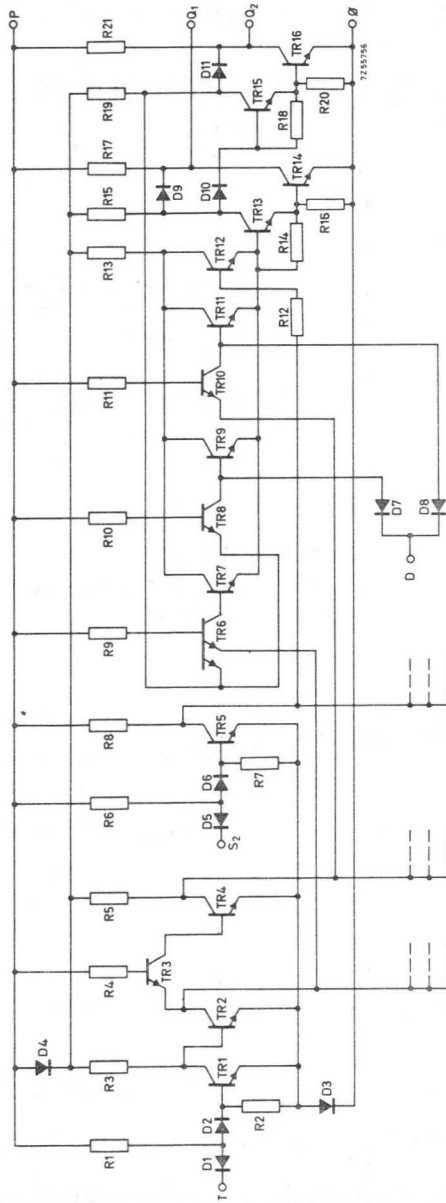
| | | | |
|---------------------------------------------------------------|------------------|----------|-----|
| Supply voltage | V _p | 6.0 ± 5% | V |
| Operating ambient temperature range | T _{amb} | 0 to +75 | °C |
| Clock rate at T _{amb} = 25 °C | f _c | typ. 5 | MHz |
| Available d. c. fan out T _{amb} = 25 °C | N _a | ≥ 10 | |
| D. C. noise margin T _{amb} = 25 °C | M _L | typ. 1.2 | V |
| Power consumption 50% duty cycle, T _{amb} = 25 °C | P _{av} | typ. 250 | mW |

The FCJ221 is a quadruple latch flip-flop with D inputs, a common clock (T) and a reset input (S₂).

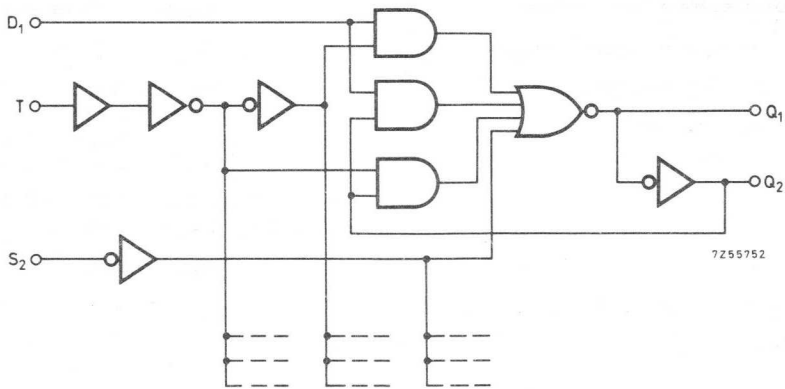
A LOW input signal at D arrives after the last T signal goes HIGH at output Q₁. The information follows after a LOW signal at the T input.

It is possible to influence the output state of the flip-flop.

CIRCUIT DIAGRAM



LOGIC DIAGRAM



LOGIC FUNCTION

Function tables

| | |
|-------|-----------|
| t_n | t_{n+1} |
| D | Q1 |
| H | L |
| L | H |

| | |
|----|----|
| S2 | Q1 |
| H | H |
| L | X |

H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)
 t_n = bit time before trigger pulse
 t_{n+1} = bit time after trigger pulse
 X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|------------------------------------------|-------------------------|------|-------------|------------------|
| Supply voltage at $T_{amb} < 40^\circ C$ | V_p | max. | 8 | V |
| Output voltage | V_Q | max. | 8 | V |
| Input voltage | V_G | max. | 8 | V |
| Input current | $-I_D ; -I_T ; -I_{S2}$ | max. | 20 | mA ¹⁾ |
| Storage temperature | T_{stg} | | -55 to +125 | $^\circ C$ |
| Operating ambient temperature | T_{amb} | | 0 +75 | $^\circ C$ |

1) At negative input voltage

SYSTEM DESIGN DATA

| | | | |
|--------------------------------------------------------------------|-------------------------------------------------------------------------------------|------------|---------------------|
| Uniform system temperature | T_{amb} | 0 to +75 | $^{\circ}C$ |
| Uniform system supply voltage | V_p | 5.7 to 6.3 | V |
| Available d. c. fan-out | N_a | \geq | 10 |
| D. C. noise margin to D input to T, S ₂ input | $\left\{ \begin{array}{l} MDL \\ MDH \\ MTL; MS2L \\ MTH; MS2H \end{array} \right.$ | min. | 0.2 V |
| | | min. | 3.0 V |
| | | min. | 0.3 V |
| | | min. | 3.1 V |
| Supply current | I_{pav} | max. | 47 mA ¹⁾ |
| Power dissipation at $T_{amb} = 75^{\circ}C$ | P_{tot} | max. | 300 mW |

1) Input open and $V_D = 0$ V

CHARACTERISTICS

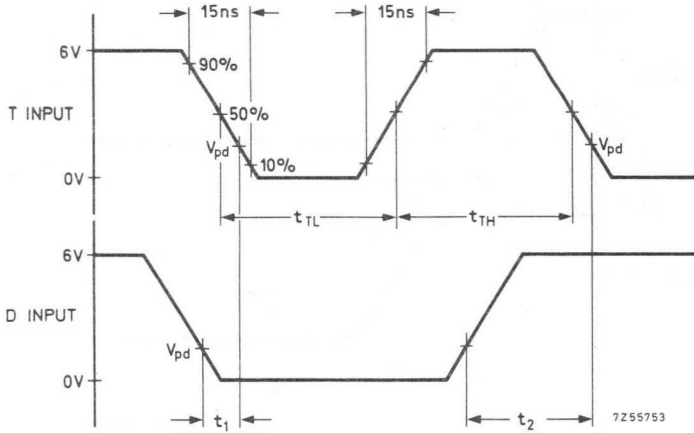
| STATIC DATA | | T _{amb} (°C) | | | Conditions and references | |
|--------------------------------------------|---------------------------------------------|-----------------------|--------------|--------------|---------------------------|-----------------------------------------------------------------|
| | | 0 | 25 | 75 | V _P (V) | |
| Output voltage LOW | V _{QLmax} | 0.4 | 0.4 | 0.4 | V | 5.7 and 6.3 |
| at: | | | | | | |
| Output current LOW | I _{QLmax} | 17.5 20.0 | 16.5 19.0 | 15.5 18.0 | mA mA | 5.7 6.3 |
| Output voltage HIGH | V _{QHmin} | 5.3 | 5.3 | 5.3 | V | 5.7 -I _Q = 0 |
| Input voltage LOW | | | | | | 5.7 and 6.3 |
| D | V _{DLmax} | 0.9 | 0.8 | 0.6 | V | 5.7 and 6.3 |
| T; S ₂ | V _{TLmax} V _{S2Lmax} | 1.0 | 0.9 | 0.7 | V | 5.7 and 6.3 |
| Input voltage HIGH | | | | | | 5.7 and 6.3 |
| D | V _{DHmin} | 2.3 | 2.2 | 2.1 | V | 5.7 and 6.3 |
| T; S ₂ | V _{THmin} V _{S2Hmin} | 2.2 | 2.1 | 2.0 | V | 5.7 and 6.3 |
| Input current LOW | | | | | | |
| D | -I _{DLmax} | 2.55 | 2.5 | 2.45 | mA | 5.7 V _D = 0.4 V |
| T; S ₂ | -I _{TLmax} -I _{S2Lmax} | 1.75 | 1.65 | 1.55 | mA | 5.7 V _T = V _{S2} = 0.4 V |
| D | -I _{DLmax} | 2.85 | 2.8 | 2.75 | mA | 6.3 V _D = 0.4 V |
| T; S ₂ | -I _{TLmax} -I _{S2Lmax} | 2.0 | 1.9 | 1.8 | mA | 6.3 V _T = V _{S2} = 0.4 V |
| Input current HIGH | | | | | | |
| D | I _{DHmax} | 2 | 2 | 50 | μA | 6.3 V _D = V _P |
| T; S ₂ | I _{THmax} I _{S2Hmax} | 1 | 1 | 25 | μA | 6.3 V _T = V _{S2} = V _P |
| Output current changing output state | | | | | | |
| Q ₁ | -I _{Q1max} | 4.2 | 4.05 | 3.75 | mA | 6.3 } V _Q = 0.4 V |
| Q ₂ | -I _{Q2max} | 6.3 | 6.1 | 5.65 | mA | 6.3 } |
| Supply current | I _{Pmax} | - | - | 47 | mA | 6.3 { V _D = 0 V; T and S ₂ inputs open |

CHARACTERISTICS

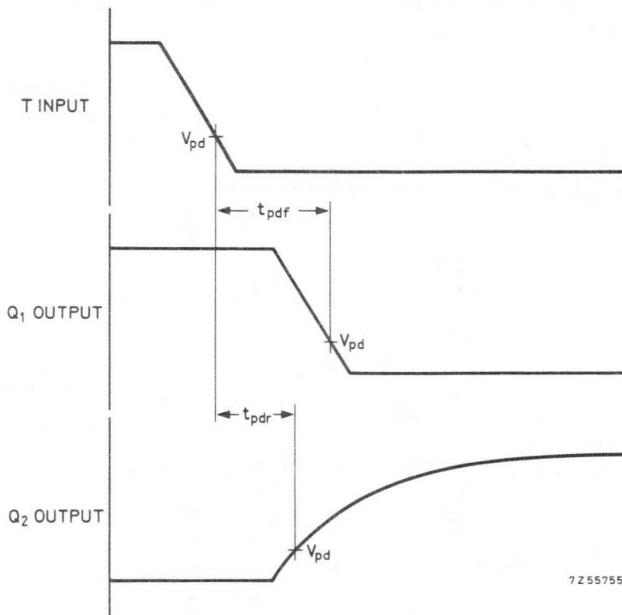
| | | T _{amb} (°C) | | | Conditions and references | |
|-------------------------------------------|-----------------------------------------------------------------------|-----------------------|-----|-----|---------------------------|-------------------|
| | | 0 | 25 | 75 | V _P (V) | |
| <u>STATIC DATA</u> | | | | | | |
| <u>D.C. noise margin</u> | | | | | | |
| LOW: D | MDL _{min} | 0.5 | 0.4 | 0.2 | V | |
| T; S ₂ | M _{TL} _{min} } M _{S2L} _{min} } | 0.6 | 0.5 | 0.3 | V | |
| HIGH: D | MDH _{min} | 3.0 | 3.1 | 3.2 | V | |
| T; S ₂ | M _{TH} _{min} } M _{S2H} _{min} } | 3.1 | 3.2 | 3.3 | V | |
| <u>DYNAMIC DATA</u> | | | | | | |
| <u>Input time LOW</u> | | | | | | |
| T | t _{TL} _{min} | - | 100 | - | ns | 5.7 and 6.3 |
| <u>Input time HIGH</u> | | | | | | |
| T | t _{TH} _{min} | - | 70 | - | ns | 5.7 and 6.3 |
| <u>Input time LOW</u> | | | | | | |
| S ₂ | t _{S2L} _{min} | - | 100 | - | ns | 5.7 and 6.3 |
| S ₂ (changing output state) | t _{S2L} _{min} | - | 100 | - | ns | 5.7 and 6.3 |
| <u>Set-up times:</u> | | | | | | |
| t ₁ | t _{su1} _{min} | - | 0 | - | ns | 5.7 and 6.3 |
| t ₂ | t _{su2} _{min} | - | 30 | - | ns | 6.3 |
| <u>Propagation delay times:</u> | | | | | | |
| Rise propagation delay times | | | | | | |
| T → Q ₁ | t _{pdr} _{max} | - | 95 | - | ns | 6.0 |
| T → Q ₂ | t _{pdr} _{max} | - | 105 | - | ns | 6.0 |
| S ₂ → Q ₂ | t _{pdr} _{max} | - | 85 | - | ns | 6.0 |
| Fall propagation delay times | | | | | | |
| T → Q ₁ | t _{pdf} _{max} | - | 60 | - | ns | 6.0 |
| T → Q ₂ | t _{pdf} _{max} | - | 120 | - | ns | 6.0 |
| S ₂ → Q ₂ | t _{pdf} _{max} | - | 60 | - | ns | 6.0 |

} N = 1; C_L = 40 pF
V_{pd} = 1.5 V

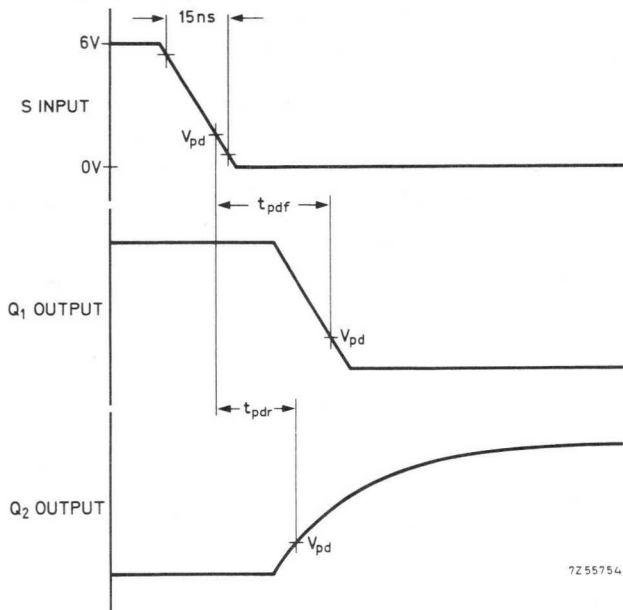
} N = 8; C_L = 70 pF
V_{pd} = 1.5 V

CHARACTERISTICS (continued)


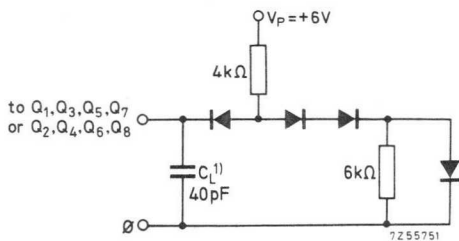
Waveform illustrating conditions for change of state


 Waveforms illustrating t_{pdr} and t_{pdf}

CHARACTERISTICS (continued)



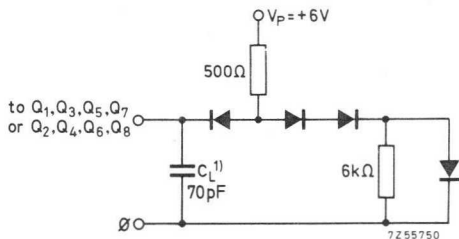
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diodes FCY101

N = 1

7255751



diodes FCY101

N = 8

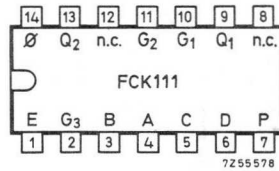
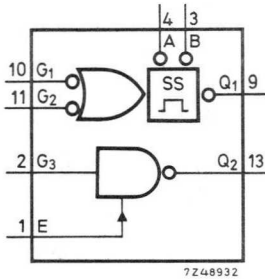
7255750

Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf} .

¹) Including jig and probe capacitance.

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication and industrial control.

MONOSTABLE MULTIVIBRATOR



QUICK REFERENCE DATA

| | | |
|-----------------------------------------------------|-------------------------------------------------------------------------------------------|----------------------|
| Supply voltage | V_P | $6.0 \pm 5\% V$ |
| Operating ambient temperature | T_{amb} | 0 to +75 °C |
| Propagation delay time | $\left. \begin{array}{l} G_1 \rightarrow Q_1 \\ G_3 \rightarrow Q_2 \end{array} \right\}$ | t_{pdf} typ. 70 ns |
| $T_{amb} = 25^\circ C$ at $V_{pd} = 1.5 V$ | | t_{pdf} typ. 40 ns |
| Output pulse width: | | |
| $R_t = 10 k\Omega \pm 1\%$; $C_t = 160 pF \pm 1\%$ | t_{Q1L} | typ. 1.0 μs |
| Available d. c. fan-out | $\left. \begin{array}{l} Q_1 \\ Q_2 \end{array} \right\}$ | $N_a \geq 14$ |
| | $T_{amb} = 0$ to +75 °C | $N_a \geq 14$ |
| | A | $N_a = 1$ |
| D. C. noise margin | | |
| $T_{amb} = 25^\circ C$ | M_L | typ. 1.2 V |
| Power consumption | | |
| 50% duty cycle, $T_{amb} = 25^\circ C$ | P_{av} | typ. 58 mW |

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

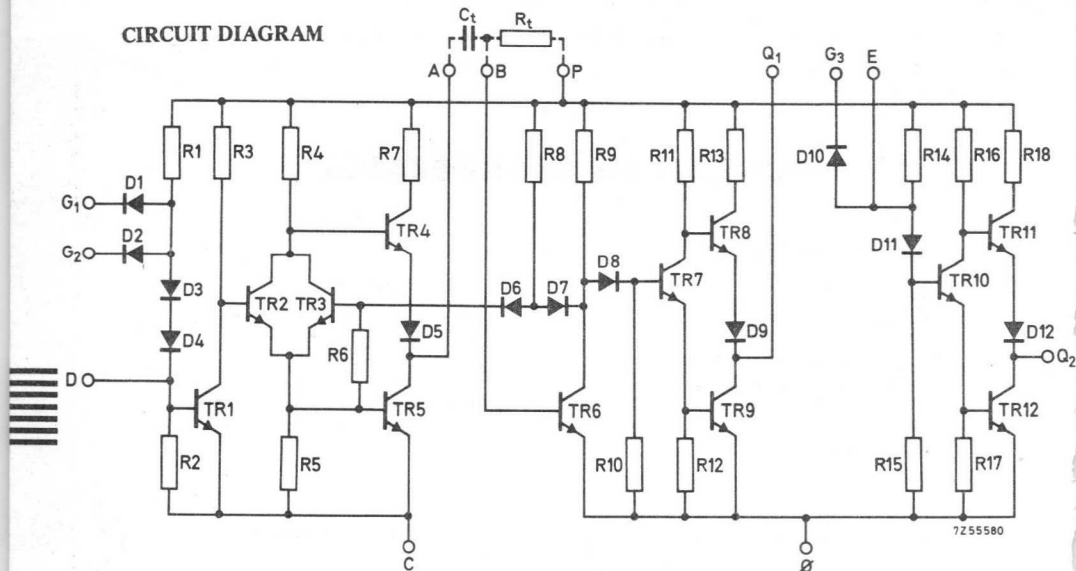
The FCK111 comprises a threshold triggered monostable circuit and an independent expandable inverter.

The monostable function is obtained by an externally connected resistor and capacitor. Each time one of the inputs G_1 or G_2 is going LOW a negative going pulse appears at output Q_1 .

The pulse width is adjustable over a very wide range by varying the resistor and capacitor values.

If the input (G_3) of the inverter is connected to A a positive going pulse is obtained at the output Q_2 , almost coinciding and practically having the same width as the output pulse Q_1 , provided that the width of the input pulse does not exceed the width of the output pulse. The outputs Q_1 and Q_2 are bi-directional and have a high fan-out drive capability.

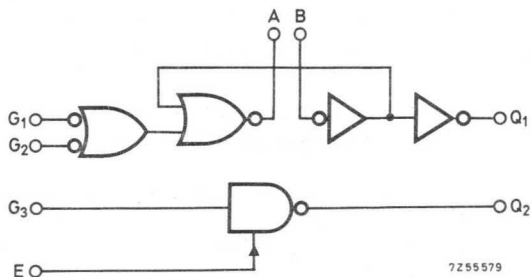
CIRCUIT DIAGRAM



Notes

1. Terminals C and D make the circuit compatible with the FCK101.
2. To ensure conformity with the characteristics given in the data sheets, terminal C must be connected to terminal ϕ .
If terminals C and ϕ are not interconnected, the output pulse can be shortened by connecting a diode or a voltage source to C (positive to ϕ); however, this will alter a number of characteristics, including special input levels and output level A.
3. The noise margin for a.c. disturbances at the trigger inputs G_1 and G_2 can be increased by connecting a capacitor between terminals C and D, but this reduces the minimum operating frequency.

LOGIC DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|------------------------------------------------------------------------------|-------------|------|-------------|------------------|
| Supply voltage | V_P | max. | 8.0 | V |
| Output voltage | V_Q | max. | 8.0 | V |
| Input voltage | V_G | max. | 8.0 | V |
| Output current | $-I_Q$ | max. | 20.0 | mA ¹⁾ |
| Input current | $-I_G$ | max. | 20.0 | mA ²⁾ |
| Voltage difference between any two inputs | | max. | 8.0 | V |
| Expander input voltages: | | | | |
| - with respect to supply | $V_P - V_E$ | max. | 8.0 | V |
| - with respect to other inputs | $V_G - V_E$ | max. | 8.0 | V |
| Expander input current | I_E | max. | 5.0 | mA |
| Storage temperature | T_{stg} | | -55 to +125 | °C |
| Operating ambient temperature | T_{amb} | | 0 to +75 | °C |
| Output short circuit duration (duty cycle 10%, either output, or both) | t_{Qsc} | max. | 60 | ms |
| Timing resistor (R_t connected to 6.3 V) | R_t | min. | 5 | k Ω |
| | | max. | 20 | k Ω |
| Timing capacitor | C_t | max. | 160 | μ F |
| | | min. | 30 | pF ³⁾ |

¹⁾ for negative output voltage in LOW state.

²⁾ at this limit, input voltage typ: - 1.5 V.

³⁾ C_t min 30 pF is not a rating, but is to be considered as the minimum value at which the circuit still performs its function.

FCK111
monostable

FC family
standard temperature range

SYSTEM DESIGN DATA

| | | | | | |
|------------------------------------------------------------|----------------------------------------------------------------|-----------|-------------|-------------|---|
| Uniform system temperature | T_{amb} | | 0 to +75 | $^{\circ}C$ | |
| Uniform system supply voltage | V_P | | 5.7 to 6.5 | V | |
| Available d. c. fan-out | $\left\{ \begin{array}{l} Q_1 \\ Q_2 \\ A \end{array} \right.$ | N_a | \geq | 14 | |
| | | N_a | \geq | 14 | |
| | | N_a | = | 1 | |
| D. C. noise margin FCK111 \rightarrow gate | M_L | min. | 0.4 | V | |
| | M_H | min. | 1.2 | V | |
| | gate \rightarrow FCK111 | M_L | min. | 0.4 | V |
| | | M_H | min. | 1.8 | V |
| Propagation delay time: | $G_1 \rightarrow Q_1$ | t_{pdf} | max. | 170 ns | |
| | $G_1 \rightarrow Q_2$ | t_{pdr} | max. | 200 ns | |
| | $G_3 \rightarrow Q_2$ | t_{pdr} | max. | 120 ns | |
| | $G_3 \rightarrow Q_2$ | t_{pdf} | max. | 55 ns | |
| | | | | | |
| Equivalent input capacitance | C_G | typ. | 4 | pF | |
| Supply current (duty cycle 50%) | I_{Pav} | typ. | 10.9 | mA | |
| Power dissipation at $T_{amb} = 75^{\circ}C$ | P_{tot} | max. | 98 | mW | |
| Relative change of output pulse width vs supply voltage | | | see page 10 | | |
| Output pulse width vs timing capacitor (C_T) | | | see page 10 | | |

CHARACTERISTICS : (pin C connected to pin ϕ)

| STATIC DATA | | T _{amb} (°C) | | | Conditions and References | |
|-------------------------------------------------------------------|-------------------------------------------------|-----------------------|------------|----------------|---------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| | | 0 | 25 | 75 | V _P (V) | |
| <u>Output Q₁</u> | | | | | | |
| <u>Output voltage LOW</u> at: | V _{Q1L} max | 0.4 | 0.4 | 0.4 V | 5.7 and 6.3 | V _B (pin 3) at 0 V |
| Output current LOW | I _{Q1L} max | 25 28 | 27 27 | 26 mA 26 mA | 5.7 6.3 | |
| <u>Output voltage HIGH</u> | V _{Q1H} min | 3.5 2.6 | 3.7 2.8 | 4.0 V 2.9 V | 5.7 5.7 | -I _{Q1H} = 30 μ A } and -I _{Q1H} = 5 mA } B (pin 3) connected to V _P via 20 k Ω (\pm 1 %) |
| <u>Output short circuit current</u> | -I _{Q1sc} min | 16.5 | 19.5 | 18.0 mA | 5.7 | |
| <u>Output Q₂</u> | | | | | | { B (pin 3) connected to V _P via 20 k Ω (\pm 1 %) (max. duration 60 ms; duty cycle 10%) |
| <u>Output voltage LOW</u> at: | V _{Q2L} max | 0.4 | 0.4 | 0.4 V | 5.7 and 6.3 | |
| Output current LOW and Input voltage HIGH G ₃ | I _{Q2L} max V _{GH} min | 25 2.3 | 27 2.2 | 26 mA 2.1 V | 5.7 6.3 and 6.3 | |
| <u>Output voltage HIGH</u> at: | V _{Q2H} min | 3.5 2.6 | 3.7 2.8 | 4.0 V 2.9 V | 5.7 5.7 | -I _{Q2H} = 30 μ A -I _{Q2H} = 5 mA |
| Input voltage LOW G ₃ | V _{GL} max | 1.0 | 1.0 | 0.8 V | 5.7 and 6.3 | |
| <u>Output short circuit current</u> | -I _{Q2sc} min | 16.5 | 19.5 | 18.0 mA | 5.7 | { V _{GL} max (max. dura- tion 60 ms; duty cycle 10%) |

CHARACTERISTICS (continued)

| STATIC DATA (continued) | | T _{amb} (°C) | | | Conditions and references | |
|--------------------------------------------------------------------------------------------------|-----------------------|-----------------------|-----|--------|---------------------------|-------------------------------------------------------------------------------------------------------|
| | | 0 | 25 | 75 | V _P (V) | |
| <u>Output A</u> | | | | | | |
| <u>Output voltage LOW</u> | V _{AL} max | 0.4 | 0.4 | 0.4 V | 5.7 and 6.3 | |
| at: | | | | | | |
| <u>Output current LOW</u> | I _{AL} max | 2.0 | 2.0 | 2.0 mA | 5.7 and 6.3 | see note |
| and | | | | | | |
| <u>Input voltage LOW;</u> G ₁ , G ₂ or V _B (pin 3) at 0 V | V _{GL} max | 1.0 | 1.0 | 0.8 V | 5.7 and 6.3 | |
| <u>Output voltage HIGH</u> | V _{AH} min | 3.9 | 4.0 | 4.1 V | 5.7 | -I _{AH} = 30 μA |
| | | 3.2 | 3.4 | 3.4 V | 5.7 | -I _{AH} = 5 mA |
| at: | | | | | | |
| <u>Input voltage HIGH</u> | V _{GH} min | 2.3 | 2.2 | 2.1 V | 5.7 and 6.3 | |
| or: B (pin 3) connected to V _P via 20 kΩ (± 1%) | | | | | | |
| <u>Output short circuit current</u> | -I _{Asc} min | 30 | 30 | 25 mA | 5.7 | B (pin 3) connected to V _P via 20 kΩ (± 1%) (max. duration 60 ms; duty cycle 10%) |

Note

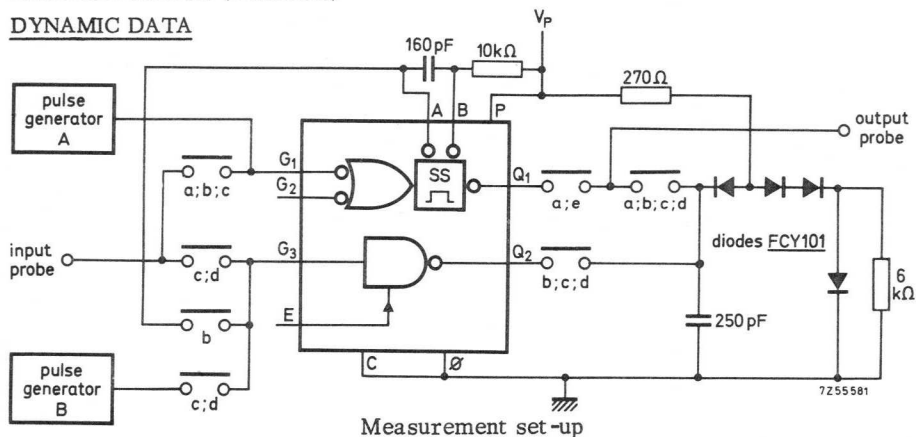
I_{AL} max is an extra static current, which can be applied to output A under both static and dynamic conditions without disturbing the output pulse width.

CHARACTERISTICS (continued)

| STATIC DATA (continued) | | T _{amb} (°C) 0 25 75 | | | Conditions and references | | |
|-------------------------------------------------------------|----------------------|----------------------------------|------|------|---------------------------|-------------------|-----------------------------------------------------------------------------------------------------------|
| | | | | | V _P (V) | | |
| <u>Input current LOW</u> | -I _{GL} max | 1.75 | 1.65 | 1.85 | mA | 5.7 | V _G = 0.4 V other inputs floating |
| | | 2.00 | 1.90 | 1.80 | mA | 6.3 | |
| <u>Input current HIGH</u> | I _{GH} max | 1.0 | 1.0 | 25.0 | µA | 5.7 | V _G = 5.3 V, other inputs at V _G = 0 V |
| <u>Supply current (unloaded)</u> | | | | | | | current flow in R _t not included |
| output Q ₁ HIGH } output Q ₂ LOW } | I _{PH} typ | 8.3 | 8.0 | 7.5 | mA | 6.0 | |
| output Q ₁ LOW } output Q ₂ LOW } | I _{PL} typ | 13.5 | 11.3 | 10.3 | mA | 6.0 | |
| | I _{PL} max | 17.3 | 16.6 | 15.6 | mA | 6.3 | |
| Average supply current | I _{Pav} | 14.7 | 14.1 | 13.2 | mA | 6.3 | duty cycle 50% |
| <u>DYNAMIC DATA</u> | | | | | | | |
| <u>Propagation delay times</u> | | | | | | | |
| Rise : G ₁ → Q ₂ | t _{pdr} max | 170 | 150 | 200 | ns | 6.0 | } V _{pd} = 1.5 V N = 15 C _L = 250 pF t _f = t _r = 15 ns |
| G ₃ → Q ₂ | t _{pdr} max | 80 | 85 | 120 | ns | 6.0 | |
| Fall : G ₁ → Q ₁ | t _{pdf} max | 170 | 130 | 170 | ns | 6.0 | |
| G ₃ → Q ₂ | t _{pdf} max | 55 | 50 | 55 | ns | 6.0 | |
| <u>Pulse width</u> | t _{Q1L} max | 1.10 | | | µs | 6.0 | } R _t = 10 kΩ ± 1 % C _t = 160 pF ± 1 % |
| | t _{Q1L} typ | 1.00 | | | µs | 6.0 | |
| | t _{Q1L} min | 0.90 | | | µs | 6.0 | |
| <u>Duration input LOW</u> | t _{GL} min | 30 | 30 | 40 | ns | 5.7 and 6.3 | |

CHARACTERISTICS (continued)

DYNAMIC DATA



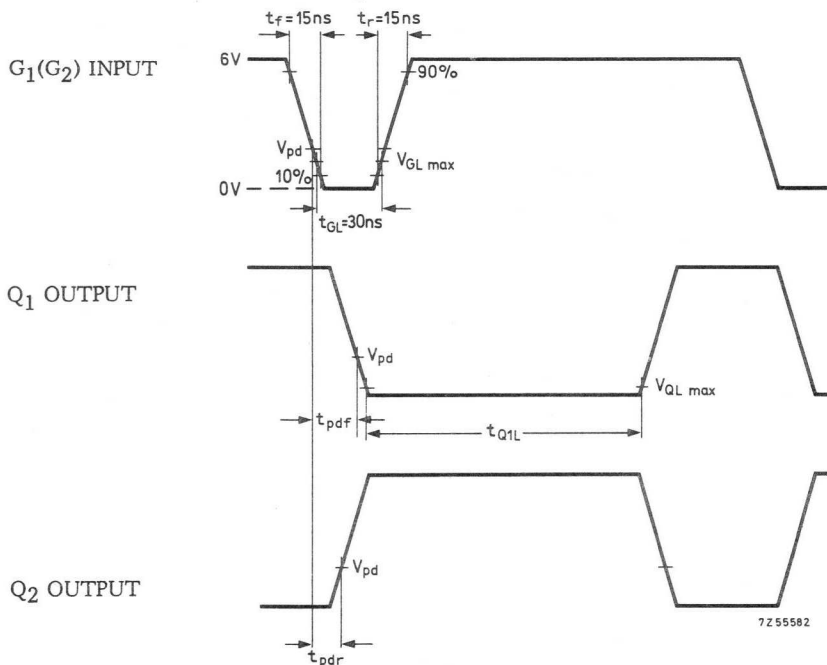
$$a = t_{pdf} : G_1 \rightarrow Q_1$$

$$c = t_{pdf} : G_3 \rightarrow Q_2$$

$$e = t_{Q1L}$$

$$b = t_{pdr} : G_1 \rightarrow Q_2$$

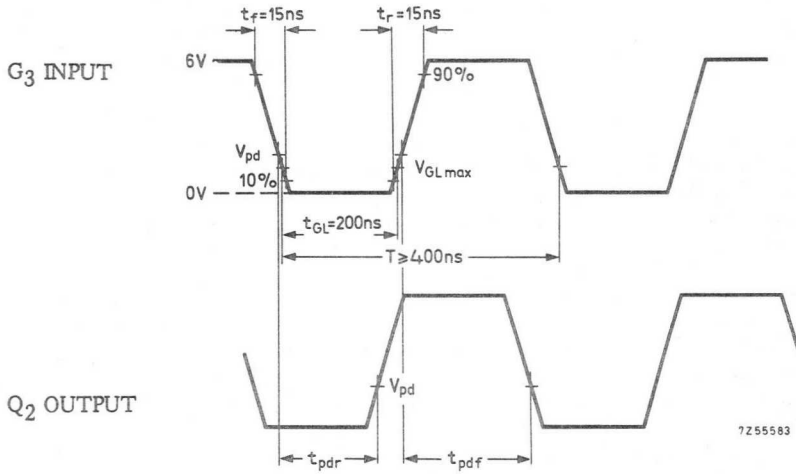
$$d = t_{pdr} : G_3 \rightarrow Q_2$$



Waveform illustrating measurement of t_{pdr} , t_{pdf} , t_{GL} and t_{Q1L} for A pulse generator.

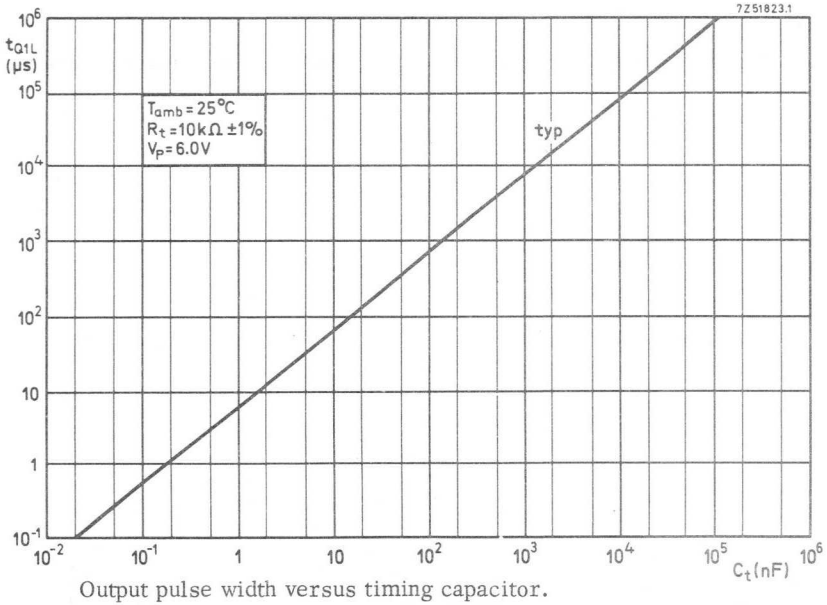
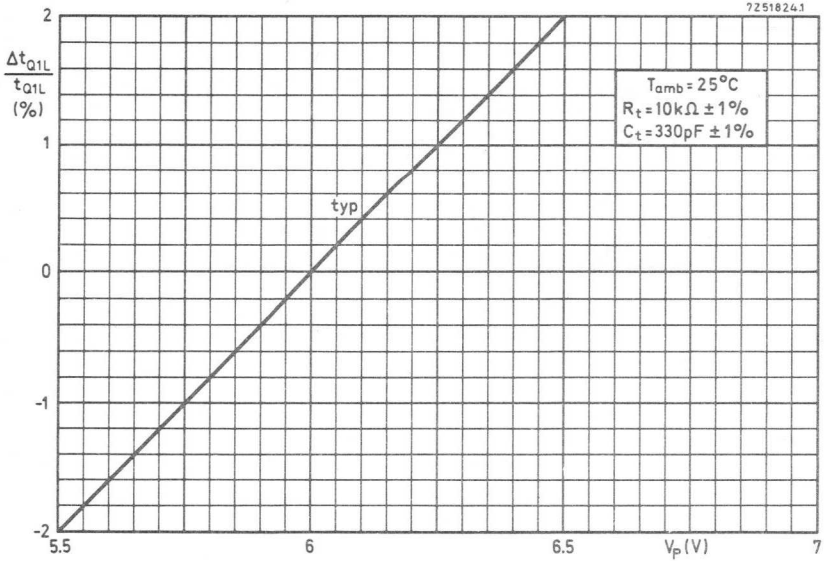
CHARACTERISTICS (continued)

DYNAMIC DATA



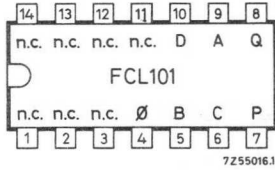
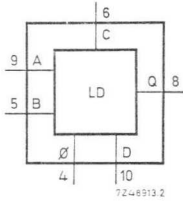
Waveforms illustrating measurement of t_{pdr} , t_{pdf} and t_{GL} for B pulse generator.

CHARACTERISTICS (continued)



The FC family of DTL silicon monolithic integrated circuit has been designed for medium speed digital applications in computing, office electronics, telecommunication and industrial control.

LEVEL DETECTOR



QUICK REFERENCE DATA

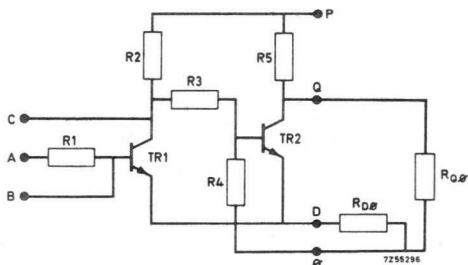
| | | |
|------------------------------------------------------------------------------------------------|-----------------|---------------------------|
| Supply voltage | V_P | $6.0 \pm 5\%$ V |
| Operating ambient temperature range | T_{amb} | 0 to +75 °C |
| Input hysteresis voltage $R_{D\emptyset} = 100 \Omega, T_{amb} = 25 \text{ }^\circ\text{C}$ | ΔV_{At} | min. 60 mV max. 200 mV |
| Available output current $R_{D\emptyset} = 100 \Omega, T_{amb} = 25 \text{ }^\circ\text{C}$ | I_{QL} | 2.7 mA |
| Operating frequency $T_{amb} = 25 \text{ }^\circ\text{C}$ | f | typ. 5 MHz |
| Power consumption 50% duty cycle, $T_{amb} = 25 \text{ }^\circ\text{C}$ | P_{av} | typ. 12 mW |

The FCL101 is a non-inverting Schmitt-trigger circuit. Tripping levels are set by an external resistor or zener diode.

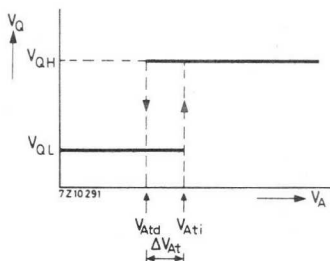
Typical applications are discrimination, restoration, level shifting and pulse-shaping (squaring).

PACKAGE OUTLINE 14 lead dual in-line (See General Section)

CIRCUIT DIAGRAM



VOLTAGE TRANSFER CURVE



Letter symbols:

$R_{Q\emptyset}$ = external resistor between Q and \emptyset

$R_{D\emptyset}$ = external resistor between D and \emptyset

V_Q = short for $V_{Q\emptyset}$ = voltage at Q with respect to \emptyset , the common reference and supply return terminal

V_{Ati} = tripping level for increasing input voltage V_A (short for $V_{A\emptyset}$)

V_{Atd} = tripping level for decreasing input voltage V_A

$\Delta V_{At} = V_{Ati} - V_{Atd}$ = input hysteresis voltage.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|--------------------------------|-------------|------|----------------|
| Supply voltage | V_P | max. | 8.0 V |
| Output voltage | V_Q | max. | 8.0 V |
| Input voltage | V_A | max. | 8.0 V |
| with respect to supply voltage | $V_A - V_P$ | max. | 2.0 V |
| Output current ¹⁾ | $-I_Q$ | max. | 20 mA |
| Input current ²⁾ | $-I_A$ | max. | 0.5 mA |
| Other terminals | I_B | max. | 5 mA |
| | V_C | max. | 5.0 V |
| | V_D | max. | 5.0 V |
| | T_{stg} | | -55 to +125 °C |
| Storage temperature | | | |
| Operating ambient temperature | T_{amb} | | 0 to +75 °C |

SYSTEM DESIGN DATA

| | | | |
|--------------------------------------------------------------------|-----------|------|--------------|
| Uniform system temperature | T_{amb} | | 0 to +75 °C |
| Uniform system supply voltage | V_P | | 5.7 to 6.3 V |
| Output resistance | P_O | max. | 7.6 kΩ |
| Supply current at $T_{amb} = 25$ °C, $V_P = 6$ V duty cycle 50% | I_{Pav} | typ. | 2.0 mA |
| Power dissipation at $T_{amb} = 75$ °C | P_{tot} | max. | 27 mW |

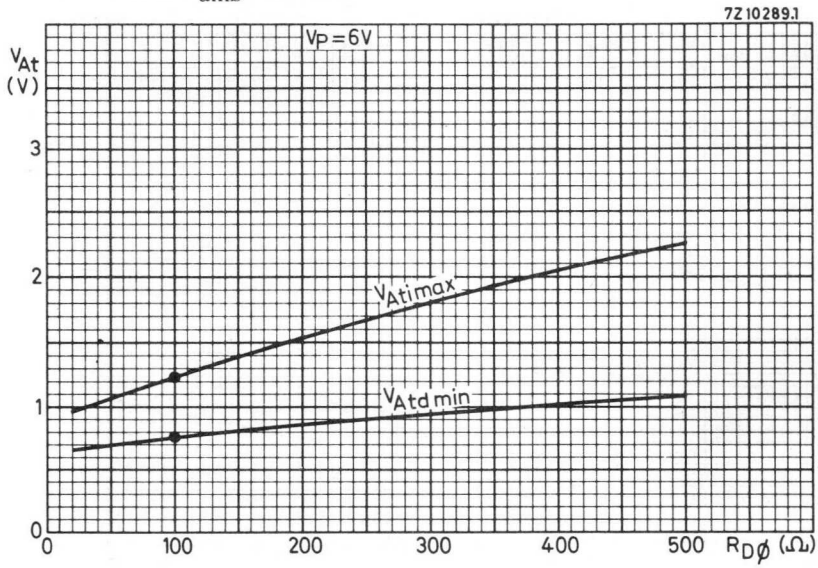
¹⁾ For negative output voltage.

²⁾ Input voltage typ. -9 V when D grounded; no input current protection required for input voltages down to -5 V.

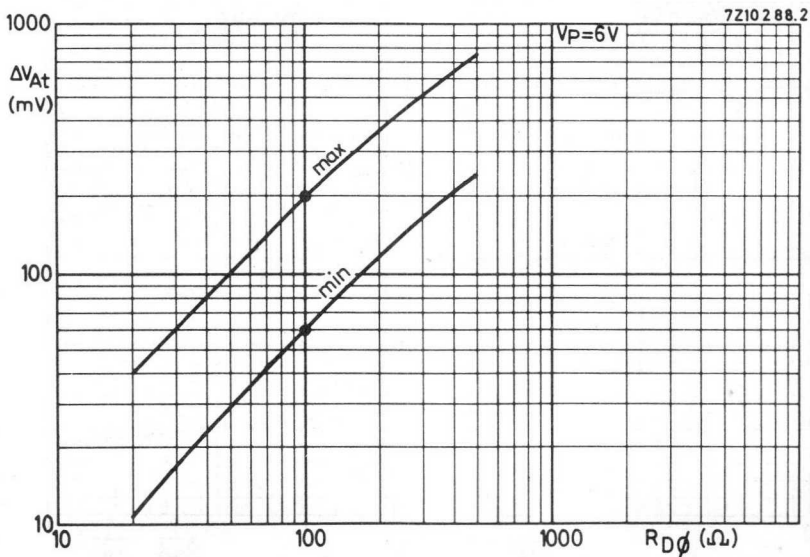
CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and references | | |
|---------------------------------------------------------------------------------------------------------|----------------------|-----------------------|------------|------------|---------------------------|---------------------|---------------------------------------------------------------|
| | | 0 | +25 | +75 | V _P (V) | R _{DO} (Ω) | |
| <u>STATIC DATA</u> | | | | | | | |
| Tripping levels - input voltage increasing - input voltage decreasing Input hysteresis voltage | V _{Atimax} | 1.40 | 1.25 | 1.15 | V | 6.0 | 100 ± 1% |
| | V _{Atdmin} | 0.75 | 0.75 | 0.60 | V | 6.0 | 100 ± 1% |
| | ΔV _{Atmin} | 60 | 60 | 50 | mV | 6.0 | 100 ± 1% |
| | ΔV _{Atmax} | 220 | 200 | 180 | mV | 6.0 | 100 ± 1% |
| Output voltage LOW | V _{QLmax} | 0.4 | 0.4 | 0.4 | V | 5.7 and 6.3 | 0 |
| at: | | | | | | | |
| Output current LOW and at: | I _{QLmax} | 10 | 10 | 7 | mA | | |
| Input voltage LOW | V _{ALmax} | 0.60 | 0.60 | 0.45 | V | | |
| Output voltage LOW | V _{QLmax} | 0.8 | 0.8 | 0.8 | V | 5.7 and 6.3 | 100 ± 1% |
| at: | | | | | | | |
| Output current LOW | I _{QLmax} | 2.5 2.1 | 2.9 2.5 | 1.9 1.6 | mA | 5.7 6.3 | V _{ALmax} = V _{Atdmin} |
| Output voltage HIGH | V _{QHmin} | 5.3 | 5.3 | 5.3 | V | 5.7 | 0 |
| at: | | | | | | | I _Q = 0 |
| Input voltage HIGH | V _{AHmin} | 0.95 | 0.90 | 0.80 | V | | |
| Input current HIGH | I _{AHmax} | 2.2 | 2.0 | 2.0 | mA | 5.7 and 6.3 | 0 |
| Input current HIGH | I _{AHmax} | 1.2 | 1.1 | 1.2 | mA | 5.7 and 6.3 | 100 ± 1% |
| Output current LOW | -I _{QLLmin} | 1.0 | 0.95 | 0.75 | mA | 5.7 | 0 |
| | -I _{QLLmax} | 2.5 | 2.1 | 2.0 | mA | 6.3 | 0 |
| | | | | | | | V _A = 2V, V _Q externally forced to 0 V. |
| Supply current | | | | | | | |
| - output LOW | I _{PLmax} | 4.2 | 3.7 | 3.5 | mA | 6.3 | 0 |
| - output HIGH | I _{PHmax} | 2.9 | 2.6 | 2.5 | mA | 6.3 | 0 |
| | | | | | | | V _A = 0V V _A = 2V |
| <u>DYNAMIC DATA</u> | | | | | | | |
| Operating frequency | f _{min} | - | 1 | - | MHz | 6.0 | 100 ± 1% |
| | f _{typ} | - | 5 | - | MHz | | |

DESIGN CURVES at $T_{amb} = 25\text{ }^{\circ}\text{C}$ (dots indicate guaranteed values)

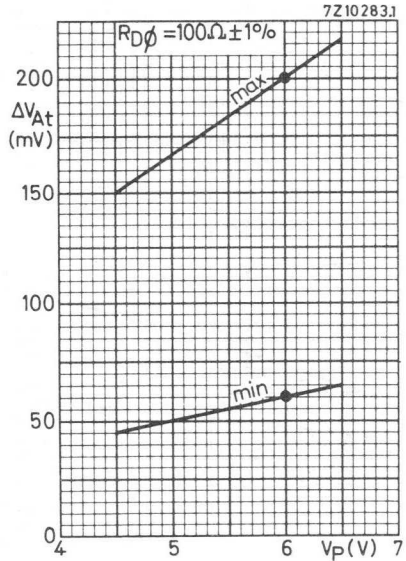
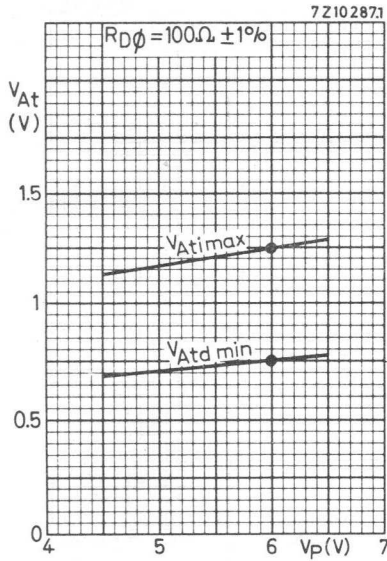


Input tripping levels versus feedback resistance

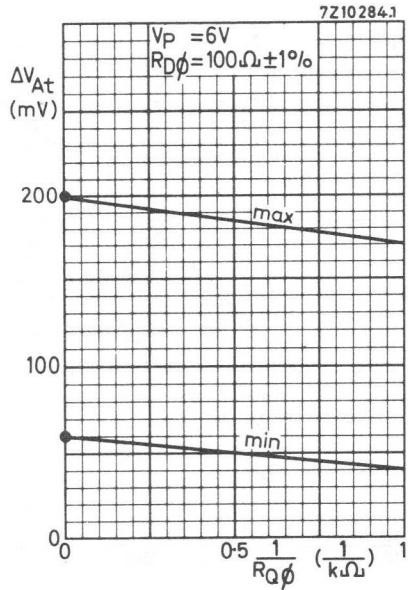
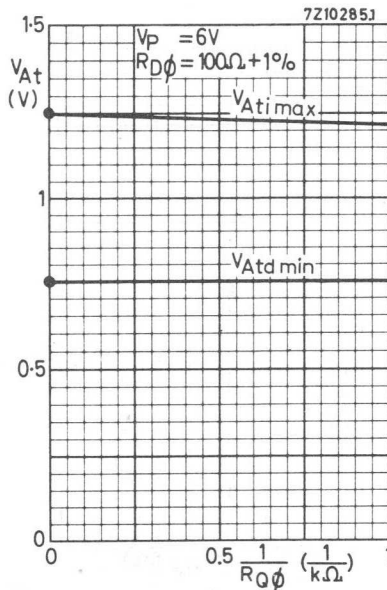


Input hysteresis voltage versus feedback resistance

DESIGN CURVES(continued) at $T_{amb} = 25^{\circ}C$

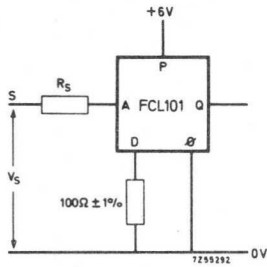


Input tripping levels and hysteresis voltage versus supply voltage

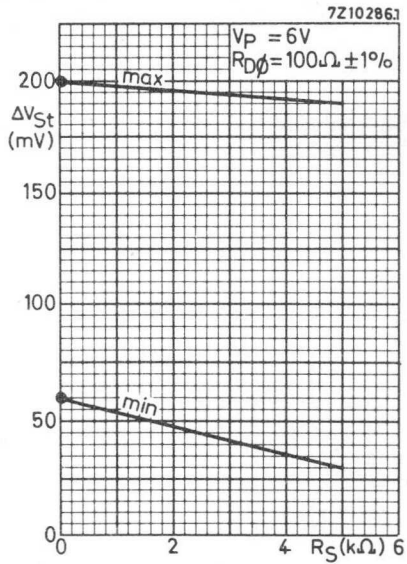


Input tripping levels and hysteresis voltage versus load conductance

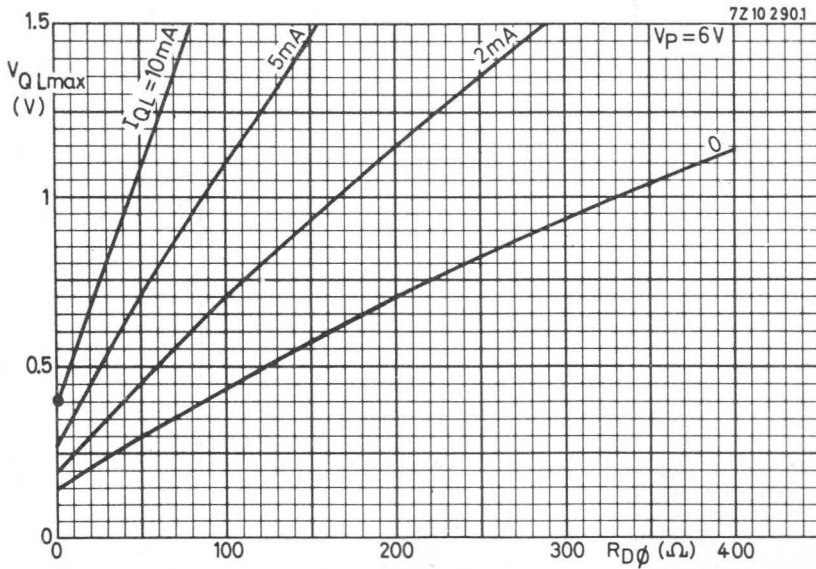
DESIGN CURVES (continued) at $T_{amb} = 25\text{ }^{\circ}\text{C}$



ΔV_{St} = hysteresis at point S.



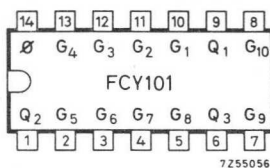
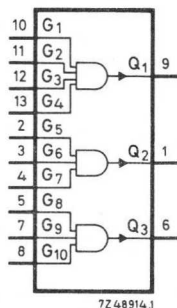
Hysteresis at signal source versus resistance



Low output voltage versus feedback resistance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

TRIPLE GATE EXPANDER



CHARACTERISTICS

| | T_{amb} ($^{\circ}C$) | |
|--------------------------------------------------|---------------------------|--------------|
| | 25 | 75 |
| Reverse breakdown voltage at $I_R = 50 \mu A$ | $V_{(BR)R}$ min. 8.0 | V |
| Reverse leakage current at $V_R = 8.0 V$ | I_R max. 1.0 | 25 μA |
| Forward voltage at $I_F = 2.0 mA$ | V_F max. 1.0 | V |
| Capacitance at $V_R = 0; f = 1 MHz$ | C_d max. 11 | pF |
| Reverse recovery time at $I_F = I_R = 2.0 mA$ | t_{rr} typ. 4 | ns ← |
| | | max. 11 ns ← |

The FCY101 comprises three independent diode arrays. It is intended primarily for expanding the fan-in capability of those FCH gates that have an expansion input terminal.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | |
|-------------------------------|-----------------------|-------------|
| Reverse voltage | V_R max. 8.0 | V |
| Forward current | I_F max. 30 | mA |
| Storage temperature | T_{stg} -55 to +125 | $^{\circ}C$ |
| Operating ambient temperature | T_{amb} 0 to +75 | $^{\circ}C$ |

PACKAGE OUTLINE : 14 lead plastic dual in-line (type A) (See General Section)

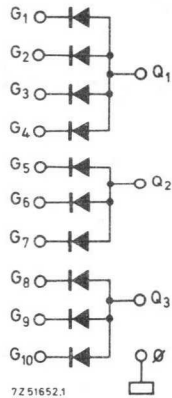
FCY101

expander

FC family

standard temperature range

CIRCUIT DIAGRAM



T T L

FJ family



The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

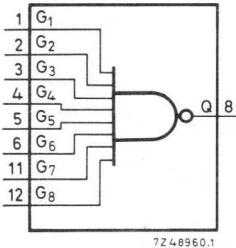
Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

NAND GATES

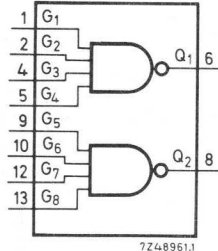
In the standard temperature range the FJ family comprises the following NAND gates (positive logic):

- Single 8-input NAND gate
- Dual 4-input NAND gate
- Triple 3-input NAND gate
- Quadruple 2-input NAND gate

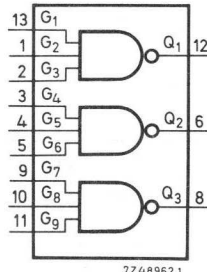
- FJH101/7430
- FJH111/7420
- FJH121/7410
- FJH131/7400



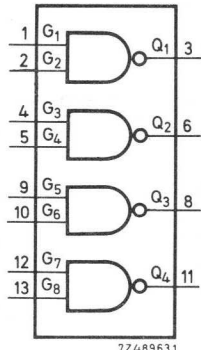
FJH101/7430



FJH111/7420



FJH121/7410



FJH131/7400

QUICK REFERENCE DATA

| | | | |
|--------------------------------------------------|------------------|----------|-------|
| Supply voltage | V _p | 5.0 ± 5% | V |
| Operating ambient temperature range | T _{amb} | 0 to +70 | °C |
| Average propagation delay time | t _{pd} | typ. | 11 ns |
| N = fan-out = 10; T _{amb} = 25 °C | N _a | ≥ | 10 |
| Available d. c. fan-out (full temperature range) | M _L | { > | 0.4 V |
| D. C. noise margin (full temperature range) | | { typ. | 1.0 V |
| Average power consumption (per gate) | P _{av} | typ. | 10 mW |
| T _{amb} = 25 °C | | | |

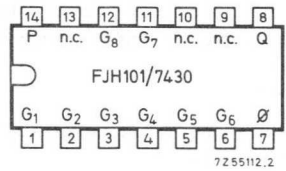
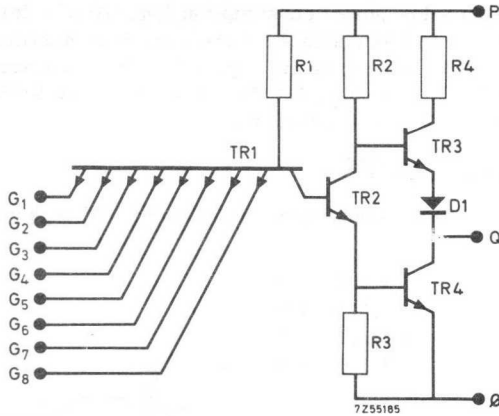
Each gate comprises a multi-emitter AND input gate followed by an inverting amplifier and a totem pole output stage.

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAMS AND TERMINAL CONNECTIONS

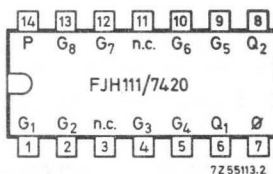
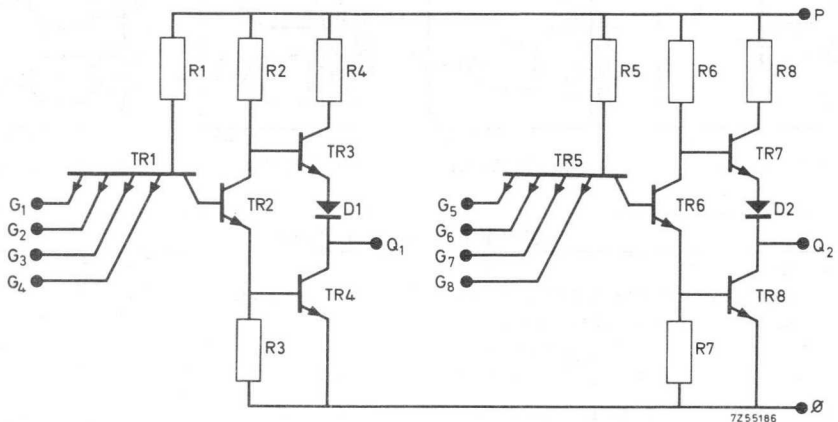
FJH101/7430

Single 8-input NAND gate



FJH111/7420

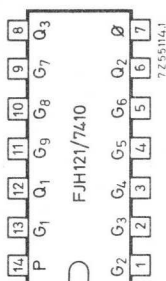
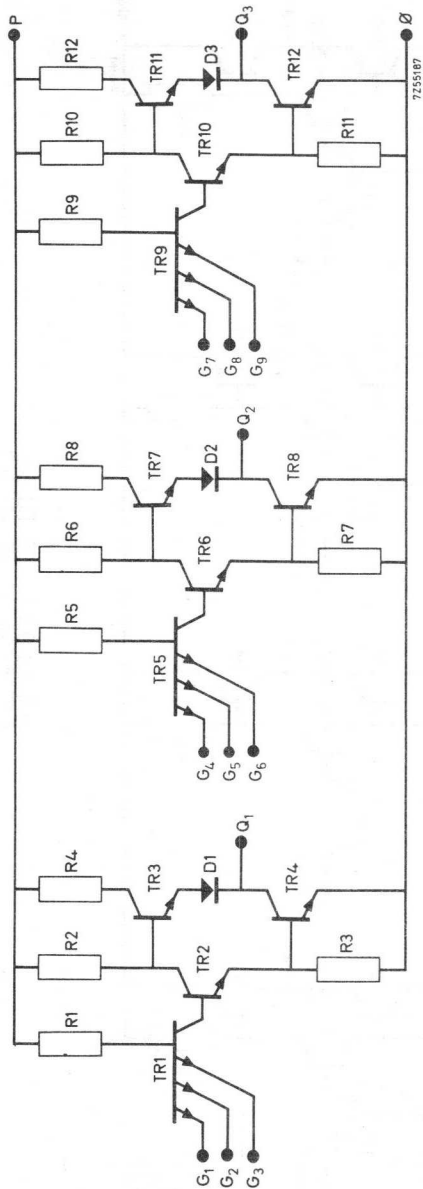
Dual 4-input NAND gate



CIRCUIT DIAGRAMS AND TERMINAL CONNECTIONS (continued)

FJH121/7410

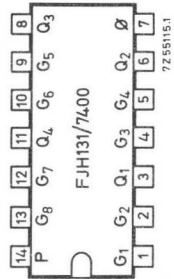
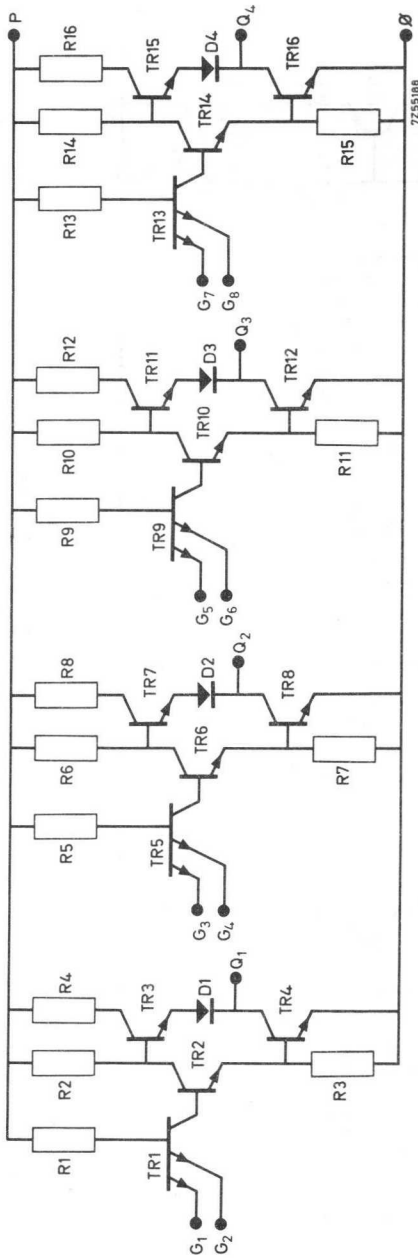
Triple 3-input NAND gate



CIRCUIT DIAGRAMS AND TERMINAL CONNECTIONS (continued)

FJH131/7400

Quadruple 2-input NAND gate



LOGIC FUNCTION

Individual gate operation



$C = \overline{A \cdot B}$ positive logic

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

Function table

| A | B | C |
|---|---|---|
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

| | | |
|-------------------------------|-----------|--------------------------|
| Supply voltage | V_P | max. 7.0 V |
| Output voltage | V_Q | max. 5.5 V |
| G input voltage | V_G | 0 to 5.5 V ¹⁾ |
| Peak negative G input voltage | $-V_{GM}$ | max. 2 V ²⁾ |
| Storage temperature | T_{stg} | -55 to +150 °C |
| Operating ambient temperature | T_{amb} | 0 to + 70 °C |

¹⁾ In addition the voltage difference between any two inputs max. 5.5 V

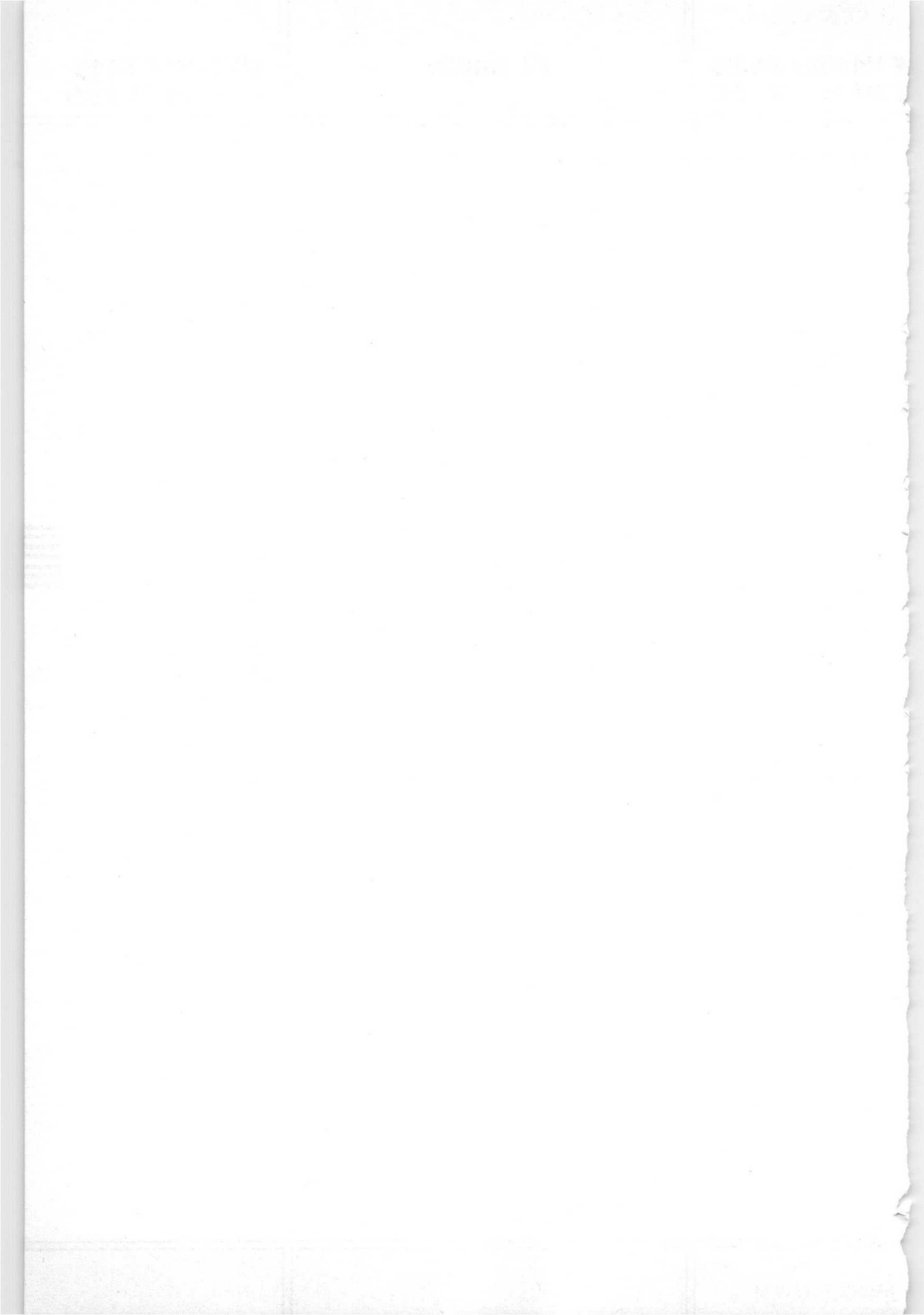
²⁾ Pulse duration $t_p = 20$ ns; repetition frequency $f = 5$ MHz; source resistance $R_S \geq 75 \Omega$.

CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and references | |
|------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------|-----------------------|----------|----------|---------------------------|------|
| | | 0 | 25 | 70 | V _P (V) | |
| <u>STATIC DATA</u> | | | | | | |
| <u>Voltages</u> | | | | | | |
| Input threshold LOW | V _{GLmax} | 0.8 | 0.8 | 0.8 | V | |
| Input threshold HIGH | V _{GHmin} | 2.0 | 2.0 | 2.0 | V | |
| Output LOW | V _{QLmax} | 0.4 | 0.4 | 0.4 | V | 4.75 |
| Output HIGH | V _{QHmin} | 2.4 | 2.4 | 2.4 | V | 4.75 |
| I _Q =I _{QLmax} ; V _G =V _{GHmin} -I _Q =-I _{QHmax} ; V _G =V _{GLmax} | | | | | | |
| <u>Currents</u> | | | | | | |
| Input LOW | -I _{GLmax} | 1.6 | 1.6 | 1.6 | mA | 5.25 |
| Input HIGH | I _{GHmax} | 40 | 40 | 40 | μA | 5.25 |
| Output LOW | I _{QLmax} | 16 | 16 | 16 | mA | |
| Output HIGH | -I _{QHmax} | 0.4 | 0.4 | 0.4 | mA | |
| Output short-circuited | -I _{Qsc min} -I _{Qsc max} | 18 55 | 18 55 | 18 55 | mA mA | 5.25 |
| V _Q =0; V _G =0 | | | | | | |
| <u>DYNAMIC DATA</u> | | | | | | |
| Rise propagation delay time | t _{pdr} typ. | - | 13 | - | ns | 5.0 |
| | t _{pdr} < | - | 22 | - | ns | |
| Fall propagation delay time | t _{pdf} typ. | - | 8 | - | ns | 5.0 |
| | t _{pdf} < | - | 15 | - | ns | |
| | | | | | N=10 | |
| | | | | | N=10 | |

CHARACTERISTICS (continued)

| | | T _{amb} (°C) | | | Conditions and references | | | |
|-----------------------|----------------------|-----------------------|------|------|---------------------------|--|------------------------------------------------|--|
| | | 0 | 25 | 70 | V _P (V) | | | |
| <u>SUPPLY DATA</u> | | | | | | | 5.0 | |
| <u>Supply current</u> | | | | | | | | |
| Output LOW | | | | | | | } V _G = 5.0 V I _Q = 0 | |
| FJH101/7430 | I _{PL} typ. | 3 | 3 | 3 | mA | | | |
| | < | 6 | 6 | 6 | mA | | | |
| FJH111/7420 | I _{PL} typ. | 6 | 6 | 6 | mA | | | |
| | < | 11 | 11 | 11 | mA | | | |
| FJH121/7410 | I _{PL} typ. | 9 | 9 | 9 | mA | | | |
| | < | 16.5 | 16.5 | 16.5 | mA | | | |
| FJH131/7400 | I _{PL} typ. | 12 | 12 | 12 | mA | | | |
| | < | 22 | 22 | 22 | mA | | | |
| Output HIGH | | | | | | | } V _G = 0 I _Q = 0 | |
| FJH101/7430 | I _{PH} typ. | 1 | 1 | 1 | mA | | | |
| | < | 2 | 2 | 2 | mA | | | |
| FJH111/7420 | I _{PH} typ. | 2 | 2 | 2 | mA | | | |
| | < | 4 | 4 | 4 | mA | | | |
| FJH121/7410 | I _{PH} typ. | 3 | 3 | 3 | mA | | | |
| | < | 6 | 6 | 6 | mA | | | |
| FJH131/7400 | I _{PH} typ. | 4 | 4 | 4 | mA | | | |
| | < | 8 | 8 | 8 | mA | | | |



FJ family

standard temperature range

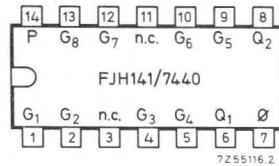
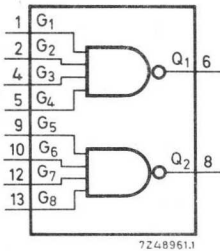
FJH141/7440

dual NAND POWER gate

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

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DUAL NAND POWER GATE



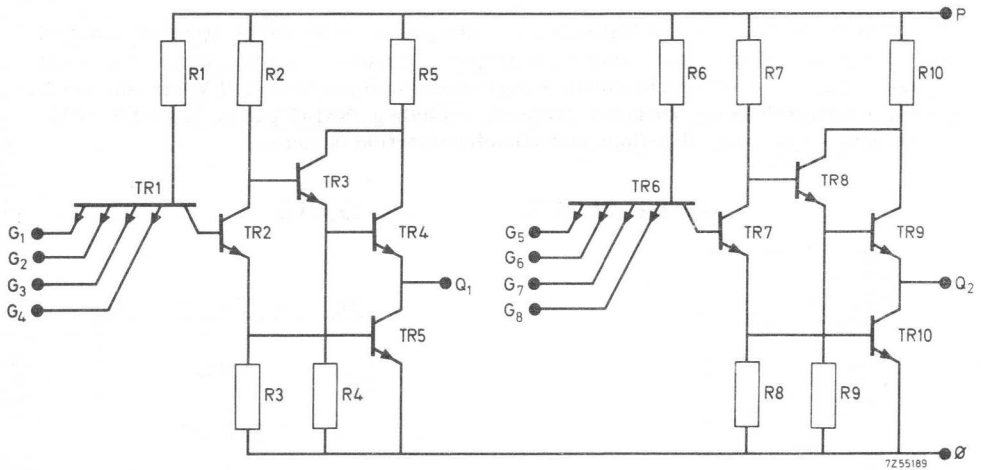
QUICK REFERENCE DATA

| | | | |
|-------------------------------------------------|-----------|---------------|-------|
| Supply voltage | V_p | $5.0 \pm 5\%$ | V |
| Operating ambient temperature | T_{amb} | 0 to +70 | °C |
| Average propagation delay time | t_{pd} | typ. 11 | ns |
| N = fan-out = 30; $T_{amb} = 25$ °C | N_a | \geq | 30 |
| Available d.c. fan-out (full temperature range) | M_L | $>$ | 0.4 V |
| D.C. noise margin (full temperature range) | | typ. 1.0 | V |
| Average power consumption (per gate) | P_{av} | typ. 26.5 | mW |
| $T_{amb} = 25$ °C | | | |

Each gate comprises a multi-emitter AND gate followed by an inverting amplifier and a totem pole power output stage.

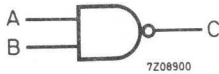
PACKAGE OUTLINE 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM (each gate)



LOGIC FUNCTION

Individual gate operation



$C = \overline{A \cdot B}$ (positive logic)

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

Function table

| A | B | C |
|---|---|---|
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|-------------------------------|-----------|------|---------------------|
| Supply voltage | V_P | max. | 7.0 V |
| Output voltage | V_Q | max. | 5.5 V |
| G input voltage | V_G | max. | 5.5 V ¹⁾ |
| Peak negative G input voltage | $-V_{GM}$ | max. | 2 V ²⁾ |
| Storage temperature | T_{stg} | | -55 to +150 °C |
| Operating ambient temperature | T_{amb} | | 0 to +70 °C |

¹⁾ In addition, peak voltage difference between any two inputs = max. 5.5 V.

²⁾ Pulse duration $t_p = 20$ ns; repetition frequency $f = 5$ MHz; source resistance $R_S \geq 75 \Omega$.

CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and references | | |
|-----------------------------|-----------------------|-----------------------|------|------|---------------------------|-----------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------|
| | | 0 | 25 | 70 | VP (V) | | |
| <u>STATIC DATA</u> | | | | | | | |
| <u>Voltages</u> | | | | | | | |
| Input threshold LOW | V _{GLmax} | 0.8 | 0.8 | 0.8 | V | | |
| Input threshold HIGH | V _{GHmin} | 2.0 | 2.0 | 2.0 | V | | |
| Output LOW | V _{QLmax} | 0.4 | 0.4 | 0.4 | V | 4.75 I _Q =I _{QLmax} ; V _G =V _{GHmin} | |
| Output HIGH | V _{QHmin} | 2.4 | 2.4 | 2.4 | V | 4.75 -I _Q =-I _{QHmax} ; V _G =V _{GLmax} | |
| <u>Currents</u> | | | | | | | |
| Input LOW | -I _{GLmax} | 1.6 | 1.6 | 1.6 | mA | 5.25 V _G =V _{QLmax} ; I _Q =0 | |
| Input HIGH | I _{GHmax} | 40 | 40 | 40 | μA | 5.25 V _G =V _{QHmin} ; I _Q =0 other inputs 0V | |
| Output LOW | I _{QLmax} | 48 | 48 | 48 | mA | | |
| Output HIGH | -I _{QHmax} | 1.2 | 1.2 | 1.2 | mA | | |
| Output short-circuited | -I _{Qsc min} | 18 | 18 | 18 | mA | 5.25 V _Q =0; V _G =0 | |
| | -I _{Qsc max} | 70 | 70 | 70 | mA | | |
| <u>SUPPLY DATA</u> | | | | | | | |
| <u>Supply current</u> | | | | | | | |
| Output LOW | I _{PL} | typ. | 17.2 | 17.2 | 17.2 | mA | 5.0 } V _G =5.0 V; I _Q =0 5.0 } 5.0 } V _G =0; I _Q =0 5.0 } |
| | | < | 27 | 27 | 27 | mA | |
| Output HIGH | I _{PH} | typ. | 4.0 | 4.0 | 4.0 | mA | |
| | | < | 8.0 | 8.0 | 8.0 | mA | |
| <u>DYNAMIC DATA</u> | | | | | | | |
| Rise propagation delay time | t _{pdr} | typ. | - | 13 | - | ns | 5.0 N=30 |
| | | < | - | 22 | - | ns | |
| Fall propagation delay time | t _{pdf} | typ. | - | 8 | - | ns | |
| | | < | - | 15 | - | ns | |

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The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

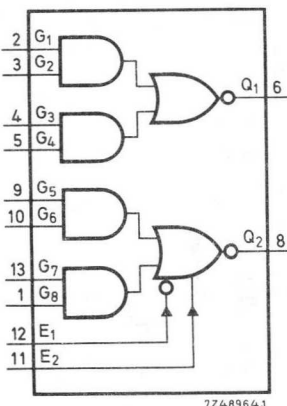
Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

DUAL AND-OR-NOT GATES

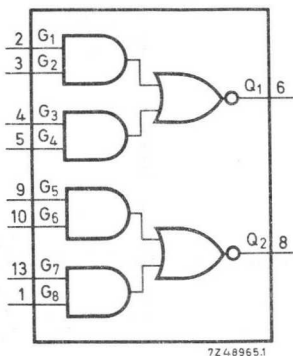
Dual expandable

2+2 input AND-OR-NOT gate FJH151/7450

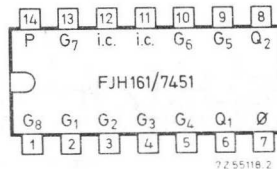
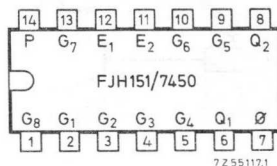
Dual 2+2 input AND-OR-NOT gate FJH161/7451



FJH151/7450



FJH161/7451



QUICK REFERENCE DATA

| | | | |
|-------------------------------------------------|-----------|--------------------------------------------------------------------------|---------------------------------------------------------------------|
| Supply voltage | V_P | $5.0 \pm 5\%$ | V |
| Operating ambient temperature range | T_{amb} | 0 to +70 | °C |
| Average propagation delay time | t_{pd} | typ. 11 | ns |
| N = fan-out = 10; $T_{amb} = 25$ °C | N_a | ≥ 10 | |
| Available d.c. fan-out (full temperature range) | M_L | $\left\{ \begin{array}{l} > 0.4 \\ \text{typ. } 1.0 \end{array} \right.$ | $\left\{ \begin{array}{l} \text{V} \\ \text{V} \end{array} \right.$ |
| D.C. noise margin (full temperature range) | | | |
| Average power consumption (per gate) | P_{av} | typ. 14.25 | mW |
| $T_{amb} = 25$ °C | | | |

The FJH151/7450 is a dual 2+2 input AND-OR-NOT gate, one of the two gates having additional inputs for up to four FJY101/7460 expander circuits. It can be arranged to perform the exclusive OR function.

The FJH161/7451 is similar to the FJH151/7450, except for being non-expandable.

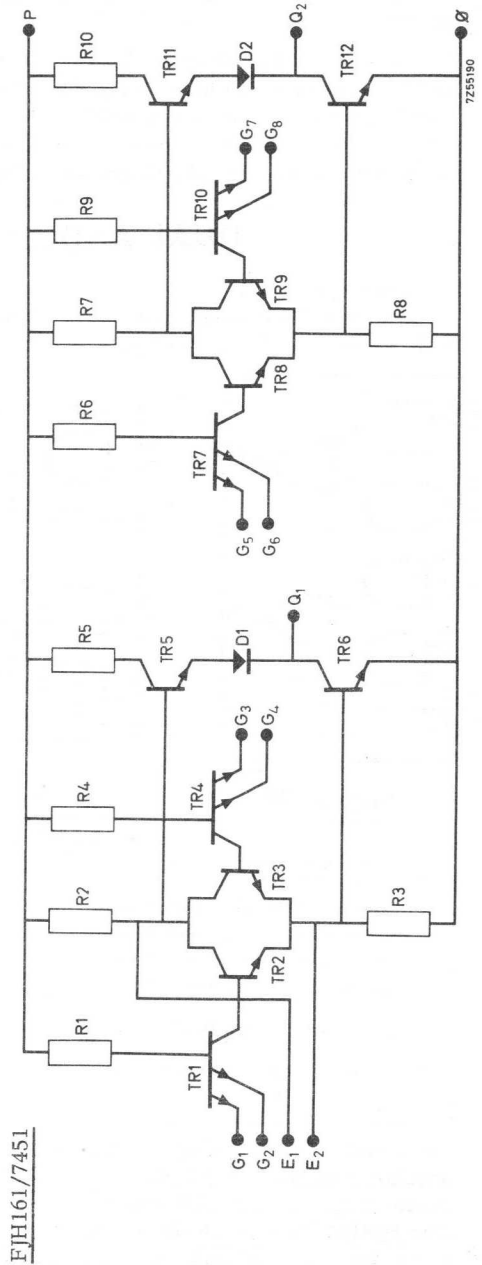
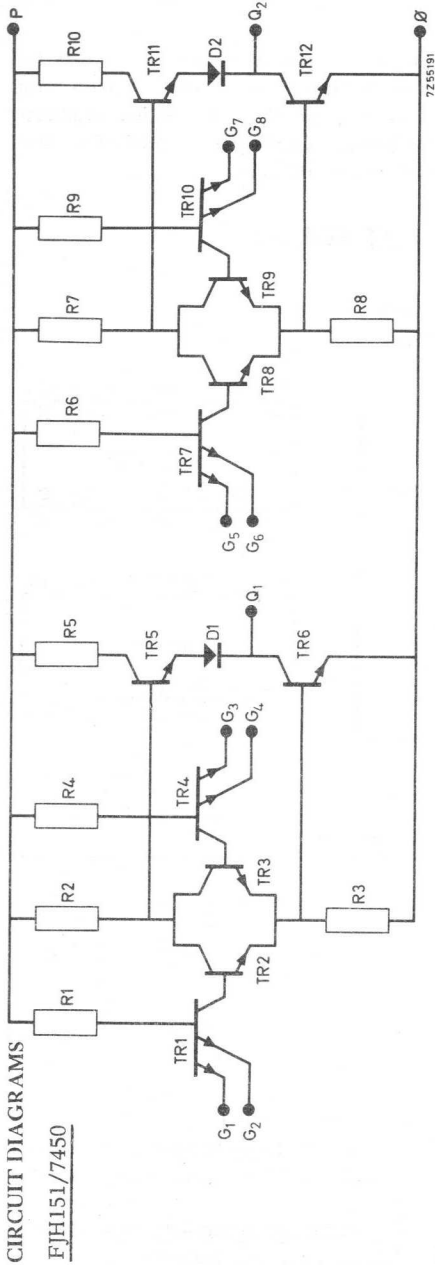
PACKAGE OUTLINE 14 lead plastic dual in-line (type A) (See General Section)

FJH151/7450 FJH161/7451

dual AND-OR-NOR gates

FJ family

standard temperature range



FJ family
standard temperature range

FJH 151/7450
FJH 161/7451
dual AND-OR-NOT gates

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|-------------------------------|-----------|------|---------------------|
| Supply voltage | V_P | max. | 7.0 V |
| Output voltage | V_Q | max. | 5.5 V |
| G input voltage | V_G | max. | 5.5 V ¹⁾ |
| Peak negative G input voltage | $-V_{GM}$ | max. | 2 V ²⁾ |
| Storage temperature | T_{stg} | | -55 to +150 °C |
| Operating ambient temperature | T_{amb} | | 0 to 70 °C |



¹⁾ In addition, peak voltage difference between any two inputs = max. 5.5 V.
²⁾ Pulse duration $t_p = 20$ ms; repetition frequency $f = 5$ MHz; source resistance $R_S \geq 75 \Omega$.

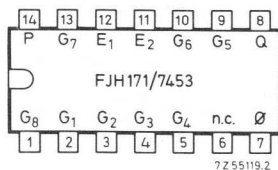
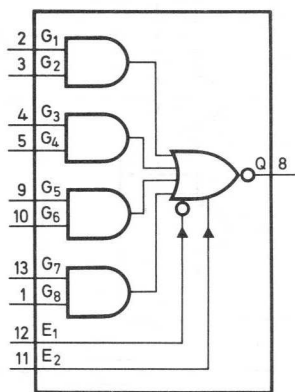
CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and references | |
|-----------------------------|----------------------------------------------|-----------------------|------------|------------|---------------------------|-----------------------------------------------------------------------------------|
| | | | | | 0 | 25 |
| <u>STATIC DATA</u> | | | | | | |
| <u>Voltages</u> | | | | | | |
| Input threshold LOW | V _{GLmax} | 0.8 | 0.8 | 0.8 | V | |
| Input threshold HIGH | V _{GHmin} | 2.0 | 2.0 | 2.0 | V | |
| Output LOW | V _{QLmax} | 0.4 | 0.4 | 0.4 | V | 4.75 I _Q =I _{QLmax} ; V _G =V _{GHmin} |
| Output HIGH | V _{QHmin} | 2.4 | 2.4 | 2.4 | V | 4.75 -I _Q =-I _{QHmax} ; V _G =V _{GLmax} |
| <u>Currents</u> | | | | | | |
| Input LOW | -I _{GLmax} | 1.6 | 1.6 | 1.6 | mA | 5.25 V _G =V _{QLmax} ; I _Q =0 |
| Input HIGH | I _{GHmax} | 40 | 40 | 40 | μA | 5.25 V _G =V _{QHmin} ; I _Q =0 other inputs 0V |
| Output LOW | I _{QLmax} | 16 | 16 | 16 | mA | |
| Output HIGH | -I _{QHmax} | 0.4 | 0.4 | 0.4 | mA | |
| Output short-circuited | -I _{Qscmin} -I _{Qscmax} | 18 55 | 18 55 | 18 55 | mA | 5.25 V _Q =0; V _G =0 |
| <u>SUPPLY DATA</u> | | | | | | |
| <u>Supply current</u> | | | | | | |
| Output LOW | I _{PL} | typ. 7.4 < 14 | 7.4 14 | 7.4 14 | mA | 5.0 } V _G =5.0 V; I _Q =0 5.0 } |
| Output HIGH | I _{PH} | typ. 4.0 < 8.0 | 4.0 8.0 | 4.0 8.0 | mA | 5.0 } V _G =0; I _Q =0 5.0 } |
| <u>DYNAMIC DATA</u> | | | | | | |
| Rise propagation delay time | t _{pdr} | typ. - < - | 13 22 | - - | ns | 5.0 } N = 10, one pair of AND inputs at V _G = 0.4V |
| Fall propagation delay time | t _{pdf} | typ. - < - | 8 15 | - - | ns | 5.0 } |

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EXPANDABLE 2+2+2+2 INPUT AND-OR-NOT GATE



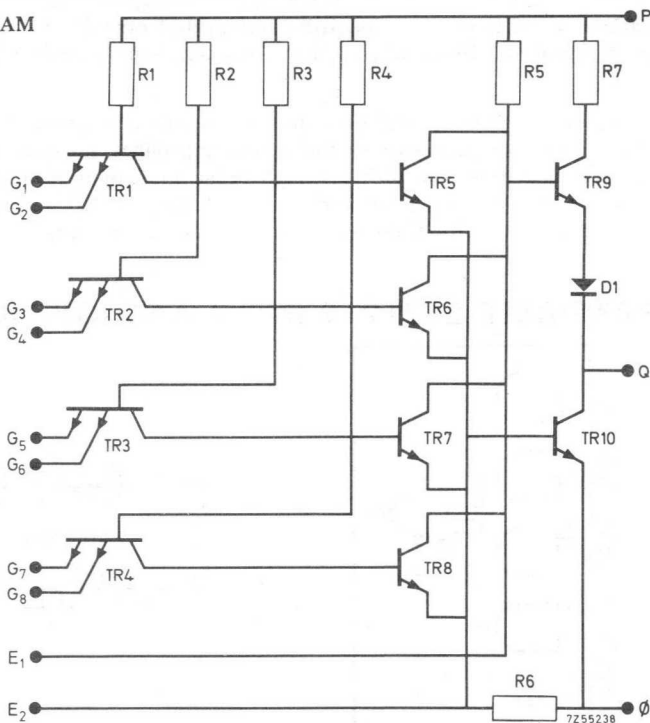
QUICK REFERENCE DATA

| | | |
|-----------------------------------------------------------------------|-----------|-------------------------|
| Supply voltage | V_p | $5.0 \pm 5\%$ V |
| Operating ambient temperature | T_{amb} | 0 to +70 °C |
| Average propagation delay time N = fan-out = 10; $T_{amb} = 25$ °C | t_{pd} | typ. 11 ns |
| Available d. c. fan-out (full temperature range) | N_a | ≥ 10 |
| D. C. noise margin (full temperature range) | M_L | > 0.4 V typ. 1.0 V |
| Average power consumption $T_{amb} = 25$ °C | P_{av} | typ. 22.75 mW |

The FJH171/7453 has additional inputs for up to four FJY101/7460 expander circuits.

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



LOGIC FUNCTION

$$Q = \overline{G_1 \cdot G_2 + G_3 \cdot G_4 + G_5 \cdot G_6 + G_7 \cdot G_8 + EX} \quad (\text{for positive logic})$$

EX represents the extra function available if gate expander FJY101 is used. (Connect E₁, E₂ to Q₁, Q₂ respectively or to Q₃, Q₄ respectively, of the FJY101 to get a 4-input NAND function).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|-------------------------------|------------------|------|---------------------|
| Supply voltage | V _P | max. | 7.0 V |
| Output voltage | V _Q | max. | 5.5 V |
| G input voltage | V _G | max. | 5.5 V ¹⁾ |
| Peak negative G input voltage | -V _{GM} | max. | 2 V ²⁾ |
| Storage temperature | T _{stg} | | -55 to +150 °C |
| Operating ambient temperature | T _{amb} | | 0 to +70 °C |

¹⁾ In addition, the voltage between any two inputs must not exceed 5.5 V.

²⁾ Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance R_S ≥ 75 Ω.

CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and references | |
|-------------------------------------|------------------------------------------------|-----------------------|------------|------------|---------------------------|----------------------------------------------------------------------------------------------|
| | | 0 | 25 | 70 | V _P (V) | |
| <u>STATIC DATA</u> | | | | | | |
| <u>Voltages</u> | | | | | | |
| Input threshold LOW | V _{GLmax} | 0.8 | 0.8 | 0.8 | V | |
| Input threshold HIGH | V _{GHmin} | 2.0 | 2.0 | 2.0 | V | |
| Output LOW | V _{QLmax} | 0.4 | 0.4 | 0.4 | V | 4.75 I _Q =I _{QLmax} V _G =V _{GHmin} |
| Output HIGH | V _{QHmin} | 2.4 | 2.4 | 2.4 | V | 4.75 -I _Q =-I _{QHmax} ; V _G =V _{GLmax} |
| <u>Currents</u> | | | | | | |
| Input LOW | -I _{GLmax} | 1.6 | 1.6 | 1.6 | mA | 5.25 V _G =V _{QLmax} ; I _Q =0 |
| Input HIGH | I _{GHmax} | 40 | 40 | 40 | μA | 5.25 V _G =V _{QHmin} ; I _Q =0 |
| Output LOW | I _{QLmax} | 16 | 16 | 16 | mA | other inputs 0 V |
| Output HIGH | -I _{QHmax} | 0.4 | 0.4 | 0.4 | mA | |
| Output short-circuited (see note 1) | -I _{Qsc min} -I _{Qsc max} | 18 55 | 18 55 | 18 55 | mA | 5.25 V _Q =0; V _G =0 |
| <u>SUPPLY DATA</u> | | | | | | |
| <u>Supply current</u> | | | | | | |
| Output LOW | I _{PL} typ. < | 5.1 9.5 | 5.1 9.5 | 5.1 9.5 | mA | 5.0 } V _G =5.0 V; I _Q =0 5.0 } V _G =0; I _Q =0 |
| Output HIGH | I _{PH} typ. < | 4.0 8.0 | 4.0 8.0 | 4.0 8.0 | mA | |
| <u>DYNAMIC DATA</u> | | | | | | |
| Rise propagation delay time | t _{pdr} typ. | - | 13 | - | ns | 5.0 } N = 10 5.0 } one pair of AND inputs at V _G =0.4 V |
| | t _{pdr} < | - | 22 | - | ns | |
| Fall propagation delay time | t _{pdf} typ. | - | 8 | - | ns | 5.0 } 5.0 } |
| | t _{pdf} < | - | 15 | - | ns | |

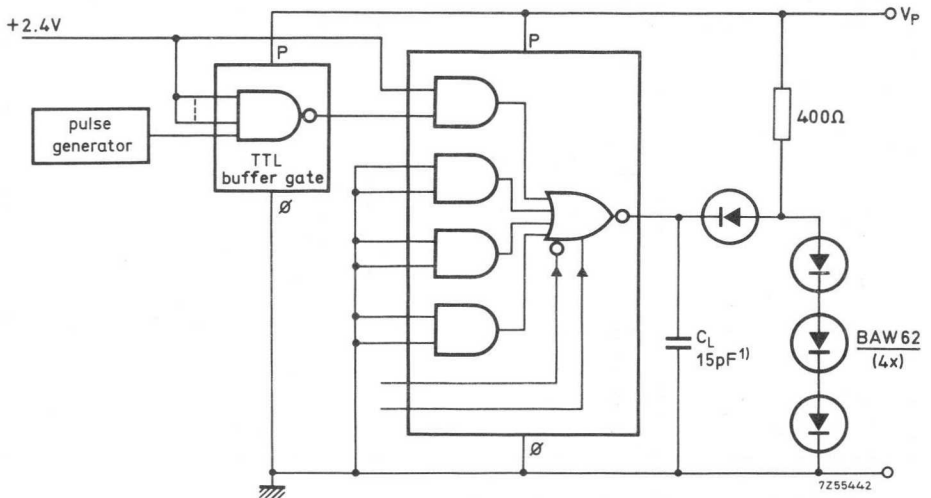
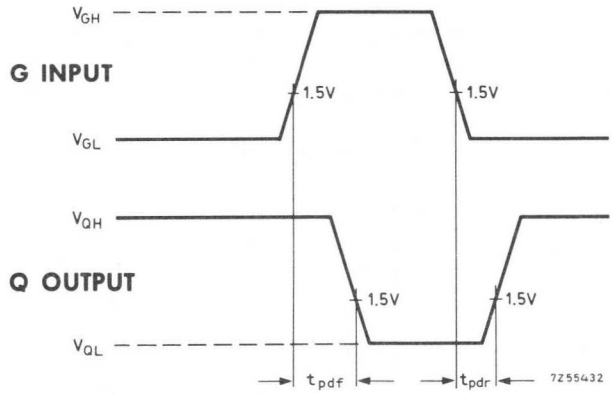
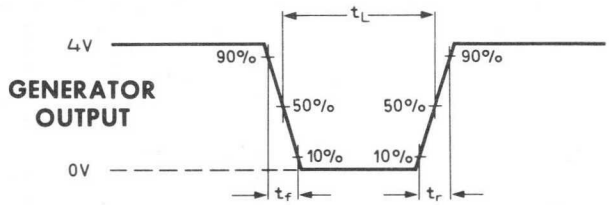
Note 1: Not more than one output must be short circuited at any time.

CHARACTERISTICS (continued)

DYNAMIC DATA

Generator:

- $f = 1 \text{ MHz}$
- $t_L = 0.5 \mu\text{s}$
- $t_f \leq 15 \text{ ns}$
- $t_r \leq 15 \text{ ns}$
- $R_S = 50 \Omega$

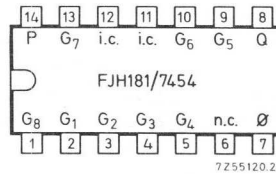
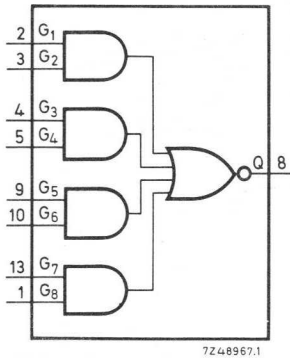


1) Including probe and jig capacitance.

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2+2+2+2 INPUT AND-OR-NOT GATE

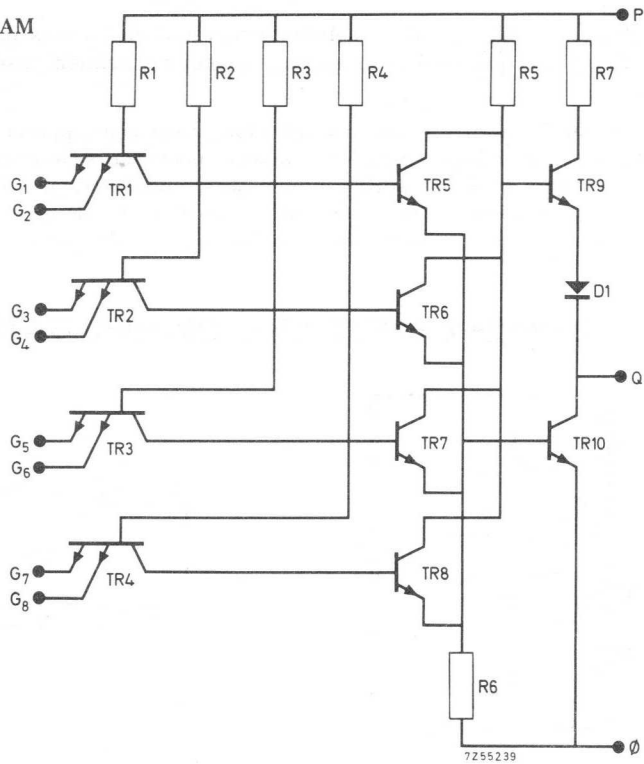


QUICK REFERENCE DATA

| | | | |
|-----------------------------------------------------------------------|-----------|-----------------|----|
| Supply voltage | V_P | $5.0 \pm 5\%$ | V |
| Operating ambient temperature | T_{amb} | 0 to +70 | °C |
| Average propagation delay time N = fan-out = 10; $T_{amb} = 25$ °C | t_{pd} | typ. 11 | ns |
| Available d.c. fan-out (full temperature range) | N_a | \geq | 10 |
| D.C. noise margin (full temperature range) | M_L | $>$ typ. 1.0 | V |
| Average power consumption $T_{amb} = 25$ °C | P_{av} | typ. 22.75 | mW |

PACKAGE OUTLINE 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



LOGIC FUNCTION

$$Q = G_1 \cdot G_2 + G_3 \cdot G_4 + G_5 \cdot G_6 + G_7 \cdot G_8 \text{ (for positive logic)}$$

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

| | | | |
|-------------------------------|-----------|------|---------------------|
| Supply voltage | V_P | max. | 7.0 V |
| Output voltage | V_Q | max. | 5.5 V |
| G input voltage | V_G | max. | 5.5 V ¹⁾ |
| Peak negative G input voltage | $-V_{GM}$ | max. | 2 V ²⁾ |
| Storage temperature | T_{stg} | | -55 to +150 °C |
| Operating ambient temperature | T_{amb} | | 0 to +70 °C |

¹⁾ In addition the voltage between any two inputs must not exceed 5.5 V.

²⁾ Pulse duration $t_p = 20$ ns; repetition frequency $f = 5$ MHz; source resistance $R_S \geq 75 \Omega$.

CHARACTERISTICS

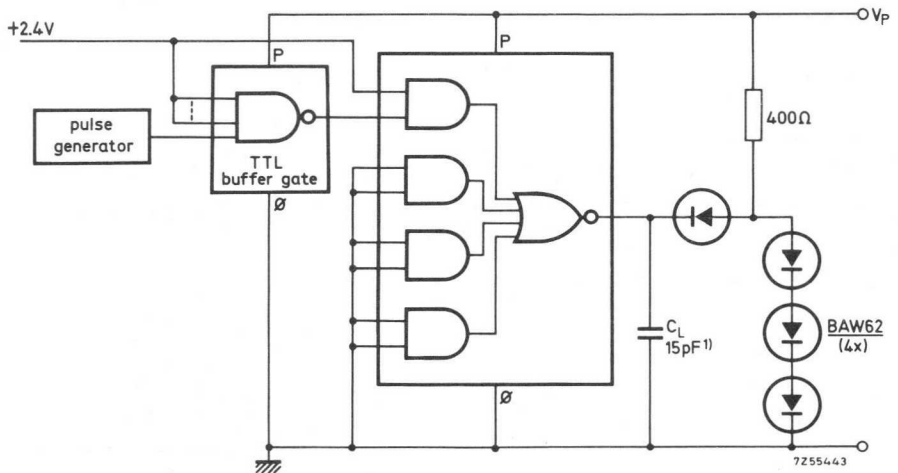
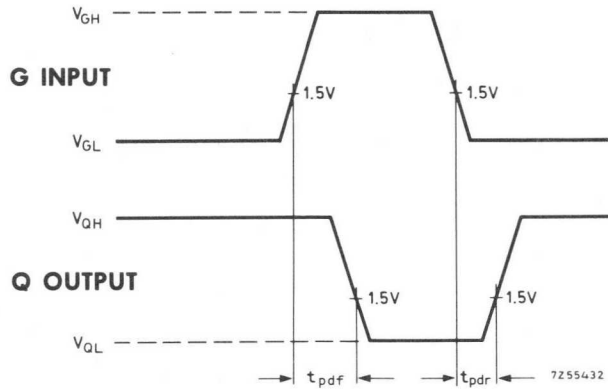
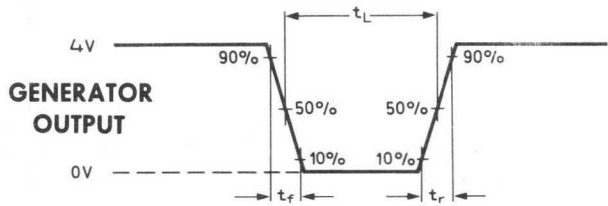
| | | T _{amb} (°C) | | | Conditions and references | |
|------------------------------------------------------------------------------------|------------------------------------------------|-----------------------|----------|----------|---------------------------|------|
| | | 0 | 25 | 70 | V _P (V) | |
| <u>STATIC DATA</u> | | | | | | |
| <u>Voltages</u> | | | | | | |
| Input threshold LOW | V _{GLmax} | 0.8 | 0.8 | 0.8 | V | |
| Input threshold HIGH | V _{GHmin} | 2.0 | 2.0 | 2.0 | V | |
| Output LOW | V _{QLmax} | 0.4 | 0.4 | 0.4 | V | 4.75 |
| Output HIGH | V _{QHmin} | 2.4 | 2.4 | 2.4 | V | 4.75 |
| $I_Q = I_{QLmax}$ $V_G = V_{GHmin}$ $-I_Q = -I_{QHmax}$ $V_G = V_{GLmax}$ | | | | | | |
| <u>Currents</u> | | | | | | |
| Input LOW | -I _{GLmax} | 1.6 | 1.6 | 1.6 | mA | 5.25 |
| Input HIGH | I _{GHmax} | 40 | 40 | 40 | μA | 5.25 |
| Output LOW | I _{QLmax} | 16 | 16 | 16 | mA | |
| Output HIGH | -I _{QHmax} | 0.4 | 0.4 | 0.4 | mA | |
| Output short-circuited | -I _{Qsc min} -I _{Qsc max} | 18 55 | 18 55 | 18 55 | mA | 5.25 |
| $V_Q = 0; V_G = 0$ | | | | | | |
| <u>SUPPLY DATA</u> | | | | | | |
| <u>Supply current</u> | | | | | | |
| Output LOW | I _{PL} | typ. < 5.1 | 5.1 | 5.1 | mA | 5.0 |
| Output HIGH | I _{PH} | typ. < 4.0 | 4.0 | 4.0 | mA | 5.0 |
| $V_G = 5.0 V; I_Q = 0$ $V_G = 0; I_Q = 0$ | | | | | | |
| <u>DYNAMIC DATA</u> | | | | | | |
| Rise propagation delay time | t _{pdr} | typ. < - | 13 | - | ns | 5.0 |
| Fall propagation delay time | t _{pdf} | typ. < - | 8 | - | ns | 5.0 |
| $N = 10$ one pair AND inputs at V _G = 0.4 V | | | | | | |
| | | | | | | 5.0 |

CHARACTERISTICS (continued)

DYNAMIC DATA

Generator

- $f = 1 \text{ MHz}$
- $t_L = 0.5 \mu\text{s}$
- $t_f \leq 15 \text{ ns}$
- $t_r \leq 15 \text{ ns}$
- $R_S = 50 \Omega$

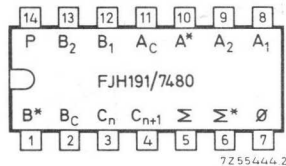
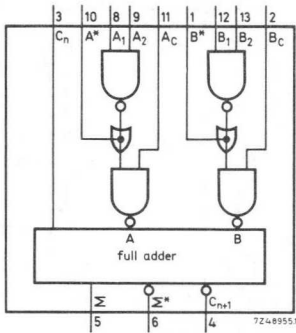


1) Including probe and jig capacitance.

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

FULL ADDER



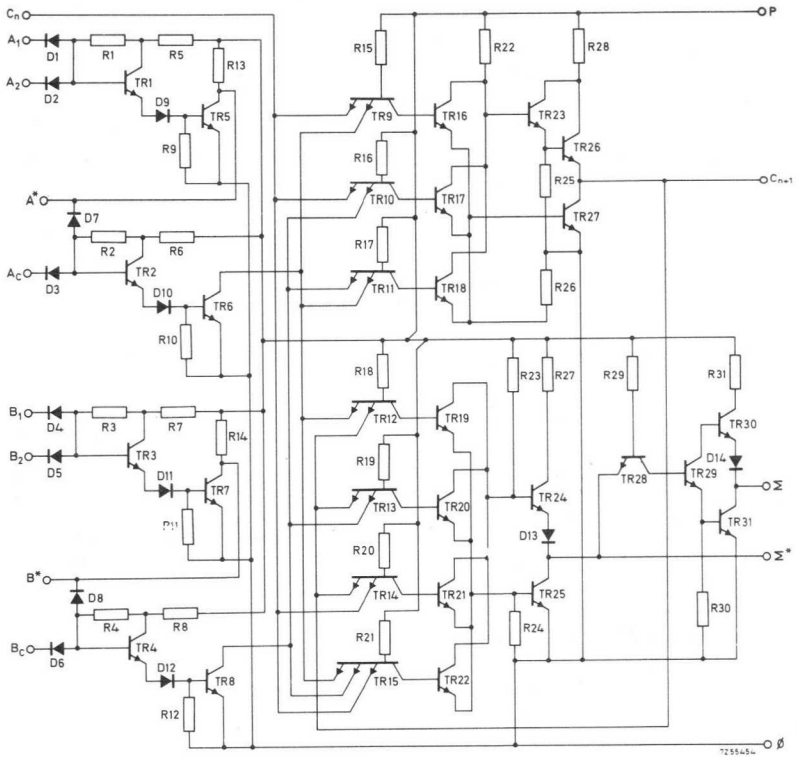
QUICK REFERENCE DATA

| | | | |
|----------------------------------------------------------------------------|-----------|---------------|--------|
| Supply voltage | V_P | $5.0 \pm 5\%$ | V |
| Operating ambient temperature | T_{amb} | 0 to +70 | °C |
| Available d.c. fan-out for outputs: Σ ; Σ^* (sum outputs) | N_a | \geq | 10 |
| C_{n+1} (inverted carry output) | N_a | \geq | 5 |
| Average power consumption | P_{av} | typ. | 105 mW |

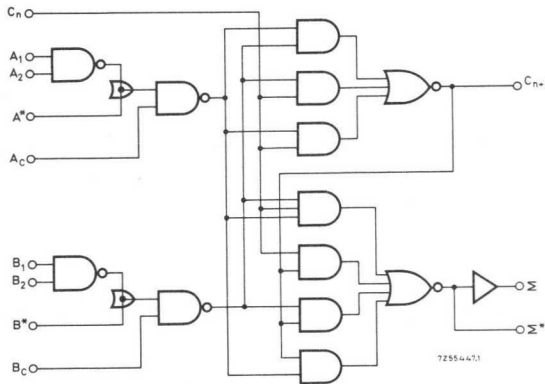
The FJH191/7480 is a single-bit, high speed, binary full adder with gated complementary inputs, complementary sum outputs (Σ and Σ^*), and inverted carry output.

PACKAGE OUTLINE :14 lead plastic dual in-line (type A) See General Section

CIRCUIT DIAGRAM



LOGIC DIAGRAM



FUNCTION TABLE

| C _n | A | B | C _{n+1} | Σ | Σ* |
|----------------|---|---|------------------|---|----|
| L | L | L | H | L | H |
| L | H | L | H | H | L |
| L | L | H | H | H | L |
| L | H | H | L | L | H |
| H | L | L | H | H | L |
| H | H | L | L | L | H |
| H | L | H | L | L | H |
| H | H | H | L | H | L |

$$A = \overline{A^* \cdot AC}$$

$$A^* = A_1 \cdot A_2$$

$$B = \overline{B^* \cdot BC}$$

$$B^* = B_1 \cdot B_2$$

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

Notes

When A* is used as an input, A₁ and A₂ must be connected to φ; when B* is used as an input, B₁ and B₂ must be connected to φ.

When A₁ and A₂ are used as inputs, A* must either be open or in wired-OR use; the same applies to B* when B₁ and B₂ are used as inputs.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|-------------------------------|----------------------------------------------------|------|-------------------|
| Supply voltage | V _p | max. | 7.0 V |
| Input voltage | V _G ; V _{Q1} ; V _{Q2} | max. | 5.5 V |
| Peak negative input voltage | -V _{IM} | max. | 2 V ¹⁾ |
| Operating ambient temperature | T _{amb} | | 0 to +70 °C |
| Storage temperature | T _{stg} | | -55 to +125 °C |

1) Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance R_S > 75 Ω

CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and References | |
|---------------------------------------------------------------------------------------------------------------|--------------------------|-----------------------|-----|-----|---------------------------|---------------------------------------------------------------|
| | | 0 | 25 | 70 | V _P (V) | |
| <u>STATIC DATA</u> | | | | | | |
| Input threshold LOW | V _{ILmax} | 0.8 | 0.8 | 0.8 | V | 4.75 |
| Input threshold HIGH | V _{IHmin} | 2.0 | 2.0 | 2.0 | V | 4.75 |
| Output LOW | | | | | | |
| at Σ ; Σ^* | V _{OLmax} | 0.4 | 0.4 | 0.4 | V | 4.75 I _O = 16 mA |
| at C _{n+1} | V _{OLmax} | 0.4 | 0.4 | 0.4 | V | 4.75 I _O = 8 mA |
| at A*; B* | V _{OLmax} | 0.4 | 0.4 | 0.4 | V | 4.75 I _O = 4.8 mA |
| Output HIGH | | | | | | |
| at Σ ; Σ^* | V _{OHmin} | 2.4 | 2.4 | 2.4 | V | 4.75 I _O = -400 μ A |
| at C _{n+1} | V _{OHmin} | 2.4 | 2.4 | 2.4 | V | 4.75 I _O = -200 μ A |
| at A*; B* | V _{OHmin} | 2.4 | 2.4 | 2.4 | V | 4.75 I _O = -120 μ A |
| <u>Currents</u> | | | | | | |
| Input LOW | | | | | | |
| at C _n | -I _{ILmax} | 8.0 | 8.0 | 8.0 | mA | 5.25 V _I = V _{OLmax} ; I _O = 0 |
| at A ₁ ; A ₂ ; A _C ; } B ₁ ; B ₂ ; B _C } | -I _{ILmax} | 1.6 | 1.6 | 1.6 | mA | 5.25 V _I = V _{OLmax} ; I _O = 0 |
| at A*; B* | -I _{ILmax} | 2.6 | 2.6 | 2.6 | mA | 5.25 V _O = V _{OLmax} ; I _O = 0 |
| Input HIGH | | | | | | |
| at C _n | I _{IHmax} | 200 | 200 | 200 | μ A | 5.25 V _I = V _{OLmax} ; I _O = 0 |
| | I _{IHmax} | 1 | 1 | 1 | mA | 5.25 V _I = 5.5 V; I _O = 0 |
| at A ₁ ; A ₂ ; A _C | I _{IHmax} | 15 | 15 | 15 | μ A | 5.25 V _I = V _{OHmin} ; I _O = 0 |
| B ₁ ; B ₂ ; B _C | I _{IHmax} | 1 | 1 | 1 | mA | 5.25 V _I = 5.5 V; I _O = 0 |
| Output short circuit | | | | | | |
| at Σ ; Σ^* | -I _{Oscmin} | 18 | 18 | 18 | mA | 5.25 } V _O = 0; V _O = 0 |
| | -I _{Oscmax} | 57 | 57 | 57 | mA | |
| at C _{n+1} | I _{Oscmin} | 18 | 18 | 18 | mA | 5.25 } V _O = 0; V _I = 0 |
| | I _{Oscmax} | 70 | 70 | 70 | mA | |
| <u>SUPPLY DATA</u> | | | | | | |
| Supply current | I _p typ. < | 21 | 21 | 21 | mA | 5.0 } All terminals open |
| | | 35 | 35 | 35 | mA | |

CHARACTERISTICS (continued)

| | | T _{amb} (°C) | | | Conditions and References | | | |
|-----------------------------------|------------------|-----------------------|----|----|---------------------------|-------------------|--------------------|-------|
| | | 0 | 25 | 70 | V _p (V) | Waveform Fig.1 | loading circuit | |
| <u>DYNAMIC DATA</u> | | | | | | | | |
| Rise propagation delay times: | | | | | | | | |
| C _n → C _{n+1} | t _{pdr} | typ. | - | 13 | - ns | 5.0 | } A | Fig.2 |
| | | < | - | 17 | - ns | 5.0 | | |
| A ₁ → A* | t _{pdr} | typ. | - | 48 | - ns | 5.0 | } A | Fig.3 |
| | | < | - | 65 | - ns | 5.0 | | |
| B ₁ → B* | t _{pdr} | typ. | - | 48 | - ns | 5.0 | } A | Fig.4 |
| | | < | - | 65 | - ns | 5.0 | | |
| BC → C _{n+1} | t _{pdr} | typ. | - | 18 | - ns | 5.0 | } B | Fig.5 |
| | | < | - | 25 | - ns | 5.0 | | |
| AC → Σ | t _{pdr} | typ. | - | 52 | - ns | 5.0 | } B | Fig.6 |
| | | < | - | 70 | - ns | 5.0 | | |
| BC → Σ* | t _{pdr} | typ. | - | 38 | - ns | 5.0 | } B | Fig.7 |
| | | < | - | 55 | - ns | 5.0 | | |
| Fall propagation delay times: | | | | | | | | |
| C _n → C _{n+1} | t _{pdf} | typ. | - | 8 | - ns | 5.0 | } A | Fig.2 |
| | | < | - | 12 | - ns | 5.0 | | |
| A ₁ → A* | t _{pdf} | typ. | - | 17 | - ns | 5.0 | } A | Fig.3 |
| | | < | - | 25 | - ns | 5.0 | | |
| B ₁ → B* | t _{pdf} | typ. | - | 17 | - ns | 5.0 | } A | Fig.4 |
| | | < | - | 25 | - ns | 5.0 | | |
| BC → C _{n+1} | t _{pdf} | typ. | - | 38 | - ns | 5.0 | } B | Fig.5 |
| | | < | - | 55 | - ns | 5.0 | | |
| AC → Σ | t _{pdf} | typ. | - | 62 | - ns | 5.0 | } B | Fig.6 |
| | | < | - | 80 | - ns | 5.0 | | |
| BC → Σ* | t _{pdf} | typ. | - | 56 | - ns | 5.0 | } B | Fig.7 |
| | | < | - | 75 | - ns | 5.0 | | |

CHARACTERISTICS (continued)

DYNAMIC DATA

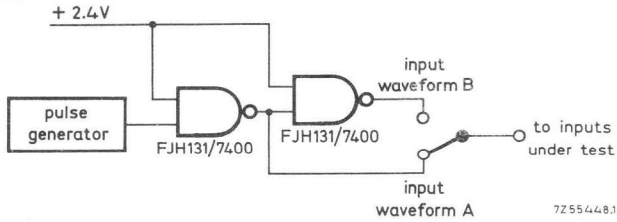


Fig. 1

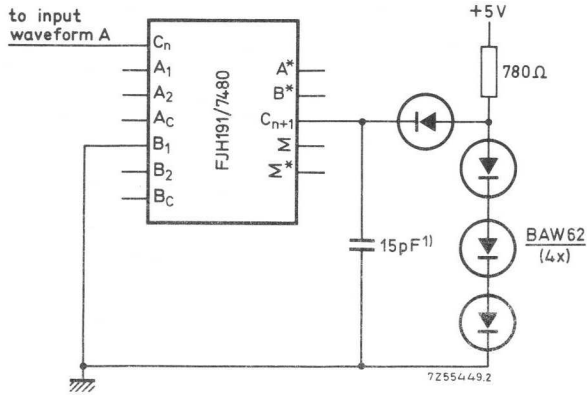


Fig. 2 Fan out: N = 5

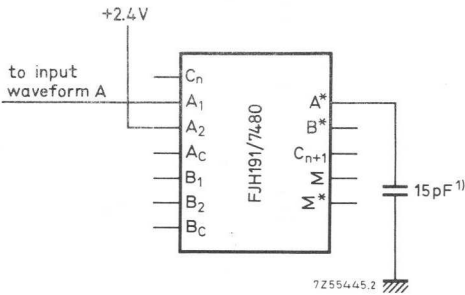


Fig. 3

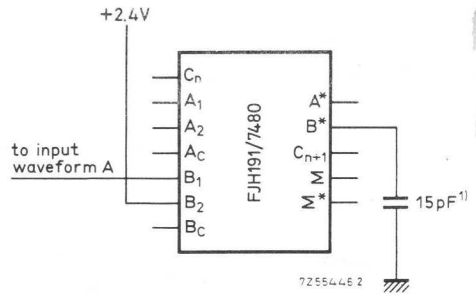


Fig. 4

1) Including probe and jig capacitance

CHARACTERISTICS (continued)

DYNAMIC DATA

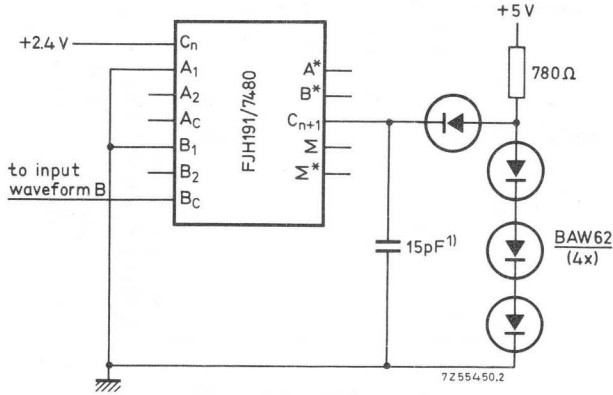


Fig.5 Fan out: N = 5

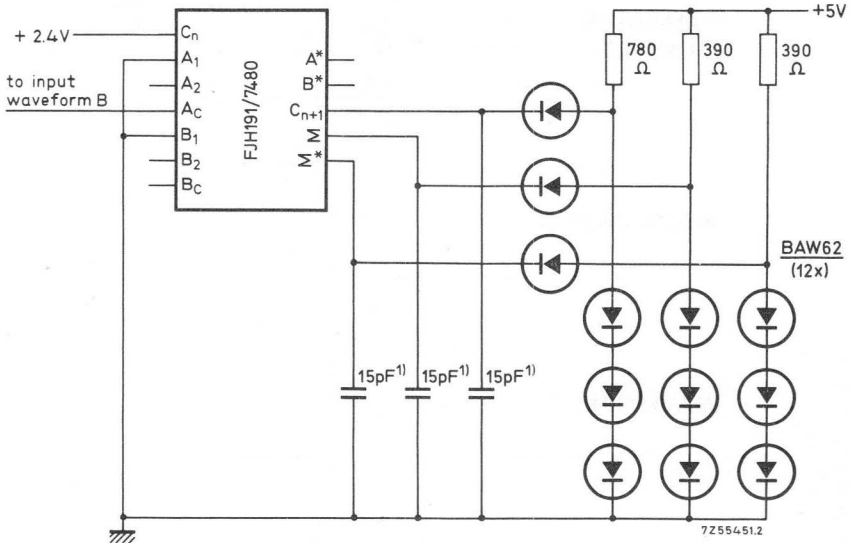


Fig.6 Fan out Q_4 : N = 10
Fan out Q_5 : N = 10
Fan out Q_3 : N = 5

1) Including probe and jig capacitance

CHARACTERISTICS (continued)

DYNAMIC DATA

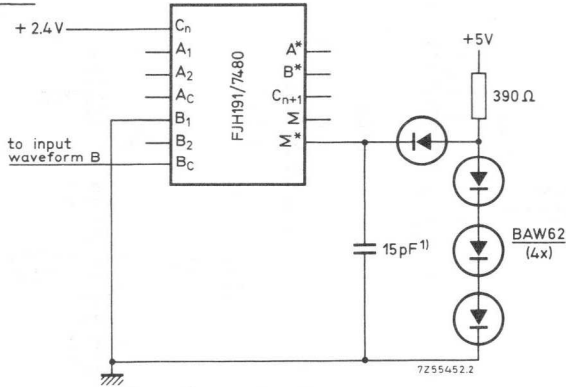
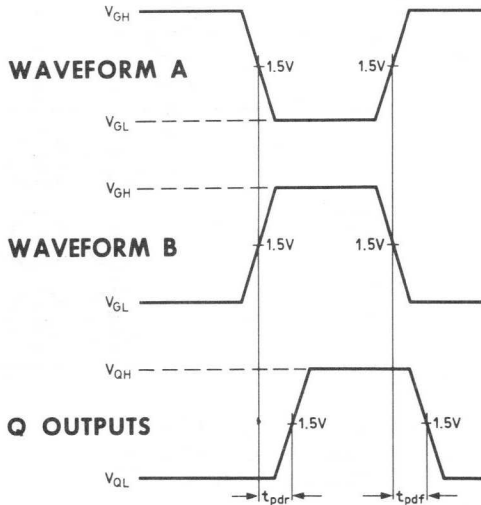
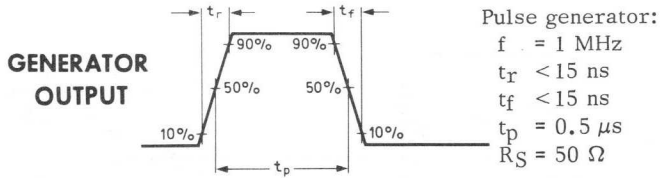


Fig.7 Fan out: N = 10

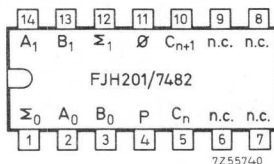
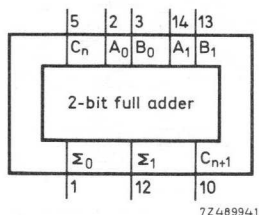


1) Including probe and jig capacitance

The FJ family TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

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2 - BIT BINARY FULL ADDER

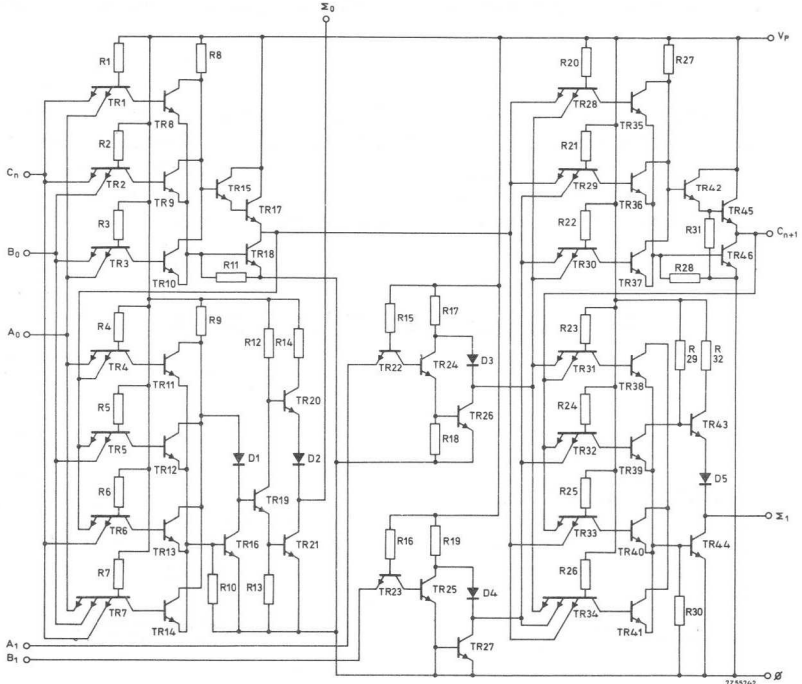


QUICK REFERENCE DATA

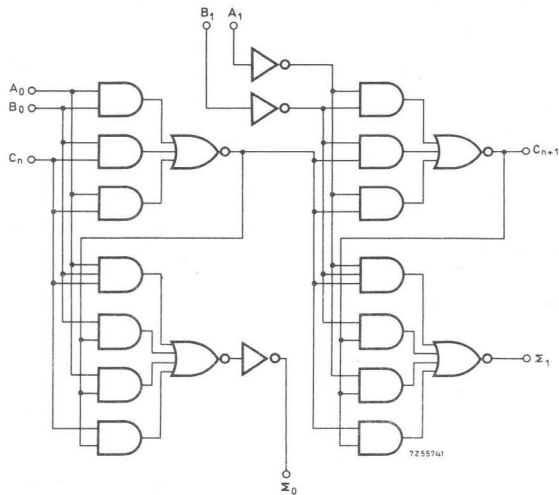
| | | | | |
|----------------------------------------------------|-----------|----------|-----|----|
| Supply voltage | V_p | 5.0 | ±5% | V |
| Operating ambient temperature | T_{amb} | 0 to +70 | | °C |
| Available d.c. fan-out | | | | |
| for outputs: Σ_0 ; Σ_1 (sum outputs) | N_a | ≥ | 10 | |
| C_{n+1} (carry output) | N_a | ≥ | 5 | |
| Average power consumption | P_{av} | | 175 | mW |

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM



The FJH201/7482 full adder is designed for medium-to-high speed, multiple-bit, parallel-add/serial-carry applications and performs the addition of two 2-bit binary numbers. The summation outputs (Σ_0 and Σ_1) are provided for each bit and the resultant carry output (C_{n+1}) is obtained from the second bit. High speed serial-carry circuitry within each bit minimises the necessity for extensive "look-ahead" and carry-cascading circuits.

| INPUT | | | | OUTPUT | | | | | |
|-------|-------|-------|-------|------------|------------|-----------|------------|------------|-----------|
| | | | | $C_n = L$ | | | $C_n = H$ | | |
| A_0 | B_0 | A_1 | B_1 | Σ_0 | Σ_1 | C_{n+1} | Σ_0 | Σ_1 | C_{n+1} |
| L | L | L | L | L | L | L | H | L | L |
| H | L | L | L | H | L | L | L | H | L |
| L | H | L | L | H | L | L | L | H | L |
| H | H | L | L | L | H | L | H | H | L |
| L | L | H | L | L | H | L | H | H | L |
| H | L | H | L | H | H | L | L | L | H |
| L | H | H | L | H | H | L | L | L | H |
| H | H | H | L | L | L | H | H | L | H |
| L | L | L | H | L | H | L | H | H | L |
| H | L | L | H | H | H | L | L | L | H |
| L | H | L | H | H | H | L | L | L | H |
| H | H | L | H | L | L | H | H | L | H |
| L | L | H | H | L | L | H | H | L | H |
| H | L | H | H | H | L | H | L | H | H |
| L | H | H | H | H | L | H | L | H | H |
| H | H | H | H | L | H | H | H | H | H |

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---------------------------------------|-----------|------|---------------------|
| Supply voltage | V_p | max. | 7.0 V |
| D. C. input voltage | V_I | max. | 5.5 V ¹⁾ |
| Peak negative transient input voltage | $-V_{IM}$ | max. | 2.0 V ²⁾ |
| Operating ambient temperature | T_{amb} | | 0 to +70 °C |
| Storage temperature | T_{stg} | | -65 to +150 °C |

1) In addition, the voltage between any two inputs must not exceed 5.5 V.

2) Pulse duration $t_p = 20$ ns; repetition frequency $f = 5$ MHz; source resistance $R_S \geq 75 \Omega$

CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and references | |
|----------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|-----------------------|-----|-----|---------------------------|------|
| | | 0 | 25 | 70 | V _p (V) | |
| <u>STATIC DATA</u> | | | | | | |
| <u>Voltages</u> | | | | | | |
| Input threshold LOW | V _{ILmax} | 0.8 | 0.8 | 0.8 | V | 4.75 |
| Input threshold HIGH | V _{IHmin} | 2.0 | 2.0 | 2.0 | V | 4.75 |
| Output LOW at Σ ₀ ; Σ ₁ at C _{n+1} | V _{OLmax} | 0.4 | 0.4 | 0.4 | V | 4.75 |
| | V _{OLmax} | 0.4 | 0.4 | 0.4 | V | 4.75 |
| Output HIGH at Σ ₀ ; Σ ₁ at C _{n+1} | V _{OHmin} | 2.4 | 2.4 | 2.4 | V | 4.75 |
| | V _{OHmin} | 2.4 | 2.4 | 2.4 | V | 4.75 |
| <u>Currents</u> | | | | | | |
| Input LOW at A ₁ ; B ₁ at A ₀ ; B ₀ ; C _n | -I _{ILmax} | 1.6 | 1.6 | 1.6 | mA | 5.25 |
| | -I _{ILmax} | 6.4 | 6.4 | 6.4 | mA | 5.25 |
| Input HIGH at A ₁ ; B ₁ at A ₀ ; B ₀ ; C _n | I _{IHmax} | 40 | 40 | 40 | μA | 5.25 |
| | I _{IHmax} | 1 | 1 | 1 | mA | 5.25 |
| | I _{IHmax} | 160 | 160 | 160 | μA | 5.25 |
| | I _{IHmax} | 1 | 1 | 1 | mA | 5.25 |
| Output LOW at Σ ₀ ; Σ ₁ at C _{n+1} | I _{OLmax} | 16 | 16 | 16 | mA | |
| | I _{OLmax} | 8 | 8 | 8 | mA | |
| Output HIGH at Σ ₀ ; Σ ₁ at C _{n+1} | -I _{OHmax} | 0.4 | 0.4 | 0.4 | mA | |
| | -I _{OHmax} | 0.2 | 0.2 | 0.2 | mA | |
| Output short circuit ¹⁾ at Σ ₀ ; Σ ₁ ; C _{n+1} at Σ ₀ ; Σ ₁ at C _{n+1} | -I _{scmin} | 18 | 18 | 18 | mA | 5.25 |
| | -I _{scmax} | 55 | 55 | 55 | mA | 5.25 |
| | -I _{scmax} | 70 | 70 | 70 | mA | 5.25 |
| <u>SUPPLY DATA</u> | | | | | | |
| Supply current | I _p typ. | 35 | 35 | 35 | mA | 5.0 |
| | I _p < | 58 | 58 | 58 | mA | 5.0 |

I_O = 16 mA
I_O = 8 mA

I_O = -400 μA
I_O = -200 μA

} V_I = 0.4 V

V_I = 2.4 V
V_I = 5.5 V
V_I = 2.4 V
V_I = 5.5 V

All terminals
open

1) Only one output to be shorted at a time

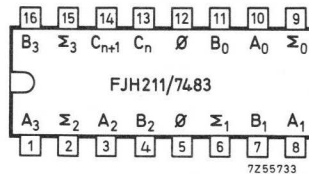
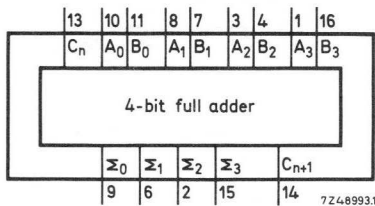
CHARACTERISTICS (continued)

| | | T _{amb} (°C) | | | Conditions and references | |
|-----------------------------------|----------------------------|-----------------------|----|------------|---------------------------|-----------------------------------------------|
| | | 0 | 25 | 70 | V _P (V) | |
| <u>DYNAMIC DATA</u> | | | | | | |
| Rise propagation delay times | | | | | | |
| C _n → Σ ₀ | t _{pdr} < | - | 34 | - ns | 5.0 | } C _L = 15 pF; N _a = 10 |
| B ₁ → Σ ₁ | t _{pdr} < | - | 40 | - ns | 5.0 | |
| C _n → Σ ₁ | t _{pdr} < | - | 38 | - ns | 5.0 | |
| C _n → C _{n+1} | t _{pdr} typ. < | - | 12 | - ns 29 | 5.0 5.0 | } C _L = 15 pF; N _a = 5 |
| Fall propagation delay times | | | | | | |
| C _n → Σ ₀ | t _{pdf} < | - | 40 | - ns | 5.0 | } C _L = 15 pF; N _a = 10 |
| B ₁ → Σ ₁ | t _{pdf} < | - | 35 | - ns | 5.0 | |
| C _n → Σ ₁ | t _{pdf} < | - | 42 | - ns | 5.0 | |
| C _n → C _{n+1} | t _{pdf} typ. < | - | 17 | - ns 27 | 5.0 5.0 | } C _L = 15 pF; N _a = 5 |

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

4 - BIT FULL ADDER

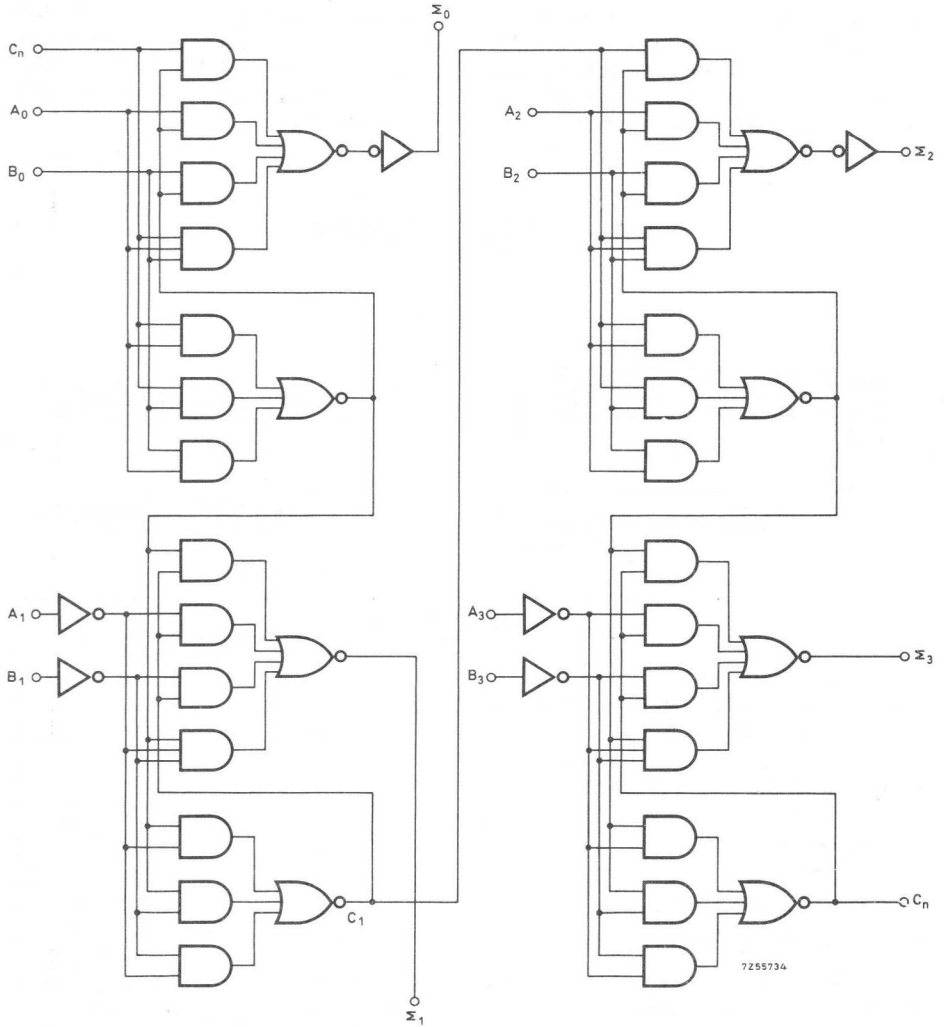


QUICK REFERENCE DATA

| | | | |
|-------------------------------------------------|-----------|---------------|-------------|
| Supply voltage | V_P | $5.0 \pm 5\%$ | V |
| Operating ambient temperature | T_{amb} | 0 to +70 | $^{\circ}C$ |
| Available d.c. fan-out (full temperature range) | | | |
| from $\Sigma_0, \Sigma_1, \Sigma_2, \Sigma_3$ | N_a | > 10 | |
| from C_{n+1} | N_a | > 5 | |
| Average propagation delay time | | | |
| $C_n \rightarrow C_{n+1}$ | t_{pd} | typ. 29 | ns |
| $C_n \rightarrow \Sigma_3$ | t_{pd} | < 55 | ns |
| $B_3 \rightarrow \Sigma_3$ | t_{pd} | < 38 | ns |
| D.C. noise margin (full temperature range) | M | > 0.4 | V |
| Average power consumption | | typ. 1.0 | V |
| $T_{amb} = 25^{\circ}C$ | P_{av} | typ. 390 | mW |

PACKAGE OUTLINE : 16 lead plastic dual in-line (type A) (See General Section)

LOGIC FUNCTION



The FJH211/7483 consists of a full adder for two words of four bits each plus a carry input (C_n). Sum outputs (Σ) are provided for each bit and the carry output (C_{n+1}) is obtained from the last bit. The high-speed internal serial carry circuitry used in the FJH211/7483 minimises the need for external "carry look ahead" logic when cascading adders for long word-length addition.

FUNCTION TABLE

To simplify the function table, it is presented in two parts:

Input conditions at A_0, A_1, B_0, B_1 and C_n determine the outputs Σ_0 and Σ_1 together with the internal carry (C_1) obtained from this addition.

Input conditions at A_2, A_3, B_2, B_3 and the internal carry C_1 determine the outputs Σ_2, Σ_3 and C_{n+1} .

| INPUT | | | | OUTPUT | | | | | |
|-------|-------|-------|-------|------------|------------|-----------|------------|------------|-----------|
| | | | | $C_n = L$ | | | $C_n = H$ | | |
| A_0 | B_0 | A_1 | B_1 | Σ_0 | Σ_1 | C_1 | Σ_0 | Σ_1 | C_1 |
| A_2 | B_2 | A_3 | B_3 | Σ_2 | Σ_3 | C_{n+1} | Σ_2 | Σ_3 | C_{n+1} |
| L | L | L | L | L | L | L | H | L | L |
| H | L | L | L | H | L | L | L | H | L |
| L | H | L | L | H | L | L | L | H | L |
| H | H | L | L | L | H | L | H | H | L |
| L | L | H | L | L | H | L | H | H | L |
| H | L | H | L | H | H | L | L | L | H |
| L | H | H | L | H | H | L | L | L | H |
| H | H | H | L | L | L | H | H | L | H |
| L | L | L | H | L | H | L | H | H | L |
| H | L | L | H | H | H | L | L | L | H |
| L | H | L | H | H | H | L | L | L | H |
| H | H | L | H | L | L | H | H | L | H |
| L | L | H | H | L | L | H | H | L | H |
| H | L | H | H | H | L | H | L | H | H |
| L | H | H | H | H | L | H | L | H | H |
| H | H | H | H | L | H | H | H | H | H |

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|-------------------------------|-----------|------|-------------|-----------------|
| Supply voltage | V_P | max. | 7.0 | V |
| Output voltage | V_O | max. | 5.5 | V |
| D. C. input voltage | V_I | max. | 5.5 | V ¹⁾ |
| Peak negative input voltage | $-V_{IM}$ | max. | 2 | V ²⁾ |
| Operating ambient temperature | T_{amb} | | 0 to +70 | °C |
| Storage temperature | T_{stg} | | -65 to +150 | °C |

CHARACTERISTICS

| | | $T_{amb}(^{\circ}C)$ | | | Conditions and references | |
|---------------------------------------------|--------------|----------------------|-----|-----|---------------------------|------|
| | | 0 | 25 | 70 | V_P (V) | |
| <u>STATIC DATA</u> | | | | | | |
| <u>Voltages</u> | | | | | | |
| Input threshold LOW | V_{ILmax} | 0.8 | 0.8 | 0.8 | V | 4.75 |
| Input threshold HIGH | V_{IHmin} | 2.0 | 2.0 | 2.0 | V | 4.75 |
| Output LOW | V_{OLmax} | 0.4 | 0.4 | 0.4 | V | 4.75 |
| at $\Sigma_0, \Sigma_1, \Sigma_2, \Sigma_3$ | | | | | | |
| at C_{n+1} | V_{OLmax} | 0.4 | 0.4 | 0.4 | V | 4.75 |
| Output HIGH | V_{OHmin} | 2.4 | 2.4 | 2.4 | V | 4.75 |
| at $\Sigma_0, \Sigma_1, \Sigma_2, \Sigma_3$ | | | | | | |
| at C_{n+1} | V_{OHmin} | 2.4 | 2.4 | 2.4 | V | 4.75 |
| <u>Currents</u> | | | | | | |
| Input LOW | | | | | | |
| at A_0, A_2, B_0, B_2, C_n | $-I_{ILmax}$ | 6.4 | 6.4 | 6.4 | mA | 5.25 |
| at A_1, A_3, B_1, B_3 | $-I_{ILmax}$ | 1.6 | 1.6 | 1.6 | mA | 5.25 |
| } $V_I = 0.4$ V | | | | | | |
| Input HIGH | | | | | | |
| at A_0, A_2, B_0, B_2, C_n | I_{IHmax} | 160 | 160 | 160 | μA | 5.25 |
| at A_1, A_3, B_1, B_3 | I_{IHmax} | 40 | 40 | 40 | μA | 5.25 |
| at all inputs | I_{IHmax} | 1 | 1 | 1 | mA | 5.25 |
| } $V_I = 2.4$ V | | | | | | |
| } $V_I = 5.5$ V | | | | | | |
| Output LOW | | | | | | |
| at $\Sigma_0, \Sigma_1, \Sigma_2, \Sigma_3$ | I_{OLmax} | 16 | 16 | 16 | mA | |
| at C_{n+1} | I_{OLmax} | 8 | 8 | 8 | mA | |

1) In addition, the voltage between any two inputs max. 5.5 V

2) Pulse duration $t_p = 20$ ns; repetition frequency $f = 5$ MHz; source resistance $R_S \geq 75 \Omega$

CHARACTERISTICS (continued)

| | | T _{amb} (°C) | | | Conditions and references | |
|----------------------------------------------------------------------------------------------------------------|----------------------|-----------------------|-----|-----|---------------------------|------|
| | | | | | V _P (V) | |
| | | 0 | 25 | 70 | | |
| <u>STATIC DATA</u> | | | | | | |
| Output HIGH at $\Sigma_0; \Sigma_1; \Sigma_2; \Sigma_3$ at C _{n+1} | -I _{OHmax} | 400 | 400 | 400 | μA | |
| | -I _{OHmax} | 200 | 200 | 200 | μA | |
| Output short-circuited 1) all outputs at $\Sigma_0; \Sigma_1; \Sigma_2; \Sigma_3$ at C _{n+1} | -I _{scmin} | 18 | 18 | 18 | mA | 5.25 |
| | -I _{scmax} | 55 | 55 | 55 | mA | 5.25 |
| | -I _{scmax} | 70 | 70 | 70 | mA | 5.25 |
| | | | | | | |
| <u>SUPPLY DATA</u> | | | | | | |
| Supply current | I _p typ | - | 78 | - | mA | 5.0 |
| | I _p < | 128 | 128 | 128 | mA | 5.25 |
| <u>DYNAMIC DATA</u> | | | | | | |
| Rise propagation delay time | | | | | | |
| C _n → Σ_0 | t _{pdr} < | - | 34 | - | ns | 5.0 |
| C _n → Σ_1 | t _{pdr} < | - | 38 | - | ns | 5.0 |
| C _n → Σ_2 | t _{pdr} < | - | 50 | - | ns | 5.0 |
| C _n → Σ_3 | t _{pdr} < | - | 55 | - | ns | 5.0 |
| C _n → C _{n+1} | t _{pdr} typ | - | 35 | - | ns | 5.0 |
| | t _{pdr} < | - | 48 | - | ns | 5.0 |
| A ₁ ; B ₁ → Σ_1 | t _{pdr} < | - | 40 | - | ns | 5.0 |
| A ₃ ; B ₃ → Σ_3 | t _{pdr} < | - | 40 | - | ns | 5.0 |
| Fall propagation delay time | | | | | | |
| C _n → Σ_0 | t _{pdf} < | - | 40 | - | ns | 5.0 |
| C _n → Σ_1 | t _{pdf} < | - | 42 | - | ns | 5.0 |
| C _n → Σ_2 | t _{pdf} < | - | 60 | - | ns | 5.0 |
| C _n → Σ_3 | t _{pdf} < | - | 55 | - | ns | 5.0 |
| C _n → C _{n+1} | t _{pdf} typ | - | 22 | - | ns | 5.0 |
| | t _{pdf} < | - | 32 | - | ns | 5.0 |
| A ₁ ; B ₁ → Σ_1 | t _{pdf} < | - | 35 | - | ns | 5.0 |
| A ₃ ; B ₃ → Σ_3 | t _{pdf} < | - | 35 | - | ns | 5.0 |



1) Not more than one output must be shorted at a time

1871

FJ family

standard temperature range

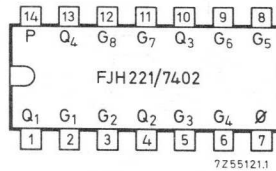
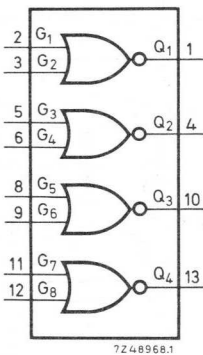
FJH221/7402

2-input NOR gate

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

QUADRUPLE 2-INPUT NOR GATE

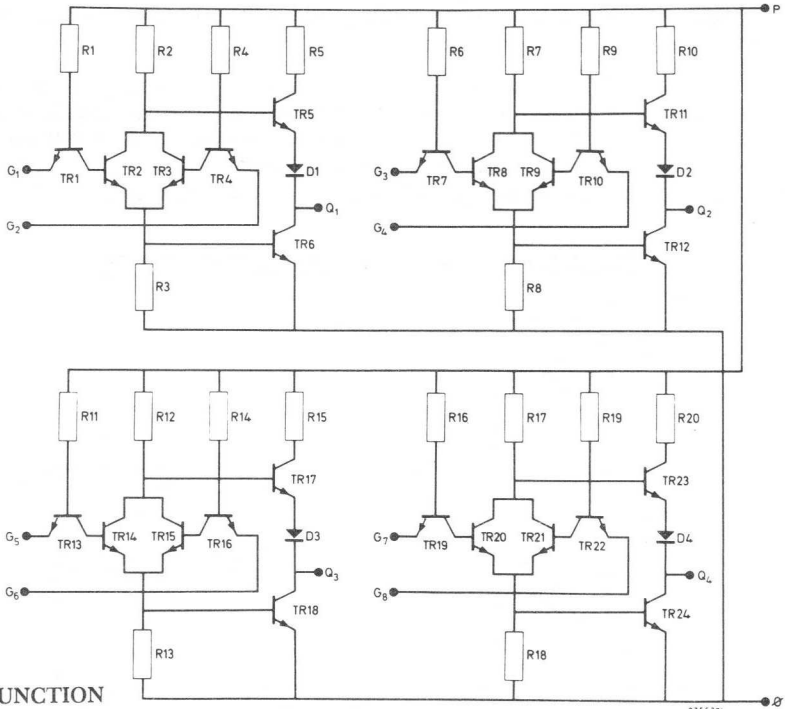


QUICK REFERENCE DATA

| | | | |
|-----------------------------------------------------------------------|-----------|---------------|-------|
| Supply voltage | V_P | $5.0 \pm 5\%$ | V |
| Operating ambient temperature | T_{amb} | 0 to +70 | °C |
| Average propagation delay time N = fan-out = 10; $T_{amb} = 25$ °C | t_{pd} | typ. 10 | ns |
| Available d.c. fan-out (full temperature range) | N_a | \geq | 10 |
| D.C. noise margin (full temperature range) | M_L | $>$ | 0.4 V |
| Average power consumption (per gate) $T_{amb} = 25$ °C | P_{av} | typ. 14.25 | mW |

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



LOGIC FUNCTION

$$Q_1 = \overline{G_1 + G_2}$$

$$Q_2 = \overline{G_3 + G_4}$$

$$Q_3 = \overline{G_5 + G_6}$$

$$Q_4 = \overline{G_7 + G_8}$$

} for positive logic

Function table

| G ₁ ;G ₃ G ₅ ;G ₇ | G ₂ ;G ₄ G ₆ ;G ₈ | Q ₁ ;Q ₂ Q ₃ ;Q ₄ |
|------------------------------------------------------------------|------------------------------------------------------------------|------------------------------------------------------------------|
| L | L | H |
| L | H | L |
| H | L | L |
| H | H | L |

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134)

| | | | |
|-------------------------------|------------------|------|---------------------|
| Supply voltage | V _P | max. | 7.0 V |
| Output voltage | V _Q | max. | 5.5 V |
| G input voltage | V _G | max. | 5.5 V ¹⁾ |
| Peak negative G input voltage | -V _{GM} | max. | 2 V ²⁾ |
| Storage temperature | T _{stg} | | -55 to +150 °C |
| Operating ambient temperature | T _{amb} | | 0 to +70 °C |

¹⁾ In addition, the voltage between any two inputs must not exceed 5.5 V.

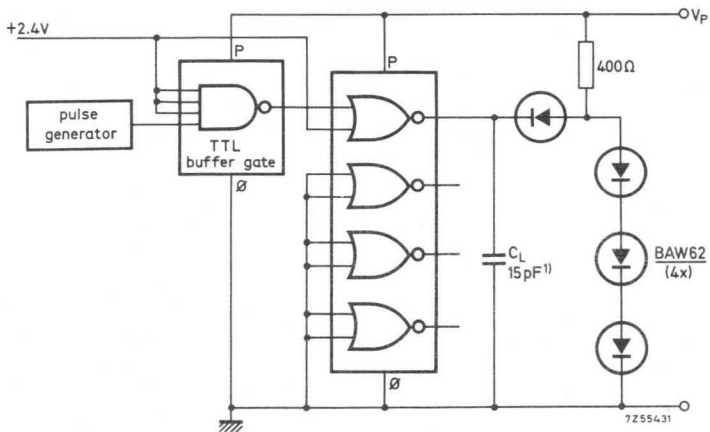
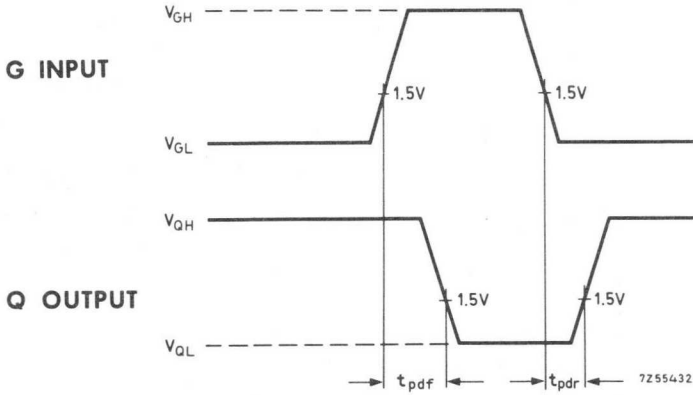
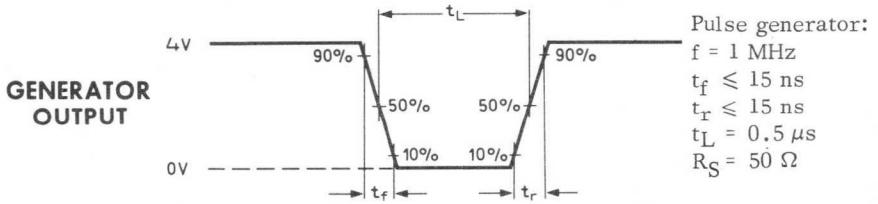
²⁾ Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance R_S ≥ 75 Ω.

CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and references | | | |
|-----------------------------|-----------------------|-----------------------|------|------|---------------------------|-----------------------------------------------------------------------------------|--------------------------------------------------------------------|--------------------------------------------|
| | | 0 | 25 | 70 | V _P (V) | | | |
| <u>STATIC DATA</u> | | | | | | | | |
| <u>Voltages</u> | | | | | | | | |
| Input threshold LOW | V _{GLmax} | 0.8 | 0.8 | 0.8 | V | | | |
| Input threshold HIGH | V _{GHmin} | 2.0 | 2.0 | 2.0 | V | | | |
| Output LOW | V _{QLmax} | 0.4 | 0.4 | 0.4 | V | 4.75 I _Q =I _{QLmax} V _G =V _{GHmin} | | |
| Output HIGH | V _{QHmin} | 2.4 | 2.4 | 2.4 | V | 4.75 -I _Q =-I _{QHmax} ; V _G =V _{GLmax} | | |
| <u>Currents</u> | | | | | | | | |
| Input LOW | -I _{GLmax} | 1.6 | 1.6 | 1.6 | mA | 5.25 V _G =V _{QLmax} ; I _Q =0 | | |
| Input HIGH | I _{GHmax} | 40 | 40 | 40 | μA | 5.25 V _G =V _{QHmin} ; I _Q =0 other inputs 0 V | | |
| Output LOW | I _{QLmax} | 16 | 16 | 16 | mA | | | |
| Output HIGH | -I _{QHmax} | 0.4 | 0.4 | 0.4 | mA | | | |
| Output short-circuited | -I _{Qsc min} | 18 | 18 | 18 | mA | 5.25 V _Q =0; V _G =0 | | |
| | -I _{Qsc max} | 55 | 55 | 55 | mA | | | |
| <u>SUPPLY DATA</u> | | | | | | | | |
| <u>Supply current</u> | | | | | | | | |
| Output LOW | I _{PL} | typ. | 14.8 | 14.8 | 14.8 | mA | 5.0 } V _G =5.0 V; I _Q =0 | |
| | | < | 27 | 27 | 27 | mA | | 5.0 |
| Output HIGH | I _{PH} | typ. | 8.0 | 8.0 | 8.0 | mA | | 5.0 } V _G =0; I _Q =0 |
| | | < | 16 | 16 | 16 | mA | | |
| <u>DYNAMIC DATA</u> | | | | | | | | |
| Rise propagation delay time | t _{pdr} | typ. | - | 12 | - | ns | 5.0 } N = 10 one pair AND inputs at V _G =0.4 V | |
| | | < | - | 22 | - | ns | | 5.0 |
| Fall propagation delay time | t _{pdf} | typ. | - | 8 | - | ns | | 5.0 |
| | | < | - | 15 | - | ns | | |

CHARACTERISTICS (continued)

DYNAMIC DATA

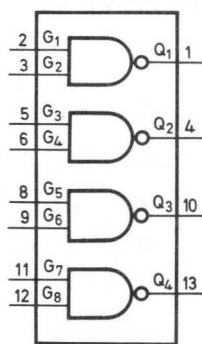


¹⁾ Including probe and jig capacitance

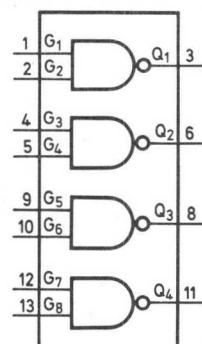
The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

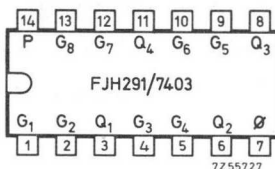
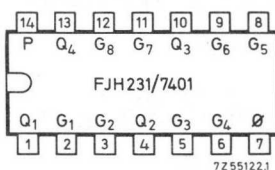
QUADRUPLE 2-INPUT NAND GATE



FJH231/7401



FJH291/7403



QUICK REFERENCE DATA

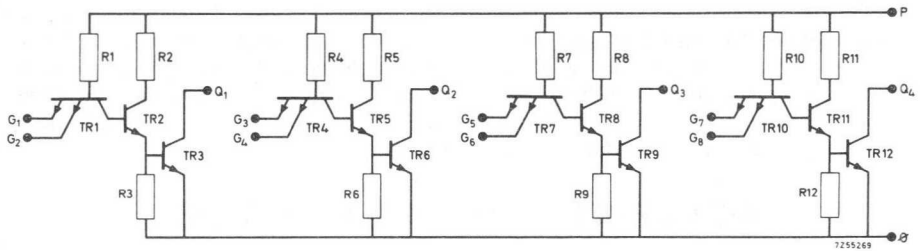
| | | | |
|----------------------------------------------------------------------------------|-----------|---------------|---------------------|
| Supply voltage | V_P | $5.0 \pm 5\%$ | V |
| Operating ambient temperature | T_{amb} | 0 to +70 | °C |
| Average propagation delay time N = fan-out = 10; $T_{amb} = 25^\circ\text{C}$ | t_{pd} | typ. 22 | ns |
| Available d. c. fan-out (full temperature range) | N_a | \geq | 10 |
| D. C. noise margin (full temperature range) | M_L | $>$ | 0.4 V typ. 1.0 V |
| Average power consumption (each gate) $T_{amb} = 25^\circ\text{C}$ | P_{av} | typ. 7.5 | mW |

The FJH231/7401 and FJH291/7403 are quadruple 2-input NAND gates with open-collector output transistors for use in "wired-OR" connection with other gates of the FJ family.

The FJH291/7403 is pin-compatible with the FJH131/7400 NAND gate.

PACKAGE OUTLINE 14 lead plastic dual in-line (type A) (See general Section)

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|------------------------------------------------------------------|-----------|------|---------------------|
| Supply voltage | V_P | max. | 7.0 V |
| D. C. output voltage (applied through $R_L \geq 270 \Omega$) | V_Q | max. | 7.0 V |
| G input voltage | V_G | max. | 5.5 V ¹⁾ |
| Peak negative G input voltage | $-V_{GM}$ | max. | 2 V ²⁾ |
| Storage temperature | T_{stg} | | -55 to +150 °C |
| Operating ambient temperature | T_{amb} | | 0 to +70 °C |

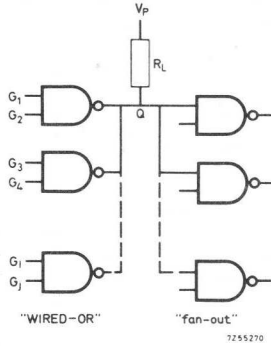
¹⁾ In addition, the voltage between any two inputs must not exceed 5.5 V.

²⁾ Pulse duration $t_p = 20$ ms; repetition frequency $f = 5$ MHz; source resistance $R_S \geq 75 \Omega$.

Fan-out and the "wired-OR" function

TTL gates with open collector can be connected to a common load resistor (R_L) to give a wired-OR function.

A gate alone will drive 10 TTL loads; when it is paralleled with other gates, it can drive from 1 to 9 loads.



To find the proper value of R_L , see application information on page 6.

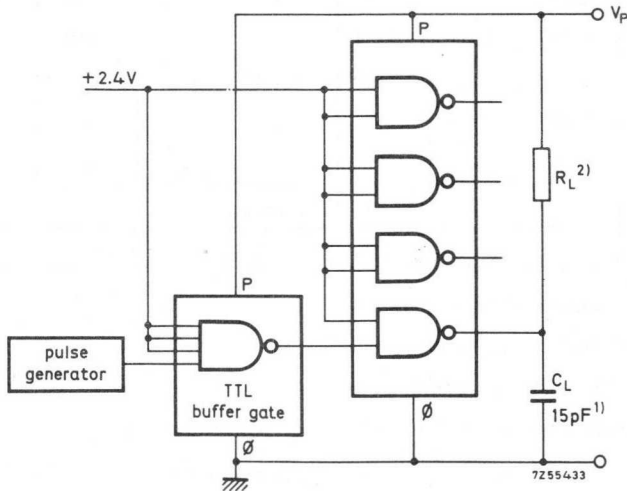
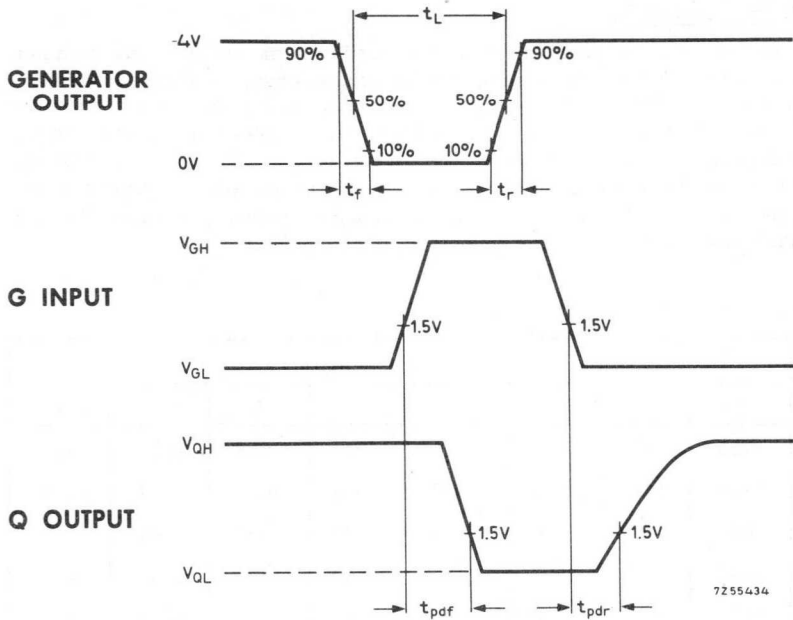
Wired-OR logic function (positive logic)

$$Q = \bar{G}_1 \cdot \bar{G}_2 + \bar{G}_3 \cdot \bar{G}_4 + \dots + \bar{G}_i \cdot \bar{G}_j$$

CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and references | |
|-----------------------------|----------------------------|-----------------------|-----|-----|---------------------------|-------------------------------------------------------------------------------------|
| | | 0 | 25 | 70 | V _P (V) | |
| <u>STATIC DATA</u> | | | | | | |
| <u>Voltages</u> | | | | | | |
| Input threshold LOW | V _{GLmax} | 0.8 | 0.8 | 0.8 | V | |
| Input threshold HIGH | V _{GHmin} | 2.0 | 2.0 | 2.0 | V | |
| Output LOW | V _{QLmax} | 0.4 | 0.4 | 0.4 | V | 4.75 I _Q = I _{QLmax} ; V _G = V _{GHmin} |
| Output HIGH | V _{QHmin} | 2.4 | 2.4 | 2.4 | V | 4.75 -I _Q = -I _{QHmax} ; V _G = V _{GLmax} |
| <u>Currents</u> | | | | | | |
| Input LOW | -I _{GLmax} | 1.6 | 1.6 | 1.6 | mA | 5.25 V _G = V _{QLmax} ; I _Q = 0 |
| Input HIGH | I _{GHmax} | 40 | 40 | 40 | μA | 5.25 V _G = V _{QHmin} ; I _Q = 0 other inputs 0 V |
| Output LOW | I _{QLmax} | 16 | 16 | 16 | mA | |
| Output HIGH(reverse) | I _{QHmax} | 250 | 250 | 250 | μA | 4.75 V _G = V _{GLmax} V _Q = 5.5 V |
| <u>SUPPLY DATA</u> | | | | | | |
| <u>Supply current</u> | | | | | | |
| Output LOW | I _{PL} typ. < | 12 | 12 | 12 | mA | 5.0 } V _G = 5.0 V; I _Q = 0 |
| | | 22 | 22 | 22 | mA | |
| Output HIGH | I _{PH} typ. < | 4.0 | 4.0 | 4.0 | mA | 5.0 } V _G = 0; I _Q = 0 |
| | | 8 | 8 | 8 | mA | |
| <u>DYNAMIC DATA</u> | | | | | | |
| Rise propagation delay time | t _{pdr} typ. < | - | 35 | - | ns | 5.0 } R _L = 3.9 kΩ; C _L = 15 pF |
| | | - | 45 | - | ns | |
| Fall propagation delay time | t _{pdf} typ. < | - | 8 | - | ns | 5.0 } R _L = 390 Ω; C _L = 15 pF |
| | | - | 15 | - | ns | |

CHARACTERISTICS (continued)



¹⁾ Including probe and jig capacitance

²⁾ $R_L = 390 \Omega$ for t_{pdf}
 $R_L = 3900 \Omega$ for t_{pdr}

APPLICATION INFORMATION

Determining the value of R_L

Proper operation of the functions mentioned depends on the value of the common load resistor. The maximum value is set by the need to ensure sufficient load current to TTL loads and off current I_{QHmax} through paralleled outputs when the output is HIGH. A minimum value is set by the need to limit the total current through the resistor, including the "sink" current of the TTL loads, so that the output voltage does not rise above the LOW level, even when one of the paralleled outputs is absorbing all the current. The table shows minimum and maximum resistor values for up to 10 TTL loads and up to 7 gates connected in wired-OR.

Table I

| fan-out to TTL loads | wired-OR outputs | | | | | | | | |
|------------------------------|------------------|------|------|------|------|------|------|--------|------|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 1 to 7 | |
| 1 | 8965 | 4814 | 3291 | 2500 | 2015 | 1688 | 1452 | 319 | |
| 2 | 7878 | 4482 | 3132 | 2407 | 1954 | 1645 | 1420 | 359 | |
| 3 | 7027 | 4193 | 2988 | 2321 | 1897 | 1604 | 1390 | 410 | |
| 4 | 6341 | 3939 | 2857 | 2241 | 1843 | 1566 | 1361 | 479 | |
| 5 | 5777 | 3714 | 2736 | 2166 | 1793 | 1529 | 1333 | 575 | |
| 6 | 5306 | 3513 | 2626 | 2096 | 1744 | 1494 | 1306 | 718 | |
| 7 | 4905 | 3333 | 2524 | 2031 | 1699 | 1460 | 1280 | 958 | |
| 8 | 4561 | 3170 | 2429 | 1969 | 1656 | X | X | 1437 | |
| 9 | 4262 | 3023 | X | X | X | X | X | 2875 | |
| 10 | 4000 | X | X | X | X | X | X | 4000* | |
| | maximum | | | | | | | | min. |
| load resistor values in ohms | | | | | | | | | |

X = not recommended or not possible

* = the thoretical value is ∞

All values shown in the table are based on:

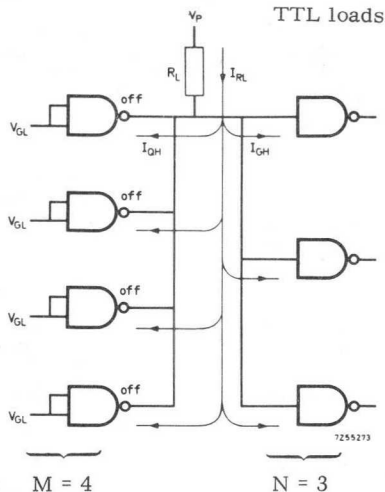
Logical HIGH conditions: $V_P = 5\text{ V}$; V_{QH} required = 2.4 V

Logical LOW conditions: $V_P = 5\text{ V}$; V_{QL} required = 0.4 V

APPLICATION INFORMATION (continued)

Circuit calculations

HIGH (off level) configurations (see figure below)



$$M \cdot I_{QH} = 4 \times 250 \mu A \quad N \cdot I_{GH} = 3 \times 40 \mu A \quad R_{Lmax} = \frac{(5 - 2.4)V}{(0.001 + 0.00012)A} = 2321 \Omega$$

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_p applied and the output voltage V_{QH} required at the TTL load.

$$V_{RL} = V_p - V_{QHmin}$$

The total current through the load resistor (I_{RL}) is the sum of the load currents I_{GH} and off-level reverse current I_{QH} through each of the "wired-OR" connected outputs. Putting N as the number of TTL loads, and M as the number of outputs, the current is given by

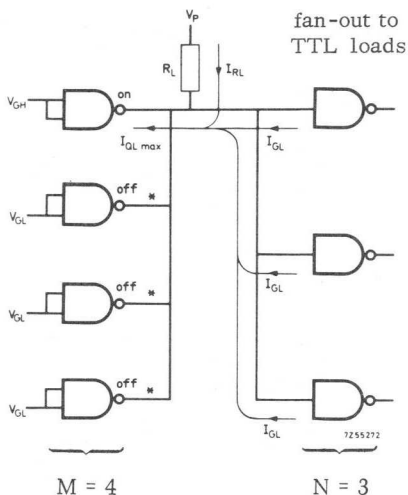
$$I_{RL} = M \cdot I_{QH} + N \cdot I_{GH}$$

Therefore, the maximum value of R_L is

$$R_{Lmax} = \frac{V_p - V_{QHmin}}{M \cdot I_{QH} + N \cdot I_{GH}}$$

APPLICATION INFORMATION (continued)

LOW (on level) configurations (see figure below)



$$I_{QLmax} = 16 \text{ mA} \quad N \cdot |I_{GLmax}| = 3 \times 1.6 \text{ mA} \quad R_{Lmin} = \frac{(5 - 0.4)V}{(0.016 - 0.0048)A} = 410 \Omega$$

* current through OFF outputs negligible at LOW output state

The current through the resistor must be limited to the maximum for one output transistor. If several outputs are "wired-OR" connected the current through R_L may be shared among the paralleled output transistors, but, unless it can be guaranteed that more than one transistor will be in the ON(= conducting) state during the LOW output periods, the current must be limited to 16 mA, i.e. the maximum current that will still ensure a maximum LOW output voltage of 0.4 V.

The fan-out current must be considered as well. Part of the 16 mA will be supplied from the inputs being driven, which further reduces the current through R_L .

These considerations lead to the minimum value of R_L

$$R_{Lmin} = \frac{V_P - V_{QLmax}}{I_{QLmax} - N \cdot |I_{GLmax}|}$$

For up to 10 TTL loads and up to 7 "wired-OR" connected outputs table I gives the maximum and minimum values of R_L calculated in this way.

For a single output the values are determined by the fan-out plus the leakage current of one transistor.

More than 7 outputs can be connected in "wired-OR" provided valid maximum and minimum resistor values are possible.

The value of R_L for driving 10 loads should be infinite according to these calculations but 4 k Ω is sufficient to satisfy logic HIGH while keeping logic LOW to less than 0.43 V.

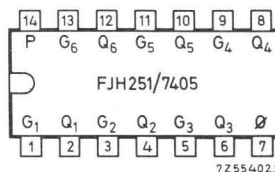
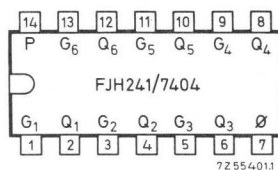
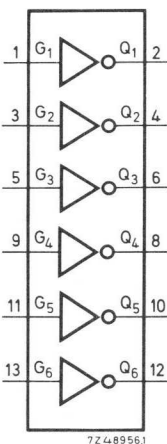
The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

SEXTUPLE SINGLE INPUT INVERTERS

Sextuple single input inverter with an active output (totem pole): FJH241/7404

Sextuple single input inverter with an open collector output: FJH251/7405



QUICK REFERENCE DATA

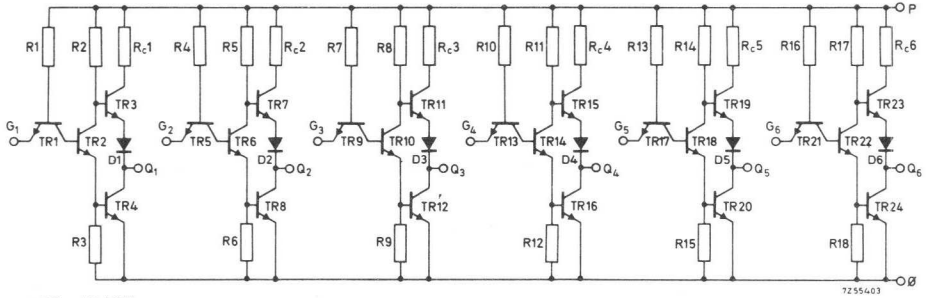
| | | |
|------------------------------------------------------------------------------------------|------------------------------------------------|--------------------------|
| Supply voltage | V_P | $5.0 \pm 5\%$ V |
| Operating ambient temperature | T_{amb} | 0 to +70 °C |
| Average propagation delay time N = fan-out = 10; $T_{amb} = 25\text{ °C}$ | FJH241/7404: t_{pd} FJH251/7405: t_{pd} | typ. 10 ns typ. 24 ns |
| Available d. c. fan-out; full temperature range (for FJH251/7405 see table on page 5) | N_a | < 10 |
| D. C. noise margin (full temperature range) | M_L | > 0.4 V typ. 1.0 V |
| Average power consumption (each gate) $T_{amb} = 25\text{ °C}$ | P_{av} | typ. 10 mW |

The FJH241/7404 is a sextuple single-input inverter with an active output (totem pole). The FJH251/7405 is a sextuple single-input inverter with an open collector output transistor. It can be used in wired-OR connections with other gates of the FJ family.

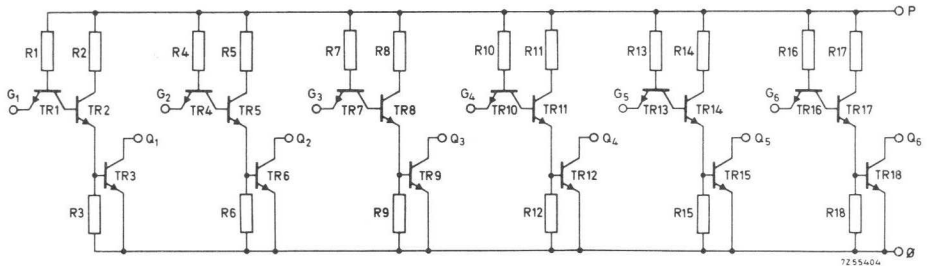
PACKAGE OUTLINE : 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAMS

FJH241/7404



FJH251/7405



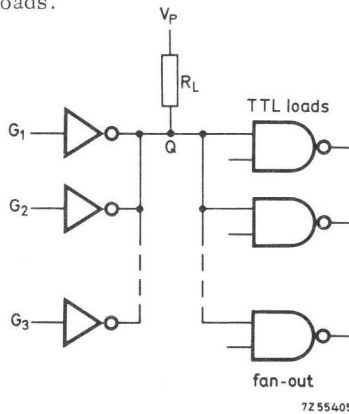
RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|-------------------------------|-----------|------|-------------|-----------------|
| Supply voltage | V_P | max. | 7.0 | V |
| G input voltage | V_G | max. | 5.5 | V |
| Peak negative G input voltage | $-V_{GM}$ | max. | 2 | V ¹⁾ |
| Storage temperature | T_{stg} | | -55 to +150 | °C |
| Operating ambient temperature | T_{amb} | | 0 to +70 | °C |

Fan-out and "wired-OR" function of FJH251/7405

TTL inverters with open collector can be connected to a common load resistor (R_L) to give a wired-OR function.

An inverter **alone** will drive 10 TTL loads; when it is paralleled with other inverters it can drive from 1 to 9 TTL loads.



To find the proper value of R_L see application information on page 5.

Wired-OR logic function (positive logic)

$$Q = \overline{G_1 + G_2 + \dots + G_i}$$

¹⁾ Pulse duration $t_p = 20$ ns; repetition frequency $f = 5$ MHz; source resistance $R_S \geq 75 \Omega$.

CHARACTERISTICS

| | | T _{amb} (°C) 0 25 75 | | | Conditions and References | |
|-------------------------------------------------------|---------------------------------------------|----------------------------------|-----|--------|---------------------------|-----------------------------------------------------------------------------|
| | | | | | V _P (V) | |
| <u>STATIC DATA</u> | | | | | | |
| <u>Voltages</u> | | | | | | |
| Input threshold LOW | V _{GLmax} | 0.8 | 0.8 | 0.8 V | | |
| Input threshold HIGH | V _{GHmin} | 2.0 | 2.0 | 2.0 V | | |
| Output LOW | V _{QLmax} | 0.4 | 0.4 | 0.4 V | 4.75 | I _Q = I _{QLmax} ; V _G = V _{GHmin} |
| Output HIGH | V _{QHmin} | 2.4 | 2.4 | 2.4 V | 4.75 | -I _Q = -I _{QHmax} ; V _G = V _{GLmax} |
| <u>Currents</u> | | | | | | |
| Input LOW | -I _{GLmax} | 1.6 | 1.6 | 1.6 mA | 5.25 | V _G = V _{QLmax} ; I _Q = 0 |
| Input HIGH | I _{GHmax} | 40 | 40 | 40 μA | 5.25 | V _G = V _{QHmin} ; I _Q = 0 |
| Output LOW | I _{QLmax} | 16 | 16 | 16 mA | | |
| Output HIGH FJH241/7404 | -I _{QHmax} | 400 | 400 | 400 μA | 4.75 | V _Q = V _{QHmin} |
| Output reverse HIGH; FJH251/7405 | I _{QHmax} | 250 | 250 | 250 μA | 4.75 | V _G = V _{GLmax} ; V _Q = 5.5 V |
| Output short circuit- ed FJH241/7404 See note 1 | -I _{Qscmin} | 18 | 18 | 18 mA | 5.25 | } V _G = 0; V _Q = 0 |
| | -I _{Qscmax} | 55 | 55 | 55 mA | 5.25 | |
| <u>SUPPLY DATA</u> | | | | | | |
| Output LOW | I _{PL} typ. < | 18 | 18 | 18 mA | 5.0 | } V _G = 5 V; I _Q = 0 |
| | | 33 | 33 | 33 mA | 5.0 | |
| Output HIGH | I _{PH} typ. < | 6 | 6 | 6 mA | 5.0 | } V _G = 0; I _Q = 0 |
| | | 12 | 12 | 12 mA | 5.0 | |
| <u>DYNAMIC DATA</u> | | | | | | |
| Rise propagation delay time: FJH241/7404 | t _{pdr} typ. t _{pdr} < | - | 12 | - ns | 5.0 | } R _L = 390 Ω; C _L = 15 pF |
| | | - | 22 | - ns | 5.0 | |
| FJH251/7405 | t _{pdr} typ. t _{pdr} < | - | 40 | - ns | 5.0 | |
| | | - | 55 | - ns | 5.0 | |
| Fall propagation delay time | t _{pdf} typ. t _{pdf} < | - | 8 | - ns | 5.0 | } R _L = 390 Ω; C _L = 15 pF |
| | | - | 15 | - ns | 5.0 | |

Note 1: Not more than one output should be short circuited at a time

APPLICATION INFORMATION for FJH251/7405

Determining the value of R_L

Proper operation of the functions mentioned depends on the value of the common load resistor. The maximum value is set by the need to ensure sufficient load current to TTL loads and off current I_{QHmax} through paralleled outputs when the output is HIGH. A minimum value is set by the need to limit the total current through the resistor, including the "sink" current of the TTL loads, so that the output voltage does not rise above the LOW level, even when one of the paralleled outputs is absorbing all the current. The table shows minimum and maximum resistor values for up to 10 TTL loads and up to 7 gates connected in wired-OR.

Table I

| fan-out to TTL loads | wired-OR outputs | | | | | | | |
|------------------------------|------------------|------|------|------|------|------|------|--------|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 1 to 7 |
| 1 | 8965 | 4814 | 3291 | 2500 | 2015 | 1688 | 1452 | 319 |
| 2 | 7878 | 4482 | 3132 | 2407 | 1954 | 1645 | 1420 | 359 |
| 3 | 7027 | 4193 | 2988 | 2321 | 1897 | 1604 | 1390 | 410 |
| 4 | 6341 | 3939 | 2857 | 2241 | 1843 | 1566 | 1361 | 479 |
| 5 | 5777 | 3714 | 2736 | 2166 | 1793 | 1529 | 1333 | 575 |
| 6 | 5306 | 3513 | 2626 | 2096 | 1744 | 1494 | 1306 | 718 |
| 7 | 4905 | 3333 | 2524 | 2031 | 1699 | 1460 | 1280 | 958 |
| 8 | 4561 | 3170 | 2429 | 1969 | 1656 | X | X | 1437 |
| 9 | 4262 | 3023 | X | X | X | X | X | 2875 |
| 10 | 4000 | X | X | X | X | X | X | 4000* |
| maximum | | | | | | | | min. |
| load resistor values in ohms | | | | | | | | |

X = not recommended or not possible

* = the theoretical value is ∞

All values shown in the table are based on:

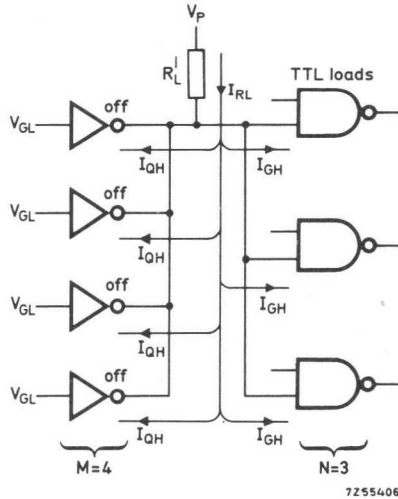
Logical HIGH conditions: $V_P = 5\text{ V}$; V_{QH} required = 2.4 V

Logical LOW conditions: $V_P = 5\text{ V}$; V_{QL} required = 0.4 V

APPLICATION INFORMATION (continued)

Circuit calculations

HIGH (off level) configurations (see figure below)



$$M \cdot I_{QH} = 4 \times 250 \mu A \quad N \cdot I_{GH} = 3 \times 40 \mu A \quad R_{Lmax} = \frac{(5-2.4)V}{(0.001 + 0.00012)A} = 2321 \Omega$$

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_P applied and the output voltage V_{QH} required at the TTL load.

$$V_{RL} = V_P - V_{QHmin}$$

The total current through the load resistor (I_{RL}) is the sum of the load currents I_{GH} and off-level reverse current I_{QH} through each of the "wired-OR" connected outputs. Putting N as the number of TTL loads, and M as the number of outputs, the current is given by

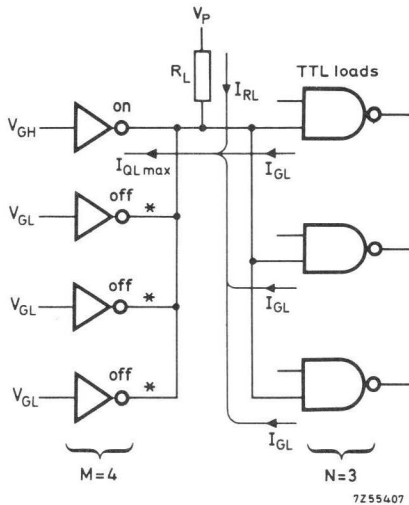
$$I_{RL} = M \cdot I_{QH} + N \cdot I_{GH}$$

Therefore, the maximum value of R_L is

$$R_{Lmax} = \frac{V_P - V_{QHmin}}{M \cdot I_{QH} + N \cdot I_{GH}}$$

APPLICATION INFORMATION (continued)

LOW (on level) configurations (see figure below)



$$I_{QLmax} = 16 \text{ mA} \quad N \cdot |I_{GLmax}| = 3 \times 1.6 \text{ mA} \quad R_{Lmin} = \frac{(5-0.4)V}{(0.016-0.0048)A} = 410 \Omega$$

*current through OFF outputs negligible at LOW output state

The current through the resistor must be limited to the maximum for one output transistor. If several outputs are "wired-OR" connected the current through \$R_L\$ may be shared among the paralleled output transistor, but, unless it can be guaranteed that more than one transistor will be in the ON-(= conducting) state during the LOW output periods, the current must be limited to 16 mA, i.e. the maximum current that will still ensure a maximum LOW output voltage of 0.4 V.

The fan-out current must be considered as well. Part of the 16 mA will be supplied from the inputs being driven, which further reduces the current through \$R_L\$;

These considerations lead to the minimum value of \$R_L\$

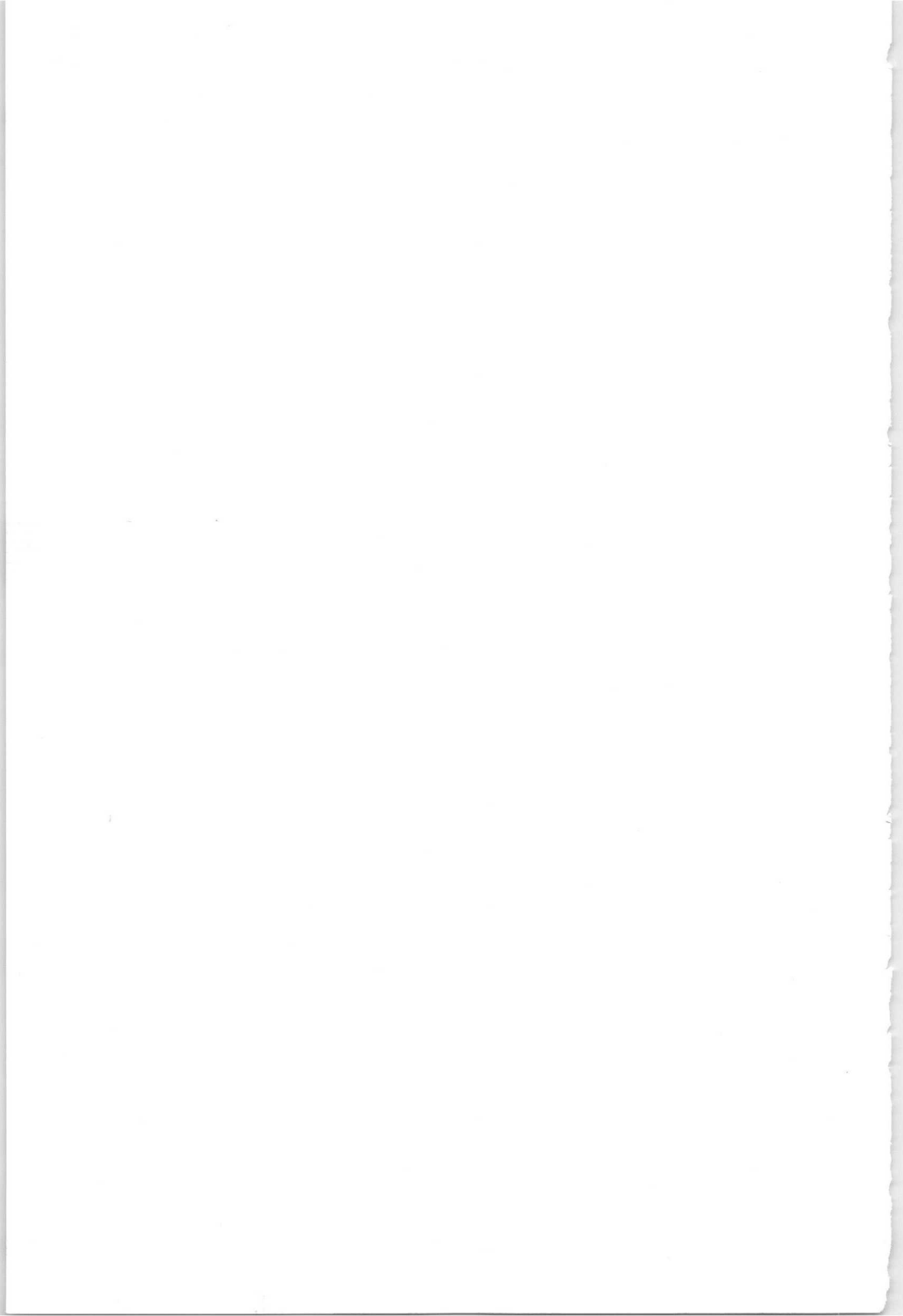
$$R_{Lmin} = \frac{V_P - V_{QLmax}}{I_{QLmax} - N \cdot |I_{GLmax}|}$$

For up to 10 TTL loads and up to 7 "wired-OR" connected outputs table I gives the maximum and minimum values of \$R_L\$ calculated in this way.

For a single output the values are determined by the fan-out plus the leakage current of one transistor.

More than 7 outputs can be connected in "wired-OR" provided valid maximum and minimum resistor values are possible.

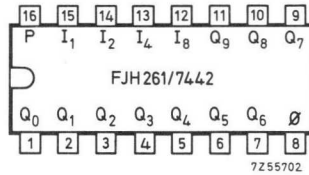
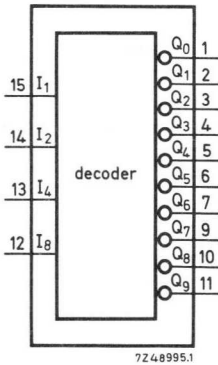
The value of \$R_L\$ for driving 10 loads should be infinite according to these calculations but 4 kΩ is sufficient to satisfy logic HIGH while keeping logic LOW to less than 0.43 V.



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BCD-to-DECIMAL DECODER



QUICK REFERENCE DATA

| | | | |
|---------------------------------------|------------------|----------|--------|
| Supply voltage | V _P | 5 ± 5% | V |
| Operating ambient temperature | T _{amb} | 0 to +70 | °C |
| Available d. c. fan-out (each output) | N _a | ≥ | 10 |
| Average propagation delay | t _{pd} | typ. | 20 ns |
| Average power consumption | P _{av} | typ. | 140 mW |

PACKAGE OUTLINE 16 lead plastic dual in-line (type A) (See General Section)

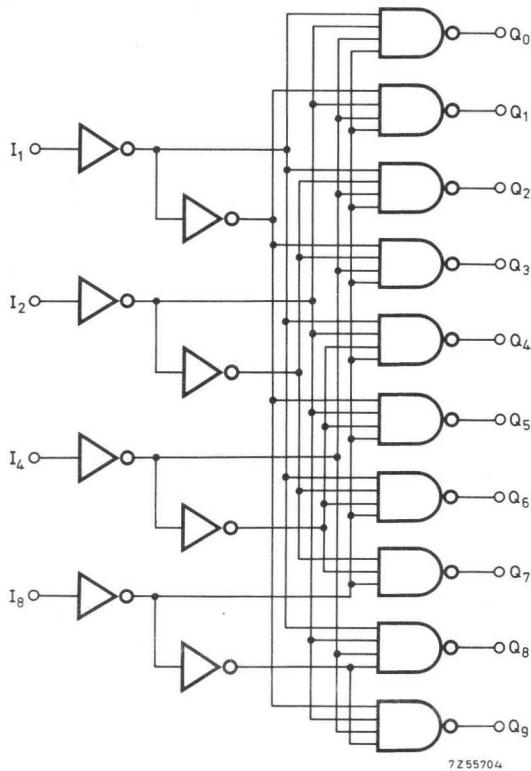
GENERAL DESCRIPTION

The FJH261/7442 is a multipurpose decoder which accepts four BCD (8-4-2-1 code) inputs and provides ten mutually exclusive outputs.

The active LOW outputs facilitate addressing functions when inverting drivers are used. Full decoding of valid input logic ensures that all outputs remain HIGH (off) for input binary codes greater than nine.

The most significant input (I_8) provides a useful inhibit function when the FJH261/7442 is used as a 1-of-8 decoder, as shown in the APPLICATION INFORMATION section on page 6.

LOGIC DIAGRAM



FUNCTION TABLE

| inputs | | | | outputs | | | | | | | | | |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| I ₈ | I ₄ | I ₂ | I ₁ | Q ₀ | Q ₁ | Q ₂ | Q ₃ | Q ₄ | Q ₅ | Q ₆ | Q ₇ | Q ₈ | Q ₉ |
| L | L | L | L | L | H | H | H | H | H | H | H | H | H |
| L | L | L | H | H | L | H | H | H | H | H | H | H | H |
| L | L | H | L | H | H | L | H | H | H | H | H | H | H |
| L | L | H | H | H | H | H | L | H | H | H | H | H | H |
| L | H | L | L | H | H | H | H | L | H | H | H | H | H |
| L | H | L | H | H | H | H | H | H | L | H | H | H | H |
| L | H | H | L | H | H | H | H | H | H | L | H | H | H |
| L | H | H | H | H | H | H | H | H | H | H | L | H | H |
| H | L | L | L | H | H | H | H | H | H | H | H | L | H |
| H | L | L | H | H | H | H | H | H | H | H | H | H | L |
| H | L | H | L | H | H | H | H | H | H | H | H | H | H |
| H | L | H | H | H | H | H | H | H | H | H | H | H | H |
| H | H | L | L | H | H | H | H | H | H | H | H | H | H |
| H | H | L | H | H | H | H | H | H | H | H | H | H | H |
| H | H | H | L | H | H | H | H | H | H | H | H | H | H |
| H | H | H | H | H | H | H | H | H | H | H | H | H | H |

H = HIGH (the more positive voltage)

L = LOW (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|------------------------------------------------------------------------------------------|-----------|------|---------------------|
| Supply voltage | V_P | max. | 7 V |
| Input voltage (d. c.) | V_I | max. | 5.5 V ¹⁾ |
| Negative transient input voltage ($t_p = 20$ ns; $f = 5$ MHz, $R_S \geq 75 \Omega$) | $-V_{IM}$ | max. | 2 V |
| Operating ambient temperature | T_{amb} | | 0 to +70 °C |
| Storage temperature | T_{stg} | | -65 to +150 °C |

¹⁾ In addition, the voltage between any two inputs must not exceed 5.5 V.

CHARACTERISTICS

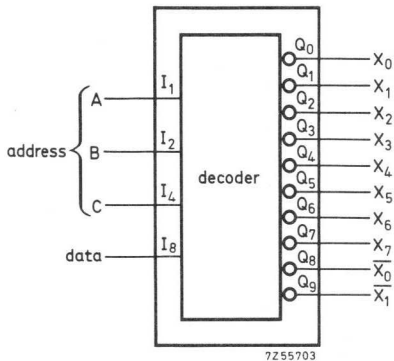
| | | T _{amb} (°C) | | | Conditions and references | |
|----------------------------------------------------------------|-----------------------|-----------------------|-----|-----|---------------------------|------|
| | | 0 | 25 | 70 | V _P (V) | |
| <u>STATIC DATA</u> | | | | | | |
| <u>Voltages</u> | | | | | | |
| Input threshold LOW | V _{ILmax} | 0.8 | 0.8 | 0.8 | V | 4.75 |
| Input threshold HIGH | V _{IHmin} | 2.0 | 2.0 | 2.0 | V | 4.75 |
| Output LOW | V _{QLmax} | 0.4 | 0.4 | 0.4 | V | 4.75 |
| Output HIGH | V _{QHmin} | 2.4 | 2.4 | 2.4 | V | 4.75 |
| <u>Currents</u> | | | | | | |
| Input LOW (each input) | -I _{ILmax} | 1.6 | 1.6 | 1.6 | mA | 5.25 |
| Input HIGH (each input) | I _{IHmax} | 40 | 40 | 40 | μA | 5.25 |
| | I _{IHmax} | 1 | 1 | 1 | mA | 5.25 |
| Output LOW | I _{QLmax} | 16 | 16 | 16 | mA | |
| Output short circuited ¹⁾ | -I _{Qsc min} | 18 | 18 | 18 | mA | 5.25 |
| | -I _{Qsc max} | 55 | 55 | 55 | mA | 5.25 |
| <u>SUPPLY DATA</u> | | | | | | |
| Supply current | I _{P typ.} | -- | 28 | - | mA | 5.0 |
| | I _{P ≤} | 56 | 56 | 56 | mA | 5.25 |
| } V _I = 0 V | | | | | | |
| <u>DYNAMIC DATA</u> | | | | | | |
| <u>Propagation delay times</u> | | min. typ. max. | | | | |
| Rise: through two logic levels | t _{pdr} | 10 | 17 | 25 | ns | 5.0 |
| through three logic levels | t _{pdr} | - | 26 | 35 | ns | 5.0 |
| Fall: through two logic levels | t _{pdf} | 10 | 22 | 30 | ns | 5.0 |
| through three logic levels | t _{pdf} | - | 23 | 35 | ns | 5.0 |
| } C _L = 15 pF N = 10 T _{amb} = 25 °C | | | | | | |

¹⁾ Only one output to be shorted at a time.

APPLICATION INFORMATION

Digital demultiplexer

Data may be routed from a single source to any of 8 outputs by addressing that output. All other outputs remain HIGH. Complements of outputs Q_0 and Q_1 are available at Q_8 and Q_9 respectively.

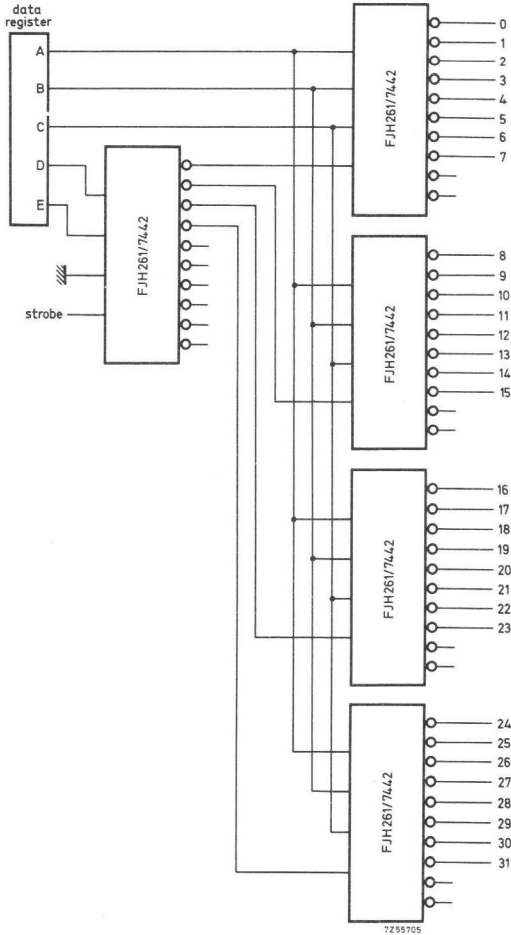


| address | | | output |
|---------|---|---|--------|
| A | B | C | line |
| L | L | L | X_0 |
| H | L | L | X_1 |
| L | H | L | X_2 |
| H | H | L | X_3 |
| L | L | H | X_4 |
| H | L | H | X_5 |
| L | H | H | X_6 |
| H | H | H | X_7 |

APPLICATION INFORMATION (continued)

1-of-32 decoding

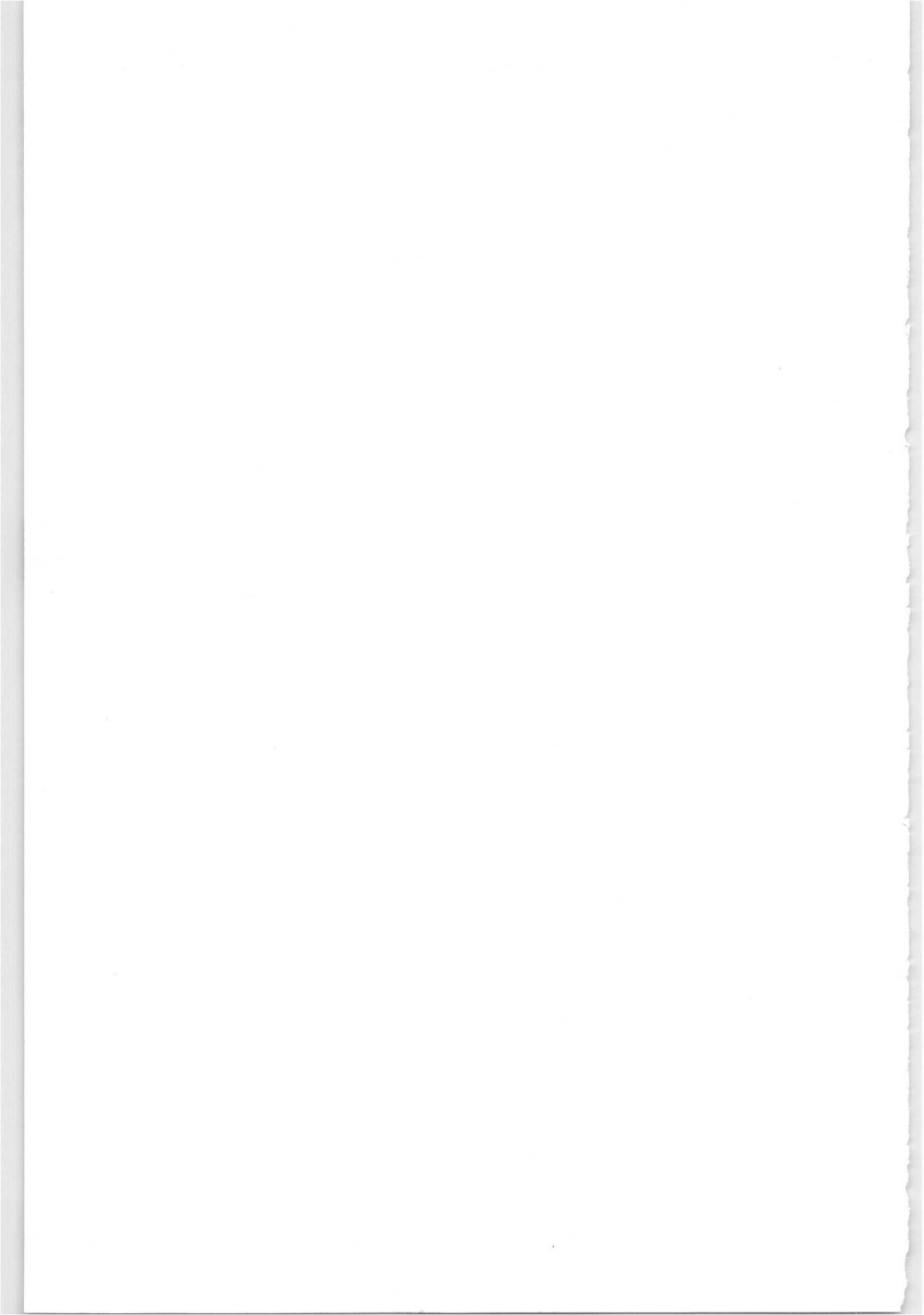
The general purpose nature of the FJH261/7442 is shown by this application, where the most significant input (I₈) is used as an inhibit in the four 1-of-8 decoders.



QUADRUPLE 2-INPUT NAND GATE

For data of this type please refer to FJH231/7401





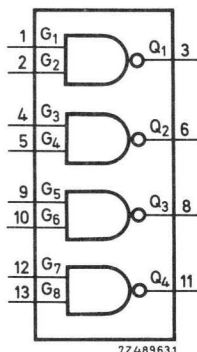
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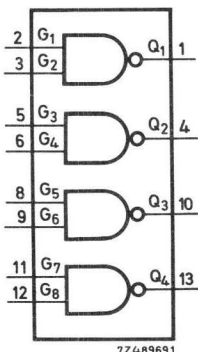
NAND GATES

Quadruple 2-input NAND gate, with open collector
 Quadruple 2-input NAND gate, with open collector
 Sextuple single input inverter, with open collector

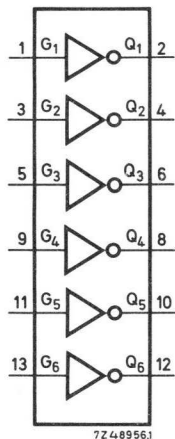
FJH301/7426
 FJH311/7401-S1
 FJH321/7405-S1



FJH301/7426



FJH311/7401-S1



FJH321/7405-S1

QUICK REFERENCE DATA

| | | | |
|-------------------------------------------------------|------------------|----------|-------|
| Supply voltage | V _P | 5.0 ± 5% | V |
| Operating ambient temperature | T _{amb} | 0 to +70 | °C |
| Output voltage | V _Q | max. | 15 V |
| Average propagation delay | t _{pd} | max. | 22 ns |
| N = fan-out = 10; T _{amb} = 25 °C | N _a | ≥ | 10 |
| Available d. c. fan-out (full temperature range) | M _L | > | 0.4 V |
| D. C. noise margin (full temperature range) | | typ. | 1.0 V |
| Average power consumption at T _{amb} = 25 °C | P _{av} | typ. | 10 mW |

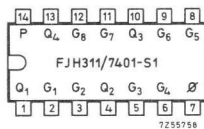
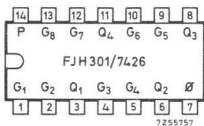
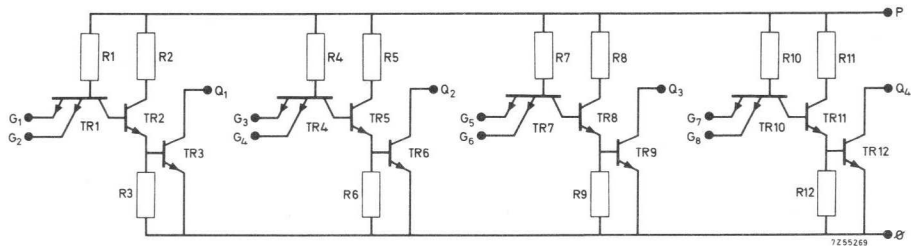
PACKAGE OUTLINE : 14 lead plastic dual in-line (type A) See General Section

FJH301/7426
FJH311/7401-S1
FJH321/7405-S1

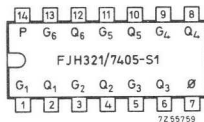
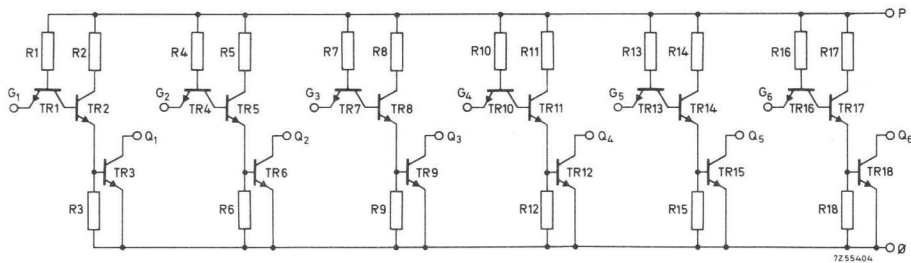
FJ family
 standard temperature range

CIRCUIT DIAGRAMS

FJH301/7426 and FJH311/7401-S1



FJH321/7405-S1



This series of open-collector NAND gates features 15 V output voltage ratings and is intended to be used for interfacing with MOS logic or as open-collector drivers for indicator lamps and relays.

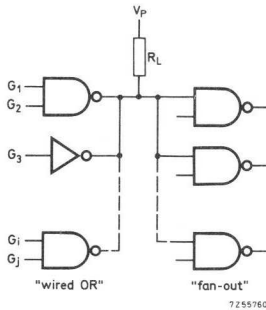
RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|-------------------------------|-----------|------|-------------|-----------------|
| Supply voltage | V_P | max. | 7.0 | V |
| D. C. output voltage | V_Q | max. | 15 | V |
| D. C. input voltage | V_G | max. | 5.5 | V ¹⁾ |
| Peak negative input voltage | $-V_{GM}$ | max. | 2 | V ²⁾ |
| Storage temperature | T_{stg} | | -65 to +150 | °C |
| Operating ambient temperature | T_{amb} | | 0 to +70 | °C |

Fan-out and the "wired-OR" function

TTL gates with open collector can be connected to a common load resistor (R_L) to give a wired-OR function.

A gate alone will drive 10 TTL loads; when it is paralleled with other gates, it can drive from 1 to 9 loads.



To find the proper value of R_L , see application information on page 6.

Wired-OR logic function (positive logic)

$$Q = G_1 \cdot G_2 + G_3 + \dots + G_i \cdot G_j$$

1) In addition, the voltage between any two inputs must not exceed 5.5 V

2) Pulse duration $t_p = 20$ ns; repetition frequency $f = 5$ MHz; source resistance $R_S \geq 75 \Omega$

CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and References | | |
|------------------------------|---------------------|-----------------------|-----|-----|---------------------------|--------------------------------------------------------------------------------|------------------------------------------------------|
| | | 0 | 25 | 70 | V _p (V) | | |
| <u>STATIC DATA</u> | | | | | | | |
| <u>Voltages</u> | | | | | | | |
| Input threshold LOW | V _{GLmax} | 0.8 | 0.8 | 0.8 | V | | |
| Input threshold HIGH | V _{GHmin} | 2.0 | 2.0 | 2.0 | V | | |
| Output LOW | V _{GLmax} | 0.4 | 0.4 | 0.4 | V | 4.75 I _Q = I _{QLmax} ; V _G = V _{GHmin} | |
| Output HIGH | V _{QHmin} | 15 | 15 | 15 | V | 4.75 -I _Q = 1 mA; V _G = V _{GLmax} | |
| <u>Currents</u> | | | | | | | |
| Input LOW | -I _{GLmax} | 1.6 | 1.6 | 1.6 | mA | 5.25 V _G = V _{QLmax} ; I _Q = 0 | |
| Input HIGH | I _{GHmax} | 40 | 40 | 40 | μA | 5.25 V _G = 2.4 V; I _Q = 0 | |
| Output LOW | I _{QLmax} | 16 | 16 | 16 | mA | | |
| Output reverse HIGH | I _{QHmax} | 50 | 50 | 50 | μA | 4.75 { V _G = V _{GLmax} ; V _Q = 12 V | |
| <u>SUPPLY DATA</u> | | | | | | | |
| <u>Supply current</u> | | | | | | | |
| Output LOW | I _{PL} | typ. | - | 12 | - | mA | 5.0 } V _G = 5 V; I _Q = 0 |
| | | < | - | 22 | - | mA | |
| Output HIGH | I _{PH} | typ. | - | 4 | - | mA | 5.0 } V _G = 0; I _Q = 0 |
| | | < | - | 8 | - | mA | |
| <u>DYNAMIC DATA</u> | | | | | | | |
| Rise propagation delay time: | t _{pdr} | typ. | - | 35 | - | ns | 5.0 } R _L = 390 Ω; C _L = 15 pF |
| | | < | - | 45 | - | ns | |
| Fall propagation delay time: | t _{pdf} | typ. | - | 8 | - | ns | 5.0 } R _L = 390 Ω; C _L = 15 pF |
| | | < | - | 15 | - | ns | |

APPLICATION INFORMATION

Determining the value of R_L

Proper operation of the functions mentioned depends on the value of the common load resistor. The maximum value is set by the need to ensure sufficient load current to TTL loads and off current I_{QHmax} through paralleled outputs when the output is HIGH. A minimum value is set by the need to limit the total current through the resistor, including the "sink" current of the TTL loads, so that the output voltage does not rise above the LOW level, even when one of the paralleled outputs is absorbing all the current. The table shows minimum and maximum resistor values for up to 10 TTL loads and up to 7 gates connected in wired-OR.

Table 1

| fan-out to TTL loads | wired-OR outputs | | | | | | | |
|------------------------------|------------------|------|------|------|------|------|------|--------|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 1 to 7 |
| 1 | 8965 | 4814 | 3291 | 2500 | 2015 | 1688 | 1452 | 319 |
| 2 | 7878 | 4482 | 3132 | 2407 | 1954 | 1645 | 1420 | 359 |
| 3 | 7027 | 4193 | 2988 | 2321 | 1897 | 1604 | 1390 | 410 |
| 4 | 6341 | 3939 | 2857 | 2241 | 1843 | 1566 | 1361 | 479 |
| 5 | 5777 | 3714 | 2736 | 2166 | 1793 | 1529 | 1333 | 575 |
| 6 | 5306 | 3513 | 2626 | 2096 | 1744 | 1494 | 1306 | 718 |
| 7 | 4905 | 3333 | 2524 | 2031 | 1699 | 1460 | 1280 | 958 |
| 8 | 4561 | 3170 | 2429 | 1969 | 1656 | X | X | 1437 |
| 9 | 4262 | 3023 | X | X | X | X | X | 2875 |
| 10 | 4000 | X | X | X | X | X | X | 4000* |
| maximum | | | | | | | | min. |
| load resistor values in ohms | | | | | | | | |

X = not recommended or not possible

* = the theoretical value is ∞

All values shown in the table are based on:

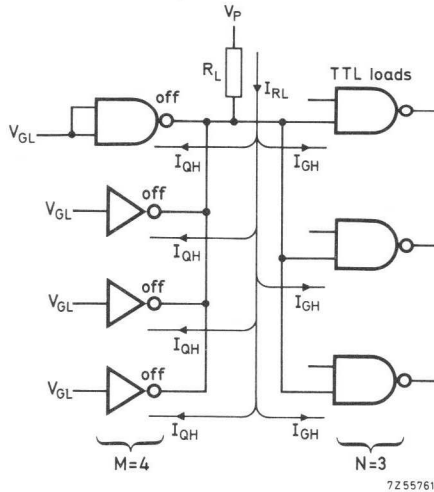
Logical HIGH conditions: $V_p = 5\text{ V}$; V_{QH} required = 2.4 V

Logical LOW conditions: $V_p = 5\text{ V}$; V_{QL} required = 0.4 V

APPLICATION INFORMATION (continued)

Circuit calculations

HIGH (off level) configurations (see figure below)



$$M \cdot I_{QH} = 4 \times 250 \mu A \quad N \cdot I_{GH} = 3 \times 40 \mu A \quad R_{Lmax} = \frac{(5 - 2.4)V}{(0.001 + 0.00012)A} = 2321 \Omega$$

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_P applied and the output voltage V_{QH} required at the TTL load.

$$V_{RL} = V_P - V_{QHmin}$$

The total current through the load resistor (I_{RL}) is the sum of the load currents I_{GH} and off-level reverse current I_{QH} through each of the "wired-OR" connected outputs. Putting N as the number of TTL loads, and M as the number of outputs, the current is given by

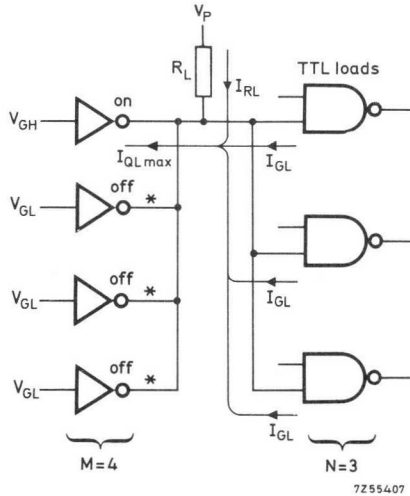
$$I_{RL} = M \cdot I_{QH} + N \cdot I_{GH}$$

Therefore, the maximum value of R_L is

$$R_{Lmax} = \frac{V_P - V_{QHmin}}{M \cdot I_{QH} + N \cdot I_{GH}}$$

APPLICATION INFORMATION (continued)

LOW (on level) configurations (see figure below)



$$I_{QLmax} = 16 \text{ mA} \quad N \cdot |I_{GLmax}| = 3 \times 1.6 \text{ mA} \quad R_{Lmin} = \frac{(5 - 0.4)V}{(0.016 - 0.0048)A} = 410 \Omega$$

*current through OFF outputs negligible at LOW output state

The current through the resistor must be limited to the maximum for one output transistor. If several outputs are "wired-OR" connected the current through R_L may be shared among the paralleled output transistor, but, unless it can be guaranteed that more than one transistor will be in the ON-(= conducting) state during the LOW output periods, the current must be limited to 16 mA, i.e. the maximum current that will still ensure a maximum LOW output voltage of 0.4 V.

The fan-out current must be considered as well. Part of the 16 mA will be supplied from the inputs being driven, which further reduces the current through R_L ;

These considerations lead to the minimum value of R_L

$$R_{Lmin} = \frac{V_P - V_{QLmax}}{I_{QLmax} - N \cdot |I_{GLmax}|}$$

For up to 10 TTL loads and up to 7 "wired-OR" connected outputs table I gives the maximum and minimum values of R_L calculated in this way.

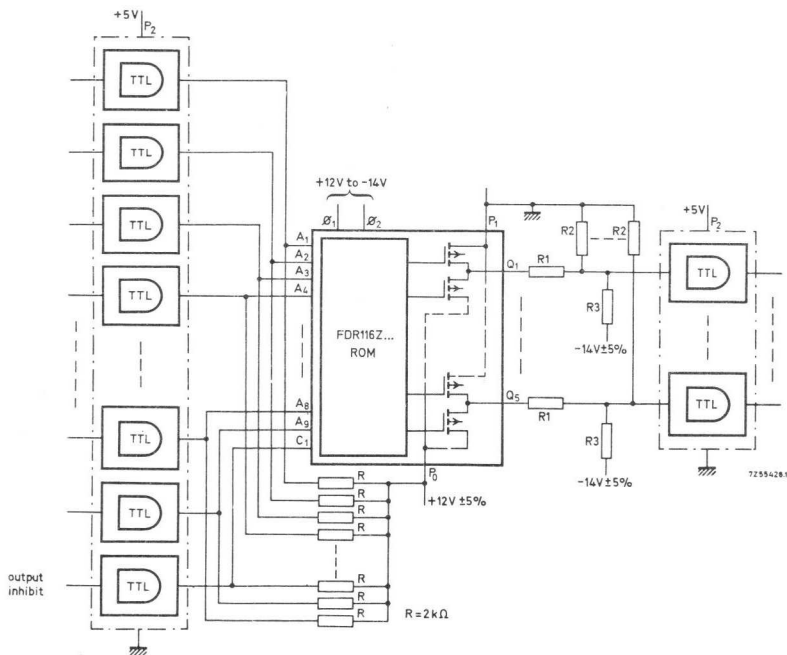
For a single output the values are determined by the fan-out plus the leakage current of one transistor.

More than 7 outputs can be connected in "wired-OR" provided valid maximum and minimum resistor values are possible.

The value of R_L for driving 10 loads should be infinite according to these calculations but 4 k Ω is sufficient to satisfy logic HIGH while keeping logic LOW to less than 0.43 V.

APPLICATION INFORMATION (continued)

Typical application of open-collector gates as interface with MOS circuit.



The example above shows a FDR116Z 2560-bit read-only memory being used together with TTL.

Open-collector gates are used at the input interface, each collector being taken through a 2 kΩ resistor to the 12V positive supply voltage of the FDR116Z. A normal totem-pole output FJ type is used as the output to restore the TTL logic levels.

FJ family

standard temperature range

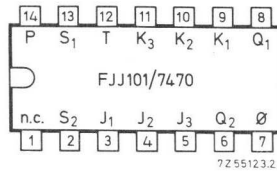
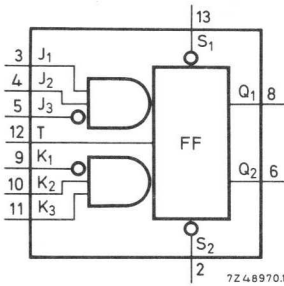
FJJ101/7470

JK flip-flop

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

SINGLE JK FLIP-FLOP (AND INPUTS)



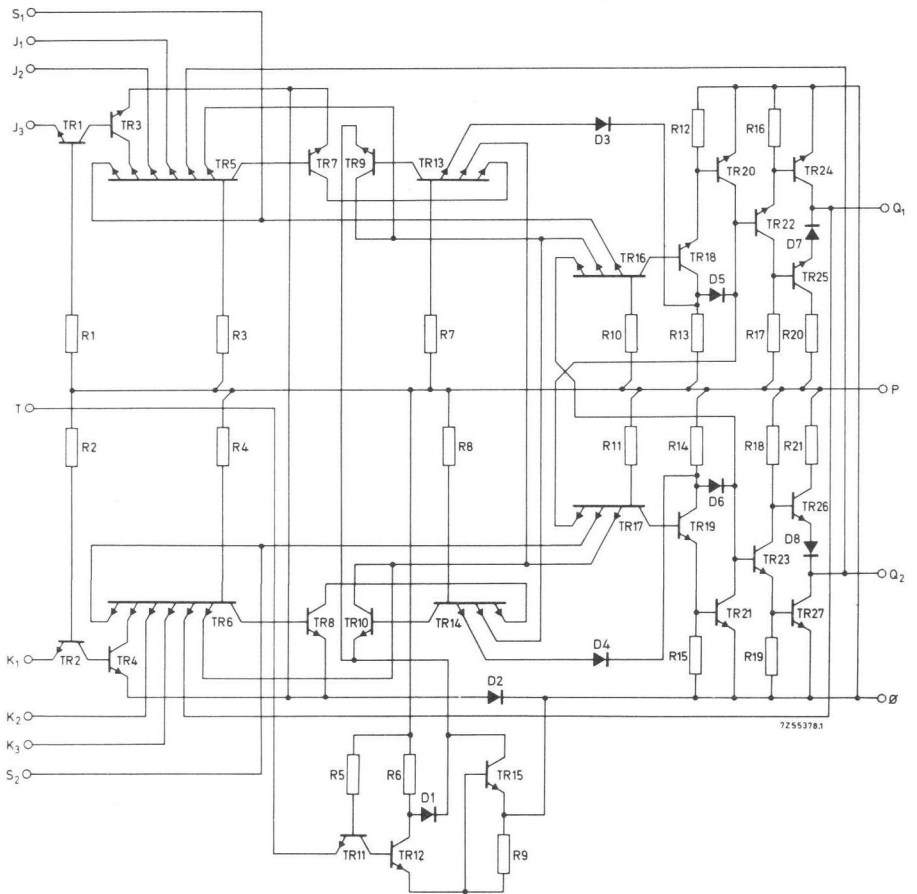
QUICK REFERENCE DATA

| | | |
|-------------------------------------------------|-----------|-----------------|
| Supply voltage | V_P | $5.0 \pm 5\%$ V |
| Operating ambient temperature range | T_{amb} | 0 to +70 °C |
| Available d.c. fan-out (full temperature range) | N_a | ≥ 10 |
| Max. operating frequency; $T_{amb} = 25$ °C | f | > 20 MHz |
| Average power consumption; $T_{amb} = 25$ °C | P_{av} | typ. 70 mW |

The FJJ101/7470 is a monolithic, edge-triggered JK flip-flop with gated inputs, direct S_1 and S_2 inputs, and complementary Q_1 and Q_2 outputs. It is suited for medium and high speed applications. In systems where input gating is required, its use can lead to a lower package count and reduced system power dissipation. Input information is transferred to the outputs in time with the positive-going edge of the trigger pulse. Direct-coupled input triggering occurs as soon as the trigger pulse reaches a fixed threshold voltage; thereafter the gated inputs are locked out.

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



FUNCTION TABLE

| t_n | | t_{n+1} |
|-------|-----|------------------|
| J* | K** | Q |
| L | L | Q_n |
| L | H | L |
| H | L | H |
| H | H | $\overline{Q_n}$ |

* $J = J_1 \cdot J_2 \cdot \overline{J_3}$

** $K = \overline{K_1} \cdot K_2 \cdot K_3$

S_1 and S_2 function can only occur when T is LOW.

H=HIGH state (the more positive voltage)

L=LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|------------------------------------------|----------------------|------|---------------------|
| Supply voltage | V_P | max. | 7.0 V |
| Input voltage | V_J, V_K, V_T, V_S | max. | 5.5 V ¹⁾ |
| Peak negative input voltage (J, K, T, S) | $-V_M$ | max. | 2 V ²⁾ |
| Storage temperature | T_{stg} | | -55 to +150 °C |
| Operating ambient temperature | T_{amb} | | 0 to +70 °C |

1) In addition the input voltage between any two J inputs or between any two K inputs:
max. 5.5 V.

2) Pulse duration $t_p = 20$ ns; repetition frequency $f = 5$ MHz; source resistance
 $R_S \geq 75 \Omega$.

CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and references | |
|----------------------------------|----------------------|-----------------------|-----|-----|---------------------------|-------------------------------------------------------------|
| | | 0 | 25 | 70 | V _P (V) | |
| STATIC DATA | | | | | | |
| <u>Voltages</u> | | | | | | |
| Input threshold LOW (any input) | V _{ILmax} | 0.8 | 0.8 | 0.8 | V | |
| Input threshold HIGH (any input) | V _{IHmin} | 2.0 | 2.0 | 2.0 | V | |
| Output LOW | V _{QLmax} | 0.4 | 0.4 | 0.4 | V | 4.75 I _Q =I _{QLmax} |
| Output HIGH | V _{QHmin} | 2.4 | 2.4 | 2.4 | V | 4.75 -I _Q =-I _{QHmax} |
| <u>Currents</u> | | | | | | |
| Input LOW (T, J, K) | -I _{ILmax} | 1.6 | 1.6 | 1.6 | mA | 5.25 V _I =V _{QLmax} ; I _Q =0 |
| Input HIGH (T, J, K) | I _{IHmax} | 40 | 40 | 40 | μA | 5.25 V _I =V _{QHmin} ; I _Q =0 |
| Input LOW (S) | -I _{SLmax} | 3.2 | 3.2 | 3.2 | mA | 5.25 V _S =V _{QLmax} ; I _Q =0 |
| Input HIGH (S) | I _{SHmax} | 80 | 80 | 80 | μA | 5.25 V _S =V _{QHmin} ; I _Q =0 |
| Output LOW | I _{QLmax} | 16 | 16 | 16 | mA | |
| Output HIGH | -I _{QHmax} | 0.4 | 0.4 | 0.4 | mA | |
| Output short circuited | -I _{Qscmin} | 18 | 18 | 18 | mA | 5.25 } V _I =0; V _Q =0 |
| | -I _{Qscmax} | 57 | 57 | 57 | mA | |

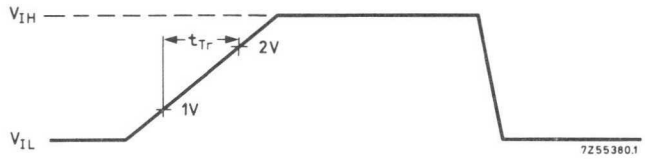
CHARACTERISTICS (continued)

| | | | T _{amb} (°C) | | | Conditions and references | | |
|--------------------------------------------------------------------------------|-----------------------|-----------|-----------------------|----------|----------|---------------------------|------------|---------------------|
| | | | 0 | 25 | 70 | V _P (V) | | |
| <u>SUPPLY DATA</u> | | | | | | | | |
| Supply current | I _P | typ. < | 13 26 | 13 26 | 13 26 | mA mA | 5.0 5.0 | } I _Q =0 |
| <u>DYNAMIC DATA</u> | | | | | | | | |
| <u>Signal requirements</u> | | | | | | | | |
| Rise time (T input) | t _{Tr} | < | - | 150 | - | ns | 5.0 | |
| Pulse duration (T input) | t _{TH} | > | - | 20 | - | ns | 5.0 | |
| Pulse duration (S input) | t _{SL} | > | - | 25 | - | ns | 5.0 | |
| <u>Performance</u> | | | | | | | | |
| Rise propagation delay time (S→Q) | t _{pdr} | < | - | 50 | - | ns | 5.0 | N=10 |
| Fall propagation delay time (S→Q) | t _{pdf} | < | - | 50 | - | ns | 5.0 | N=10 |
| Rise propagation delay time (T→Q) | t _{pdr} | > | - | 10 | - | ns | 5.0 | } N=10 |
| | t _{pdr} | typ. | - | 27 | - | ns | 5.0 | |
| | t _{pdr} | < | - | 50 | - | ns | 5.0 | |
| Fall propagation delay time (T→Q) | t _{pdf} | > | - | 10 | - | ns | 5.0 | } N=10 |
| | t _{pdf} | typ. | - | 18 | - | ns | 5.0 | |
| | t _{pdf} | < | - | 50 | - | ns | 5.0 | |
| Set-up time (J ₃ , K ₁) | t _{su min} | < | - | 20 | - | ns | | |
| Hold time (J ₁ , J ₂ , K ₂ , K ₃) | t _{hold min} | < | - | 5 | - | ns | | |
| Preset time (S ₁) | t _{S1} | > | - | 25 | - | ns | | |
| Clear time (S ₂) | t _{S2} | > | - | 25 | - | ns | | |
| Maximum operating frequency | f | > | - | 20 | - | MHz | } 5.0 | N=10 |
| | f | typ. | - | 35 | - | MHz | | |

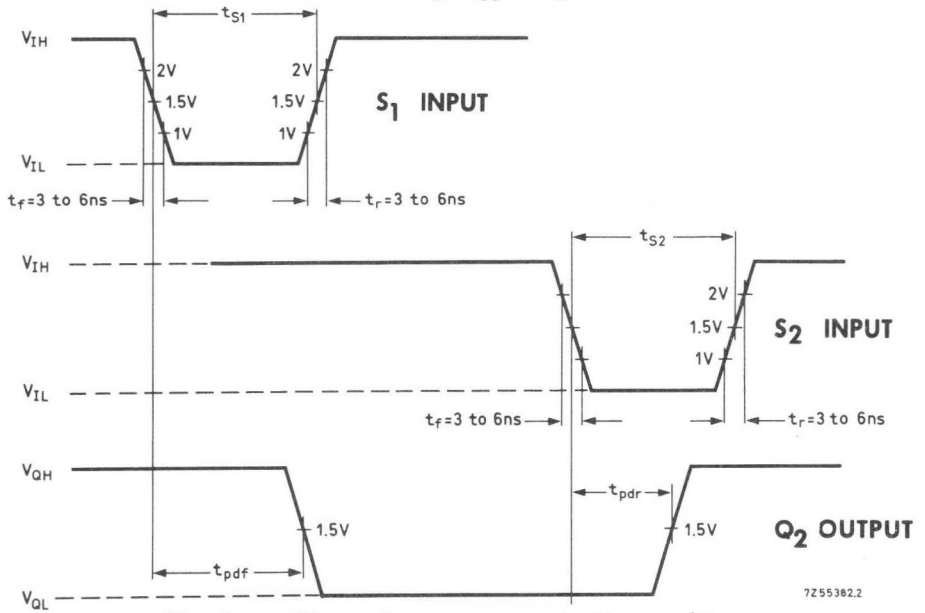


CHARACTERISTICS (continued)

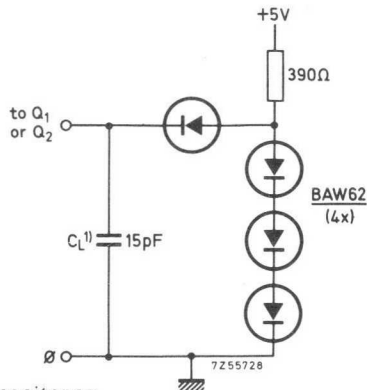
DYNAMIC DATA



Waveform illustrating trigger signal rise time



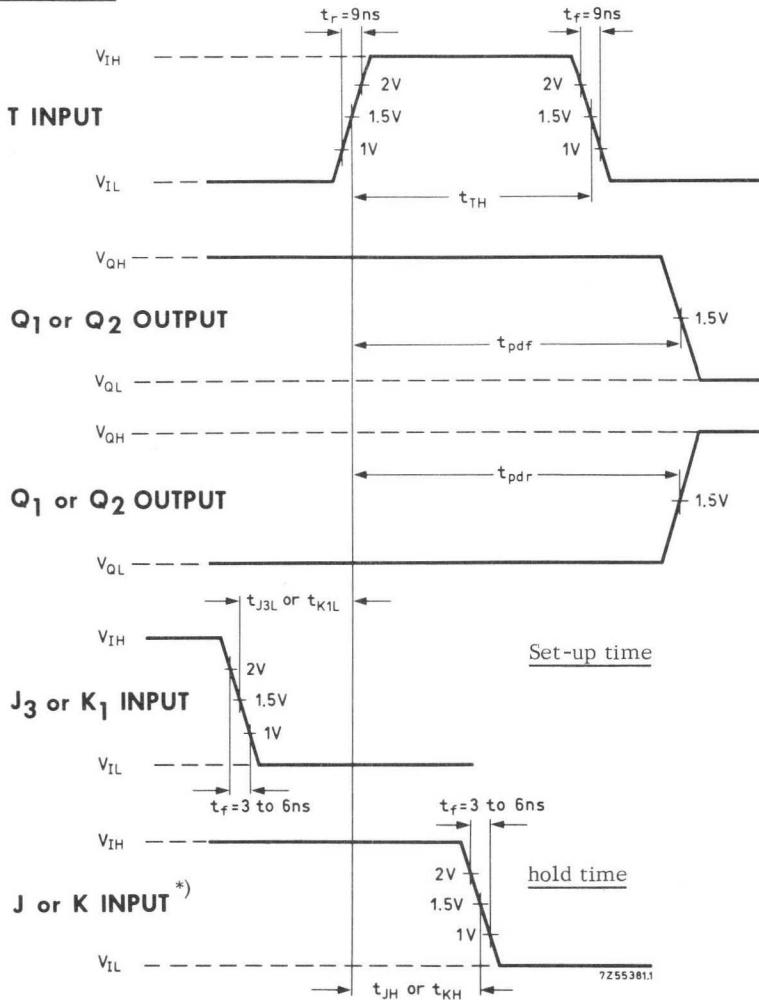
Waveforms illustrating measurement of t_{pdr} and t_{pdf} .



1) Including probe and jig capacitance.

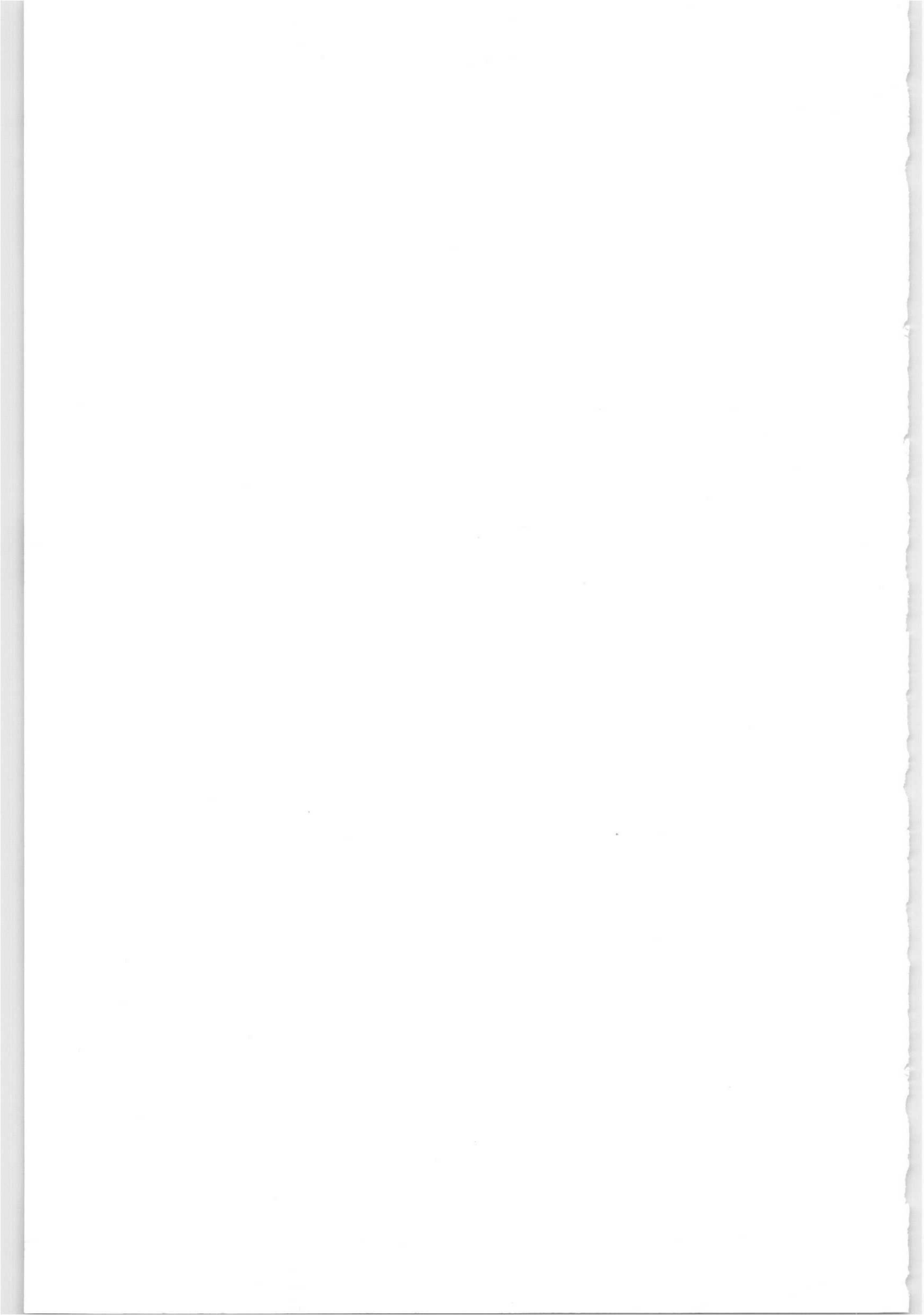
CHARACTERISTICS (continued)

DYNAMIC DATA



Waveform illustrating switching times.

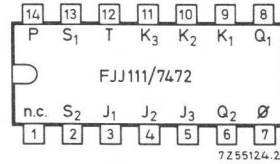
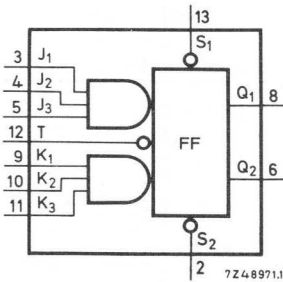
*) J = J₁ or J₂
K = K₂ or K₃



The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

SINGLE JK MASTER-SLAVE FLIP-FLOP (AND INPUTS)



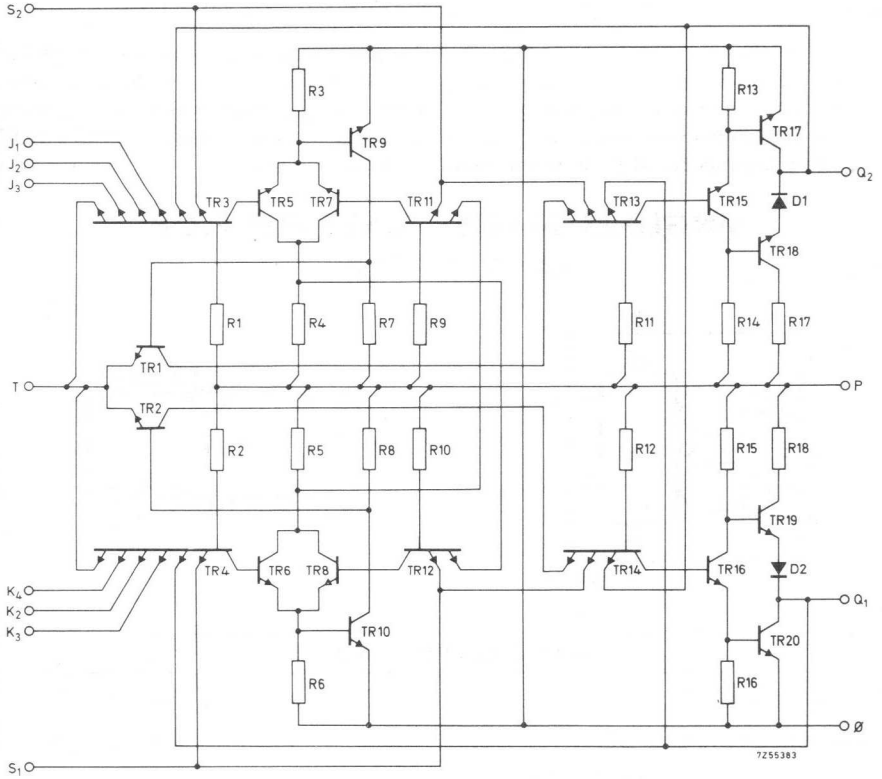
QUICK REFERENCE DATA

| | | | |
|-------------------------------------------------|-----------|---------------|--------|
| Supply voltage | V_p | $5.0 \pm 5\%$ | V |
| Operating ambient temperature range | T_{amb} | 0 to +70 | °C |
| Available d.c. fan-out (full temperature range) | N_a | \geq | 10 |
| Max. operating frequency; $T_{amb} = 25$ °C | f | $>$ | 10 MHz |
| Average power consumption; $T_{amb} = 25$ °C | P_{av} | typ. | 40 mW |

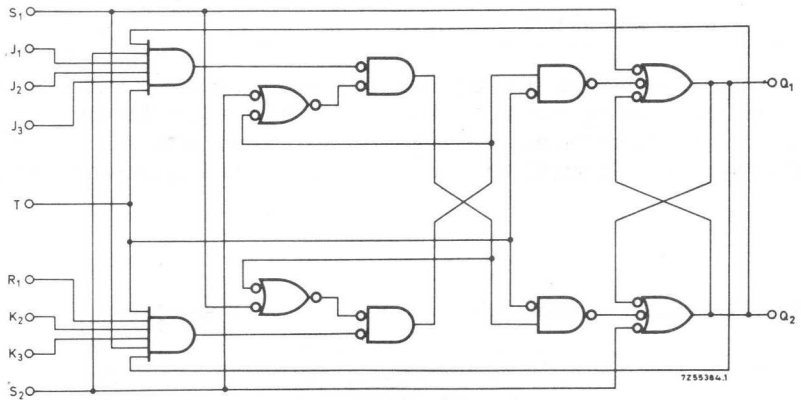
The FJJ111/7472 is a master-slave flip-flop having three J and three K input (AND function). The circuit operates at a frequency up to 15 MHz (typ.). The information at the J and K input enters the master when T is HIGH. Afterwards, when T is LOW, the information is transferred from the master to the slave and appears at the outputs.

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM



FUNCTION TABLE

| t_n | | t_{n+1} |
|-------|-----|-------------|
| J* | K** | Q |
| L | L | Q_n |
| L | H | \bar{L} |
| H | L | \bar{H} |
| H | H | \bar{Q}_n |

*J = J₁·J₂·J₃

**K = K₁·K₂·K₃

S₁ and S₂ functions are independent of T.

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|------------------------------------------|-------------------------------------------------------------------|------|-------------|-----------------|
| Supply voltage | V _p | max. | 7.0 | V |
| Input voltage | V _J , V _K , V _T , V _S | max. | 5.5 | V ¹⁾ |
| Peak negative input voltage (J, K, T, S) | -V _M | max. | 2 | V ²⁾ |
| Storage temperature | T _{stg} | | -55 to +150 | °C |
| Operating ambient temperature | T _{amb} | | 0 to +70 | °C |

¹⁾ In addition the voltage between any two J inputs, or between any two K inputs: max. 5.5 V.

²⁾ Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance R_S ≥ 75 Ω.

CHARACTERISTICS

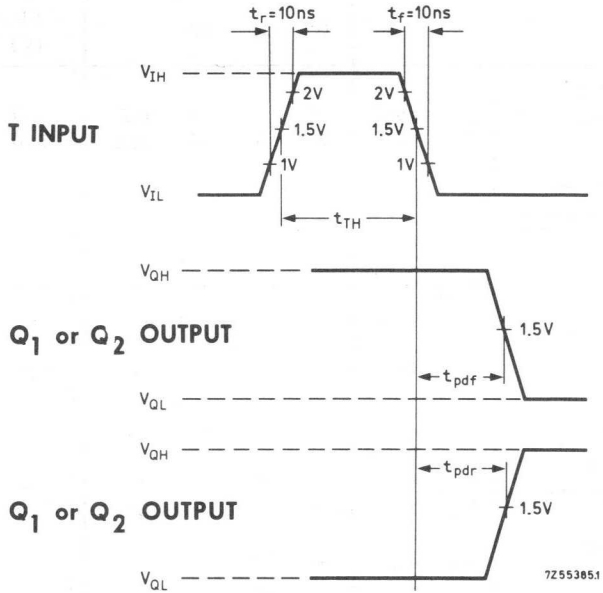
| | | T _{amb} (°C) | | | Conditions and references | |
|-------------------------------------|--------------------------------------------|-----------------------|-----|-----|---------------------------|---------------------------------------------------------|
| | | 0 | 25 | 75 | V _P (V) | |
| <u>STATIC DATA</u> | | | | | | |
| <u>Voltages</u> | | | | | | |
| Input threshold LOW (any input) | V _{ILmax} | 0.8 | 0.8 | 0.8 | | |
| Input threshold HIGH (any input) | V _{IHmin} | 2.0 | 2.0 | 2.0 | | |
| Output LOW | V _{QLmax} | 0.4 | 0.4 | 0.4 | 4.75 | I _Q = I _{QLmax} |
| Output HIGH | V _{QHmin} | 2.4 | 2.4 | 2.4 | 4.75 | -I _Q = -I _{QHmax} |
| <u>Currents</u> | | | | | | |
| Input LOW (J, K) | -I _{JLmax} -I _{KLmax} | 1.6 | 1.6 | 1.6 | 5.25 | V _{JK} =V _{QLmax} ; I _Q =0 |
| Input HIGH (J, K) | I _{JHmax} I _{KHmax} | 40 | 40 | 40 | 5.25 | V _{JK} =V _{QHmin} ; I _Q =0 |
| Input LOW (S, T) | -I _{SLmax} -I _{TLmax} | 3.2 | 3.2 | 3.2 | 5.25 | V _{ST} =V _{QLmax} ; I _Q =0 |
| Input HIGH (S, T) | I _{SHmax} I _{THmax} | 80 | 80 | 80 | 5.25 | V _{ST} =V _{QHmin} ; I _Q =0 |
| Output LOW | I _{QLmax} | 16 | 16 | 16 | } 5.25 | V _I =0; V _Q =0 |
| Output HIGH | I _{QHmax} | 0.4 | 0.4 | 0.4 | | |
| Output short circuited | -I _{Qscmin} | 18 | 18 | 18 | | |
| | -I _{Qscmax} | 57 | 57 | 57 | | |

CHARACTERISTICS (continued)

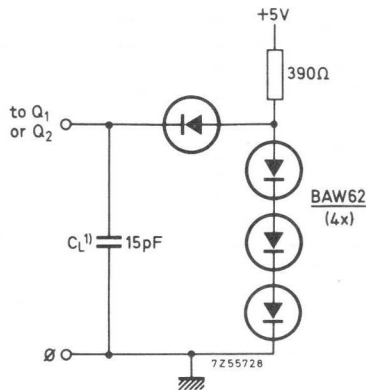
| | | T _{amb} (°C) | | | | Conditions and references | | |
|-----------------------------------|------------------|-----------------------|---------|----------------|---------|---------------------------|------------|--------|
| | | 0 | 25 | 70 | | V _P (V) | | |
| <u>SUPPLY DATA</u> | | | | | | | | |
| Supply current | I _P | typ. < | 8 20 | 8 20 | 8 20 | mA mA | 5.0 5.0 | |
| <u>DYNAMIC DATA</u> | | | | | | | | |
| <u>Signal requirements</u> | | | | | | | | |
| Pulse duration (T input) | t _{TH} | > | - | 20 | - | ns | 5.0 | |
| Pulse duration (S input) | t _{SL} | > | - | 25 | - | ns | 5.0 | |
| <u>Performance</u> | | | | | | | | |
| Rise propagation delay time (S→Q) | t _{pdr} | typ. < | - | 16 25 | - | ns ns | } 5.0 | N = 10 |
| Fall propagation delay time (S→Q) | t _{pdf} | typ. < | - | 25 40 | - | ns ns | | |
| Rise propagation delay time (T→Q) | t _{pdr} | > typ. < | - | 10 16 25 | - | ns ns ns | } 5.0 | N = 10 |
| Fall propagation delay time (T→Q) | t _{pdf} | > typ. < | - | 10 25 40 | - | ns ns ns | | |
| Set-up time | t _{su} | > | - | 0 | - | ns | | |
| Clear time | t _c | > | - | 25 | - | ns | | |
| Maximum operating frequency | f | > typ. | - | 10 15 | - | MHz MHz | 5.0 | N = 10 |

CHARACTERISTICS (continued)

DYNAMIC DATA



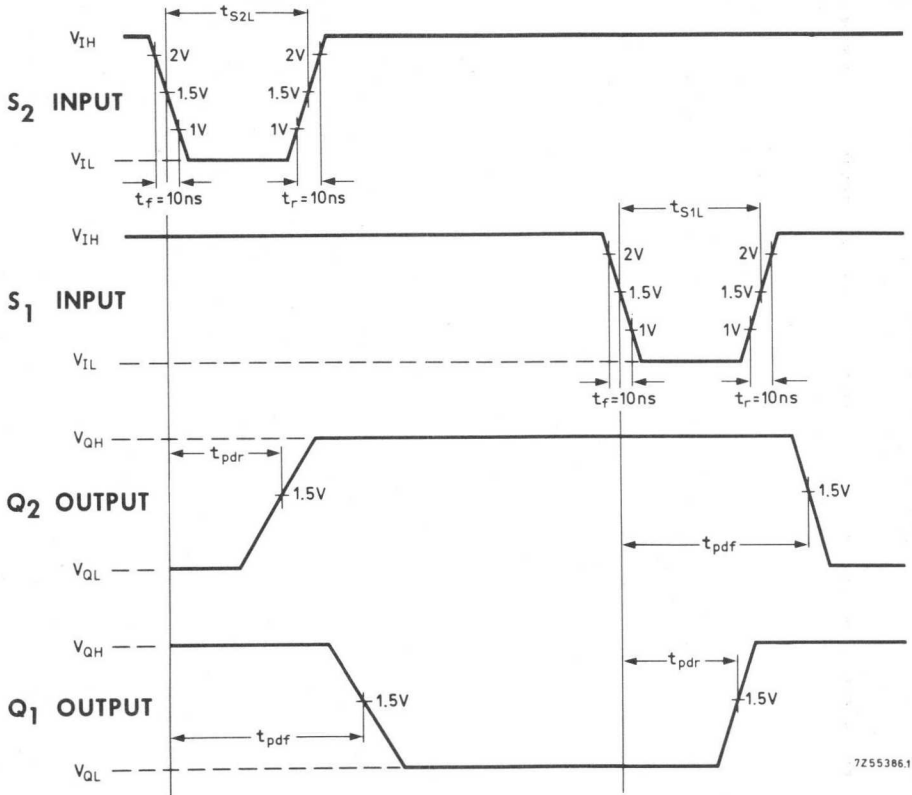
Waveforms illustrating measurement of t_{pdr} and t_{pdf} .



¹) Including probe and jig capacitance

CHARACTERISTICS (continued)

DYNAMIC DATA



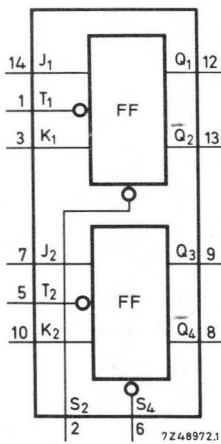
Waveforms illustrating switching times.

100
100
100
100
100

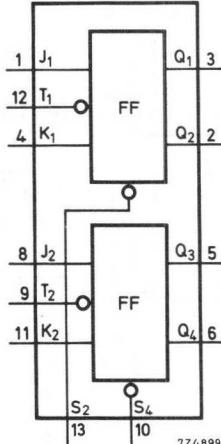
The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

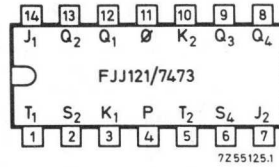
DUAL JK MASTER-SLAVE FLIP-FLOP



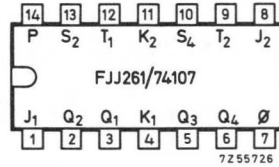
FJJ121/7473



FJJ261/74107



7255125.1



7255726

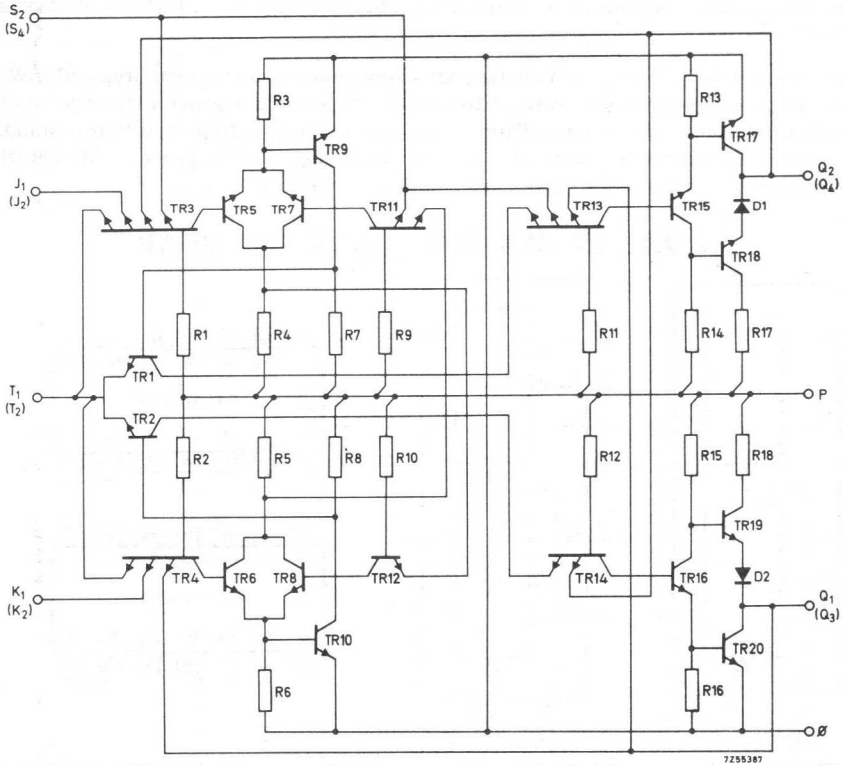
QUICK REFERENCE DATA

| | | | |
|-----------------------------------------------------------------|-----------|---------------|-----|
| Supply voltage | V_P | $5.0 \pm 5\%$ | V |
| Operating ambient temperature range | T_{amb} | 0 to +70 | °C |
| Available d.c. fan-out (full temperature range) | N_a | ≥ 10 | |
| Max. operating frequency; $T_{amb} = 25$ °C | f | > 10 | MHz |
| Average power consumption; $T_{amb} = 25$ °C (per flip-flop) | P_{av} | < 40 | mW |

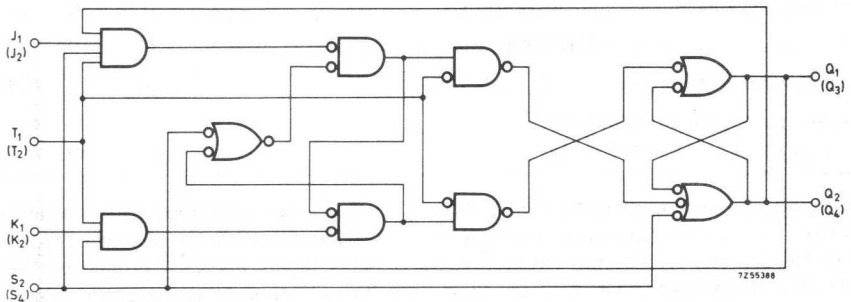
The FJJ121/7473 comprises two independent flip-flops, each provided with one J and one K input and based on the master-slave principle. The circuits operate at a frequency up to 15 MHz (typ.). The information at the J and K inputs enters the master when T is HIGH. Afterwards, when T is LOW, the information is transferred from the master to the slave and appears at the outputs. The FJJ261/74107 is electrically identical to the FJJ121/7473 but has power supply and ground on corner pins. (7 and 14)

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM



FUNCTION TABLE

| t_n | | t_{n+1} |
|-------|---|------------------|
| J | K | $Q_1 (Q_3)$ |
| L | L | Q_n |
| L | H | L |
| H | L | \overline{H} |
| H | H | $\overline{Q_n}$ |

S_2 and S_4 functions are independent of T_1 and T_2 .

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|------------------------------------------|----------------------|------|-------------------|
| Supply voltage | V_P | max. | 7.0 V |
| Input voltage | V_J, V_K, V_S, V_T | max. | 5.5 V |
| Peak negative input voltage (J, K, T, S) | $-V_M$ | max. | 2 V ¹⁾ |
| Storage temperature | T_{stg} | | -55 to +150 °C |
| Operating ambient temperature | T_{amb} | | 0 to +70 °C |

¹⁾ Pulse duration $t_p = 20$ ns; repetition frequency $f = 5$ MHz; source resistance $R_S \geq 75 \Omega$.

CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and references | |
|-------------------------------------|--------------------------------------------|-----------------------|-----|-----|---------------------------|----------------------------------------------------------------|
| | | 0 | 25 | 70 | V _P (V) | |
| <u>STATIC DATA</u> | | | | | | |
| <u>Voltages</u> | | | | | | |
| Input threshold LOW (any input) | V _{ILmax} | 0.8 | 0.8 | 0.8 | V | |
| Input threshold HIGH (any input) | V _{IHmin} | 2.0 | 2.0 | 2.0 | V | |
| Output LOW | V _{QLmax} | 0.4 | 0.4 | 0.4 | V | 4.75 I _Q = I _{QLmax} |
| Output HIGH | V _{QHmin} | 2.4 | 2.4 | 2.4 | V | 4.75 -I _Q = -I _{QHmax} |
| <u>Currents</u> | | | | | | |
| Input LOW (J, K) | -I _{JLmax} -I _{KLmax} | 1.6 | 1.6 | 1.6 | mA | 5.25 V _{JK} = V _{QLmax} ; I _Q = 0 |
| Input HIGH (J, K) | I _{JHmax} I _{KHmax} | 40 | 40 | 40 | μA | 5.25 V _{JK} = V _{QHmin} ; I _Q = 0 |
| Input LOW (S, T) | -I _{SLmax} -I _{TLmax} | 3.2 | 3.2 | 3.2 | mA | 5.25 V _{ST} = V _{QLmax} ; I _Q = 0 |
| Input HIGH (S, T) | I _{SLmax} I _{TLmax} | 80 | 80 | 80 | μA | 5.25 V _{ST} = V _{QHmin} ; I _Q = 0 |
| Output LOW | I _{QLmax} | 16 | 16 | 16 | mA | |
| Output HIGH | -I _{QHmax} | 0.4 | 0.4 | 0.4 | mA | |
| Output short circuited | -I _{Qscmin} | 18 | 18 | 18 | mA | 5.25 V _I = 0; V _Q = 0 |
| | -I _{Qscmax} | 57 | 57 | 57 | mA | 5.25 V _I = 0; V _Q = 0 |

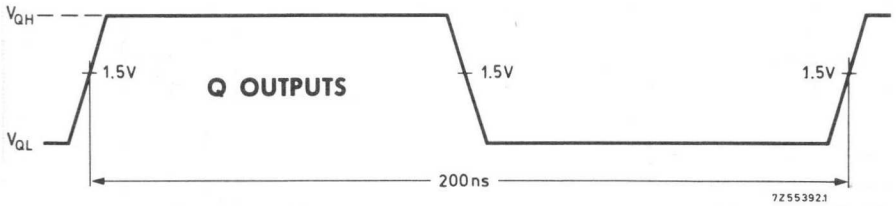
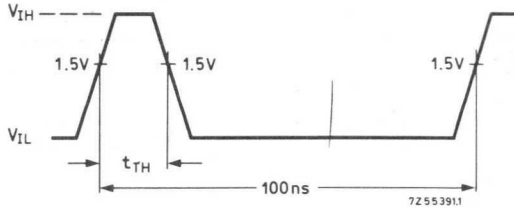
CHARACTERISTICS (continued)

| | | T _{amb} (°C) | | | | Conditions and references | | |
|------------------------------------------------|------------------|-----------------------|----|----|----|---------------------------|-------|--------|
| | | 0 | 25 | 70 | | V _P (V) | | |
| <u>SUPPLY DATA</u> | | | | | | | | |
| Supply current | I _P | typ. | 16 | 16 | 16 | mA | 5.0 | |
| | | < | 40 | 40 | 40 | mA | 5.0 | |
| <u>DYNAMIC DATA</u> | | | | | | | | |
| <u>Signal requirements</u> | | | | | | | | |
| Pulse duration (T input) | t _{TH} | > | - | 20 | - | ns | 5.0 | |
| Pulse duration (S input) | t _{SL} | > | - | 25 | - | ns | 5.0 | |
| <u>Performance</u> | | | | | | | | |
| Rise propagation delay time (S→Q) | t _{pdr} | typ. | - | 16 | - | ns | } 5.0 | N = 10 |
| | t _{pdr} | < | - | 25 | - | ns | | |
| Fall propagation delay time (S→Q) | t _{pdf} | typ. | - | 25 | - | ns | } 5.0 | N = 10 |
| | t _{pdf} | < | - | 40 | - | ns | | |
| Rise propagation delay time (T→Q) | t _{pdr} | > | - | 10 | - | ns | } 5.0 | N = 10 |
| | t _{pdr} | typ. | - | 16 | - | ns | | |
| | t _{pdr} | < | - | 25 | - | ns | | |
| Fall propagation delay time (T→Q) | t _{pdf} | > | - | 10 | - | ns | } 5.0 | N = 10 |
| | t _{pdf} | typ. | - | 25 | - | ns | | |
| | t _{pdf} | < | - | 40 | - | ns | | |
| Set-up time | t _{su} | > | - | 0 | - | ns | | |
| Clear time (S ₂ or S ₄) | t _S | > | - | 25 | - | ns | | |
| Maximum operating frequency | f | > | - | 15 | - | MHz | 5.0 | N = 10 |
| | | typ. | - | 20 | - | MHz | | |

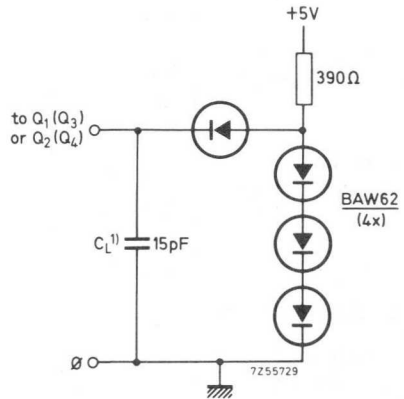
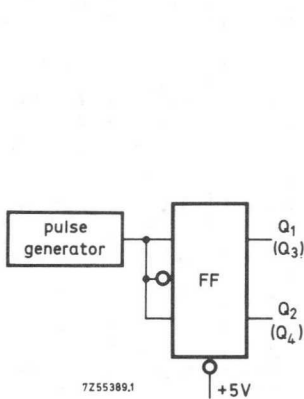
CHARACTERISTICS (continued)

DYNAMIC DATA

T, J, and K INPUTS



Waveforms illustrating in- and output pulses.

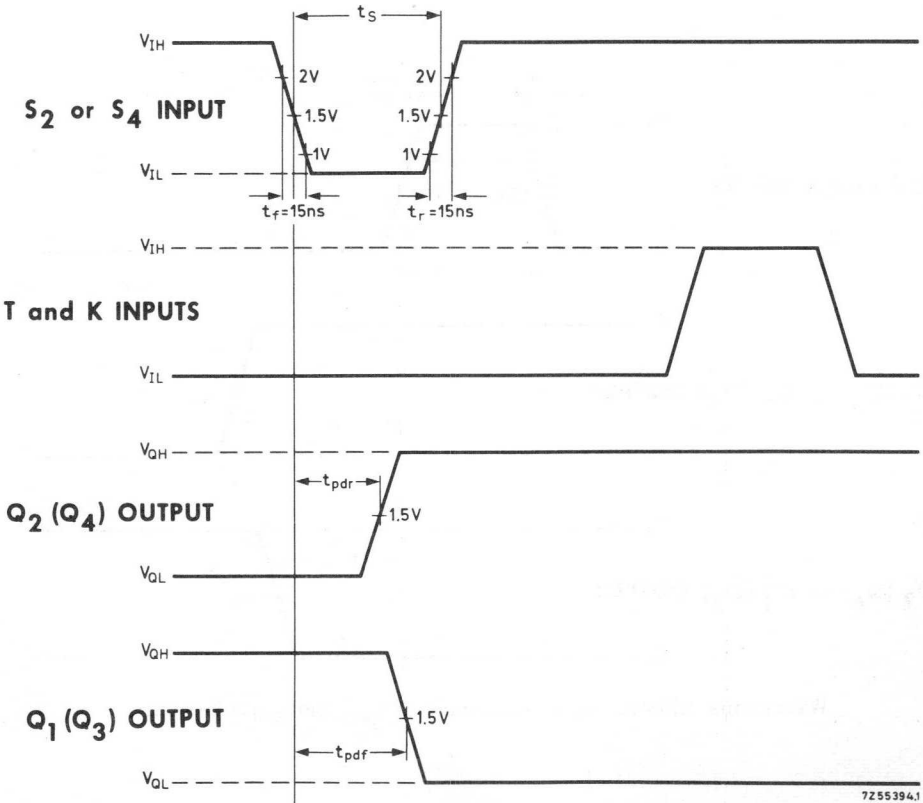
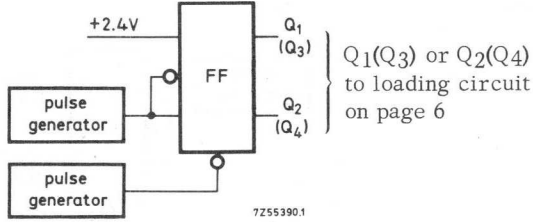


Equivalent load for $N = 10$

¹⁾ Including probe and jig capacitance

CHARACTERISTICS (continued)

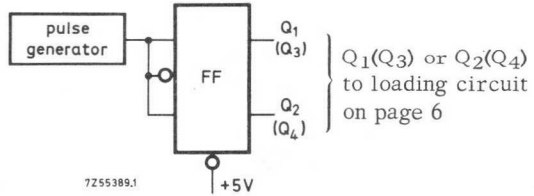
DYNAMIC DATA



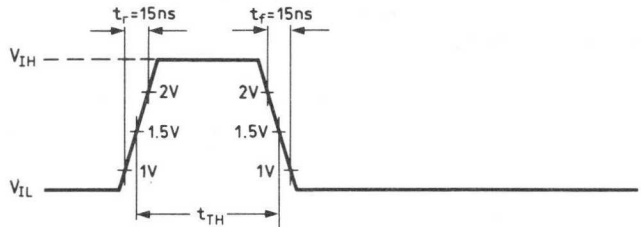
Waveforms illustrating measurement of t_{pdr} and t_{pdf} (S → Q)

CHARACTERISTICS (continued)

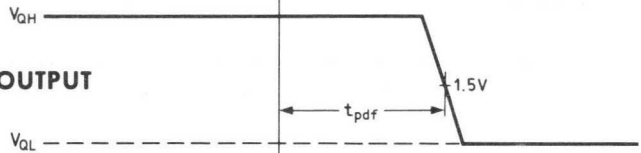
DYNAMIC DATA



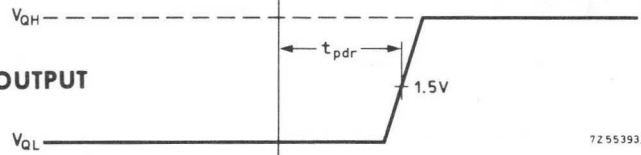
T, J and K INPUTS



Q₁ (Q₃) or Q₂ (Q₄) OUTPUT



Q₂ (Q₄) or Q₁ (Q₃) OUTPUT



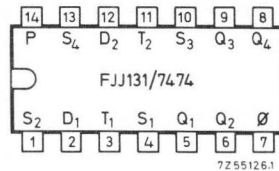
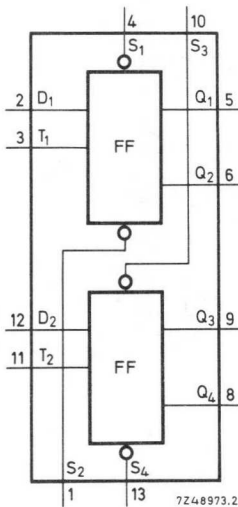
7255393.1

Waveforms illustrating measurement of t_{pdr} and t_{pdf} . (T → Q)

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP



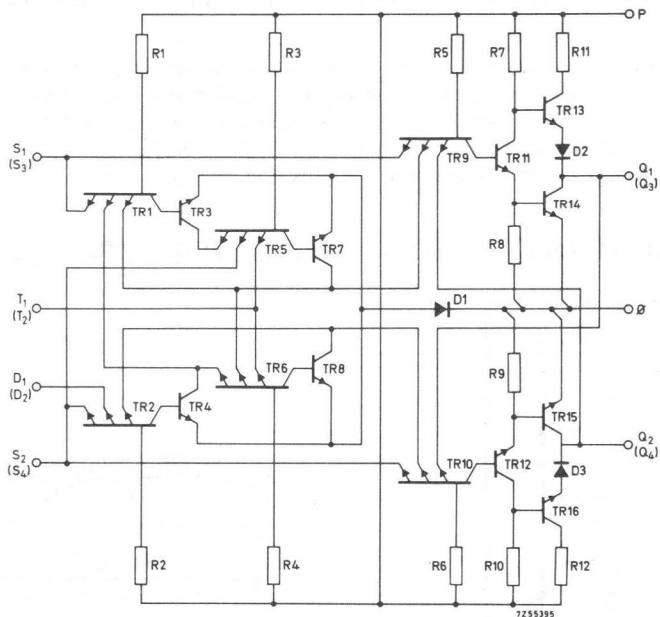
QUICK REFERENCE DATA

| | | | |
|-----------------------------------------------------------------|-----------|---------------|---------|
| Supply voltage | V_p | $5.0 \pm 5\%$ | V |
| Operating ambient temperature range | T_{amb} | 0 to + 70 | °C |
| Available d.c. fan-out (full temperature range) | N_a | \geq | 10 |
| Max. operating frequency; $T_{amb} = 25$ °C | f | $>$ | 15 MHz |
| Average power consumption; $T_{amb} = 25$ °C (per flip-flop) | P_{av} | $<$ | 42.5 mW |

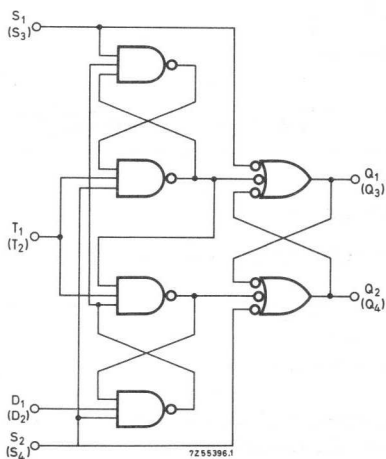
The FJJ131/7474 is an edge-triggered dual D-type flip-flop with direct SET inputs and complementary outputs. On the positive going edge of the clock pulse the information on the D input is transferred to Q_1 (or resp. Q_3).

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM



FUNCTION TABLE

| t_n | | t_{n+1} | |
|-------|----------------|----------------|--|
| D | Q ₁ | Q ₂ | |
| L | L | H | |
| H | H | L | |

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---------------------------------------|-----------------|------|-------------------|
| Supply voltage | V_P | max. | 7.0 V |
| Output voltage | V_Q | max. | 5.5 V |
| Input voltage | V_D, V_S, V_T | max. | 5.5 V |
| Peak negative input voltage (D, S, T) | $-V_M$ | max. | 2 V ¹⁾ |
| Storage temperature | T_{stg} | | -55 to +150 °C |
| Operating ambient temperature | T_{amb} | | 0 to +70 °C |

¹⁾ Pulse duration $t_p = 20$ ns; repetition frequency $f = 5$ MHz; source resistance $R_G \geq 75 \Omega$.

CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and references | |
|-----------------------------------------------|----------------------------------------------|-----------------------|-----|-----|---------------------------|-------------------------------------------------------------|
| | | 0 | 25 | 70 | V _P (V) | |
| <u>STATIC DATA</u> | | | | | | |
| <u>Voltages</u> | | | | | | |
| Input threshold LOW (any input) | V _{ILmax} | 0.8 | 0.8 | 0.8 | V | |
| Input threshold HIGH (any input) | V _{IHmin} | 2.0 | 2.0 | 2.0 | V | |
| Output LOW | V _{QLmax} | 0.4 | 0.4 | 0.4 | V | 4.75 I _Q = I _{QLmax} |
| Output HIGH | V _{QHmin} | 2.4 | 2.4 | 2.4 | V | 4.75 -I _Q = -I _{QHmax} |
| <u>Currents</u> | | | | | | |
| Input LOW (S ₁ , D ₁) | -I _{S1Lmax} -I _{D1Lmax} | 1.6 | 1.6 | 1.6 | mA | 5.25 V _{S1} , V _{D1} = V _{QLmax} |
| Input LOW (S ₂ , T ₁) | -I _{S2Lmax} -I _{T1Lmax} | 3.2 | 3.2 | 3.2 | mA | 5.25 V _{S2} , V _{T1} = V _{QLmax} |
| Input HIGH (D) | I _{DHmax} | 40 | 40 | 40 | μA | 5.25 V _D = V _{QHmin} |
| Input HIGH (S ₁ , T ₁) | I _{S1Hmax} I _{T1Hmax} | 80 | 80 | 80 | μA | 5.25 V _{S1} , V _{T1} = V _{QHmin} |
| Input HIGH (S ₂) | I _{S2Hmax} | 120 | 120 | 120 | μA | 5.25 V _{S2} = V _{QHmin} |
| Output LOW | I _{QLmax} | 16 | 16 | 16 | mA | |
| Output HIGH | -I _{QHmax} | 0.4 | 0.4 | 0.4 | mA | |
| Output short circuited | -I _{Qscmin} | 18 | 18 | 18 | mA | 5.25 } V _Q = 0 |
| | -I _{Qscmax} | 57 | 57 | 57 | mA | |

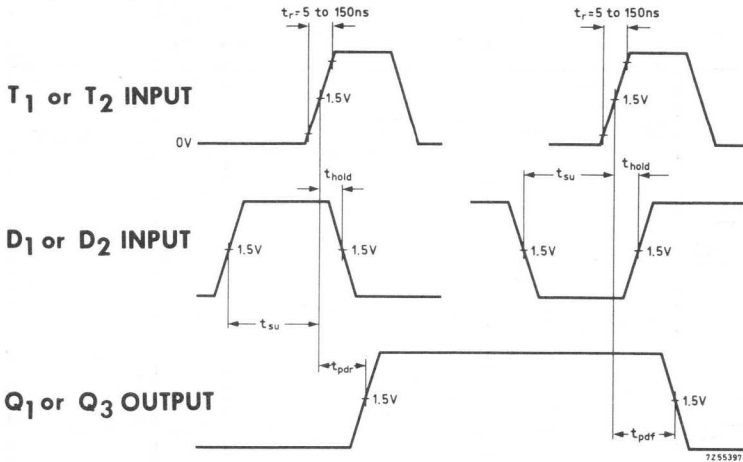
CHARACTERISTICS (continued)

| | | | T _{amb} (°C) | | | Conditions and references | |
|-----------------------------------|-----------------------------------|------------------|-----------------------|----------------|----------|---------------------------|--------------------------|
| | | | 0 | 25 | 70 | V _P (V) | |
| <u>SUPPLY DATA</u> | | | | | | | |
| Supply current | I _p | typ. < | 17 30 | 17 30 | 17 30 | mA mA | } V _I = 5.0 V |
| <u>DYNAMIC DATA</u> | | | | | | | |
| <u>Signal requirement</u> | | | | | | | |
| Pulse duration (S, T input) | t _{SL} , t _{TL} | > | 30 | 30 | 30 | ns | 5.0 |
| <u>Performance</u> | | | | | | | |
| Rise propagation delay time (S→Q) | t _{pdr} | < | - | 25 | - | ns | 5.0 N = 10 |
| Fall propagation delay time (S→Q) | t _{pdf} | < | - | 40 | - | ns | 5.0 N = 10 |
| Rise propagation delay time (T→Q) | t _{pdr} | { > typ. < | - | 10 14 25 | - | ns ns ns | } 5.0 N = 10 |
| Fall propagation delay time (T→Q) | t _{pdf} | { > typ. < | - | 10 20 50 | - | ns ns ns | |
| Set-up time | t _{su} | > | - | 20 | - | ns | } 5.0 N = 10 |
| Hold time | t _{hold} | > | - | 5 | - | ns | |
| Maximum operating frequency | f | > typ. | - - | 15 25 | - - | MHz MHz | } 5.0 N = 10 |

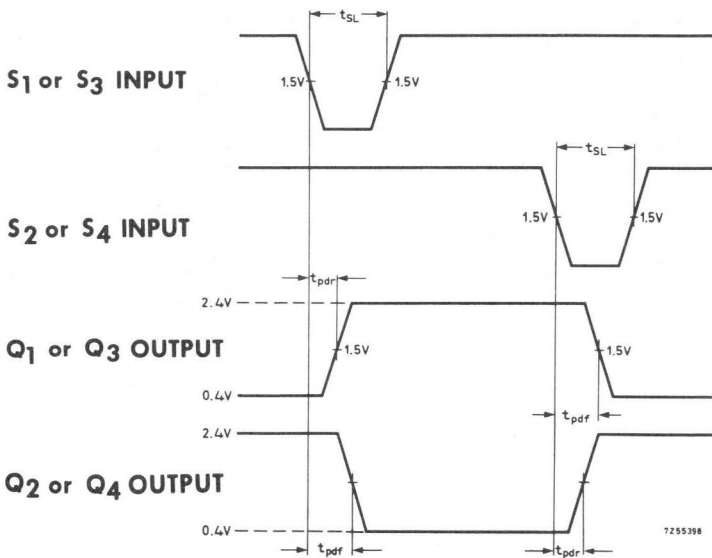


CHARACTERISTICS (continued)

DYNAMIC DATA



Waveforms illustrating set-up and hold times.

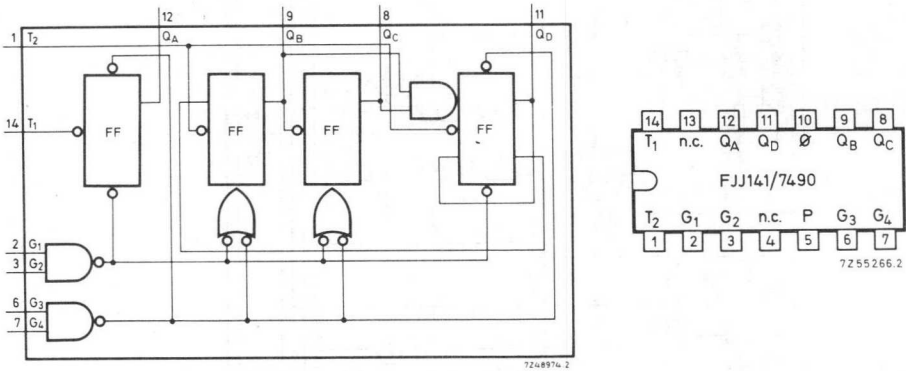


Waveforms illustrating measurement of t_{pdr} and t_{pdf} (S → Q)

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

BCD DECADE COUNTER



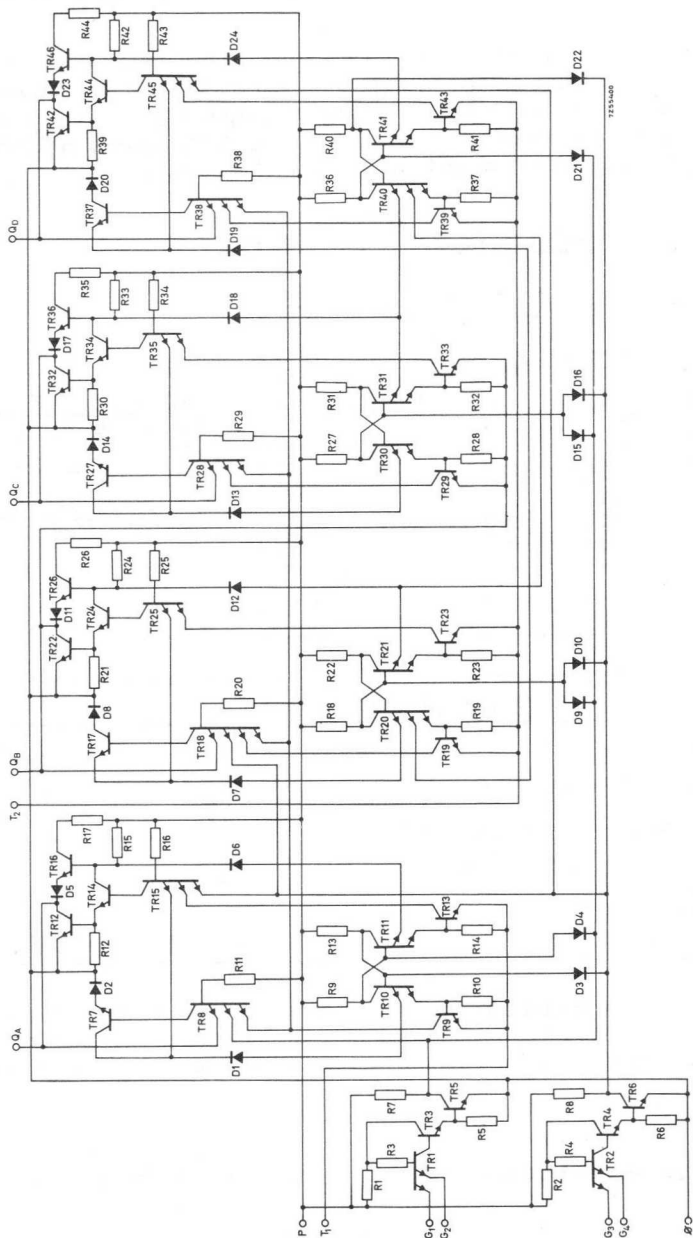
QUICK REFERENCE DATA

| | | | |
|------------------------------------------------------|-----------|---------------|-------------|
| Supply voltage | V_p | $5.0 \pm 5\%$ | V |
| Operating ambient temperature | T_{amb} | 0 to +70 | $^{\circ}C$ |
| Max. operating frequency; $T_{amb} = 25^{\circ}C$ | f_c | ≥ 10 | MHz |
| Available d. c. fan-out (full temperature range) | N_a | ≥ 10 | |
| Average power consumption $T_{amb} = 25^{\circ}C$ | P_{av} | typ. 160 | mW |

The FJJ141/7490 is a high speed decade counter, consisting of 4 master-slave flip-flops. Gated direct reset lines are provided to inhibit count inputs and return all outputs to a logical zero (inputs G_1, G_2) or to a binary coded (BCD) count of nine (inputs G_3, G_4).

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



LOGIC FUNCTION

As the output Q_A from the first flip-flop is not internally connected to the succeeding stages, the counter can be used in three different modes.

1. Binary coded decimal decade counter: the T_2 input must be externally connected to the Q_A output. T_1 is then the counter input.
2. Symmetrical divide-by-ten counter for frequency synthesizer or other applications requiring division of a binary count by the power of ten: the Q_D output must be connected to the T_1 input. In this case T_2 becomes counter input and a divide-by-ten square wave is obtained at output Q_A .
3. Divide-by-two counter and a divide-by-five counter: no external interconnections are required.

FUNCTION TABLES

BCD count sequence (output Q_A connected to input T_2)

| Count | OUTPUT | | | |
|-------|--------|-------|-------|-------|
| | Q_D | Q_C | Q_B | Q_A |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |

Reset/count

| RESET INPUTS | | | | OUTPUTS | | | |
|--------------|-------|-------|-------|-----------|-------|-------|-------|
| G_1 | G_2 | G_3 | G_4 | Q_D | Q_C | Q_B | Q_A |
| H | H | L | X | L | L | L | L |
| H | H | X | L | L | L | L | L |
| X | L | H | H | H | L | L | H |
| L | X | H | H | H | L | L | H |
| X | L | X | L | no change | | | |
| L | X | L | X | no change | | | |
| L | X | X | L | no change | | | |
| X | L | L | X | no change | | | |

H=HIGH state (the more positive voltage)
L=LOW state (the less positive voltage)
X=state is immaterial

G_1 and G_2 are "preset 0" inputs (reset all Q outputs to LOW)

G_3 and G_4 are "preset 9" inputs (set Q_A and Q_D to HIGH and reset Q_B and Q_C to LOW to provide BCD 9 count for nine complement applications)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|------------------------------------------------------------------------------------------------|-----------|-------------|-------------|
| Supply voltage | V_P | max. | 7.0 V |
| T input voltage | V_T | max. | 5.5 V |
| G input voltage | V_G | max. | 5.5 V |
| Duration of negative transient input voltage of 2 V $R_S \geq 75 \Omega$; $f = 5.0$ MHz | t_p | max. | 20 ns |
| Storage temperature | T_{stg} | -55 to +150 | $^{\circ}C$ |
| Operating ambient temperature | T_{amb} | 0 to +70 | $^{\circ}C$ |



CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and References | |
|---------------------------------------------------------------------------------|----------------------------------------|-----------------------|-----|-----|---------------------------|------|
| | | 0 | 25 | 75 | V _P (V) | |
| <u>STATIC DATA</u> | | | | | | |
| <u>Voltages</u> | | | | | | |
| Input threshold LOW (any input) | V _{ILmax} | 0.8 | 0.8 | 0.8 | V | |
| Input threshold HIGH all inputs except T ₂ | V _{IHmin} | 2.0 | 2.0 | 2.0 | V | |
| T ₂ input | V _{T2Hmin} | 2.2 | 2.2 | 2.2 | V | |
| Output LOW | V _{QLmax} | 0.4 | 0.4 | 0.4 | V | 4.75 |
| Output HIGH | V _{QHmin} | 2.4 | 2.4 | 2.4 | V | 4.75 |
| <u>Currents</u> | | | | | | |
| Input LOW (G input) | -I _{GLmax} | 1.6 | 1.6 | 1.6 | mA | 5.25 |
| Input HIGH (G input) | I _{GHmax} | 40 | 40 | 40 | μA | 5.25 |
| Input LOW (T ₁ input) | -I _{T1Lmax} | 3.2 | 3.2 | 3.2 | mA | 5.25 |
| Input HIGH (T ₁ input) | I _{T1Hmax} | 80 | 80 | 80 | μA | 5.25 |
| Input LOW (T ₂ input) | -I _{T2Lmax} | 6.4 | 6.4 | 6.4 | mA | 5.25 |
| Input HIGH (T ₂ input) | I _{T2Hmax} | 160 | 160 | 160 | μA | 5.25 |
| Output LOW | I _{QLmax} | 16 | 16 | 16 | mA | 4.75 |
| Output short-circuited ¹⁾ | -I _{Qscmin} | 18 | 18 | 18 | mA | 5.25 |
| | -I _{Qscmax} | 57 | 57 | 57 | mA | 5.25 |
| <u>SUPPLY DATA</u> | | | | | | |
| Supply current | I _p typ. < | 32 | 32 | 32 | mA | 5.0 |
| | | 53 | 53 | 53 | mA | 5.0 |
| <u>DYNAMIC DATA</u> | | | | | | |
| <u>Signal requirements</u> | | | | | | |
| Pulse duration (G inputs) | t _{GH} > t _{GL} > | - | 50 | - | ns | 5.0 |
| Pulse duration (T inputs) | t _{TH} > t _{TL} > | - | 50 | - | ns | 5.0 |
| <u>Performance</u> | | | | | | |
| Rise propagation ²⁾ delay time (T ₁ → Q _C) | t _{pdr} typ. < | - | 60 | - | ns | 5.0 |
| | | - | 100 | - | ns | 5.0 |
| Fall propagation ²⁾ delay time (T ₁ → Q _C) | t _{pdf} typ. < | - | 60 | - | ns | 5.0 |
| | | - | 100 | - | ns | 5.0 |
| Maximum counting frequency | f > typ. | - | 10 | - | MHz | 5.0 |
| | | - | 18 | - | MHz | 5.0 |

I_Q = I_{QLmax}
-I_Q = -I_{QHmax}

V_I = 0.4 V
V_I = 2.4 V
V_I = 0.4 V
V_I = 2.4 V
V_I = 0.4 V
V_I = 2.4 V

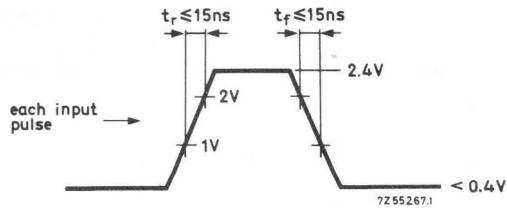
V_I = 4.5 V

¹⁾ Do not short circuit more than one output at a time.

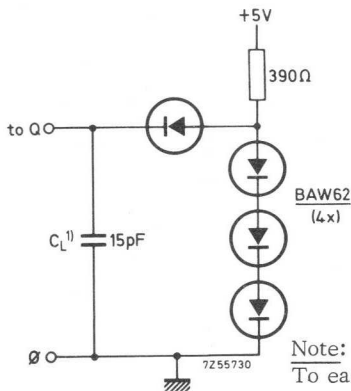
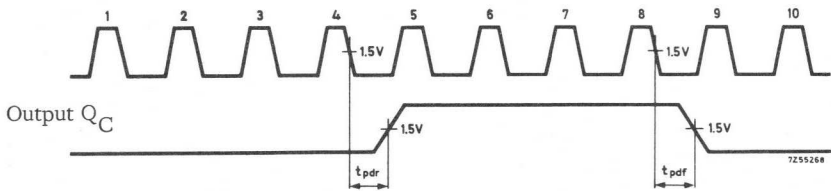
²⁾ All four outputs loaded, Q_A output connected to T₂ input, delay from T₁ input to Q_C output. (see also waveforms page 6).

CHARACTERISTICS (continued)

Input pulse



Input T_1 (Q_A output connected to T_2)



Note:

To each output the same loading circuit

¹⁾ Including probe and jig capacitance

FJ family

standard temperature range

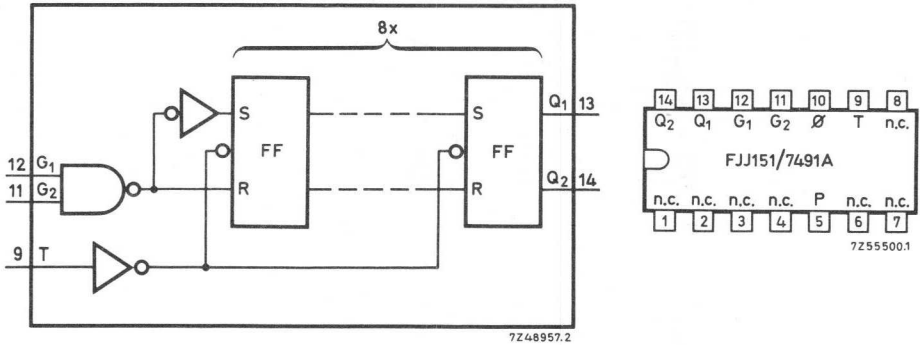
FJJ151/7491A

shift register

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices * it corresponds to the 74Nseries TTL.

8 BIT SHIFT REGISTER

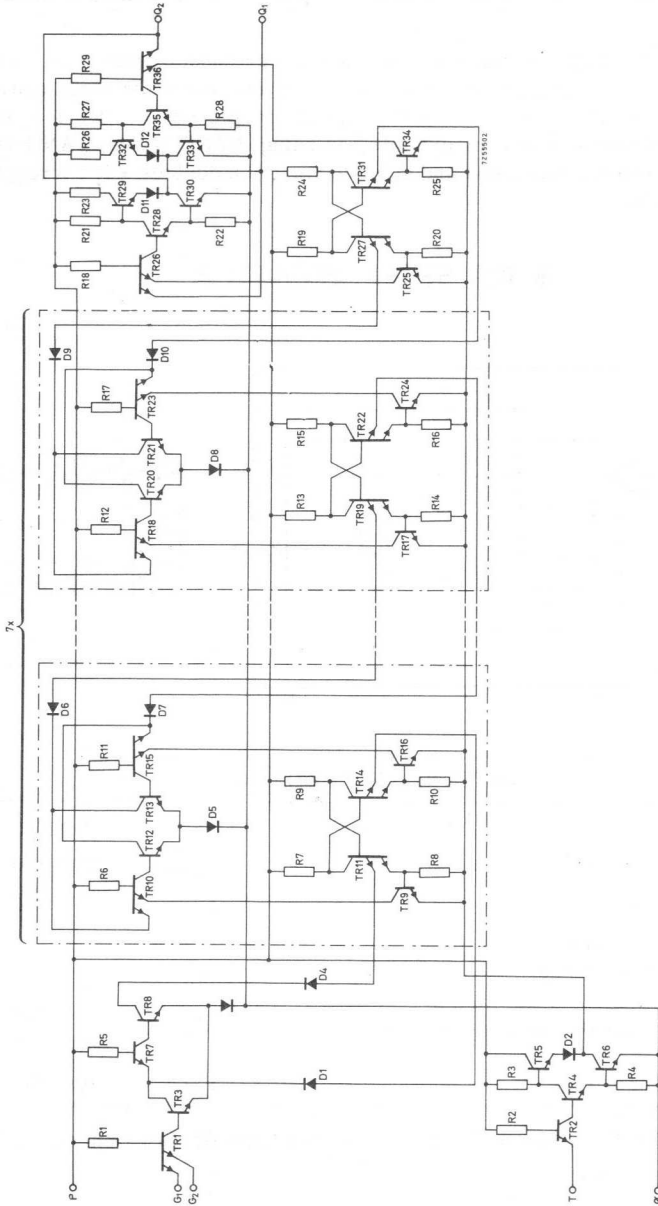


QUICK REFERENCE DATA

| | | |
|----------------------------------------------------|-----------|-----------------------|
| Supply voltage | V_P | 5.0 \pm 5% V |
| Operating ambient temperature | T_{amb} | 0 to +70 °C |
| Max. shift frequency | f | 10 MHz |
| Available d.c. fan-out (full temperature range) | N_a | 10 |
| D.C. noise margin (full temperature range) | M_L | > 0.4 V typ. 1.0 V |
| Total power dissipation | P_{tot} | typ. 175 mW |

PACKAGE OUTLINE : 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



The FJJ151 is a serial input, serial-output 8-bit shift register with complementary outputs. It consists of eight RS master-slave flip-flops, a two-input NAND gate, and a clock driver. Inputs G_1 and G_2 go to an AND gate; either one or both inputs may be used. If only one is used, the other must be kept in the HIGH state.

When the T input is HIGH, information at the input of each stage is shifted to the next; thus, information at the G_1 or G_2 input is transferred to the Q_1 or Q_2 output after 8 clock pulses.

The FJJ151 corresponds to the SN7491AN.

LOGIC FUNCTION

Function table

| t_n | | t_{n+8} |
|-------|-------|-----------|
| G_1 | G_2 | Q_1 |
| L | L | L |
| L | H | L |
| H | L | L |
| H | H | H |

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

t_n = bit time before trigger pulse

t_{n+8} = bit time after 8 trigger pulses

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|-----------------------------------------------|-----------------------|------|---------------------|
| Supply voltages | V_P | max. | 7.0 V |
| Input voltages | $V_{G1}; V_{G2}; V_T$ | max. | 5.5 V ¹⁾ |
| Peak negative input voltage (G_1, G_2, T) | $-V_M$ | max. | 2 V ²⁾ |
| Storage temperature | T_{stg} | | -65 to +150 °C |
| Operating ambient temperature | T_{amb} | | 0 to +70 °C |

1) In addition the voltage between any two inputs must not exceed 5.5 V.

2) Pulse duration $t_p = 20$ ns; repetition frequency $f = 5$ MHz; source resistance $R_S \geq 75 \Omega$.

CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and References | |
|-------------------------------------------------------------------|---------------------------|-----------------------|------|---------|---------------------------|---------------------------------------|
| | | 0 | 25 | 70 | V _P (V) | |
| <u>STATIC DATA</u> | | | | | | |
| <u>Voltages</u> | | | | | | |
| Input threshold LOW (any input) | V _{ILmax} | 0.8 | 0.8 | 0.8 V | | |
| Input threshold HIGH (any input) | V _{IHmin} | 2.0 | 2.0 | 2.0 V | | |
| Output LOW | V _{QLmax} | 0.4 | 0.4 | 0.4 V | 4.75 | I _Q = I _{QLmax} |
| Output HIGH | V _{QHmin} | 2.4 | 2.4 | 2.4 V | 4.75 | -I _Q = -I _{QHmax} |
| <u>Currents</u> | | | | | | |
| Input LOW; G ₁ G ₂ T | -I _{G1Lmax} | 1.6 | 1.6 | 1.6 mA | 5.25 | } V _I = 0.4 V |
| | -I _{G2Lmax} | 1.6 | 1.6 | 1.6 mA | 5.25 | |
| | -I _{TLmax} | 1.6 | 1.6 | 1.6 mA | 5.25 | |
| Input HIGH; G ₁ G ₂ T | I _{G1Hmax} | 40 | 40 | 40 μA | 5.25 | } V _I = 2.4 V |
| | I _{G2Hmax} | 40 | 40 | 40 μA | 5.25 | |
| | I _{THmax} | 40 | 40 | 40 μA | 5.25 | |
| G ₁ G ₂ T | I _{G1Hmax} | 1.0 | 1.0 | 1.0 mA | 5.25 | } V _I = 5.5 V |
| | I _{G2Hmax} | 1.0 | 1.0 | 1.0 mA | 5.25 | |
| | I _{THmax} | 1.0 | 1.0 | 1.0 mA | 5.25 | |
| Output LOW | I _{QLmax} | 16 | 16 | 16 mA | | V _Q = V _{QLmax} |
| Output HIGH | -I _{QHmax} | 0.4 | 0.4 | 0.4 mA | | V _Q = V _{QHmin} |
| Output short circuited (see note 1) | -I _{Qscmin} | 18.0 | 18.0 | 18.0 mA | 5.25 | } V _Q = 0 |
| | -I _{Qscmax} | 55.0 | 55.0 | 55.0 mA | 5.25 | |
| <u>SUPPLY DATA</u> | | | | | | |
| Supply current; HIGH input G ₁ ; G ₂ ; T | I _{PH} typ. < | 35 | 35 | 35 mA | 5.0 | |
| | | 60 | 60 | 60 mA | 5.0 | |

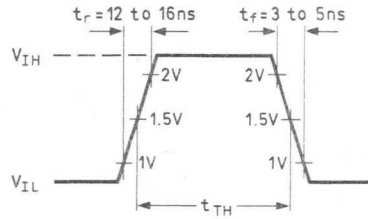
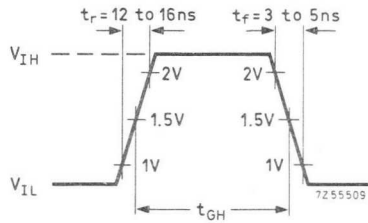
Note 1: Not more than one output should be short circuited at a time.

CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and References | |
|----------------------------------------------------------------|-----------------------|-----------------------|----|----|---------------------------|-----|
| | | 0 | 25 | 70 | VP (V) | |
| <u>DYNAMIC DATA</u> | | | | | | |
| <u>Performance</u> | | | | | | |
| Rise propagation delay time (F→Q) (see note 1) | t _{pdr} typ. | - | 24 | - | ns | 5.0 |
| | t _{pdr} ≤ | - | 40 | - | ns | 5.0 |
| Fall propagation delay time (F→Q) (see note 1) | t _{pdf} typ. | - | 27 | - | ns | 5.0 |
| | t _{pdf} ≤ | - | 40 | - | ns | 5.0 |
| <u>Signal requirements</u> | | | | | | |
| Set-up time for G ₁ ; G ₂ inputs HIGH | t _{suH} ≥ | - | 25 | - | ns | 5.0 |
| | t _{suL} ≥ | - | 25 | - | ns | 5.0 |
| Clock pulse width | t _{TH} > | - | 25 | - | ns | 5.0 |
| G ₁ ; G ₂ input width | t _{GH} > | - | 25 | - | ns | 5.0 |
| Hold time | t _{hold} ≥ | - | 0 | - | ns | 5.0 |
| Maximum operating shift frequency | f ≥ | - | 10 | - | MHz | 5.0 |



Note 1: Refers to propagation delay from seventh bit to output stage.

CHARACTERISTICS (continued)DYNAMIC DATA**T INPUT****G₁ · G₂ INPUT**

Waveforms illustrating input signals

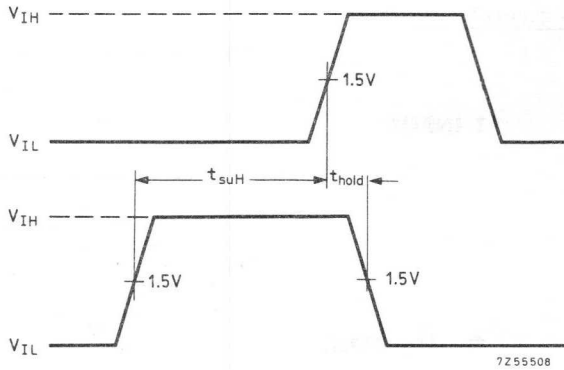
CHARACTERISTICS (continued)

DYNAMIC DATA

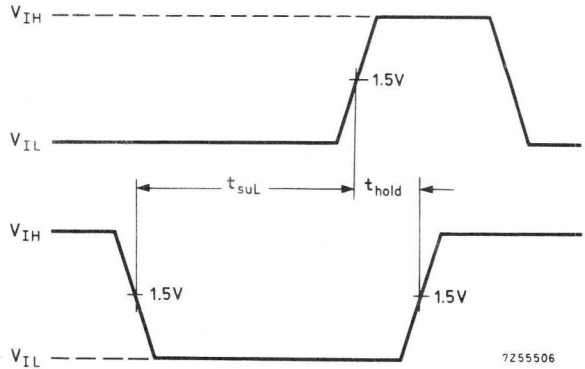
In general case

T INPUT

G₁·G₂ INPUT



Waveforms illustrating measurement of set-up and hold times to **guarantee** shifting operation, for HIGH logic level.

CHARACTERISTICS (continued)DYNAMIC DATAIn general case**T INPUT****G₁·G₂ INPUT**

Waveforms illustrating measurement of set-up and hold times to **guarantee** shifting operation, for LOW logic level.

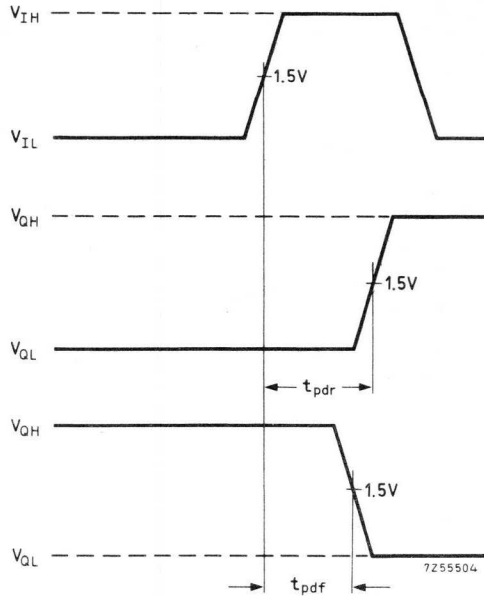
CHARACTERISTICS (continued)

DYNAMIC DATA

T INPUT

Q₁ OUTPUT

Q₂ OUTPUT



Waveforms illustrating measurement of t_{pdr} and t_{pdf} if S input of eight bit at logic HIGH level is 25 ns prior to rising edge of T input. (thold = 0 ns)

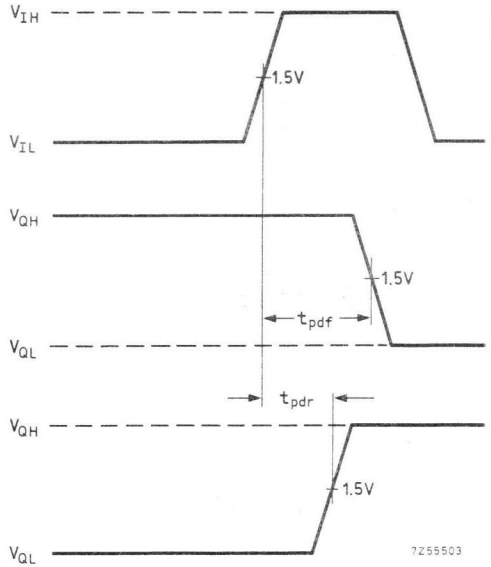
CHARACTERISTICS (continued)

DYNAMIC DATA

T INPUT

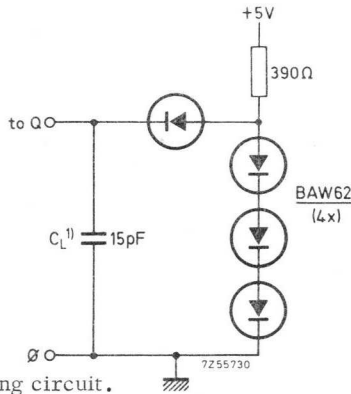
Q₁ OUTPUT

Q₂ OUTPUT



7255503

Waveforms illustrating measurement of t_{pdr} and t_{pdf} if S input of eight bit at logic LOW level is 25 ns prior to rising edge of T input ($t_{hold} = 0$ ns).

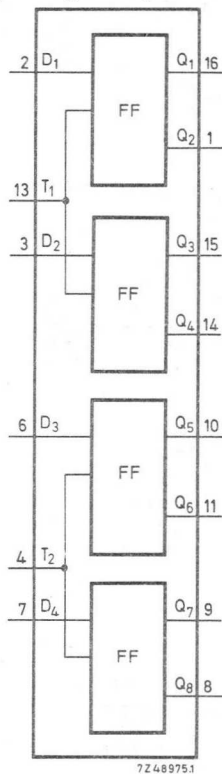


To output Q₂ the same loading circuit.

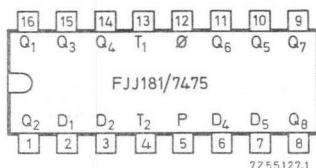
¹) Including probe and jig capacitance

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.



QUADRUPLE LATCH D FLIP-FLOP



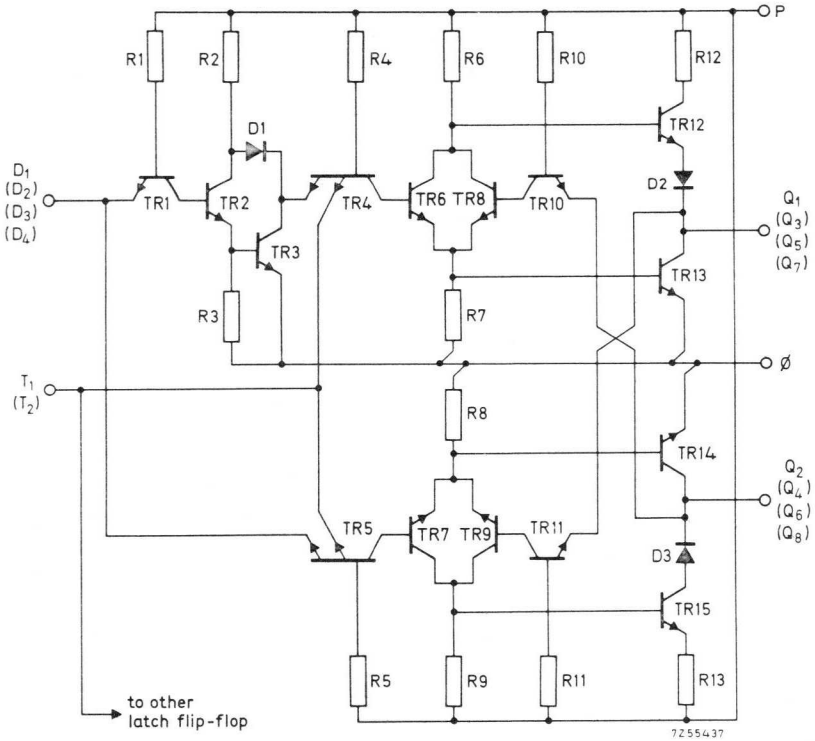
PACKAGE OUTLINE:

16 lead plastic dual in-line (type A) (See General Section)

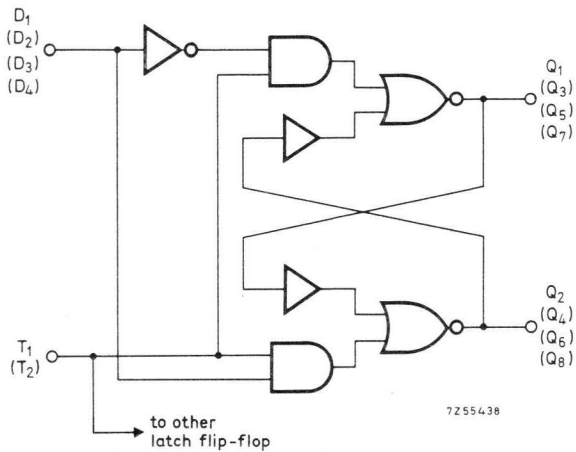
QUICK REFERENCE DATA

| | | |
|--------------------------------------------------------|-----------|-------------------------|
| Supply voltage | V_P | $5.0 \pm 5\%$ V |
| Operating ambient temperature range | T_{amb} | 0 to +70 °C |
| Available d.c. fan-out (full temperature range) | N_d | ≥ 10 |
| D.C. noise margin (full temperature range) | M_L | > 0.4 V typ. 1.0 V |
| Average power consumption (total) $T_{amb} = 25$ °C | P_{av} | typ. 160 mW |

CIRCUIT DIAGRAM



LOGIC DIAGRAM



LOGIC FUNCTION

Information present at a data input is transferred to the Q output. For so long as the trigger input is HIGH, the Q output will follow the data input. When the trigger goes LOW, the information present at the data input at the time of transition is retained at the Q output until the trigger again goes HIGH.

Function table (each gate)

| t_n data input | t_{n+1} output Q |
|---------------------|-----------------------|
| L | L |
| H | H |

H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)
 t_n = bit time before trigger pulse
 t_{n+1} = bit time after rising edge of trigger pulse

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|------------------------------------|------------|------|-------------|-----------------|
| Supply voltage | V_p | max. | 7.0 | V |
| Input voltage | V_D, V_T | max. | 5.5 | V ¹⁾ |
| Peak negative input voltage (D, T) | $-V_M$ | max. | 2 | V ²⁾ |
| Storage temperature | T_{stg} | | -55 to +150 | °C |
| Operating ambient temperature | T_{amb} | | 0 to +70 | °C |

¹⁾ In addition the voltage between any two input must not exceed 5.5 V.

²⁾ Pulse duration $t_p = 20$ ns; repetition frequency $f = 5$ MHz; source resistance $R_S \geq 75 \Omega$.

CHARACTERISTICS

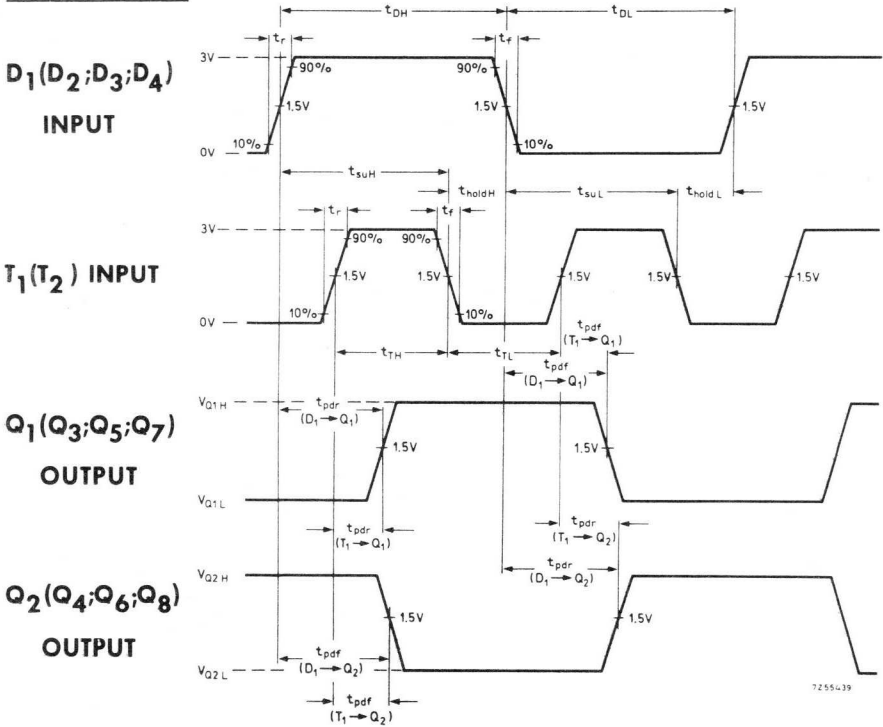
| | | T _{amb} (°C) | | | Conditions and references | |
|-------------------------------------|--------------------------|-----------------------|-----|-----|---------------------------|----------------------------------------------------------|
| | | 0 | 25 | 70 | V _P (V) | |
| <u>STATIC DATA</u> | | | | | | |
| <u>Voltages</u> | | | | | | |
| Input threshold LOW (any input) | V _{ILmax} | 0.8 | 0.8 | 0.8 | | |
| Input threshold HIGH (any input) | V _{IHmin} | 2.0 | 2.0 | 2.0 | | |
| Output LOW | V _{QLmax} | 0.4 | 0.4 | 0.4 | 4.75 | I _Q = I _{QLmax} |
| Output HIGH | V _{QHmin} | 2.4 | 2.4 | 2.4 | 4.75 | -I _Q = -I _{QHmax} |
| <u>Currents</u> | | | | | | |
| Input LOW (D) | -I _{DLmax} | 3.2 | 3.2 | 3.2 | 5.25 | V _D = V _{QLmax} ; I _Q = 0 |
| Input HIGH (D) | I _{DHmax} | 80 | 80 | 80 | 5.25 | V _D = V _{QHmin} ; I _Q = 0 |
| Input LOW (T) | -I _{TLmax} | 6.4 | 6.4 | 6.4 | 5.25 | V _T = V _{QLmax} ; I _Q = 0 |
| Input HIGH (T) | I _{THmax} | 160 | 160 | 160 | 5.25 | V _T = V _{QHmin} ; I _Q = 0 |
| Output LOW | I _{QLmax} | 16 | 16 | 16 | | |
| Output short circuited | -I _{Qscmin} | 18 | 18 | 18 | } 5.25 | |
| | -I _{Qscmax} | 57 | 57 | 57 | | |
| <u>SUPPLY DATA</u> | | | | | | |
| Supply current (total) | I _P typ. < | 32 | 32 | 32 | 5.0 | V _T = V _D = 0 V |
| | | 53 | 53 | 53 | 5.0 | |

CHARACTERISTICS

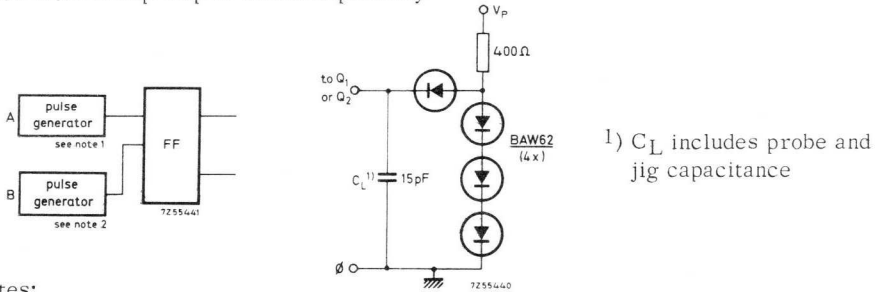
| | | T _{amb} (°C) | | Conditions and References | |
|---------------------------------|--------------------------------------------------------------------------------------------------------|--------------------------|------|------------------------------------------------|--------------------|
| | | 0 | 25 | 70 | V _p (V) |
| <u>DYNAMIC DATA</u> | | | | C _L = 15 pF; R _L = 400 Ω | |
| <u>Performance</u> | | | | | |
| Set-up time | | | | | |
| D inputs: | | | | | |
| HIGH | | t _{suH} typ. | - 7 | - ns | 5 † |
| | | t _{suH} < | - 20 | - ns | 5 |
| LOW | | t _{suL} typ. | - 14 | - ns | 5 |
| | | t _{suL} < | - 20 | - ns | 5 |
| Hold time | | | | | |
| D inputs: | | | | | |
| HIGH | | t _{hold H} typ. | - 15 | - ns | 5 |
| LOW | | t _{hold L} typ. | - 6 | - ns | 5 |
| <u>Propagation delay times:</u> | | | | | |
| Rise | D → Q ₁ (Q ₃ ; Q ₅ ; Q ₇) | t _{pdr} < | - 30 | - ns | 5 |
| Fall | D → Q ₁ (Q ₃ ; Q ₅ ; Q ₇) | t _{pdf} < | - 25 | - ns | 5 |
| Rise | D → Q ₂ (Q ₄ ; Q ₆ ; Q ₈) | t _{pdr} < | - 40 | - ns | 5 |
| Fall | D → Q ₂ (Q ₄ ; Q ₆ ; Q ₈) | t _{pdf} < | - 15 | - ns | 5 |
| Rise | T ₁ → Q ₁ (Q ₃) T ₂ → Q ₅ (Q ₇) | t _{pdr} < | - 30 | - ns | 5 |
| Fall | T ₁ → Q ₁ (Q ₃) T ₂ → Q ₅ (Q ₇) | t _{pdf} < | - 15 | - ns | 5 |
| Rise | T ₁ → Q ₂ (Q ₄) T ₂ → Q ₆ (Q ₈) | t _{pdr} < | - 30 | - ns | 5 |
| Fall | T ₁ → Q ₂ (Q ₄) T ₂ → Q ₆ (Q ₈) | t _{pdf} < | - 15 | - ns | 5 |

CHARACTERISTICS (continued)

DYNAMIC DATA



Waveforms illustrating measurement of t_{pdr} and t_{pdf} . Each latch D flip-flop is tested separately



1) C_L includes probe and jig capacitance

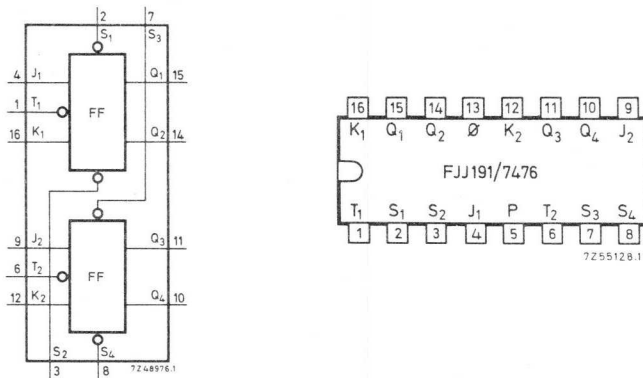
Notes:

1. Pulse generator A: $V_A = 3V$; $t_r \leq 10 \text{ ns}$; $t_f \leq 10 \text{ ns}$; $R_S = 50 \Omega$; $t_{DH} = t_{DL} = 1 \mu\text{s}$; $f = 500 \text{ kHz}$
2. Pulse generator B: $V_B = 3V$; $t_r \leq 10 \text{ ns}$; $t_f \leq 10 \text{ ns}$; $R_S = 50 \Omega$; $t_{TH} = t_{TL} = 500 \text{ ns}$; $f = 1 \text{ MHz}$

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

DUAL JK MASTER-SLAVE FLIP-FLOP



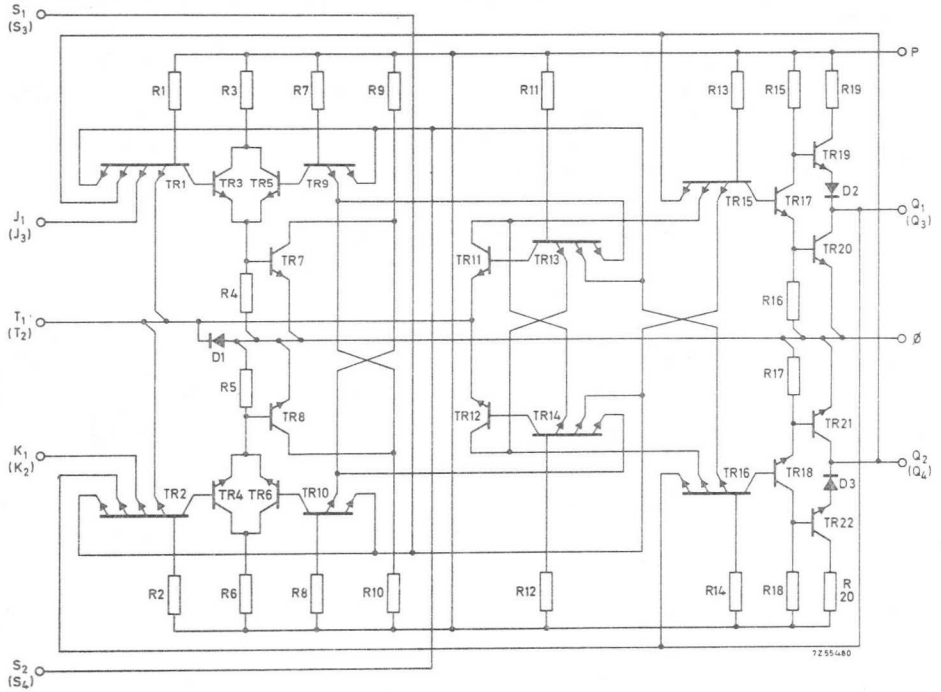
QUICK REFERENCE DATA

| | | |
|---------------------------------------------------------------|------------------|-----------------------|
| Supply voltage | V _p | 5.0 ± 5% V |
| Operating ambient temperature range | T _{amb} | 0 to +70 °C |
| Maximum operating frequency | f | ≥ 15 MHz |
| Available d. c. fan-out (full temperature range) | N _a | ≥ 10 |
| D.C. noise margin (full temperature range) | M _L | > 0.4 V typ. 1.0 V |
| Average power consumption (total) T _{amb} = 25 °C | P _{av} | typ. 80 mW |

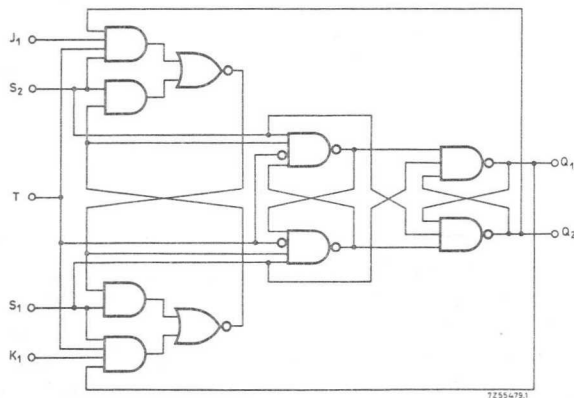
The FJJ191/7476 is a dual JK master-slave flip-flop having one J and one K input per flip-flop. The circuits operate at a frequency up to 15 MHz (typ.) The information at the J and K inputs enters the master when T is HIGH. Afterwards, when T is LOW, the information is transferred from the master to the slave and appears at the outputs. The SET signals on S₁ and S₂ (S₃ and S₄) which override any other inputs, are active at the LOW level.

PACKAGE OUTLINE: 16 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM



LOGIC FUNCTION

LOW input to $S_1(S_3)$ sets $Q_1(Q_3)$ to HIGH } independent of trigger pulse
 LOW input to $S_2(S_4)$ sets $Q_1(Q_3)$ to LOW }

Function table for J and K inputs

| t_n | | t_{n+1} |
|-------|---|---------------------|
| J | K | Q_1 |
| L | L | $\overline{Q_{1n}}$ |
| L | H | L |
| H | L | H |
| H | H | Q_{1n} |

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

t_n = bit time before trigger pulse

t_{n+1} = bit time after trigger pulse

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|------------------------------------------|----------------------|------|---------------------|
| Supply voltage | V_P | max. | 7.0 V |
| Input voltage | V_J, V_K, V_T, V_S | max. | 5.5 V ¹⁾ |
| Peak negative input voltage (J, K, T, S) | $-V_M$ | max. | 2 V ²⁾ |
| Storage temperature | T_{stg} | | -55 to +125 °C |
| Operating ambient temperature | T_{amb} | | 0 to +70 °C |

¹⁾ In addition the voltage between any two inputs must not exceed 5.5 V.

²⁾ Pulse duration $t_p = 20$ ns; repetition frequency $f = 5$ MHz; source resistance $R_S \geq 75 \Omega$.

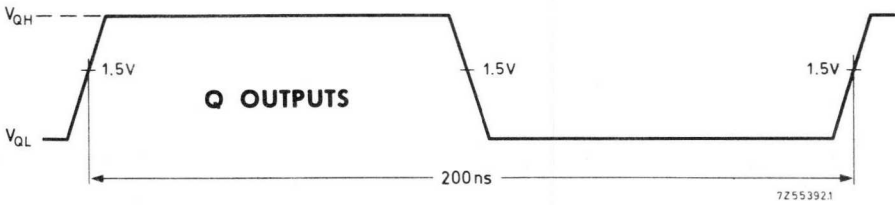
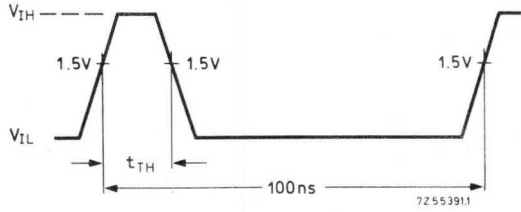
CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and references | |
|-------------------------------------|-----------------------|-----------------------|-----|-----|---------------------------|-------------------------------------------------------------|
| | | 0 | 25 | 75 | V _P (V) | |
| STATIC DATA | | | | | | |
| <u>Voltages</u> | | | | | | |
| Input threshold LOW (any input) | V _{ILmax} | 0.8 | 0.8 | 0.8 | | |
| Input threshold HIGH (any input) | V _{IHmin} | 2.0 | 2.0 | 2.0 | | |
| Output LOW | V _{QLmax} | 0.4 | 0.4 | 0.4 | 4.75 | I _Q = I _{QLmax} |
| Output HIGH | V _{QHmin} | 2.4 | 2.4 | 2.4 | 4.75 | -I _Q = -I _{QHmax} |
| <u>Currents</u> | | | | | | |
| Input LOW (J, K) | -I _{ILmax} | 1.6 | 1.6 | 1.6 | 5.25 | V _I = V _{QLmax} ; I _Q = 0 |
| Input HIGH (J, K) | I _{IHmax} | 40 | 40 | 40 | 5.25 | V _I = V _{QHmin} ; I _Q = 0 |
| Input LOW (S, T) | -I _{SLmax} | 3.2 | 3.2 | 3.2 | 5.25 | V _{S, T} = V _{QLmax} ; I _Q = 0 |
| | -I _{TLmax} | 3.2 | 3.2 | 3.2 | | |
| Input HIGH (S, T) | I _{SHmax} | 80 | 80 | 80 | 5.25 | V _{S, T} = V _{QHmin} ; I _Q = 0 |
| | I _{THmax} | 80 | 80 | 80 | | |
| Output LOW | I _{QL} | 16 | 16 | 16 | | |
| Output short circuited | -I _{Qscmin} | 18 | 18 | 18 | 5.25 | V _I = 0; V _Q = 0 |
| | -I _{Qscmax} | 57 | 57 | 57 | 5.25 | |
| <u>SUPPLY DATA</u> | | | | | | |
| Supply current (total) | I _p typ. | 16 | 16 | 16 | 5.0 | |
| | < | 40 | 40 | 40 | 5.0 | |
| <u>DYNAMIC DATA</u> | | | | | | |
| <u>Signal requirements</u> | | | | | | |
| Pulse duration (T input) | t _{TH} > | - | 20 | - | 5.0 | |
| Pulse duration (S input) | t _{SL} > | - | 25 | - | 5.0 | |
| <u>Performance</u> | | | | | | |
| Rise propagation delay time (S → Q) | t _{pdr} typ. | - | 16 | - | 5.0 | N = 10; C _L = 15 pF |
| | < | - | 25 | - | 5.0 | |
| Fall propagation delay time (S → Q) | t _{pdr} typ. | - | 25 | - | 5.0 | N = 10; C _L = 15 pF |
| | < | - | 40 | - | 5.0 | |
| Rise propagation delay time (T → Q) | t _{pdr} > | - | 10 | - | 5.0 | N = 10; C _L = 15 pF |
| | typ. | - | 16 | - | 5.0 | |
| | < | - | 25 | - | 5.0 | |
| Fall propagation delay time (T → Q) | t _{pdr} > | - | 10 | - | 5.0 | N = 10; C _L = 15 pF |
| | typ. | - | 25 | - | 5.0 | |
| | < | - | 40 | - | 5.0 | |
| Maximum operating frequency | f > | - | 15 | - | 5.0 | N = 10; C _L = 15 pF |
| | typ. | - | 20 | - | 5.0 | |

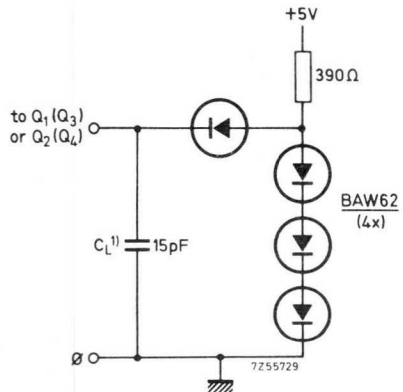
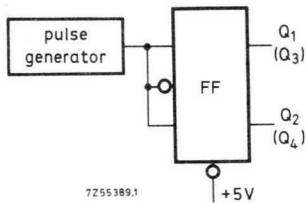
CHARACTERISTICS (continued)

DYNAMIC DATA

T, J and K INPUTS



Waveforms illustrating in- and output pulses

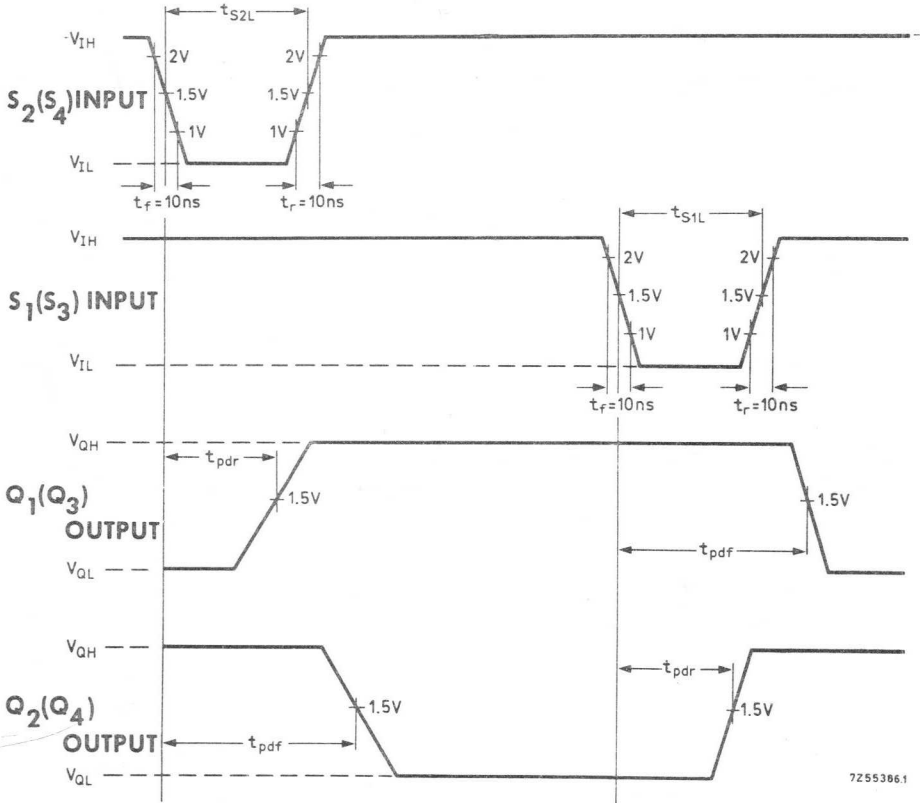


¹⁾ Including probe and jig capacitance

Equivalent load for $N = 10$

CHARACTERISTICS (continued)

DYNAMIC DATA

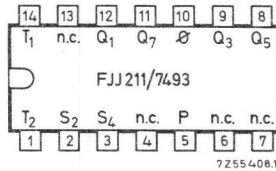
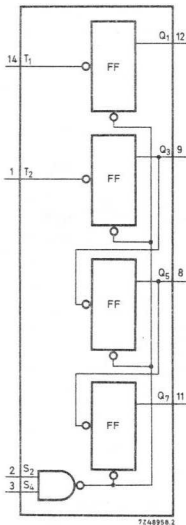


Waveforms illustrating switching times

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

SINGLE ASYNCHRONOUS 4-BIT BINARY COUNTER

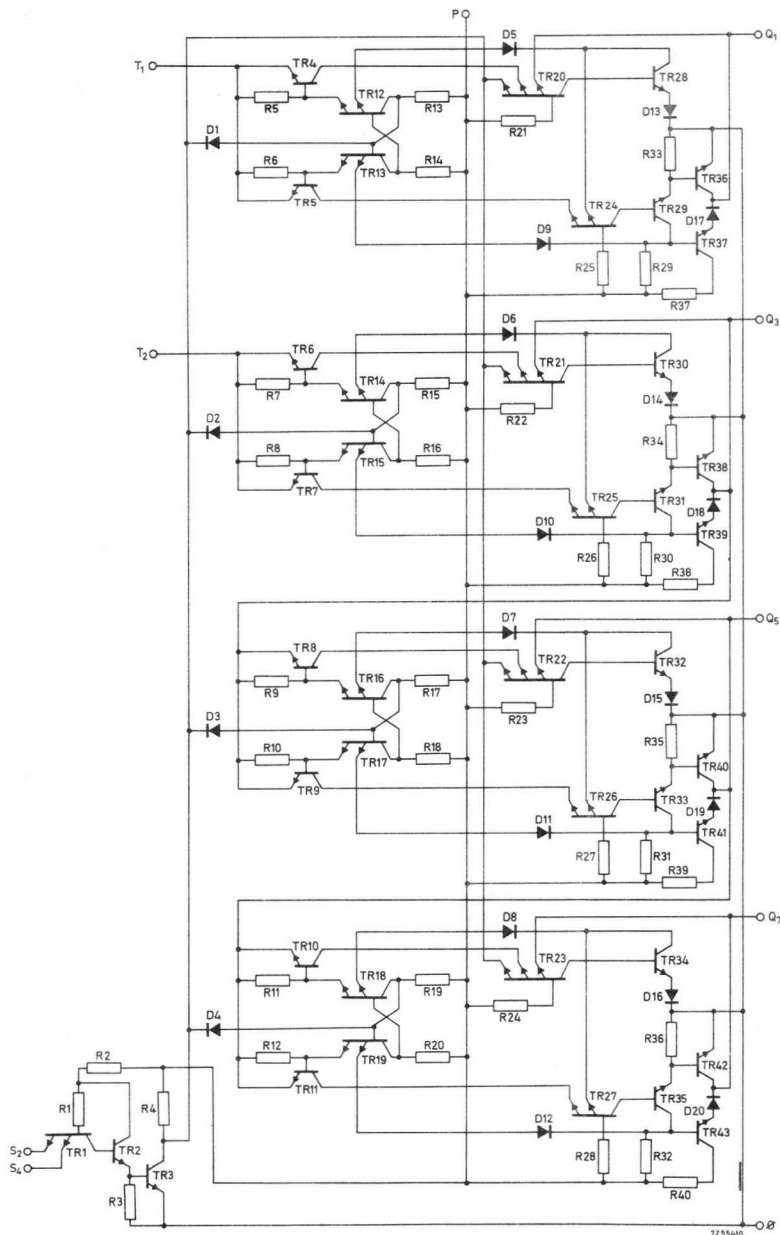


QUICK REFERENCE DATA

| | | |
|--------------------------------------------------------|-----------|-------------------------|
| Supply voltage | V_P | $5.0 \pm 5\%$ V |
| Operating ambient temperature | T_{amb} | 0 to +70 °C |
| Maximum operating frequency | f | ≥ 10 MHz |
| Available d.c. fan-out (full temperature range) | N_a | ≥ 10 |
| D.C. noise margin (full temperature range) | M_L | > 0.4 V typ. 1.0 V |
| Average power consumption (total) $T_{amb} = 25$ °C | P_{av} | typ. 128 mW |

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



725540

The FJJ211/7493 is a high-speed asynchronous 4-bit binary counter with four master-slave flip-flops which are internally connected to provide a divide-by-two and a divide-by-eight counter. By using an external connection a count of sixteen can be obtained. A gated line, direct reset inhibits the count and simultaneously all flip-flop outputs return to the LOW state.

For use as a 4-bit ripple-through counter, externally connect Q_1 to T_2 ; apply the count pulses to T_1 . As shown by the function table below, the outputs at Q_1 , Q_3 , Q_5 and Q_7 represent division by 2, 4, 8 and 16 respectively.

For use as 3-bit ripple-through counter, apply the count pulses to T_2 . Simultaneous divisions by 2, 4 and 8 are available at the outputs Q_3 , Q_5 and Q_7 . The first flip-flop (T_1 and Q_1) can be used independently if the reset function (S_2 and S_4) coincides with reset of the 3-bit ripple-through counter.

FUNCTION TABLES

| count | outputs | | | |
|-------|---------|-------|-------|-------|
| | Q_1 | Q_3 | Q_5 | Q_7 |
| 0 | L | L | L | L |
| 1 | H | L | L | L |
| 2 | L | H | L | L |
| 3 | H | H | L | L |
| 4 | L | L | H | L |
| 5 | H | L | H | L |
| 6 | L | H | H | L |
| 7 | H | H | H | L |
| 8 | L | L | L | H |
| 9 | H | L | L | H |
| 10 | L | H | L | H |
| 11 | H | H | L | H |
| 12 | L | L | H | H |
| 13 | H | L | H | H |
| 14 | L | H | H | H |
| 15 | H | H | H | H |

Notes:

1. Q_1 connected to T_2
2. To reset all outputs in the LOW state, S_2 and S_4 inputs must be HIGH.
3. Either S_2 or S_4 (or both) must be LOW to count.

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|------------------------------------|------------|------|---------------------|
| Supply voltage | V_P | max. | 7.0 V |
| Input voltage | $V_T; V_S$ | max. | 5.5 V ¹⁾ |
| Peak negative input voltage (T, S) | $-V_M$ | max. | 2 V ²⁾ |
| Storage temperature | T_{stg} | | -55 to +150 °C |
| Operating ambient temperature | T_{amb} | | 0 to +70 °C |

1) In addition the input voltage between any two T inputs or between any two S inputs: max. 5.5 V.

2) Pulse duration $t_p = 20$ ns; repetition frequency $f = 5$ MHz; source resistance $R_S \geq 75 \Omega$.

CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and References | | |
|-------------------------------------------------------------------|----------------------|-----------------------|-------|----------|---------------------------|-------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|
| | | 0 | 25 | 70 | V _P (V) | | |
| <u>STATIC DATA</u> | | | | | | | |
| <u>Voltages</u> | | | | | | | |
| Input threshold LOW | | | | | | | |
| S ₂ ; S ₄ ; T ₁ | V _{S2Lmax} | } 0.8 | } 0.8 | } 0.8 V | } 4.75 | | |
| | V _{S4Lmax} | | | | | | |
| | V _{T1Lmax} | | | | | | |
| T ₂ | V _{T2Lmax} | | | | | | |
| Input threshold HIGH | | | | | | | |
| S ₂ ; S ₄ ; T ₁ | V _{S2Hmin} | } 2.0 | } 2.0 | } 2.0 V | } 4.75 | | |
| | V _{S4Hmin} | | | | | | |
| | V _{T1Hmin} | | | | | | |
| T ₂ | V _{T2Hmin} | | | | | | |
| Output LOW | | | | | | | |
| Q ₁ ; Q ₃ ; Q ₅ ; Q ₇ | V _{Q1Lmax} | } 0.4 | } 0.4 | } 0.4 V | } 4.75 | { Q ₁ connected to T ₂ I _Q = I _{QLmax} | |
| | V _{Q3Lmax} | | | | | | |
| | V _{Q5Lmax} | | | | | | |
| | V _{Q7Lmax} | | | | | | |
| Output HIGH | | | | | | | |
| Q ₁ ; Q ₃ ; Q ₅ ; Q ₇ | V _{Q1Hmin} | } 2.4 | } 2.4 | } 2.4 V | } 4.75 | | { Q ₁ connected to T ₂ I _Q = -I _{QHmax} |
| | V _{Q3Hmin} | | | | | | |
| | V _{Q5Hmin} | | | | | | |
| | V _{Q7Hmin} | | | | | | |
| <u>Currents</u> | | | | | | | |
| Input LOW: S ₂ | -I _{S2Lmax} | } 1.6 | } 1.6 | } 1.6 mA | } 5.25 | V _S = V _{QLmax} | |
| S ₄ | -I _{S4Lmax} | | | | | | |
| T ₁ | -I _{T1Lmax} | } 3.2 | } 3.2 | } 3.2 mA | } 5.25 | | |
| T ₂ | -I _{T2Lmax} | | | | | | |
| Input HIGH: S ₂ | I _{S2Hmax} | } 40 | } 40 | } 40 μA | } 5.25 | V _S = V _{QHmin} | |
| S ₄ | I _{S4Hmax} | | | | | | |
| T ₁ | I _{T1Hmax} | } 80 | } 80 | } 80 μA | } 5.25 | | V _T = V _{QHmin} |
| T ₂ | I _{T2Hmax} | | | | | | |
| Output LOW | | | | | | | |
| Q ₁ ; Q ₃ ; Q ₅ ; Q ₇ | I _{Q1Lmax} | } 16 | } 16 | } 16 mA | } 4.75 | | |
| | I _{Q3Lmax} | | | | | | |
| | I _{Q5Lmax} | | | | | | |
| | I _{Q7Lmax} | | | | | | |

CHARACTERISTICS (continued)

| | | T _{amb} (°C) | | | Conditions and References | |
|----------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------|-----------------------|-----|-----|---------------------------|------|
| | | 0 | 25 | 70 | V _P (V) | |
| <u>STATIC DATA</u> (continued) | | | | | | |
| Output HIGH Q ₁ ; Q ₃ ; Q ₅ ; Q ₇ | -I _{Q1H} max -I _{Q3H} max -I _{Q5H} max -I _{Q7H} max | 400 | 400 | 400 | μA | 4.75 |
| Output short circuited Q ₁ ; Q ₃ ; Q ₅ ; Q ₇ (See note 2) | -I _{Q1scmin} -I _{Q3scmin} -I _{Q5scmin} -I _{Q7scmin} | 18 | 18 | 18 | mA | 5.25 |
| | -I _{Q1scmax} -I _{Q3scmax} -I _{Q5scmax} -I _{Q7scmax} | 57 | 57 | 57 | mA | 5.25 |
| <u>SUPPLY DATA</u> | | | | | | |
| Supply current | I _P typ. | - | 32 | - | mA | 5 |
| <u>DYNAMIC DATA</u> | | | | | | |
| Rise propagation delay time (note 1) | t _{pdr} typ. t _{pdr} < | - | 75 | - | ns | 5 |
| Fall propagation delay time (note 1) | t _{pdf} typ. t _{pdf} < | - | 135 | - | ns | 5 |
| Rise time | t _r < | - | 10 | - | ns | 5 |
| Fall time | t _f < | - | 10 | - | ns | 5 |
| Trigger time HIGH | t _{T1H} ; t _{T2H} < | - | 50 | - | ns | 5 |
| Trigger time LOW | t _{T1L} ; t _{T2L} < | - | 50 | - | ns | 5 |
| Width of pulse S ₂ and S ₄ , LOW | t _{S2L} ; t _{S4L} < | - | 50 | - | ns | 5 |

Note 1:

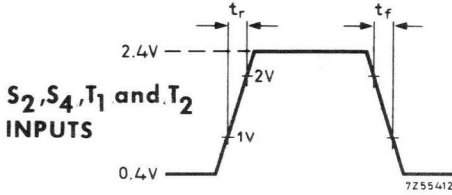
All four outputs loaded. Output Q₁ connected to input T₂.

Note 2:

Not more than one output should be short circuited at a time.

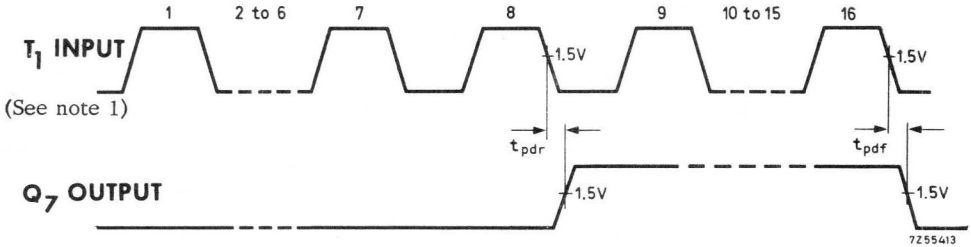
CHARACTERISTICS (continued)

DYNAMIC DATA



Pulse generator:

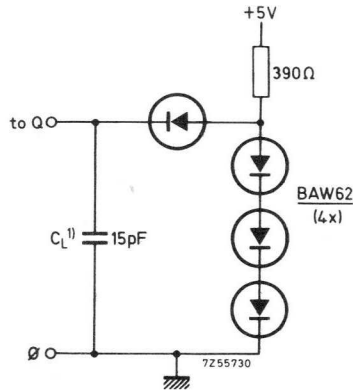
- $t_r < 10 \text{ ns}$
- $t_f < 10 \text{ ns}$
- $f = 1 \text{ MHz}$
- duty cycle $\delta = 0.5$



Waveforms illustrating measurement of t_{pdr} and t_{pdf}

Note 1:

T₁ input (Q₁ output connected to T₂ input)

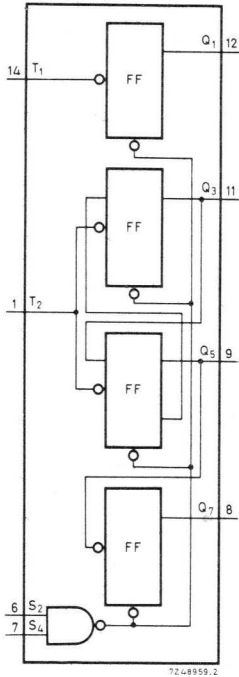


To outputs Q₃, Q₅ and Q₇ the same loading circuit.

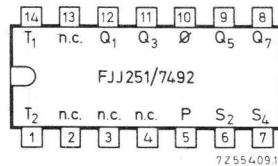
¹⁾ Including probe and jig capacitance.

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.



SINGLE ASYNCHRONOUS 4-BIT BINARY COUNTER



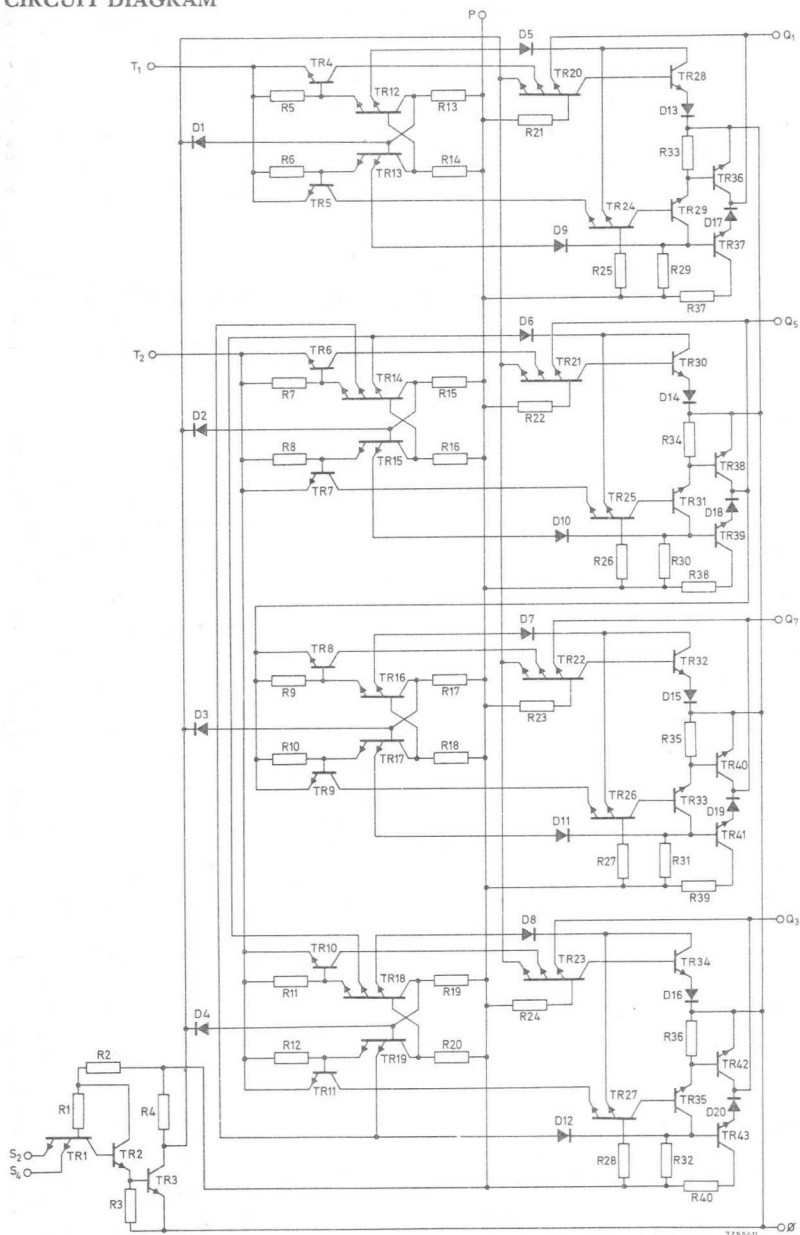
PACKAGE OUTLINE :

14 lead plastic dual in-line (type A)
(See General Section)

QUICK REFERENCE DATA

| | | |
|---------------------------------------------------------------|------------------|-----------------------|
| Supply voltage | V _p | 5.0 ± 5% V |
| Operating ambient temperature | T _{amb} | 0 to +70 °C |
| Maximum operating frequency | f | ≥ 10 MHz |
| Available d.c. fan-out (full temperature range) | N _a | ≥ 10 |
| D.C. noise margin (full temperature range) | M _L | > 0.4 V typ. 1.0 V |
| Average power consumption (total) T _{amb} = 25 °C | P _{av} | typ. 155 mW |

CIRCUIT DIAGRAM



7255411

The FJJ251/7492 is a high-speed asynchronous 4-bit binary counter with four master-slave flip-flops which are internally connected to provide a divide-by-two and a divide-by-six counter. By using an external connection a count of twelve can be obtained. A gated line, direct reset inhibits the count and simultaneously all flip-flop outputs return to the LOW state.

For use as a divide-by-twelve counter, externally connect Q_1 to T_2 ; apply the count pulses to T_1 .

Simultaneous divisions by 2, 6 and 12 are available at the outputs Q_1 , Q_5 and Q_7 as shown in the function table below. For use as a divide-by-six counter, apply the count pulses to T_2 .

Simultaneous divisions by 3 and 6 are available at the outputs Q_5 and Q_7 .

The first flip-flop (T_1 and Q_1) can be used independently if the reset function coincides with reset of the divide-by-six counter.

FUNCTION TABLE

| count | outputs | | | |
|-------|---------|-------|-------|-------|
| | Q_1 | Q_3 | Q_5 | Q_7 |
| 0 | L | L | L | L |
| 1 | H | L | L | L |
| 2 | L | H | L | L |
| 3 | H | H | L | L |
| 4 | L | L | H | L |
| 5 | H | L | H | L |
| 6 | L | L | L | H |
| 7 | H | L | L | H |
| 8 | L | H | L | H |
| 9 | H | H | L | H |
| 10 | L | L | H | H |
| 11 | H | L | H | H |

Notes:

- Q_1 connected to T_2
- To reset all outputs in the LOW state, S_2 and S_4 inputs must be HIGH.
- Either S_2 or S_4 (or both) must be LOW to count.

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|------------------------------------|------------|-------------|---------------------|
| Supply voltage | V_P | max. | 7.0 V |
| Input voltage | $V_T; V_S$ | max. | 5.5 V ¹⁾ |
| Peak negative input voltage (T, S) | $-V_M$ | max. | 2 V ²⁾ |
| Storage temperature | T_{stg} | -55 to +150 | °C |
| Operating ambient temperature | T_{amb} | 0 to +70 | °C |

¹⁾ In addition the input voltage between any two T inputs or between any two S inputs: max. 5.5 V.

²⁾ Pulse duration $t_p = 20$ ns; repetition frequency $f = 5$ MHz; source resistance $R_S \geq 75\Omega$.

CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and References | |
|----------------------------------------------------------------------------------|----------------------|-----------------------|-----|--------|---------------------------|------------------------------------------------------------------------------------|
| | | 0 | 25 | 75 | V _P (V) | |
| <u>STATIC DATA</u> | | | | | | |
| <u>Voltages</u> | | | | | | |
| Input threshold LOW S ₂ ; S ₄ ; T ₁ | V _{S2Lmax} | } 0.8 | 0.8 | 0.8 V | 4.75 | |
| | V _{S4Lmax} | | | | | |
| | V _{T1Lmax} | | | | | |
| | V _{T2Lmax} | | | | | |
| Input threshold HIGH S ₂ ; S ₄ ; T ₁ | V _{S2Hmin} | } 2.0 | 2.0 | 2.0 V | 4.75 | |
| | V _{S4Hmin} | | | | | |
| | V _{T1Hmin} | | | | | |
| | V _{T2Hmin} | | | | | |
| Output LOW Q ₁ ; Q ₃ ; Q ₅ ; Q ₇ | V _{Q1Lmax} | } 0.4 | 0.4 | 0.4 V | 4.75 | Q ₁ connected to T ₂ I _Q = I _{QLmax} |
| | V _{Q3Lmax} | | | | | |
| | V _{Q5Lmax} | | | | | |
| | V _{Q7Lmax} | | | | | |
| Output HIGH Q ₁ ; Q ₃ ; Q ₅ ; Q ₇ | V _{Q1Hmin} | } 2.4 | 2.4 | 2.4 V | 4.75 | Q ₁ connected to T ₂ I _Q = -I _{QHmax} |
| | V _{Q3Hmin} | | | | | |
| | V _{Q5Hmin} | | | | | |
| | V _{Q7Hmin} | | | | | |
| <u>Currents</u> | | | | | | |
| Input LOW: S ₂ S ₄ T ₁ T ₂ | -I _{S2Lmax} | } 1.6 | 1.6 | 1.6 mA | 5.25 | V _S = V _{QLmax} |
| | -I _{S4Lmax} | | | | | |
| | -I _{T1Lmax} | | | | | |
| | -I _{T2Lmax} | | | | | |
| Input HIGH: S ₂ S ₄ T ₁ T ₂ | I _{S2Hmax} | } 40 | 40 | 40 μA | 5.25 | V _S = V _{QHmin} |
| | I _{S4Hmax} | | | | | |
| | I _{T1Hmax} | | | | | |
| | I _{T2Hmax} | | | | | |
| Output LOW Q ₁ ; Q ₃ ; Q ₅ ; Q ₇ | I _{Q1Lmax} | } 16 | 16 | 16 mA | 4.75 | |
| | I _{Q3Lmax} | | | | | |
| | I _{Q5Lmax} | | | | | |
| | I _{Q7Lmax} | | | | | |

CHARACTERISTICS (continued)

| | | T _{amb} (°C) | | | Conditions and References | | |
|----------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------|-----------------------|-----|-----|---------------------------|------|--------------------------------------------------------------------------------------|
| | | | | | 0 | 25 | 75 |
| STATIC DATA (continued) | | | | | | | |
| Output HIGH Q ₁ ; Q ₃ ; Q ₅ ; Q ₇ | -I _{Q1Hmax} -I _{Q3Hmax} -I _{Q5Hmax} -I _{Q7Hmax} | 400 | 400 | 400 | mA | 4.75 | |
| Output short circuited Q ₁ ; Q ₃ ; Q ₅ ; Q ₇ (see note 2) | -I _{Q1scmin} -I _{Q3scmin} -I _{Q5scmin} -I _{Q7scmin} | 18 | 18 | 18 | mA | 5.25 | V _Q = 0; V _S = V _T = 0 |
| | -I _{Q1scmax} -I _{Q3scmax} -I _{Q5scmax} -I _{Q7scmax} | 57 | 57 | 57 | mA | 5.25 | V _Q = 0; V _S = V _T = 0 |
| SUPPLY DATA | | | | | | | |
| Supply current | I _p typ. < | - | 31 | - | mA | 5 | All inputs and outputs open |
| | | 51 | 51 | 51 | mA | 5 | |
| DYNAMIC DATA | | | | | | | |
| Rise propagation delay time (note 1) | t _{pdr} typ. < | - | 60 | - | ns | 5 | } C _L = 15pF; R _L = 390 Ω } f = 1 MHz; } duty cycle: 0.5 |
| Fall propagation delay time (note 1) | t _{pdf} typ. < | - | 60 | - | ns | 5 | |
| Rise time | t _r < | - | 10 | - | ns | 5 | |
| Fall time | t _f < | - | 10 | - | ns | 5 | |
| Trigger time HIGH | t _{T1H} ; t _{T2H} < | - | 50 | - | ns | 5 | |
| Trigger time LOW | t _{T1L} ; t _{T2L} < | - | 50 | - | ns | 5 | |
| Width of pulse S ₂ and S ₄ , LOW | t _{S2L} ; t _{S4L} < | - | 50 | - | ns | 5 | |

Note 1:

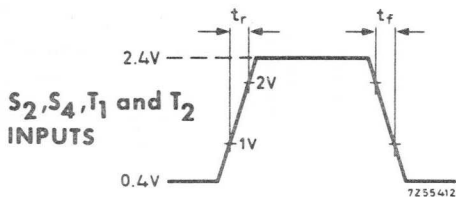
All four output loaded. Output Q₁ connected to input T₂.

Note 2:

Not more than one output should be short circuited at a time.

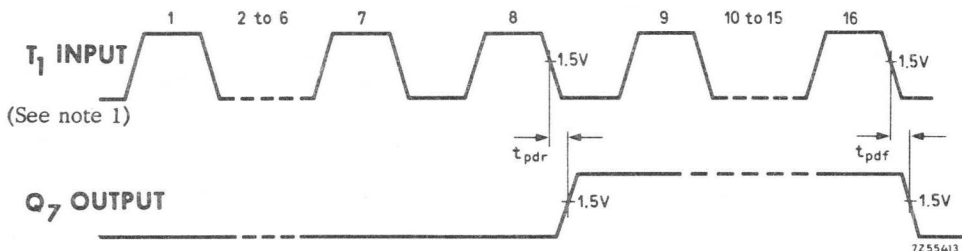
CHARACTERISTICS (continued)

DYNAMIC DATA



Pulse generator:

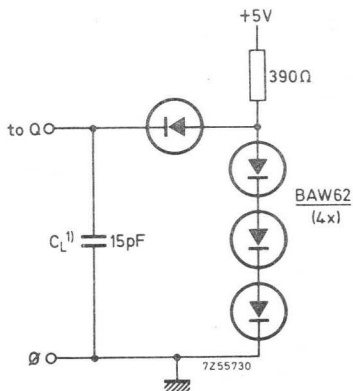
- $t_r < 10 \text{ ns}$
- $t_f < 10 \text{ ns}$
- $f = 1 \text{ MHz}$
- duty cycle $\delta = 0.5$



Waveforms illustrating measurement of t_{pdr} and t_{pdf}

Note 1:

T_1 input (Q_1 output connected to T_2 input)



To outputs Q_3 , Q_5 and Q_7 the same loading circuit.

1) Including probe and jig capacitance.

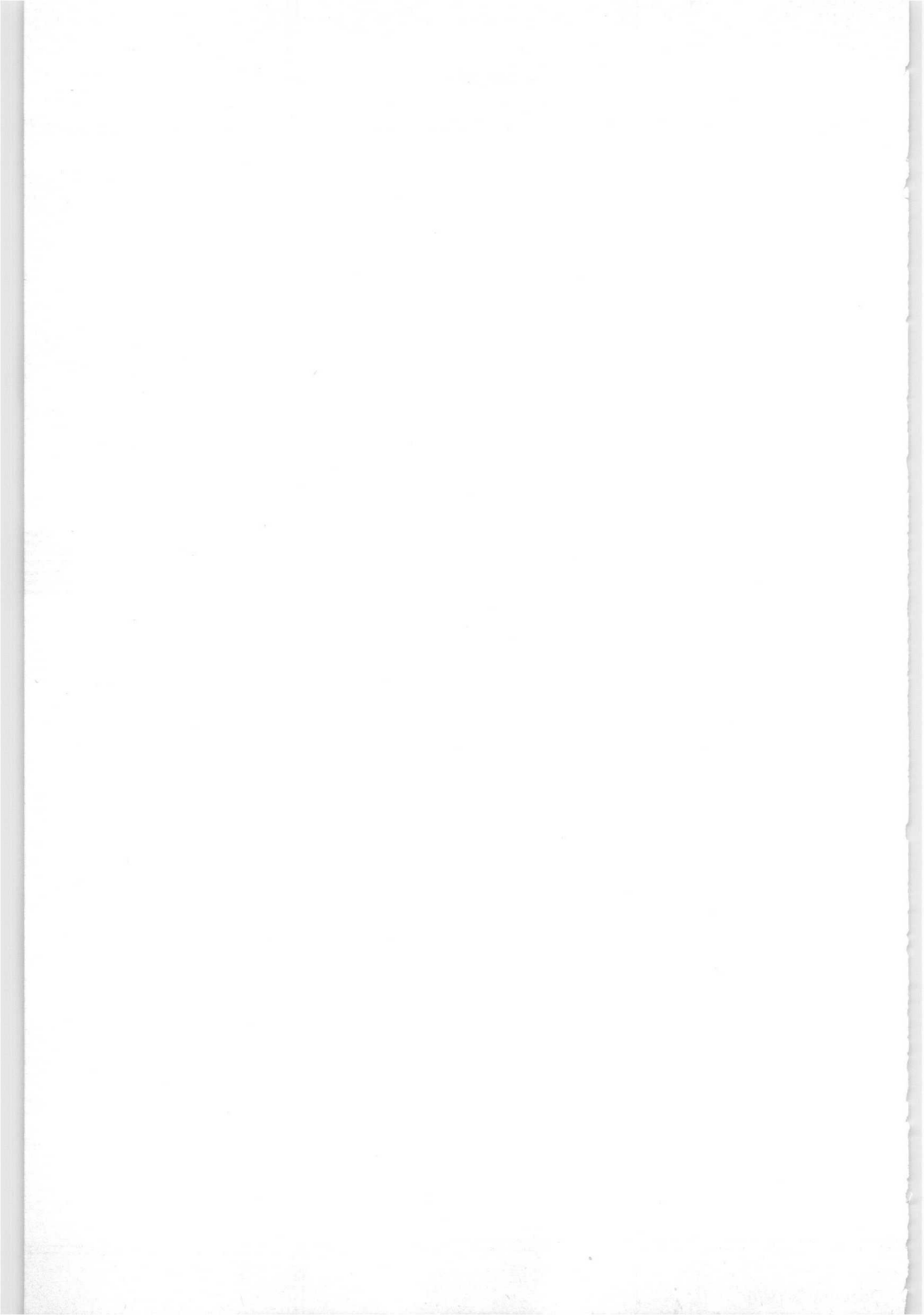
FJ family
standard temperature range

FJJ261/74107
dual JK flip-flop

DUAL JK MASTER-SLAVE FLIP-FLOP

For data of this type please refer to FJJ121/7473

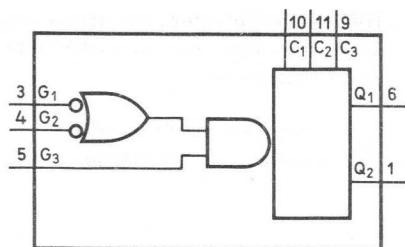




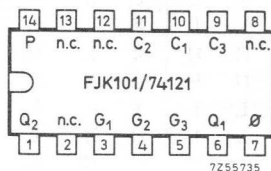
The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

MONOSTABLE MULTIVIBRATOR



7248997.1



QUICK REFERENCE DATA

| | | | |
|--------------------------------------------|-----------|---------------|-------|
| Supply voltage | V_P | $5.0 \pm 5\%$ | V |
| Operating ambient temperature | T_{amb} | 0 to +70 | °C |
| Available fan-out (each output) | N_a | \geq | 10 |
| Average power consumption (50% duty cycle) | P_{av} | typ. | 90 mW |

PACKAGE OUTLINE 14 lead plastic dual in-line (type A) (See General Section)

The FJK101/74121 monostable multivibrator features D.C. voltage level triggering which is not directly related to the input pulse transition time. The input gating allows the choice of triggering either on the positive or negative-going edge of the input pulse, as well as providing an inhibit facility. Both positive and negative output pulses are available with a full fan-out of 10 and TTL line driving capabilities.

G_1 and G_2 are negative-edge trigger inputs and will trigger the one-shot when either or both go LOW as long as G_3 is HIGH. G_3 is a positive-edge Schmitt-trigger input for slow edges or level detection, and will trigger the one-shot when G_3 goes HIGH as long as G_1 or G_2 are LOW.

Output pulse duration may be varied between 40 ns and 40 s and is determined by the value of external components used (see TIMING NOTES on page 6).

FUNCTION TABLE

| inputs | | | | | | outputs |
|--------|-------|-------|-----------|-------|-------|----------|
| t_n | | | t_{n+1} | | | |
| G_1 | G_2 | G_3 | G_1 | G_2 | G_3 | |
| H | H | L | H | H | H | inhibit |
| L | X | H | L | X | L | " |
| X | L | H | X | L | L | " |
| L | X | L | L | X | H | one-shot |
| X | L | L | X | L | H | " |
| H | H | H | X | L | H | " |
| H | H | H | L | X | H | " |
| X | L | L | X | H | L | inhibit |
| L | X | L | H | X | L | " |
| X | L | H | H | H | H | " |
| L | X | H | H | H | H | " |
| H | H | L | X | L | L | " |
| H | H | L | L | X | L | " |

H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)
 X = state immaterial

t_n = time before input transition
 t_{n+1} = time after input transition

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|----------------------------------|-----------|------|-------------|-----------------|
| Supply voltage | V_P | max. | 7.0 | V |
| D.C. input voltage | V_G | max. | 5.5 | V ¹⁾ |
| Negative transient input voltage | $-V_{GM}$ | max. | 2.0 | V ²⁾ |
| Storage temperature | T_{stg} | | -65 to +150 | °C |
| Operating ambient temperature | T_{amb} | | 0 to +70 | °C |

1) In addition, the voltage between any two inputs must not exceed 5.5 V.

2) Pulse duration $t_p = 20$ ns; repetition frequency $f = 5$ MHz; source resistance $R_S \geq 75\Omega$.

CHARACTERISTICS

| | | T _{amb} (°C) | | | Conditions and references | |
|------------------------------------------|-----------------------|-----------------------|------|-----|---------------------------|----------------------------|
| | | 0 | 25 | 70 | V _P (V) | |
| <u>STATIC DATA</u> | | | | | | |
| <u>Voltages</u> | | | | | | |
| Input threshold LOW (negative-going) | | | | | | |
| any input | V _{GLmin} | 0.8 | 0.8 | 0.8 | V | 4.75 |
| G ₁ ; G ₂ | V _{GLtyp} | - | 1.4 | - | V | 5.0 |
| G ₃ | V _{GLtyp} | - | 1.35 | - | V | 5.0 |
| Input threshold HIGH (positive-going) | | | | | | |
| any input | V _{GHmax} | 2.0 | 2.0 | 2.0 | V | 4.75 |
| G ₁ ; G ₂ | V _{GHtyp} | - | 1.4 | - | V | 5.0 |
| G ₃ | V _{GHtyp} | - | 1.55 | - | V | 5.0 |
| Output LOW | V _{QLmax} | 0.4 | 0.4 | 0.4 | V | 4.75 |
| | V _{QLtyp} | - | 0.22 | - | V | 5.0 |
| Output HIGH | V _{QHmin} | 2.4 | 2.4 | 2.4 | V | 4.75 |
| | V _{QHtyp} | - | 3.3 | - | V | 5.0 |
| | | | | | | } I _Q = 16 mA |
| | | | | | | } I _Q = -400 μA |
| <u>Currents</u> | | | | | | |
| Input LOW | | | | | | |
| G ₁ ; G ₂ | -I _{GLmax} | 1.6 | 1.6 | 1.6 | mA | 5.25 |
| G ₃ | -I _{GLmax} | 3.2 | 3.2 | 3.2 | mA | 5.25 |
| Input HIGH | | | | | | |
| G ₁ ; G ₂ | I _{GHmax} | 40 | 40 | 40 | μA | 5.25 |
| G ₃ | I _{GHmax} | 80 | 80 | 80 | μA | 5.25 |
| any input | I _{GHmax} | 1 | 1 | 1 | mA | 5.25 |
| Output LOW | I _{QLmax} | 16 | 16 | 16 | mA | |
| Output short-circuit ¹⁾ | -I _{Qsc min} | 18 | 18 | 18 | mA | 5.25 |
| | -I _{Qsc max} | 55 | 55 | 55 | mA | 5.25 |
| | | | | | | } V _I = 0.4 V |
| | | | | | | } V _I = 2.4 V |
| | | | | | | } V _I = 5.5 V |
| <u>SUPPLY DATA</u> | | | | | | |
| Supply current quiescent (unfired) | I _p typ. | 13 | 13 | 13 | mA | 5.0 |
| | I _p < | 25 | 25 | 25 | mA | 5.0 |
| fired | I _p typ. | 13 | 23 | 13 | mA | 5.0 |
| | I _p < | 40 | 40 | 40 | mA | 5.0 |

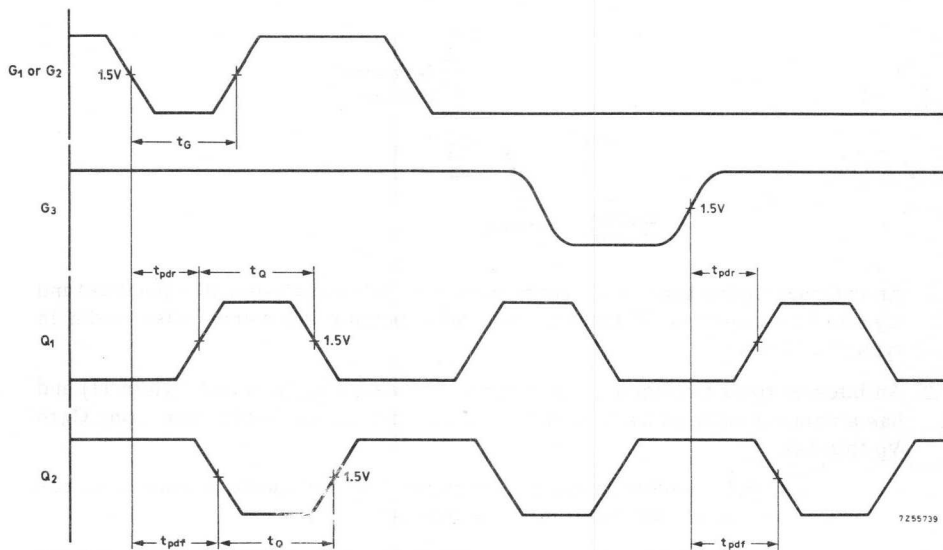
¹⁾ Only one input to be shorted at a time.

CHARACTERISTICS (continued)

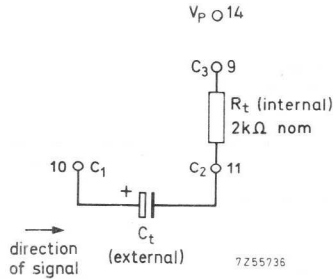
| | | T _{amb} (°C) | | | Conditions and references | | |
|--------------------------------------------------|-----------------------|-----------------------|-----|----|---------------------------|--------------------------------------------------------------------------------------------|--|
| | | 0 | 25 | 70 | V _P (V) | C _L = 15 pF; N _a = 10 | |
| <u>DYNAMIC DATA</u> | | | | | | | |
| <u>Signal requirements</u> | | | | | | | |
| Input pulse width | t _G > | - | 50 | - | ns | | |
| Input pulse rise/fall time | | | | | | | |
| G ₁ ; G ₂ | $\frac{dV_G}{dt} <$ | - | 1 | - | V/μs | | |
| G ₃ | $\frac{dV_G}{dt} <$ | - | 1 | - | V/s | | |
| <u>Performance</u> | | | | | | | |
| Rise propagation delay time | | | | | | | |
| G ₁ , G ₂ → Q ₁ | t _{pdr} > | - | 25 | - | ns | } C _t = 80 pF | |
| | t _{pdr} typ. | - | 45 | - | ns | | |
| | t _{pdr} < | - | 70 | - | ns | | |
| G ₃ → Q ₁ | t _{pdr} > | - | 15 | - | ns | | |
| | t _{pdr} typ. | - | 35 | - | ns | | |
| | t _{pdr} < | - | 55 | - | ns | | |
| Fall propagation delay time | | | | | | | |
| G ₁ , G ₂ → Q ₂ | t _{pdf} > | - | 30 | - | ns | | |
| | t _{pdf} typ. | - | 50 | - | ns | | |
| | t _{pdf} < | - | 80 | - | ns | | |
| G ₃ → Q ₂ | t _{pdf} > | - | 20 | - | ns | | |
| | t _{pdf} typ. | - | 40 | - | ns | | |
| | t _{pdf} < | - | 65 | - | ns | | |
| Output pulse width: | | | | | | | |
| with internal timing resistance | t _Q > | - | 70 | - | ns | } C _t = 80pF; R _t =open; pin C ₃ connected to 5.0 V | |
| | t _Q typ. | - | 110 | - | ns | | |
| | t _Q < | - | 150 | - | ns | | |
| with zero timing capacitance | t _Q > | - | 20 | - | ns | } C _t = 0; R _t = open; pin C ₃ connected to 5.0 V | |
| | t _Q typ. | - | 30 | - | ns | | |
| | t _Q < | - | 50 | - | ns | | |
| with external timing resistance | t _Q > | - | 600 | - | ns | } C _t = 100 pF; R _t = 10 KΩ; pin C ₃ open | |
| | t _Q typ. | - | 700 | - | ns | | |
| | t _Q < | - | 800 | - | ns | | |
| | t _Q > | - | 6 | - | ms | } C _t = 1 μF; R _t = 10 KΩ; pin C ₃ open | |
| | t _Q typ. | - | 7 | - | ms | | |
| | t _Q < | - | 8 | - | ms | | |

CHARACTERISTICS (continued)

DYNAMIC DATA

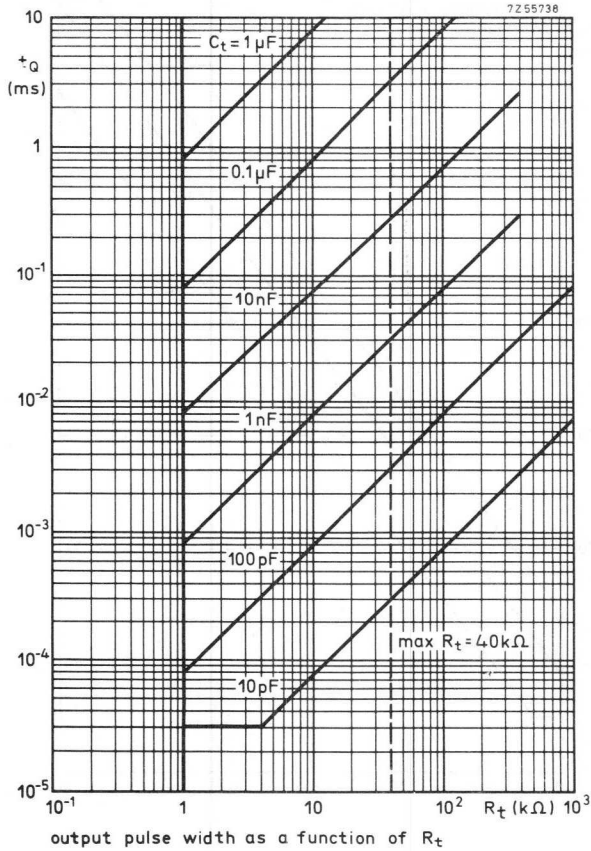


CHARACTERISTICS (continued)

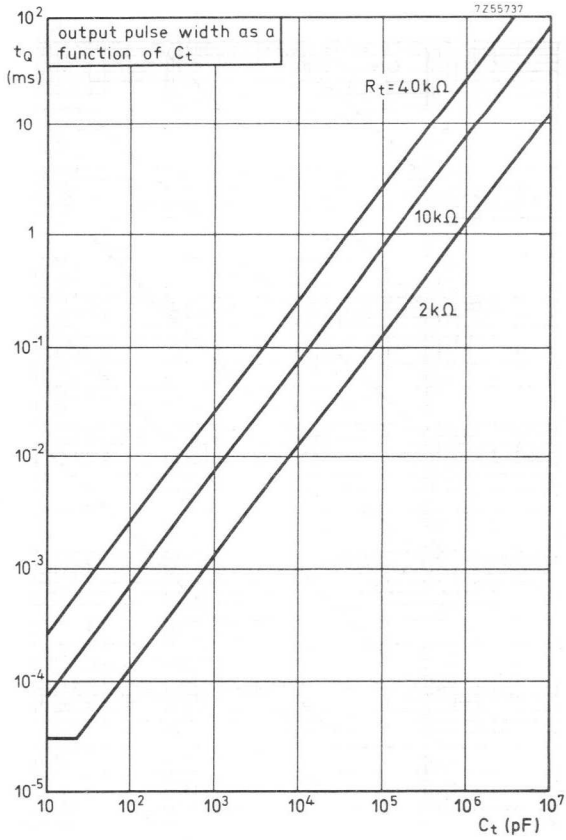
TIMING NOTES

1. An external timing capacitor may be connected between C_1 (pin 10 - positive) and C_2 (pin 11 - negative). Without an external capacitor the output pulse width is typically 30 ns.
2. An internal timing resistor is incorporated between C_3 (pin 9) and C_2 (pin 11) and has a nominal value of $2\text{ k}\Omega$. It may be brought into the circuit by connecting C_3 to V_p (pin 14).
3. For variable pulse widths an external variable resistor should be connected between C_3 and V_p ; no external limiting is then required.
4. For accurate repeatable pulse widths connect an external resistor between point C_2 and V_p , leaving point C_3 open.
5. Jitter-free operation is maintained over the full temperature and supply voltage range for timing capacitances from 10 pF to $10\text{ }\mu\text{F}$ and timing resistances from $2\text{ k}\Omega$ to $40\text{ k}\Omega$.
Within these limits the output pulse width follows the relationship $t_Q = C_t \cdot R_t \ell n Z$.
6. A duty cycle of up to 67% is achieved by using only the internal timing resistance. Duty cycles as high as 90% are obtained by using $R_t = 40\text{ k}\Omega$. Higher duty cycles are achievable if a certain amount of pulse-width jitter is allowed.

CHARACTERISTICS (continued)



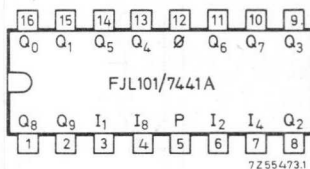
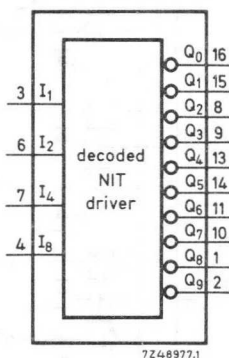
CHARACTERISTICS (continued)



The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

SINGLE DECODER N.I.T. DRIVER¹⁾



QUICK REFERENCE DATA

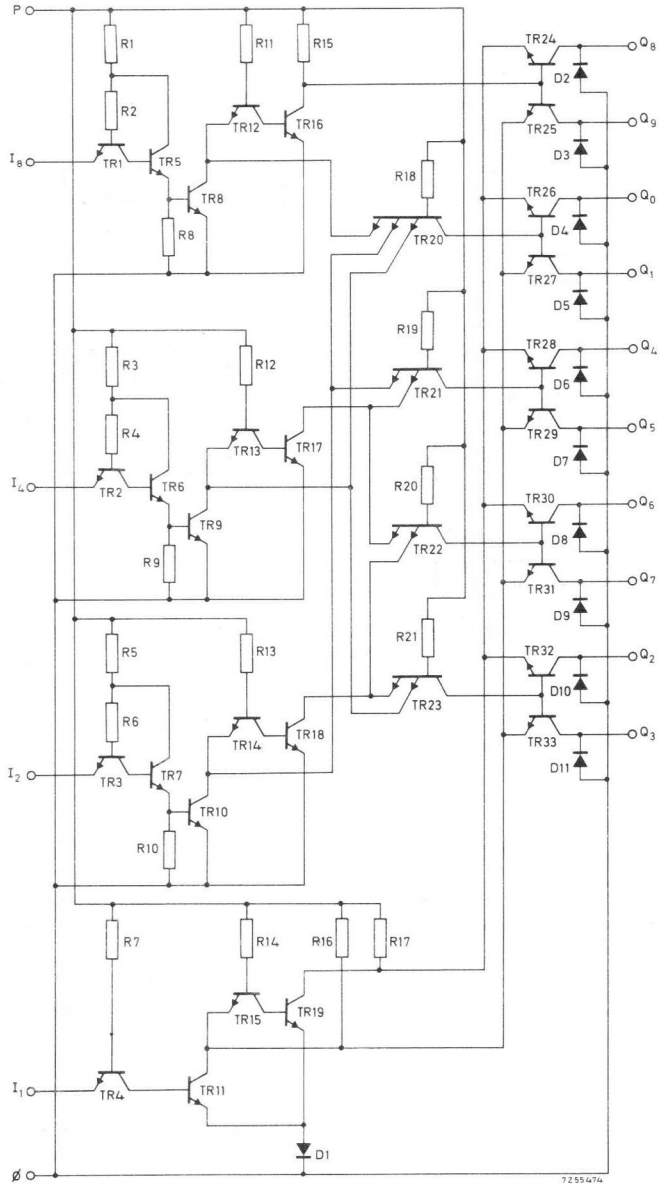
| | | |
|-------------------------------|-----------|-----------------|
| Supply voltage | V_P | $5.0 \pm 5\%$ V |
| Operating ambient temperature | T_{amb} | 0 to +70 °C |
| Supply current | I_P | typ. 19 mA |
| Drive lines | | 10 |
| Output voltage at any output | V_Q | > 55 V |

The FJL101/7441A is a BCD (1-2-4-8 code) to decimal decoder incorporating high voltage output transistors for driving numerical indication tubes. It contains a decoding array followed by ten output driver stages which can be used for parallel or serial drive. For parallel drive no external clamping diodes are needed. For serial drive the cathode voltages must be clamped to prevent excessive dissipation that may be caused by the leakage currents of non-ignited cathodes are cut-off.

PACKAGE OUTLINE: 16 lead plastic dual in-line (type A) (See General Section)

¹⁾ N.I.T.; Numerical Indicator Tube.

CIRCUIT DIAGRAM



FUNCTION TABLE

| inputs | | | | output |
|----------------|----------------|----------------|----------------|-------------|
| I ₁ | I ₂ | I ₄ | I ₈ | ON-state *) |
| L | L | L | L | 0 |
| H | L | L | L | 1 |
| L | H | L | L | 2 |
| H | H | L | L | 3 |
| L | L | H | L | 4 |
| H | L | H | L | 5 |
| L | H | H | L | 6 |
| H | H | H | L | 7 |
| L | L | L | H | 8 |
| H | L | L | H | 9 |

*) All other outputs are off.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|----------------------------------------|------------------|------|----------------|
| Supply voltage | V _p | max. | 7.0 V |
| Input voltage | V _I | max. | 5.5 V |
| Current into any output (OFF state) | I _Q | max. | 0.5 mA |
| Operating ambient temperature | T _{amb} | | 0 to +70 °C |
| Storage temperature | T _{stg} | | -65 to +150 °C |



CHARACTERISTICS

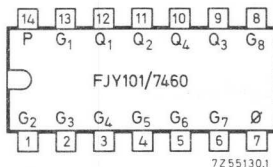
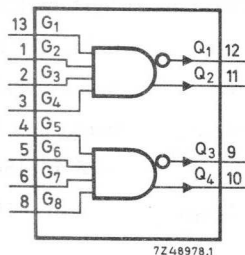
| | | T _{amb} (°C) | | | Conditions and References | |
|-------------------------------------------------------------|------------------------------------------------------------------------------------------|-----------------------|-----|--------|---------------------------|------------------------------------------------------------------------------------------------------|
| | | 0 | 25 | 70 | V _P (V) | |
| <u>STATIC DATA</u> | | | | | | |
| <u>Voltages</u> | | | | | | |
| Input threshold LOW ¹⁾ | V _{ILmax} | 0.8 | 0.8 | 0.8 V | 4.75 | |
| Input threshold HIGH ¹⁾ | V _{IHmin} | 2.0 | 2.0 | 2.0 V | 4.75 | |
| Output LOW (ON-state) ¹⁾ | V _{QLmax} | 2.5 | 2.5 | 2.5 V | 4.75 | { I _{QL} = 7 mA V _{IL} = 0.8 V; V _{IH} = 2.0 V |
| <u>Currents</u> | | | | | | |
| Input LOW I ₁ | -I _{I1Lmax} | 3.2 | 3.2 | 3.2 mA | 5.25 | V _{IL} = 0.4 V |
| I _{2, I4, I8} | -I _{I2Lmax} -I _{I4Lmax} -I _{I8Lmax} | 1.6 | 1.6 | 1.6 mA | 5.25 | V _{IL} = 0.4 V |
| Input HIGH I ₁ | I _{I1Hmax} | 80 | 80 | 80 μA | 5.25 | V _{IH} = 2.4 V |
| I _{2, I4, I8} | I _{I1Hmax} I _{I2Hmax} I _{I4Hmax} I _{I8Hmax} | 1 | 1 | 1 mA | 5.25 | V _{IH} = 5.5 V |
| I _{2, I4, I8} | I _{I2Hmax} I _{I4Hmax} I _{I8Hmax} | 40 | 40 | 40 μA | 5.25 | V _{IH} = 2.4 V |
| I _{2, I4, I8} | I _{I2Hmax} I _{I4Hmax} I _{I8Hmax} | 1 | 1 | 1 mA | 5.25 | V _{IH} = 5.5 V |
| Output leakage current HIGH (OFF-state) ¹⁾ | -I _{QHmax} | 200 | 200 | 200 μA | 5.25 | { V _Q = 55V, V _{IL} = V _{ILmax} V _{IH} = V _{IHmax} |
| <u>SUPPLY DATA</u> | | | | | | |
| Supply current | I _{p typ.} | - | 22 | - mA | 5.0 | All inputs and outputs open |

¹⁾ See function table on page 3. V_{IL} and V_{IH} to be maintained as in function table.

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

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DUAL 4-INPUT AND-OR-NOT EXPANDER



QUICK REFERENCE DATA

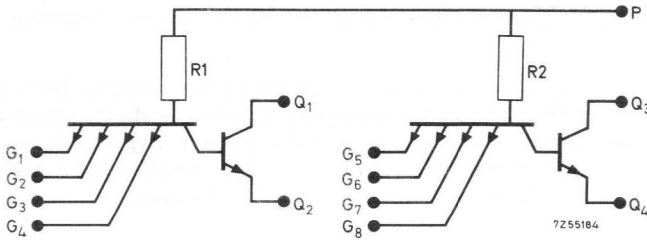
| | | |
|-------------------------------------------------------------------------------------------------------|-----------|-----------------------|
| Supply voltage | V_P | $5.0 \pm 5\%$ V |
| Operating ambient temperature range | T_{amb} | 0 to + 70 °C |
| Average propagation delay time when used with FJH151 or FJH171 N = fan-out = 10; $T_{amb} = 25$ °C | t_{pd} | typ. 15 ns |
| D.C. noise margin ¹⁾ (full temperature range) | M_L | > 0.4 V typ. 1.0 V |
| Average power consumption; (each expander) $T_{amb} = 25$ °C | P_{av} | typ. 4.0 mW |

The FJY101/7460 is a dual 4-input AND-OR-NOT expander for use with the FJH151/7450 and FJH171/7453. Up to 4 expanders may be connected to the expandable gates of FJH151/7450 and FJH171/7453.

PACKAGE OUTLINE 14 lead plastic dual in-line (type A) (See General Section)

¹⁾ When used with FJH151/7450 or FJH171/7453 as applicable.

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|-------------------------------|-----------|------|---------------------|
| Supply voltage | V_P | max. | 7.0 V |
| Input voltage | V_G | max. | 5.5 V ¹⁾ |
| Peak negative G input voltage | $-V_{GM}$ | max. | 2 V ²⁾ |
| Storage temperature | T_{stg} | | -55 to +150 °C |
| Operating ambient temperature | T_{amb} | | 0 to +70 °C |

1) In addition the voltage between any two inputs: max. 5.5 V.

2) Pulse duration $t_p = 20$ ns; repetition frequency $f = 5$ MHz; source resistance $R_S \geq 75 \Omega$.

CHARACTERISTICS ¹⁾

| | | T _{amb} (°C) | | | Conditions and references | |
|-----------------------------|-----------------------|-----------------------|-----|-----|---------------------------|--------------------------------------------------|
| | | 0 | 25 | 70 | V _P (V) | |
| <u>STATIC DATA</u> | | | | | | |
| <u> Voltages </u> | | | | | | |
| Input threshold LOW | V _{GLmax} | 0.8 | 0.8 | 0.8 | V | |
| Input threshold HIGH | V _{GHmin} | 2.0 | 2.0 | 2.0 | V | |
| <u> Currents </u> | | | | | | |
| Input LOW | -I _{GLmax} | 1.6 | 1.6 | 1.6 | mA | 5.25 V _G = 0.40 V |
| Input HIGH | I _{GHmax} | 40 | 40 | 40 | μA | 5.25 V _G = 2.4 V |
| <u>SUPPLY DATA</u> | | | | | | |
| <u> Supply current </u> | | | | | | |
| Input LOW | I _{PL} typ. | 2.0 | 2.0 | 2.0 | mA | } V _G = 0 } V _G = 5.0 V |
| | I _{PL} < | 4.0 | 4.0 | 4.0 | mA | |
| Input HIGH | I _{PH} typ. | 1.2 | 1.2 | 1.2 | mA | |
| | I _{PH} < | 2.5 | 2.5 | 2.5 | mA | |
| <u>DYNAMIC DATA</u> | | | | | | |
| Rise propagation delay time | t _{pdr} typ. | - | 15 | - | ns | } C _L = 15 pF } N = 10 |
| | < | - | 30 | - | ns | |
| Fall propagation delay time | t _{pdf} typ. | - | 10 | - | ns | |
| | < | - | 20 | - | ns | |

¹⁾ When used in conjunction with the FJH151/7450

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MOS

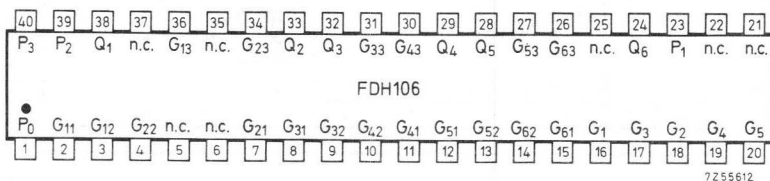
FD family



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The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

ARITHMETIC/LOGIC ARRAY

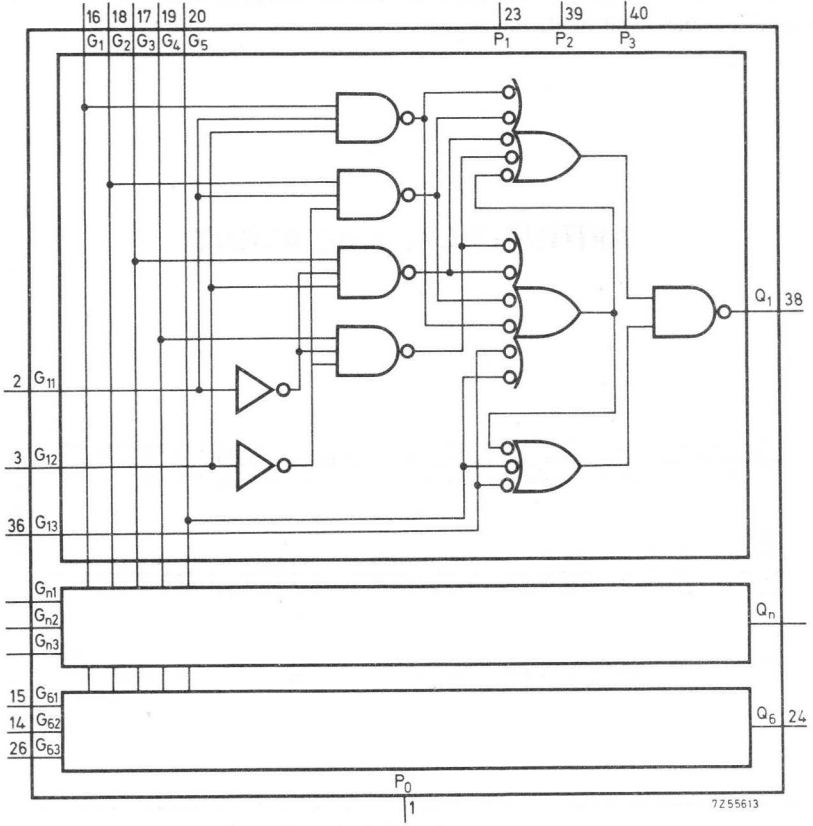


P_0 and metal lid on top of the package are connected

QUICK REFERENCE DATA

| | | | |
|----------------------------------------|------------|------------|--------|
| Supply voltage | V_{P1} | -24 to -28 | V |
| Operating ambient temperature | T_{amb} | -55 to +85 | °C |
| Average propagation delay | | | |
| $C_L = 50$ pF | t_{pd} | typ. | 250 ns |
| D. C. noise margin | M_H, M_L | > | 1.0 V |
| Average power consumption per function | | | |
| at 1 MHz switching rate | P_{av} | typ. | 35 mW |

PACKAGE OUTLINE: 40 lead ceramic dual in-line (See General Section)



GENERAL DESCRIPTION

The FDH106 consists of six, identical, 3-input gate networks. Five coded control lines determine the function of the six gate networks. Each network may function as a full adder/subtractor, or, if used as a 2-input gate, it can provide all logic functions of 2 variables.

Thus one of 32 different functions can be selected by the control lines; the selected function is available six times.

The output voltage swing is determined by the output buffer supply voltage. All inputs are protected against over-voltage caused by static charges.

Inputs G_1 to G_5 have pull-down resistors connected to P_3 , so that they assume the LOW state when left floating.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | |
|-----------------------------------------------------------------------------|-----------|------------------------------|
| Voltage on all inputs, outputs and supply terminals with reference to P_0 | | +0.5 to -30 V |
| Power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$ | P_{tot} | max. 1 W |
| Junction temperature | T_j | max. 150 $^\circ\text{C}$ |
| Storage temperature | T_{stg} | -65 to +150 $^\circ\text{C}$ |
| Total current through terminal P_3 | $-I_{P3}$ | max. 40 mA |
| Output current per output | $\pm I_Q$ | max. 20 mA |

THERMAL RESISTANCE

| | | | |
|--------------------------|---------------|---|-------------------------------|
| From junction to ambient | $R_{th\ j-a}$ | = | 125 $^\circ\text{C}/\text{W}$ |
|--------------------------|---------------|---|-------------------------------|

FUNCTION TABLE

| G5 G4 G3 G2 G1 | logic equation (positive logic) | logic function | |
|----------------|-------------------------------------------------------------------------|---------------------|---------------------|
| | | positive logic | negative logic |
| L L L L L | $Q_n = \text{HIGH}$ | - | - |
| L L L L H | $Q_n = \overline{G_{n1}} + \overline{G_{n2}}$ | NAND | NOR |
| L L L H L | $Q_n = \overline{G_{n1}} + G_{n2}$ | - | - |
| L L L H H | $Q_n = \overline{G_{n1}}$ | Complement G_{n1} | Complement G_{n1} |
| L L H L L | $Q_n = G_{n1} + G_{n2}$ | OR | AND |
| L L H L H | $Q_n = \overline{G_{n1}} \cdot G_{n2} + G_{n1} \cdot \overline{G_{n2}}$ | exclusive-OR | comparator |
| L L H H L | $Q_n = G_{n2}$ | transfer G_{n2} | transfer G_{n2} |
| L L H H H | $Q_n = \overline{G_{n1}} \cdot G_{n2}$ | - | - |
| L H L L L | $Q_n = G_{n1} + \overline{G_{n2}}$ | - | - |
| L H L L H | $Q_n = \overline{G_{n1}}$ | Complement G_{n2} | Complement G_{n2} |
| L H L H L | $Q_n = \overline{G_{n1}} \cdot G_{n2} + G_{n1} \cdot G_{n2}$ | comparator | exclusive-OR |
| L H L H H | $Q_n = \overline{G_{n1}} \cdot \overline{G_{n2}}$ | NOR | NAND |
| L H H L L | $Q_n = G_{n1}$ | transfer G_{n1} | transfer G_{n1} |
| L H H L H | $Q_n = G_{n1} \cdot \overline{G_{n2}}$ | - | - |
| L H H H L | $Q_n = G_{n1} \cdot G_{n2}$ | AND | OR |
| L H H H H | $Q_n = \text{LOW}$ | - | - |

FUNCTION TABLE (continued)

| G5 G4 G3 G2 G1 | | | | | logic equation (positive logic) | logic function | |
|----------------|---|---|---|---|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|---------------------|
| | | | | | | positive logic | negative logic |
| H | L | L | L | L | $Q_n = \overline{G_{n3}}$ | Complement G_{n3} | Complement G_{n3} |
| H | L | L | L | H | $Q_n = \overline{G_{n1}} \cdot \overline{G_{n2}} \cdot \overline{G_{n3}} + G_{n1} \cdot G_{n2} \cdot G_{n3}$ | - | - |
| H | L | L | H | L | $Q_n = \overline{G_{n1}} \cdot \overline{G_{n2}} \cdot G_{n3} + G_{n1} \cdot G_{n2} \cdot \overline{G_{n3}}$ | - | - |
| H | L | L | H | H | $Q_n = G_{n1} \cdot G_{n2} \cdot \overline{G_{n3}} + G_{n1} \cdot \overline{G_{n2}} \cdot G_{n3}$ | comparator | exclusive-OR |
| H | L | H | L | L | $Q_n = G_{n1} \cdot \overline{G_{n2}} \cdot \overline{G_{n3}} + G_{n1} \cdot G_{n2} \cdot G_{n3}$ | - | - |
| H | L | H | L | H | $Q_n = G_{n1} \cdot G_{n2} \cdot G_{n3} + G_{n1} \cdot \overline{G_{n2}} \cdot \overline{G_{n3}} + \overline{G_{n1}} \cdot G_{n2} \cdot \overline{G_{n3}} + \overline{G_{n1}} \cdot \overline{G_{n2}} \cdot G_{n3}$ | add | add |
| H | L | H | H | L | $Q_n = G_{n2} \cdot \overline{G_{n3}} + G_{n2} \cdot G_{n3}$ | exclusive-OR | comparator |
| H | L | H | H | H | $Q_n = G_{n1} \cdot \overline{G_{n2}} \cdot \overline{G_{n3}} + G_{n1} \cdot G_{n2} \cdot G_{n3}$ | - | - |
| H | H | L | L | L | $Q_n = G_{n1} \cdot \overline{G_{n2}} \cdot \overline{G_{n3}} + G_{n1} \cdot G_{n2} \cdot G_{n3}$ | - | - |
| H | H | L | L | H | $Q_n = G_{n2} \cdot \overline{G_{n3}} + G_{n2} \cdot G_{n3}$ | comparator | exclusive-OR |
| H | H | L | H | L | $Q_n = G_{n1} \cdot G_{n2} \cdot \overline{G_{n3}} + G_{n1} \cdot \overline{G_{n2}} \cdot G_{n3} + \overline{G_{n1}} \cdot G_{n2} \cdot \overline{G_{n3}} + \overline{G_{n1}} \cdot \overline{G_{n2}} \cdot G_{n3}$ | subtract | subtract |
| H | H | L | H | H | $Q_n = G_{n1} \cdot G_{n2} \cdot G_{n3} + G_{n1} \cdot \overline{G_{n2}} \cdot \overline{G_{n3}} + G_{n1} \cdot \overline{G_{n2}} \cdot G_{n3} + G_{n1} \cdot G_{n2} \cdot \overline{G_{n3}}$ | - | - |
| H | H | H | L | L | $Q_n = G_{n1} \cdot \overline{G_{n2}} \cdot \overline{G_{n3}} + G_{n1} \cdot G_{n2} \cdot G_{n3}$ | exclusive-OR | comparator |
| H | H | H | L | H | $Q_n = \overline{G_{n1}} \cdot \overline{G_{n2}} \cdot \overline{G_{n3}} + G_{n1} \cdot G_{n2} \cdot G_{n3}$ | - | - |
| H | H | H | H | L | $Q_n = \overline{G_{n1}} \cdot G_{n2} \cdot \overline{G_{n3}} + G_{n1} \cdot G_{n2} \cdot G_{n3}$ | - | - |
| H | H | H | H | H | $Q_n = G_{n3}$ | transfer G_{n3} | transfer G_{n3} |



CHARACTERISTICS

Test conditions: $V_{P1} = -24$ to -28 V; $V_{P2} = V_{P3} = -12$ to -14 V (see note 1); $T_{amb} = -55$ to $+85$ °C; $P_0 =$ grounded; standard load: 50 pF in parallel with 1 M Ω to P_0 .

| | Symbol | min. typ. ¹⁾ max. | conditions and references |
|--------------------------------|------------------------|------------------------------|---------------------------------------------------------------------------------------------------------------------|
| Input logic levels | | | |
| HIGH | V_{GH} | -2 0 +0.3 V | |
| LOW | V_{GL} | -28 - -9 V | |
| Output levels | | | |
| HIGH | V_{QH} | -1.0 - 0 V | |
| LOW | V_{QL} | -14 - -10 V | |
| Input capacitance | | | |
| $G_1; G_2; G_3; G_4; G_5$ | C_{G1} to C_{G5} | - 5.5 7 pF | bias: $V_G = 0$ V; $f = 1$ MHz |
| all other inputs | C_{G11} to C_{G63} | - 3.5 5 pF | bias: $V_G = 0$ V; $f = 1$ MHz |
| Input leakage current | $-I_{GL}$ | - - 1 μ A | $\left. \begin{array}{l} V_G = -15$ V; $T_{amb} = 25$ °C \\ all other terminals \\ at V_{P0} \end{array} \right\} |
| Output resistance | | | |
| HIGH | R_{QH} | - 1.0 - k Ω | $V_Q = -1$ V |
| LOW | R_{QL} | - 2.0 - k Ω | $V_Q = -10$ V |
| Supply current (see note 2) | | | |
| | $-I_{P1}$ | - 4.6 7.0 mA | $\left. \begin{array}{l} f = 1$ MHz; $T_{amb} = 25$ °C \end{array} \right\} |
| | $-I_{P2}$ | - 2.0 2.5 mA | |
| | $-I_{P3}$ | - 4.2 6.0 mA | |
| Output transition times: | | | |
| fall time | t_{THL} | - 150 - ns | |
| rise time | t_{TLH} | - 150 - ns | |
| Delay times: | | | |
| fall time | t_{DHL} | - 250 400 ns | $\left. \begin{array}{l} \end{array} \right\}$ see note 3 |
| rise time | t_{DLH} | - 250 400 ns | |
| Control input sink current | | | |
| | $-I_{G1}$ to $-I_{G5}$ | - 32 - μ A | bias: $V_G = -2$ V |

Note 1: V_{P2} is independent of circuit operation and is used for output LOW only.

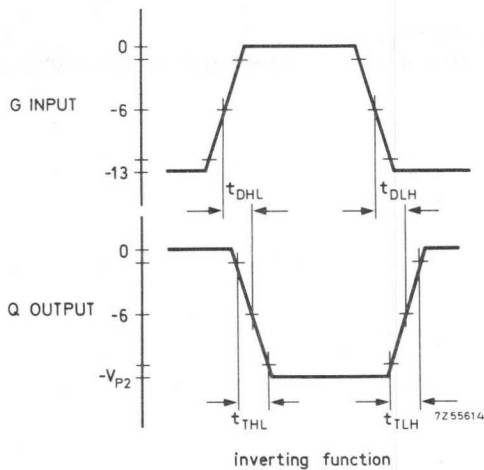
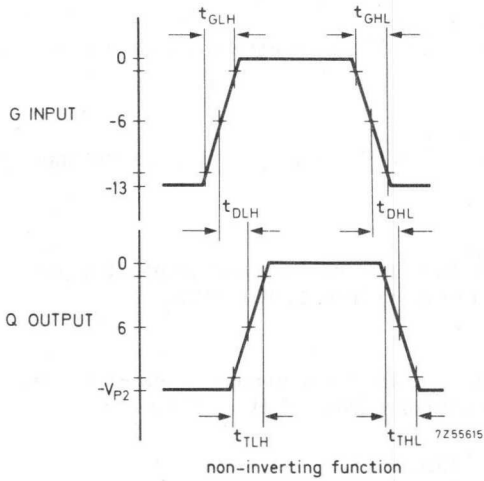
Note 2: Output buffer power supply current is almost entirely dependent on the external load.

Note 3: Delays are measured at -6 V levels of input and output signals.

¹⁾ All typ. values under test conditions: $V_{P1} = -26$ V; $V_{P2} = -13$ V; $T_{amb} = 25$ °C.

CHARACTERISTICS (continued)

TIMING DIAGRAMS



Measurements performed under the following conditions:

$$V_{P1} = -24 \text{ to } -28 \text{ V}; V_{P2} = V_{P3} = -12 \text{ to } -14 \text{ V}; t_{GLH} = t_{GHL} = 150 \text{ ns.}$$

Note: The indicated points on the vertical axis are specified in the glossary of terms.

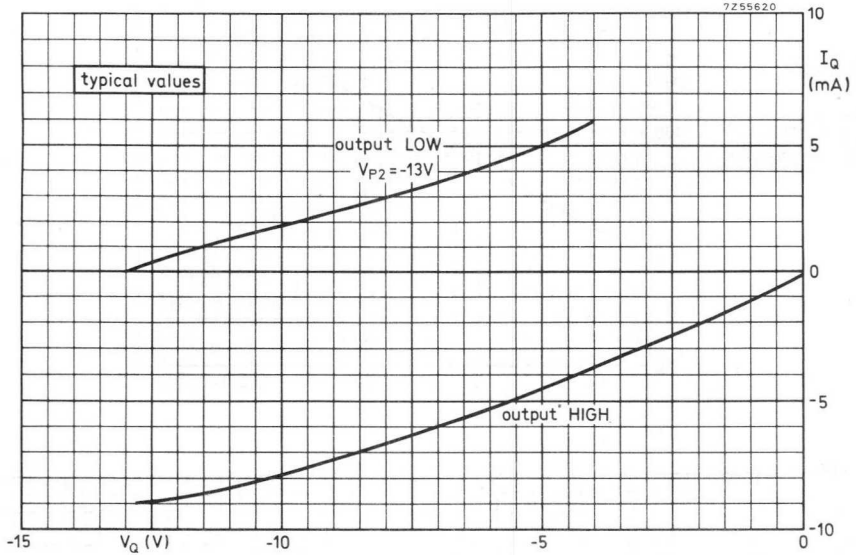
CHARACTERISTICS (continued)

GLOSSARY OF TERMS

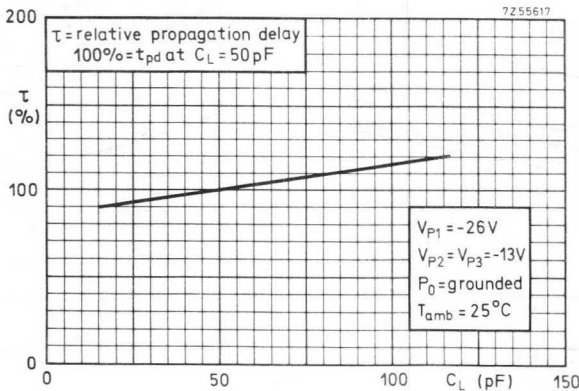
1. Input signal rise time: t_{GLH}
The time between the 90% and 10% voltage points as the input pulse goes from LOW to HIGH.
2. Input signal fall time: t_{GHL}
The time between the 10% and 90% voltage points as the input pulse goes from HIGH to LOW.
3. Rise delay time: t_{DLH}
The delay between the time the input arrives at its -6 V point and the time the output passes -6 V when going from LOW to HIGH.
4. Fall delay time: t_{DHL}
The delay between the time the input arrives at its -6 V point and the time the output passes -6 V when going from HIGH to LOW.
5. Output rise transition time: t_{TLH}
The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
6. Output fall transition time: t_{THL}
The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.

OUTPUT BUFFER DESCRIPTION

The FDH106 utilizes push-pull output buffers which exhibit the V_Q versus I_Q output curves, for both HIGH and LOW output, shown below.

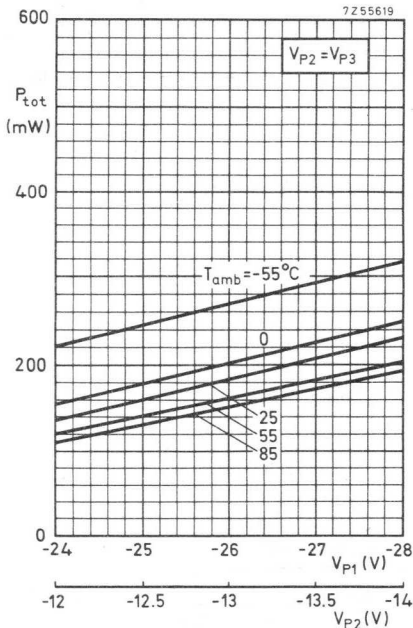
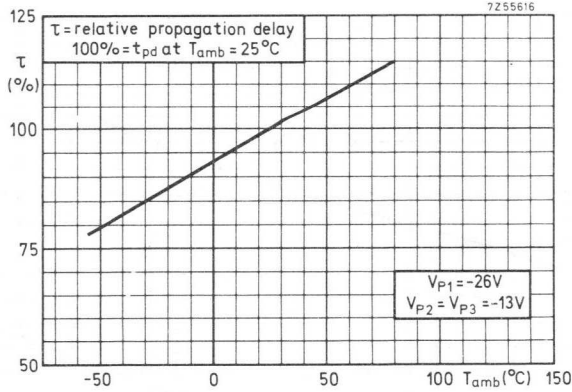


TYPICAL PERFORMANCE at load of C_L in parallel with $1 M\Omega$ to P_0 .

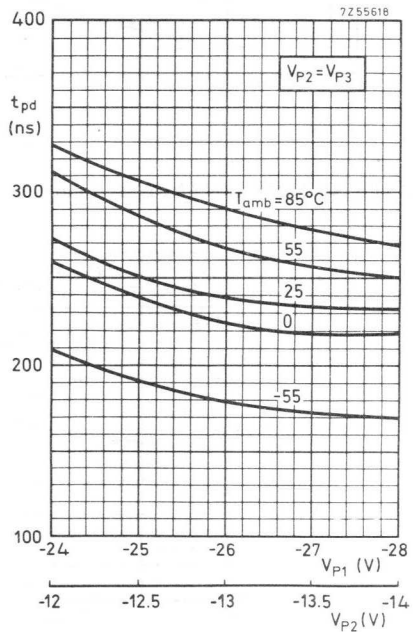


TYPICAL PERFORMANCE (continued)

Test conditions: $P_0 =$ grounded; standard load: 50 pF in parallel with 1 M Ω to P_0 .



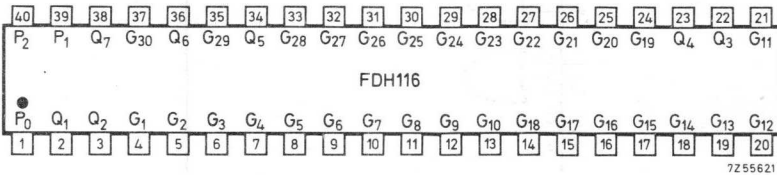
Power dissipation as a function of the supply voltages V_{P1} and V_{P2}



Propagation delay as a function of the supply voltages V_{P1} and V_{P2}

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

CONTROL LOGIC ARRAY

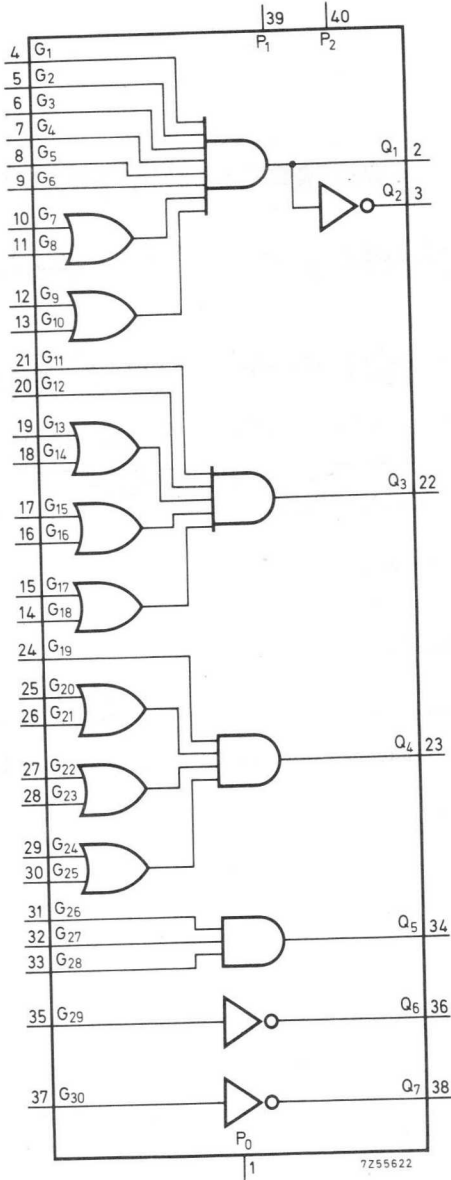


P_0 and metal lid on top of the package are connected.

QUICK REFERENCE DATA

| | | | |
|-------------------------------|------------|------------|----|
| Supply voltage | V_{P1} | -24 to -28 | V |
| Operating ambient temperature | T_{amb} | -55 to +85 | °C |
| Power dissipation (f = 1 MHz) | P_{tot} | typ. 150 | mW |
| Average propagation delay | t_{pd} | typ. 250 | ns |
| D.C. noise margin | $M_H; M_L$ | > 1.0 | V |

PACKAGE OUTLINE 40 lead ceramic dual in-line (See General Section)



GENERAL DESCRIPTION

The FDH116 contains all the logic functions shown in the diagram and described in the logic function on page 4. It is intended to perform the control logic in all MOS digital systems. The output voltage swing is determined by the output buffer supply voltage. All inputs are protected against over-voltage caused by static charges.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | |
|-----------------------------------------------------------------------------|-----------|--------------------------------|
| Voltage on all inputs, outputs and supply terminals with reference to P_0 | | +0.5 to -30 V |
| Power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$ | P_{tot} | max. 1 W |
| Junction temperature | T_j | max. 150 $^{\circ}\text{C}$ |
| Storage temperature | T_{stg} | -65 to +150 $^{\circ}\text{C}$ |
| Total current through terminal P_2 | $-I_{P2}$ | max. 40 mA |
| Output current (per output) | $\pm I_Q$ | max. 20 mA |

THERMAL RESISTANCE

| | | | |
|--------------------------|---------------|---|---------------------------------|
| From junction to ambient | $R_{th\ j-a}$ | = | 125 $^{\circ}\text{C}/\text{W}$ |
|--------------------------|---------------|---|---------------------------------|



LOGIC FUNCTIONS

Positive logic

$$Q_1 = G_1 \cdot G_2 \cdot G_3 \cdot G_4 \cdot G_5 \cdot G_6 \cdot (G_7 + G_8) \cdot (G_9 + G_{10})$$

$$Q_2 = \overline{G_1 \cdot G_2 \cdot G_3 \cdot G_4 \cdot G_5 \cdot G_6 \cdot (G_7 + G_8) \cdot (G_9 + G_{10})}$$

$$Q_3 = G_{11} \cdot G_{12} \cdot (G_{13} + G_{14}) \cdot (G_{15} + G_{16}) \cdot (G_{17} + G_{18})$$

$$Q_4 = G_{19} \cdot (G_{20} + G_{21}) \cdot (G_{22} + G_{23}) \cdot (G_{24} + G_{25})$$

$$Q_5 = G_{26} \cdot G_{27} \cdot G_{28}$$

$$Q_6 = \overline{G_{29}}$$

$$Q_7 = \overline{G_{30}}$$

Negative logic

$$Q_1 = G_1 + G_2 + G_3 + G_4 + G_5 + G_6 + G_7 \cdot G_8 + G_9 \cdot G_{10}$$

$$Q_2 = \overline{G_1 + G_2 + G_3 + G_4 + G_5 + G_6 + G_7 \cdot G_8 + G_9 \cdot G_{10}}$$

$$Q_3 = G_{11} + G_{12} + (G_{13} \cdot G_{14}) + (G_{15} \cdot G_{16}) + (G_{17} \cdot G_{18})$$

$$Q_4 = G_{19} + (G_{20} \cdot G_{21}) + (G_{22} \cdot G_{23}) + (G_{24} \cdot G_{25})$$

$$Q_5 = G_{26} + G_{27} + G_{28}$$

$$Q_6 = \overline{G_{29}}$$

$$Q_7 = \overline{G_{30}}$$

CHARACTERISTICS

Test conditions: $V_{P1} = -24$ to -28 V; $V_{P2} = -12$ to -14 V (see note 1); $T_{amb} = -55$ to $+85$ °C; $P_0 =$ grounded; standard load: 50pF in parallel with 1 M Ω to P_0 .

| | Symbol | min. | typ. 1) | max. | Conditions and references |
|------------------------------------|-----------------------|------|---------|--------------|--------------------------------------------------------------------------|
| Input logic levels | | | | | |
| HIGH | V_{GH} | -2 | - | +0.3 V | |
| LOW | V_{GL} | -28 | - | -9 V | |
| Output levels | | | | | |
| HIGH | V_{QH} | -1.0 | - | 0 V | |
| LOW | V_{QL} | -14 | - | -10 V | |
| Input capacitance | | | | | |
| $G_{29}; G_{30}$ | C_{G29}, C_{G30} | - | 5 | 7 pF | } bias: $V_G = 0$ V $f = 1$ MHz |
| all other inputs | C_{G1} to C_{G28} | - | 3.5 | 5 pF | |
| Input leakage current | $-I_{GL}$ | - | - | 1 μ A | } $V_G = -15$ V; all other terminals at V_{P0} $T_{amb} = 25$ °C |
| Output resistance | | | | | |
| HIGH | R_{QH} | - | 1 | - k Ω | $V_Q = -1$ V |
| LOW | R_{QL} | - | 2 | - k Ω | $V_Q = -10$ V |
| Supply currents | | | | | |
| $-I_{P1}$ | | - | 4.6 | 6.5 mA | } $f=1$ MHz; $T_{amb}=25$ °C see note 2 |
| $-I_{P2}$ | | - | 2.3 | 3.0 mA | |
| Output transition times: | | | | | |
| fall time | t_{THL} | - | 150 | - ns | |
| rise time | t_{TLH} | - | 150 | - ns | |
| Delay times: | | | | | |
| $G \rightarrow Q_1; Q_3; Q_4; Q_5$ | t_{DHL}, t_{DLH} | - | 150 | 250 ns | } see note 3 |
| $G \rightarrow Q_6; Q_7$ | t_{DHL}, t_{DLH} | - | 125 | 250 ns | |
| $G \rightarrow Q_2$ | t_{DHL}, t_{DLH} | - | 175 | 300 ns | |

1) All typ. values measured at: $T_{amb} = 25$ °C; $V_{P1} = -26$ V; $V_{P2} = -13$ V

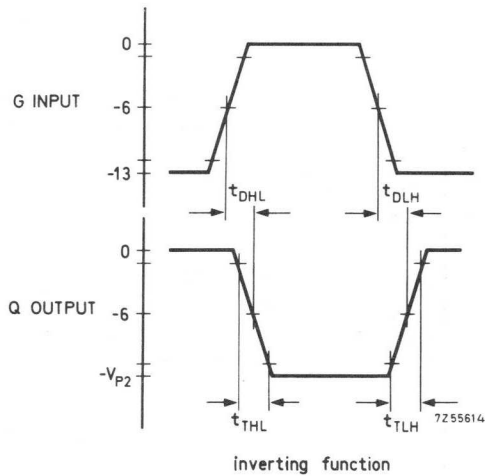
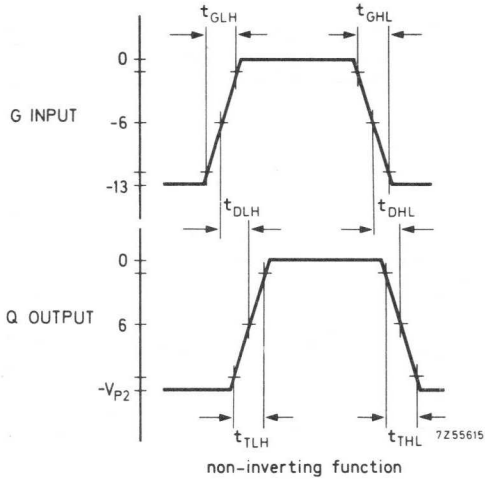
Note 1: V_{P2} is independent of circuit operation and is used for output LOW only.

Note 2: Output buffer power supply current is almost entirely dependent on the external load.

Note 3: Delays are measured at -6 V levels of input and output signals. (see also timing diagram on page 6).

CHARACTERISTICS (continued)

TIMING DIAGRAMS



Measurements performed under the following conditions:

$V_{P1} = -24$ to -28 V; $V_{P2} = -12$ to -14 V; $t_{GLH} = t_{GHL} = 150$ ns.

Note: The indicated points on the vertical axis are specified in the glossary of terms.

CHARACTERISTICS (continued)

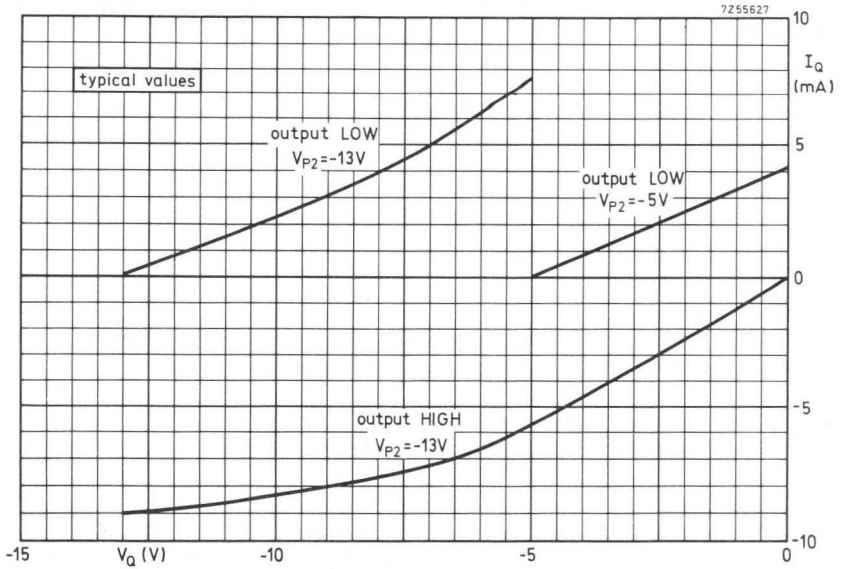
GLOSSARY OF TERMS

1. **Input signal rise time: t_{GLH}**
The time between the 90% and 10% voltage points as the input pulse goes from LOW to HIGH.
2. **Input signal fall time: t_{GHL}**
The time between the 10% and 90% voltage points as the input pulse goes from HIGH to LOW.
3. **Rise delay time: t_{DLH}**
The delay between the time the input arrives at its -6 V point and the time the output passes -6 V when going from LOW to HIGH.
4. **Fall delay time: t_{DHL}**
The delay between the time the input arrives at its -6 V point and the time the output passes -6 V when going from HIGH to LOW.
5. **Output rise transition time: t_{TLH}**
The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
6. **Output fall transition time: t_{THL}**
The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.

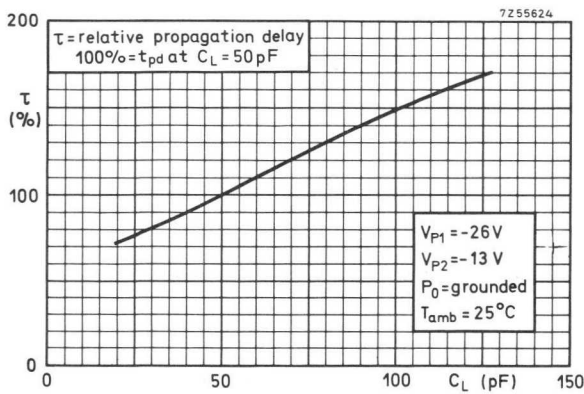


OUTPUT BUFFER DESCRIPTION

The FDH116 utilizes push-pull output buffers which exhibit the V_Q versus I_Q output curves, for both HIGH and LOW output, shown below.

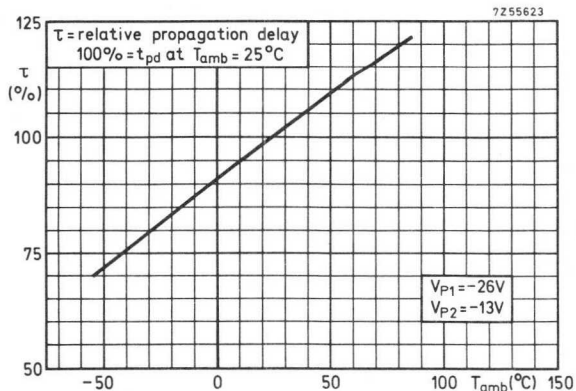


TYPICAL PERFORMANCE at load of C_L in parallel with $1\text{ M}\Omega$ to P_0 .

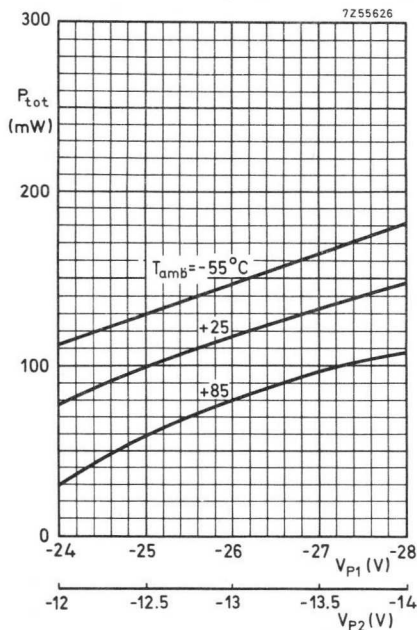


TYPICAL PERFORMANCE (continued)

Test conditions: $P_0 =$ grounded; standard load of 50 pF in parallel with 1 M Ω to P_0 .

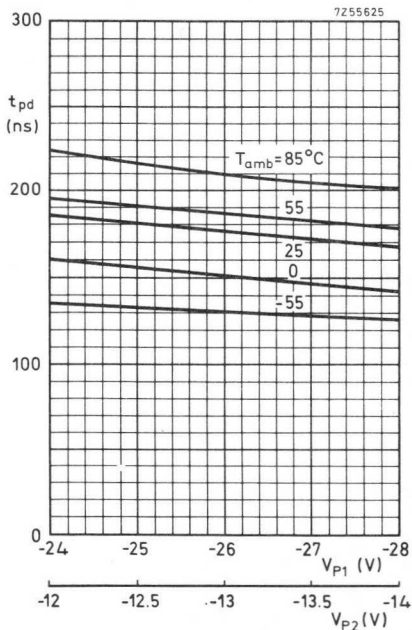


Rated propagation delay as a function of ambient temperature.



Power dissipation as a function of the supply voltage V_{P1} and V_{P2}

Note: output buffer power dissipation not included, since it is entirely dependent of loading conditions

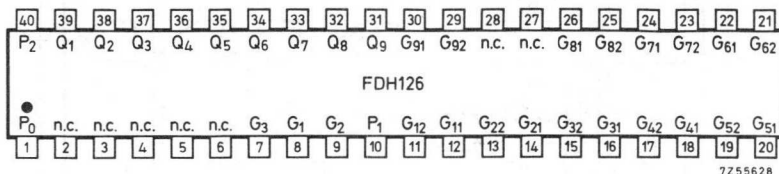


Propagation delay of Q_2 (slowest output) as a function of the supply voltages V_{P1} and V_{P2} .

1907
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1909
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1911

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

CARRY ARRAY

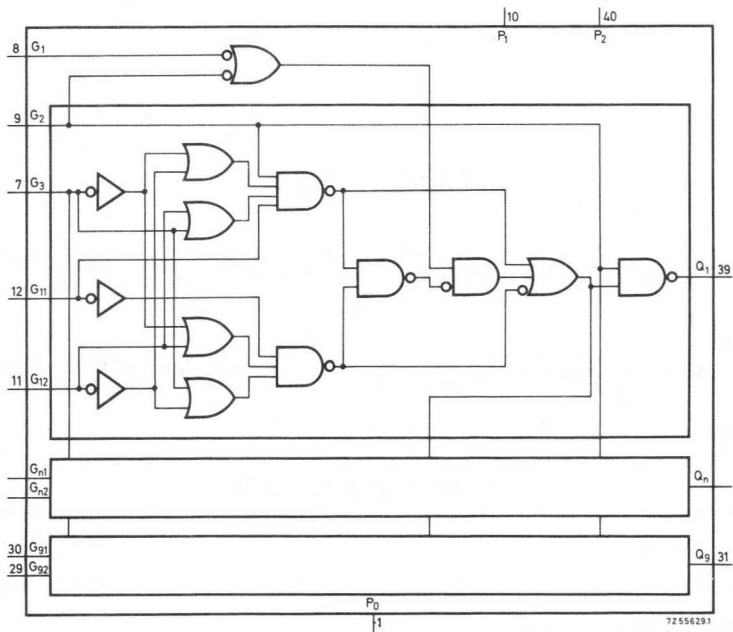


P₀ and metal lid on top of the package are connected.

QUICK REFERENCE DATA

| | | | |
|-------------------------------------------------------------------------------|---------------------------------|------------|----|
| Supply voltage | V _{P1} | -24 to -28 | V |
| Operating ambient temperature | T _{amb} | -55 to +85 | °C |
| Average propagation delay C _L = 50 pF; T _{amb} = 25 °C | t _{pd} | typ. 250 | ns |
| D. C. noise margin | M _H , M _L | > 1.0 | V |
| Power dissipation (f = 1 MHz) | P _{tot} | typ. 260 | mW |

PACKAGE OUTLINE 40 lead ceramic dual in-line (See General Section)



GENERAL DESCRIPTION

The FDH126 contains CARRY propagation circuits for a nine stage binary adder/subtractor. It can be cascaded for longer word lengths.

The device is intended to cooperate with the FDH106; e. g. three FDH106 and two FDH126 packages can be put together to make an 18-bit parallel adder/subtractor. By combining all the CARRY circuits in the same package, a very fast CARRY propagation is obtained.

All inputs are protected against over-voltage caused by static changes.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | |
|--------------------------------------------------------------------------------------|------------------|----------------|
| Voltage on all inputs, outputs and supply terminals with reference to P ₀ | | +0.5 to -30 V |
| Power dissipation up to T _{amb} = 70 °C | P _{tot} | max. 1 W |
| Junction temperature | T _j | max. 150 °C |
| Storage temperature | T _{stg} | -65 to +150 °C |
| Total current through terminal P ₂ | -I _{P2} | max. 40 mA |
| Current per output | ±I _Q | max. 20 mA |

THERMAL RESISTANCE

| | | | |
|--------------------------|---------------------|---|----------|
| From junction to ambient | R _{th j-a} | = | 125 °C/W |
|--------------------------|---------------------|---|----------|



FUNCTION TABLE

| G ₂ | G ₃ | Q _{n-1} | G _{n1} | G _{n2} | Q _n |
|----------------|----------------|------------------|-----------------|-----------------|----------------|
| H | X | H | H | X | H |
| H | H | H | L | H | L |
| H | H | H | L | L | H |
| H | H | L | H | H | L |
| H | H | L | H | L | H |
| H | X | L | L | X | L |
| H | L | H | L | H | H |
| H | L | H | L | L | L |
| H | L | L | H | H | H |
| H | L | L | H | L | L |
| L | X | X | X | X | L |

For n = 1:

$$Q_{n-1} = G_1$$

H = HIGH state (the less negative voltage)
 L = LOW state (the more negative voltage)
 X = state is immaterial

LOGIC FUNCTION

Positive logic:

$$Q_n = G_2 \cdot \{G_{n1} \cdot (\overline{G_3} \cdot G_{n2} + G_3 \cdot \overline{G_{n2}}) + Q_{n-1} (G_{n1} + \overline{G_3} \cdot G_{n2} + G_3 \cdot \overline{G_{n2}})\}$$

Negative logic:

$$Q_n = G_2 + G_{n1} \cdot (G_3 \cdot G_{n2} + \overline{G_3} \cdot \overline{G_{n2}}) + Q_{n-1} (G_{n1} + G_3 \cdot G_{n2} + \overline{G_3} \cdot \overline{G_{n2}})$$

CHARACTERISTICS

Test conditions: $V_{P1} = -24$ to -28 V; $V_{P2} = -12$ to -14 V; $T_{amb} = -55$ to $+85$ °C
 P_0 = grounded; standard load for Q_8 and Q_9 : 50 pF in parallel with $1M\Omega$ to P_0 ; for Q_1 to Q_7 , 25 pF in parallel with $1M\Omega$ to P_0 .

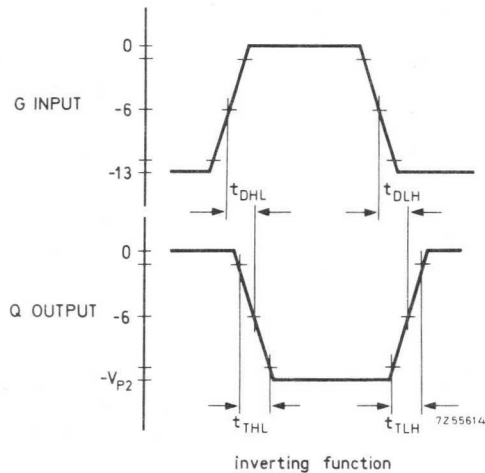
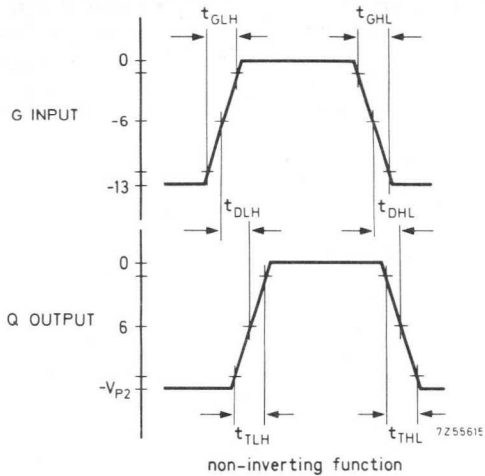
| | Symbol | min. | typ. ¹⁾ | max. | Conditions and references |
|--------------------------|-----------|------|--------------------|-------------|-----------------------------------------------------------------------|
| Input logic levels | | | | | |
| HIGH | V_{GH} | -2 | 0 | +0.3 V | |
| LOW | V_{GL} | -28 | - | -9 V | |
| Output levels | | | | | |
| HIGH | V_{QH} | -1.0 | - | 0 V | |
| LOW | V_{QL} | -14 | - | -10 V | |
| Input capacitance | | | | | |
| $G_1; G_{11}$ to G_9 | C_G | - | 4.5 | 6.0 pF | } bias: $V_G = 0$ V; $f = 1$ MHz |
| G_2 | C_{G2} | - | 6.8 | 9.0 pF | |
| G_3 | C_{G3} | - | 9.5 | 12.5 pF | |
| Input leakage current | $-I_{GL}$ | - | - | 1 μ A | { $V_G = -15$ V; $T_{amb} = 25$ °C all other terminals at V_{P0} |
| Output resistance | | | | | |
| Q_1 to Q_7 | R_{QH} | - | 1.4 | - $k\Omega$ | $V_Q = -1$ V |
| | R_{QL} | - | 3.7 | - $k\Omega$ | $V_Q = -10$ V |
| $Q_8; Q_9$ | R_{QH} | - | 0.5 | - $k\Omega$ | $V_Q = -1$ V |
| | R_{QL} | - | 1.7 | - $k\Omega$ | $V_Q = -10$ V |
| Supply currents | | | | | |
| | $-I_{P1}$ | - | 8.0 | 13.0 mA | } $f = 1$ MHz; $T_{amb} = 25$ °C |
| | $-I_{P2}$ | - | 4.0 | 6.0 mA | |
| Output transition times: | | | | | |
| fall time | t_{THL} | - | 150 | - ns | |
| rise time | t_{TLH} | - | 100 | - ns | |
| Delay times: | | | | | |
| (any input to output) | | | | | |
| fall time | t_{DHL} | - | 250 | 500 ns | } see note |
| rise time | t_{DLH} | - | 250 | 500 ns | |

1) All typ. values measured at: $V_{P1} = -26$ V; $V_{P2} = -13$ V; $T_{amb} = 25$ °C.

Note: Delays are measured at -6 V levels of input and output signals.
 (see also timing diagrams on page 6)

CHARACTERISTICS (continued)

TIMING DIAGRAMS



Measurements performed under the following conditions:

$$V_{P1} = -24 \text{ to } -28 \text{ V}; V_{P2} = -12 \text{ to } -14 \text{ V}; t_{GLH} = t_{GHL} = 150 \text{ ns.}$$

Note: The indicated points on the vertical axis are specified in the glossary of terms.

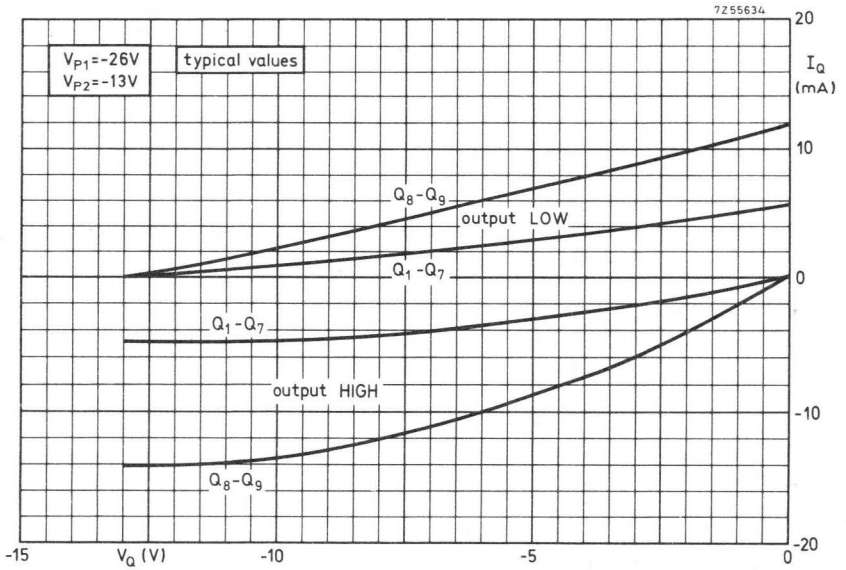
CHARACTERISTICS (continued)

GLOSSARY OF TERMS

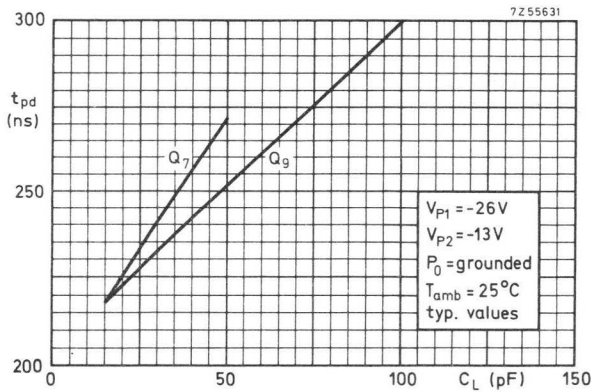
1. Input signal rise time: t_{GLH}
The time between the 90% and 10% voltage points as the input pulse goes from LOW to HIGH.
2. Input signal fall time: t_{GHL}
The time between the 10% and 90% voltage points as the input pulse goes from HIGH to LOW.
3. Rise delay time: t_{DLH}
The delay between the time the input arrives at its -6 V point and the time the output passes -6 V when going from LOW to HIGH.
4. Fall delay time: t_{DHL}
The delay between the time the input arrives at its -6 V point and the time the output passes -6 V when going from HIGH to LOW.
5. Output rise transition time: t_{TLH}
The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
6. Output fall transition time: t_{THL}
The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.

OUTPUT BUFFER DESCRIPTION

The FDH126 utilizes push-pull output buffers which exhibit the V_Q versus I_Q output curves, for both HIGH and LOW output, shown below.

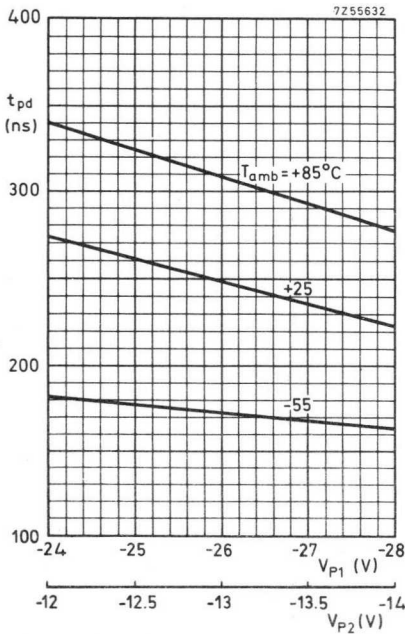
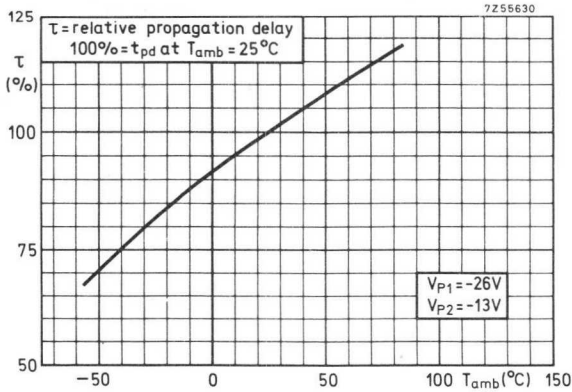


TYPICAL PERFORMANCE at load: C_L in parallel with $1 M\Omega$ to P_0 .

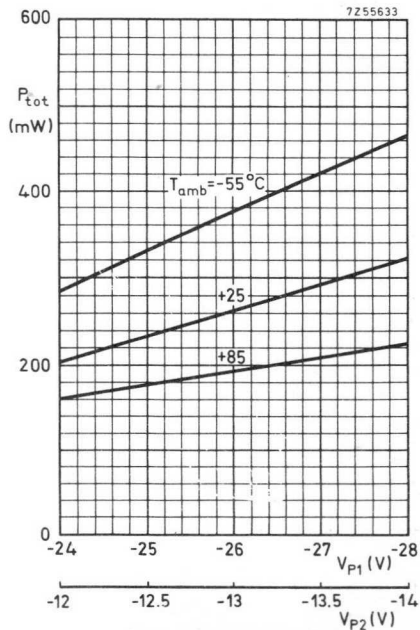


TYPICAL PERFORMANCE (continued)

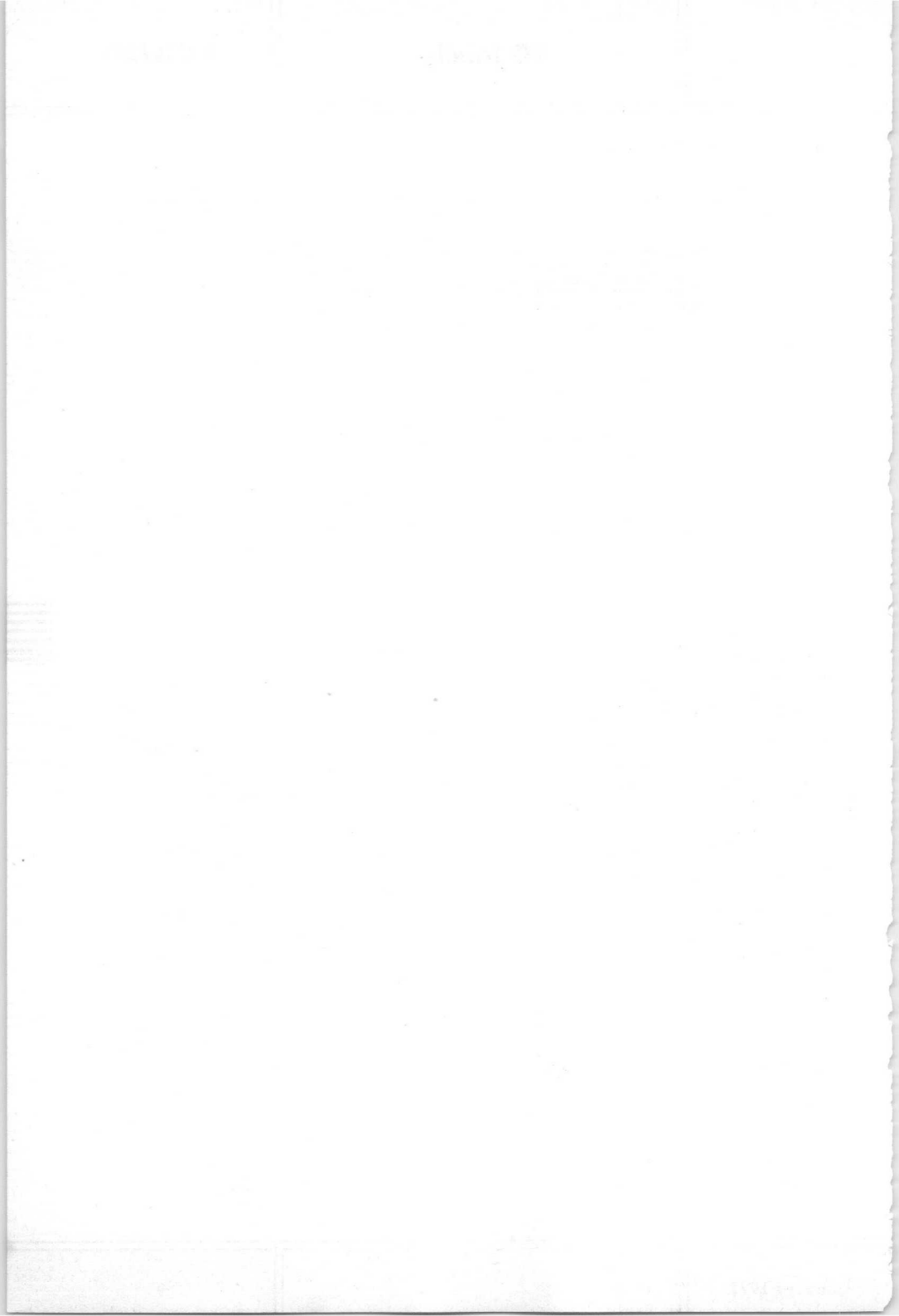
Test conditions: P_0 = grounded; standard load: 50 pF in parallel with 1 M Ω to P_0 .



Power dissipation as a function of the supply voltages V_{P1} and V_{P2}

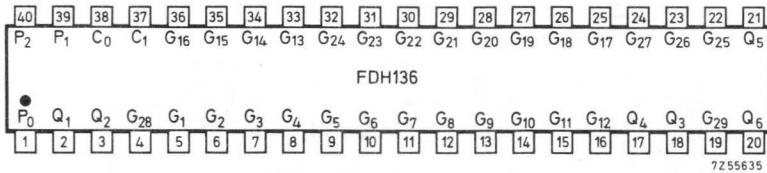


Propagation delay as a function of the supply voltages V_{P1} and V_{P2}



The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

AND-OR GATING ARRAY

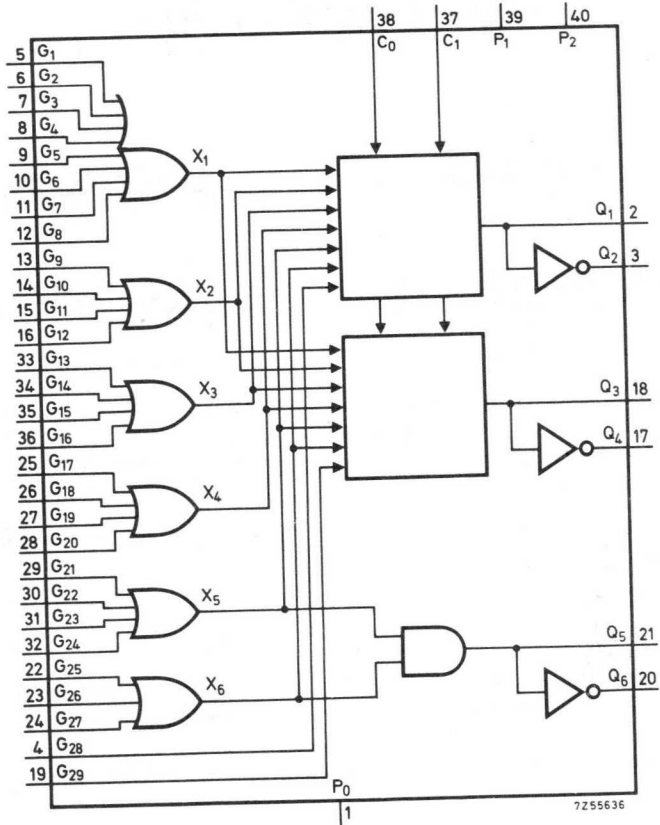


P_0 and metal lid on top of the package are connected.

QUICK REFERENCE DATA

| | | | |
|---------------------------------------------------------------|------------|------------|----|
| Supply voltage | V_{P1} | -24 to -28 | V |
| Operating ambient temperature | T_{amb} | -55 to +85 | °C |
| Average propagation delay $C_L = 50$ pF; $T_{amb} = 25$ °C | t_{pd} | typ. 180 | ns |
| D. C. noise margin | M_H, M_L | > 1.0 | V |
| Power consumption ($f = 1$ MHz) | P_{tot} | typ. 230 | mW |

PACKAGE OUTLINE 40 lead ceramic dual in-line (See General Section)



GENERAL DESCRIPTION

The FDH136 contains general purpose, expandable OR/AND/NAND gates. Two control lines C_0 and C_1 provide four different logic configurations, as shown in the function table.

Complementary outputs are available.

All inputs are protected against over-voltages caused by static charges.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|-----------------------------------------------------------------------------|-----------|-------------|------------------|
| Voltage on all inputs, outputs and supply terminals with reference to P_0 | | +0.5 to -30 | V |
| Power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$ | P_{tot} | max. 1 | W |
| Junction temperature | T_j | max. 150 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | -65 to +150 | $^\circ\text{C}$ |
| Total current through terminal P_2 | $-I_{P2}$ | max. 40 | mA |
| Output current (per output) | $\pm I_Q$ | max. 20 | mA |

THERMAL RESISTANCE

| | | | | |
|--------------------------|---------------|---|-----|--------------------|
| From junction to ambient | $R_{th\ j-a}$ | = | 125 | $^\circ\text{C/W}$ |
|--------------------------|---------------|---|-----|--------------------|

FUNCTION TABLE

| | | logic equation | |
|----------------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| C ₀ | C ₁ | positive logic | negative logic |
| X | X | $X_1 = G_1 + G_2 + G_3 + G_4 + G_5 + G_6 + G_7 + G_8$ $X_2 = G_9 + G_{10} + G_{11} + G_{12}$ $X_3 = G_{13} + G_{14} + G_{15} + G_{16}$ $X_4 = G_{17} + G_{18} + G_{19} + G_{20}$ $X_5 = G_{21} + G_{22} + G_{23} + G_{24}$ $X_6 = G_{25} + G_{26} + G_{27}$ $Q_5 = X_5 \cdot X_6$ $Q_6 = \overline{X_5} + \overline{X_6}$ | $X_1 = G_1 \cdot G_2 \cdot G_3 \cdot G_4 \cdot G_5 \cdot G_6 \cdot G_7 \cdot G_8$ $X_2 = G_9 \cdot G_{10} \cdot G_{11} \cdot G_{12}$ $X_3 = G_{13} \cdot G_{14} \cdot G_{15} \cdot G_{16}$ $X_4 = G_{17} \cdot G_{18} \cdot G_{19} \cdot G_{20}$ $X_5 = G_{21} \cdot G_{22} \cdot G_{23} \cdot G_{24}$ $X_6 = G_{25} \cdot G_{26} \cdot G_{27}$ $Q_5 = X_5 + X_6$ $Q_6 = \overline{X_5} \cdot \overline{X_6}$ |
| L | L | $Q_1 = X_1 \cdot X_2 \cdot X_3 \cdot G_{28}$ $Q_2 = \overline{X_1} + \overline{X_2} + \overline{X_3} + G_{28}$ $Q_3 = X_4 \cdot X_5 \cdot X_6 \cdot G_{29}$ $Q_4 = \overline{X_4} + \overline{X_5} + \overline{X_6} + G_{29}$ | $Q_1 = X_1 + X_2 + X_3 + G_{28}$ $Q_2 = \overline{X_1} \cdot \overline{X_2} \cdot \overline{X_3} \cdot G_{28}$ $Q_3 = X_4 + X_5 + X_6 + G_{29}$ $Q_4 = \overline{X_4} \cdot \overline{X_5} \cdot \overline{X_6} \cdot G_{29}$ |

FUNCTION TABLE (continued)

| C ₀ | C ₁ | logic equation | |
|----------------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| | | positive logic | negative logic |
| L | H | $Q_1 = X_1 \cdot X_2 \cdot X_3 \cdot X_4 \cdot X_5 \cdot X_6 \cdot G_{28}$ $Q_2 = \overline{X_1} + \overline{X_2} + \overline{X_3} + \overline{X_4} + \overline{X_5} + \overline{X_6} + G_{28}$ $Q_3 = X_1 \cdot X_2 \cdot G_{29}$ $Q_4 = \overline{X_1} + \overline{X_2} + G_{29}$ | $Q_1 = X_1 + X_2 + X_3 + X_4 + X_5 + X_6 + G_{28}$ $Q_2 = \overline{X_1} \cdot \overline{X_2} \cdot \overline{X_3} \cdot \overline{X_4} \cdot \overline{X_5} \cdot \overline{X_6} \cdot G_{28}$ $Q_3 = X_1 + X_2 + G_{29}$ $Q_4 = \overline{X_1} \cdot \overline{X_2} \cdot G_{29}$ |
| H | L | $Q_1 = X_1 \cdot X_2 \cdot G_{28}$ $Q_2 = \overline{X_1} + \overline{X_2} + G_{28}$ $Q_3 = X_3 \cdot X_4 \cdot G_{29}$ $Q_4 = \overline{X_3} + \overline{X_4} + G_{29}$ | $Q_1 = X_1 + X_2 + G_{28}$ $Q_2 = \overline{X_1} \cdot \overline{X_2} \cdot G_{28}$ $Q_3 = X_3 + X_4 + G_{29}$ $Q_4 = \overline{X_3} \cdot \overline{X_4} \cdot G_{29}$ |
| H | H | $Q_1 = X_1 \cdot X_2 \cdot X_3 \cdot X_4 \cdot G_{28}$ $Q_2 = \overline{X_1} + \overline{X_2} + \overline{X_3} + \overline{X_4} + G_{28}$ $Q_3 = X_5 \cdot X_6 \cdot G_{29}$ $Q_4 = \overline{X_5} + \overline{X_6} + G_{29}$ | $Q_1 = X_1 + X_2 + X_3 + X_4 + G_{28}$ $Q_2 = \overline{X_1} \cdot \overline{X_2} \cdot \overline{X_3} \cdot \overline{X_4} \cdot G_{28}$ $Q_3 = X_5 + X_6 + G_{29}$ $Q_4 = \overline{X_5} \cdot \overline{X_6} \cdot G_{29}$ |

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial



CHARACTERISTICS

Test conditions: $V_{P1} = -24$ to -28 V; $V_{P2} = -12$ to -14 V; $T_{amb} = -55$ to $+85$ °C;
 $P_0 =$ grounded; standard load : 50 pF in parallel with 1 M Ω to P_0 .

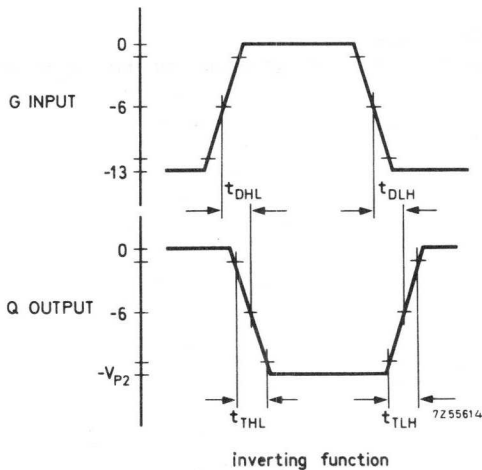
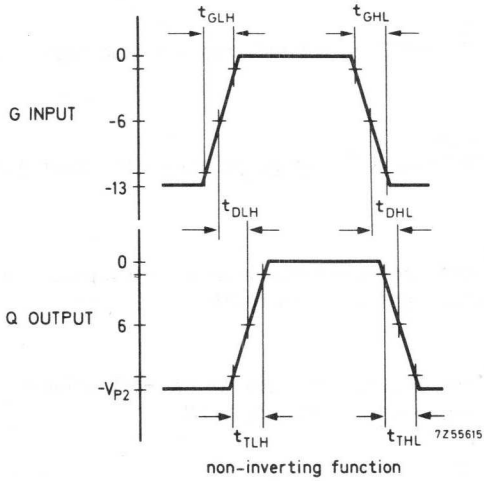
| | Symbol | min. | typ. ¹⁾ | max. | Conditions and references |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|------|--------------------|--------------|---------------------------------------------------------------------------------|
| Input logic levels | | | | | |
| HIGH | V_{GH}, V_{CH} | -2 | - | +0.3 V | |
| LOW | V_{GL}, V_{CL} | -28 | - | -9 V | |
| Output levels | | | | | |
| HIGH | V_{QH} | -1.0 | - | 0 V | |
| LOW | V_{QL} | -14 | - | -10 V | |
| Input capacitance | G_G, C_C | - | 3 | 5.5 pF | { bias: $V_G = V_C = 0$ V; f = 1 MHz |
| Leakage current | $-I_{GL},$ $-I_{CL}$ | - | - | 1 mA | { $V_G = V_C = -15$ V; $T_{amb} = 25$ °C; all other terminals at V_{P0} |
| Output resistance | | | | | |
| HIGH | R_{QH} | - | 0.4 | - k Ω | $V_Q = -1$ V |
| LOW | R_{QL} | - | 1 | - k Ω | $V_Q = -10$ V |
| Supply currents | $-I_{P1}$ $-I_{P2}$ | - | 4.5 8 | 7.5 13 mA | { f = 1 MHz; $T_{amb} = 25$ °C |
| Output transition times: | | | | | |
| fall time | t_{THL} | - | 150 | - ns | |
| rise time | t_{TLH} | - | 150 | - ns | |
| Delay times: | | | | | |
| (any input to output) | | | | | |
| fall time | t_{DHL} | - | 180 | 400 ns | |
| rise time | t_{DLH} | - | 180 | 400 ns | |
| Control input sink current: $G_1; G_2; G_4; G_5;$ $G_7; G_8; G_{10}; G_{12}; G_{13};$ $G_{15}; G_{17}; G_{19}; G_{21}; G_{23};$ $G_{26}; C_0; C_1$ | $-I_G, -I_C$ | - | 25 | - μ A | { $V_G = V_C = -2$ V; see note |

1) Typical values are measured at $V_{P1} = -26$ V; $V_{P2} = -13$ V; $T_{amb} = 25$ °C.

Note: Inputs mentioned are provided with a pull-down resistor to terminal P_2 .

These inputs, when not used, may be left floating; they will then be in the LOW state.

CHARACTERISTICS (continued)

TIMING DIAGRAMS

Measurements performed under the following conditions:

$$V_{P1} = -24 \text{ to } -28 \text{ V}; V_{P2} = -12 \text{ to } -14 \text{ V}; t_{GLH} = t_{GHL} = 150 \text{ ns.}$$

Note: The indicated points on the vertical axis are specified in the glossary of terms.

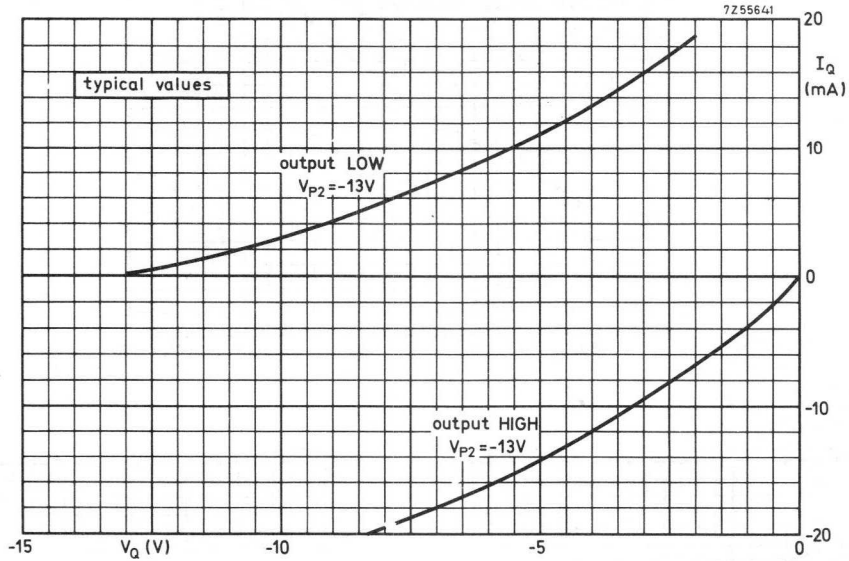
CHARACTERISTICS (continued)

GLOSSARY OF TERMS

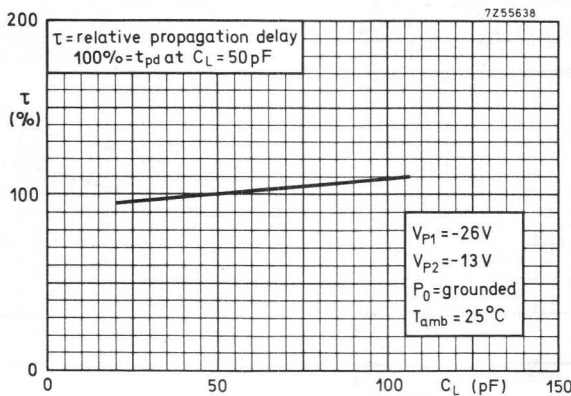
1. Input signal rise time: t_{GLH}
The time between the 90% and 10% voltage points as the input pulse goes from LOW to HIGH.
2. Input signal fall time: t_{GHL}
The time between the 10% and 90% voltage points as the input pulse goes from HIGH to LOW.
3. Rise delay time: t_{DLH}
The delay between the time the input arrives at its -6 V point and the time the output passes -6 V when going from LOW to HIGH.
4. Fall delay time: t_{DHL}
The delay between the time the input arrives at its -6 V point and the time the output passes -6 V when going from HIGH to LOW.
5. Output rise transition time: t_{TLH}
The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
6. Output fall transition time: t_{THL}
The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.

OUTPUT BUFFER DESCRIPTION

The FDH136 utilizes push-pull output buffers which exhibit the V_Q versus I_Q output curves, for both HIGH and LOW output, shown below.

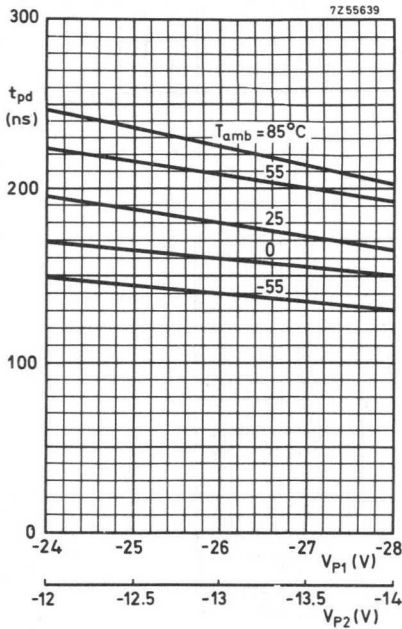
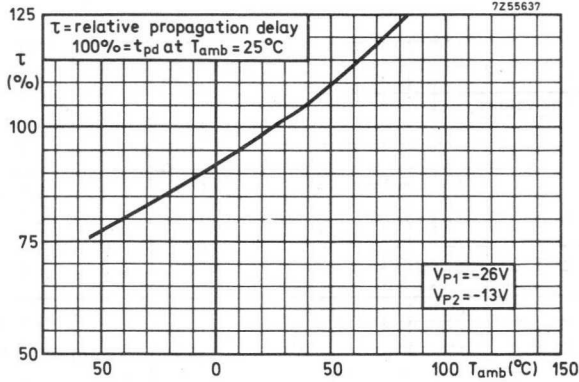


TYPICAL PERFORMANCE at load C_L in parallel with $1 M\Omega$ to P_0 .

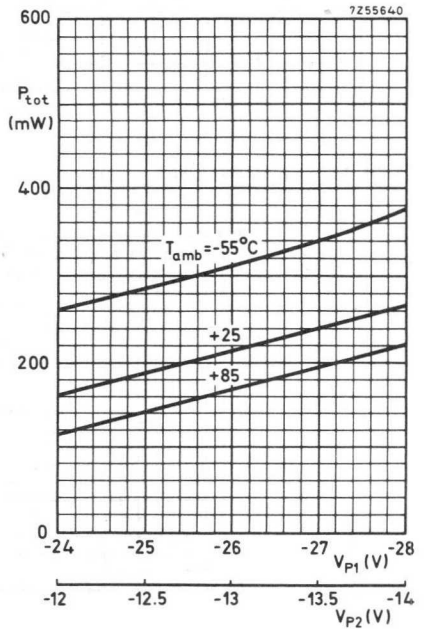


TYPICAL PERFORMANCE (continued)

Test conditions: P_0 = grounded; standard load of 50 pF in parallel with 1 M Ω to P_0 .



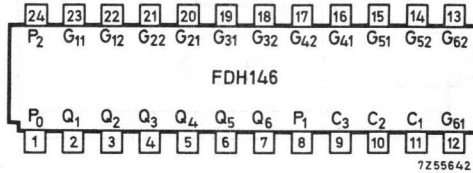
Power dissipation as a function of the supply voltages V_{P1} and V_{P2}



Propagation delay as a function of the supply voltages V_{P1} and V_{P2}

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

VARIABLE GATE ARRAY

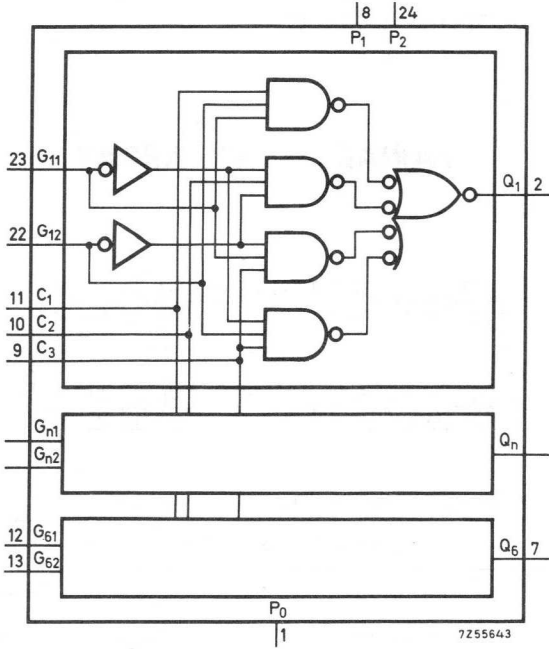


P_0 and metal lid on bottom of the package are connected.

QUICK REFERENCE DATA

| | | | |
|------------------------------------------------------------------------|------------|------------|-------------|
| Supply voltage | V_{P1} | -24 to -28 | V |
| Operating ambient temperature | T_{amb} | -55 to +85 | $^{\circ}C$ |
| Average propagation delay $C_L = 50$ pF; $T_{amb} = 25$ $^{\circ}C$ | t_{pd} | typ. 250 | ns |
| D. C. noise margin | M_H, M_L | > 1.0 | V |
| Average power consumption per function ($f = 1$ MHz) | P_{av} | typ. 35 | mW |

PACKAGE OUTLINE 24 lead ceramic dual in-line (See General Section)



GENERAL DESCRIPTION

The FDH146 consists of six, identical, 2-input gate networks. Three coded control lines determine the function of the six gate networks, so that eight different functions can be selected; the selected function is available six times.

The control inputs have pull-down resistors connected to P₂, so that they assume the LOW state, when left floating.

All inputs are protected against over-voltage caused by static charges.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | |
|--------------------------------------------------------------------------------------|------------------|----------------|
| Voltage on all inputs, outputs and supply terminals with reference to P ₀ | | +0.5 to -30 V |
| Power dissipation up to T _{amb} = 25 °C | P _{tot} | max. 1 W |
| Junction temperature | T _j | max. 150 °C |
| Storage temperature | T _{stg} | -65 to +150 °C |
| Total current through terminal P ₂ | -I _{P2} | max. 40 mA |
| Output current per output | ±I _Q | max. 20 mA |

THERMAL RESISTANCE

| | | | |
|--------------------------|---------------------|---|----------|
| From junction to ambient | R _{th j-a} | = | 125 °C/W |
|--------------------------|---------------------|---|----------|

FUNCTION TABLE

| C ₃ C ₂ C ₁ | logic equation (positive logic) | logic function | |
|----------------------------------------------|-------------------------------------------------------------------------|----------------|----------------|
| | | positive logic | negative logic |
| L L L | $Q_n = 1$ | - | - |
| L L H | $Q_n = \overline{G_{n1}} \cdot G_{n2}$ | NAND | NOR |
| L H L | $Q_n = G_{n1} + G_{n2}$ | OR | AND |
| L H H | $Q_n = G_{n1} \cdot \overline{G_{n2}} + \overline{G_{n1}} \cdot G_{n2}$ | exclusive-OR | comparator |
| H L L | $Q_n = \overline{G_{n1}} \cdot G_{n2} + G_{n1} \cdot \overline{G_{n2}}$ | comparator | exclusive-OR |
| H L H | $Q_n = \overline{G_{n1}} + G_{n2}$ | NOR | NAND |
| H H L | $Q_n = G_{n1} \cdot G_{n2}$ | AND | OR |
| H H H | $Q_n = 0$ | - | - |

CHARACTERISTICS

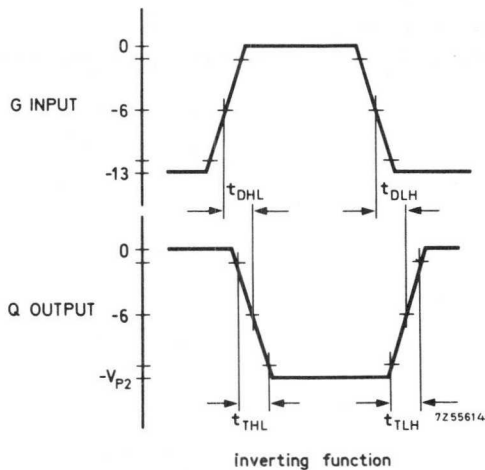
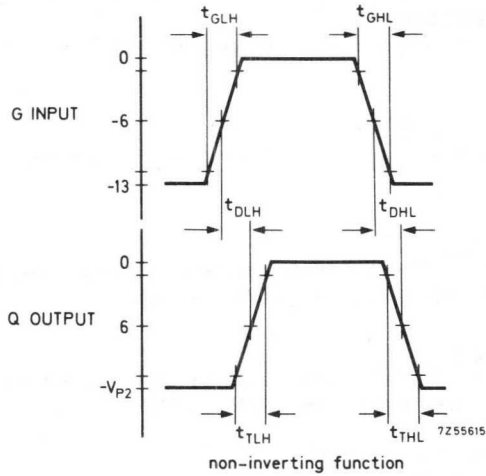
Test conditions: $V_{P1} = -24$ to -28 V; $V_{P2} = -12$ to -14 V; $T_{amb} = -55$ to $+85$ °C;
 $P_0 =$ grounded; standard load : 50 pF in parallel with 1 M Ω to P_0 .

| | Symbol | min. | typ. ¹⁾ | max. | Conditions and references |
|-----------------------------|------------------------|------|--------------------|--------------|------------------------------------------------------------------------|
| Input logic levels | | | | | |
| HIGH | V_{GH} | -2 | 0 | +0.3 V | |
| LOW | V_{GL} | -28 | - | -9 V | |
| Output levels | | | | | |
| HIGH | V_{QH} | -1.0 | - | 0 V | |
| LOW | V_{QL} | -14 | - | -10 V | |
| Input capacitance | | | | | |
| $C_1; C_2$ | C_{C1}, C_{C2} | - | 5.5 | 7 pF | } bias: $V_G = 0V$ } $f = 1MHz$ |
| C_3 | C_{C3} | - | 9.5 | 11 pF | |
| G_{11} to G_{62} | C_{G11} to C_{G62} | - | 3.5 | 5 pF | |
| Input leakage current | $-I_{GL}$ | - | - | 1 μA | } $V_G = -15V; T_{amb} = 25^\circ C$; all other terminals at V_{P0} |
| Output resistance | | | | | |
| HIGH | R_{QH} | - | 1.0 | - k Ω | $V_Q = -1 V$ |
| LOW | R_{QL} | - | 2.0 | - k Ω | $V_Q = -10 V$ |
| Supply currents | | | | | |
| $-I_{P1}$ | | - | 4.6 | 7.0 mA | } $f = 1 MHz$ } $T_{amb} = 25^\circ C$ |
| $-I_{P2}$ | | - | 6.2 | 8.5 mA | |
| Output transition times: | | | | | |
| fall time | t_{THL} | - | 150 | - ns | |
| rise time | t_{TLH} | - | 150 | - ns | |
| Delay times | | | | | |
| (any input to output) | | | | | |
| fall time | t_{DHL} | - | 250 | 400 ns | |
| rise time | t_{DLH} | - | 250 | 400 ns | |
| Control input sink current: | | | | | |
| C_1, C_2 | $-I_{C1}; -I_{C2}$ | - | 32 | - μA | } $V_G = -2 V$ |
| C_3 | $-I_{C3}$ | - | 64 | - μA | |

¹⁾ All typ. values are measured at: $T_{amb} = 25$ °C and $V_{P1} = -26$ V, $V_{P2} = -13$ V.

CHARACTERISTICS (continued)

TIMING DIAGRAMS



Measurements performed under the following conditions:

$$V_{P1} = -24 \text{ to } -28 \text{ V}; V_{P2} = -12 \text{ to } -14 \text{ V}; t_{GLH} = t_{GHL} = 150 \text{ ns.}$$

Note: The indicated points on the vertical axis are specified in the glossary of terms.

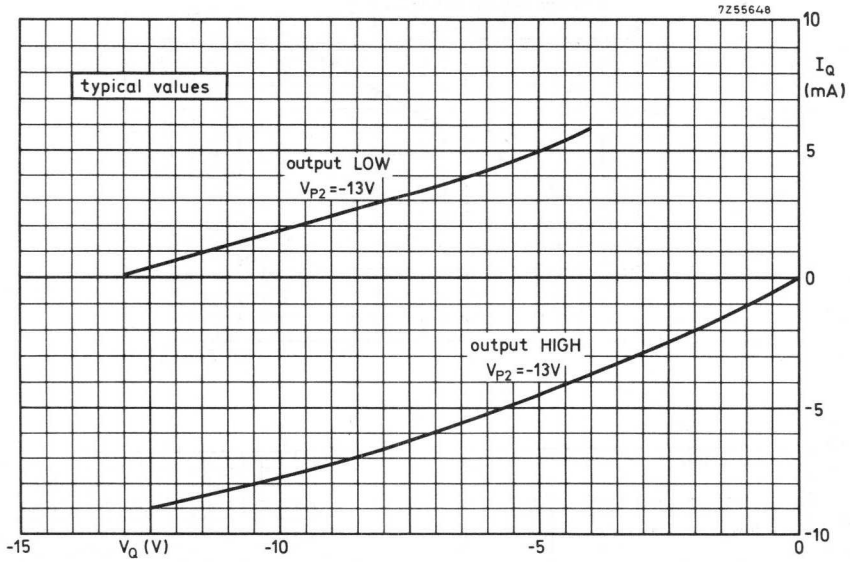
CHARACTERISTICS (continued)

GLOSSARY OF TERMS

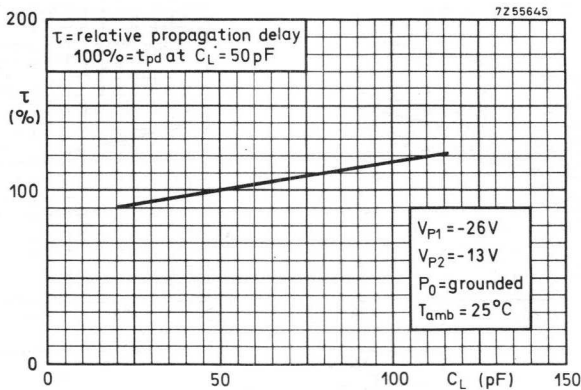
1. Input pulse rise time: t_{GLH}
The time between the 90% and 10% voltage points as the input pulse goes from LOW to HIGH.
2. Input pulse fall time: t_{GHL}
The time between the 10% and 90% voltage points as the input pulse goes from HIGH to LOW.
3. Rise delay time: t_{DLH}
The delay between the time the input arrives at its -6 V point and the time the output passes -6 V when going from LOW to HIGH.
4. Fall delay time: t_{DHL}
The delay between the time the input arrives at its -6 V point and the time the output passes -6 V when going from HIGH to LOW.
5. Output rise transition time: t_{TLH}
The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
6. Output fall transition time: t_{THL}
The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.

OUTPUT BUFFER DESCRIPTION

The FDH146 utilizes push-pull output buffers which exhibit the V_Q versus I_Q output curves, for both HIGH and LOW output, shown below.

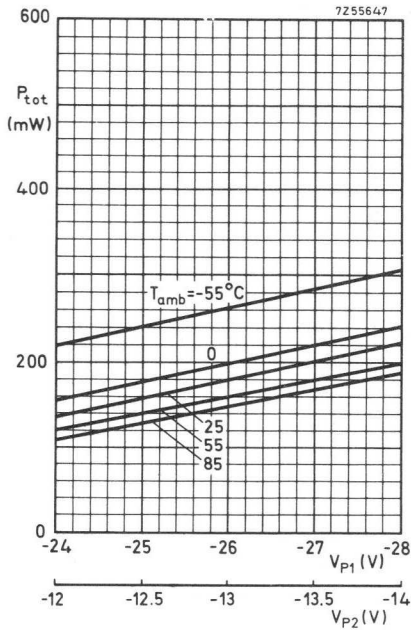
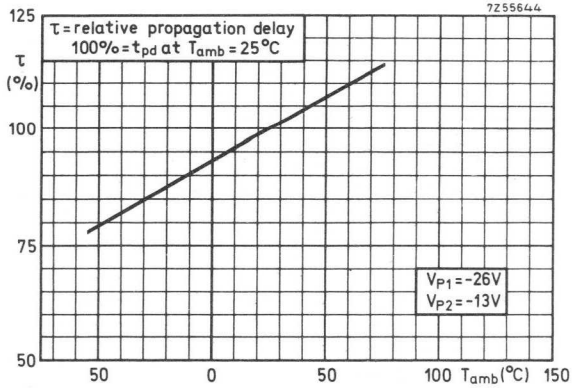


TYPICAL PERFORMANCE at load: C_L in parallel with $1 M\Omega$ to P_0

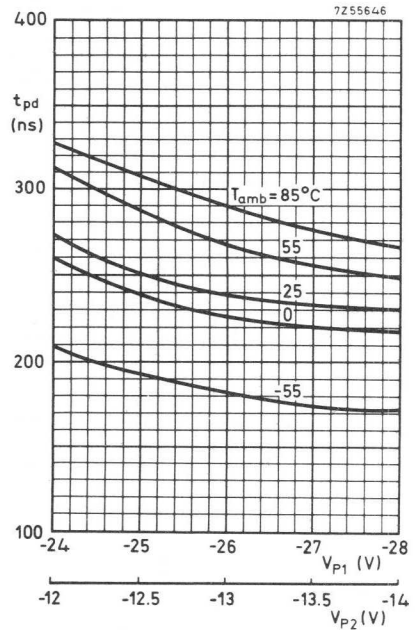


TYPICAL PERFORMANCE (continued)

Test conditions: $P_0 =$ grounded; standard load: 50 pF in parallel with 1 M Ω to P_0 .



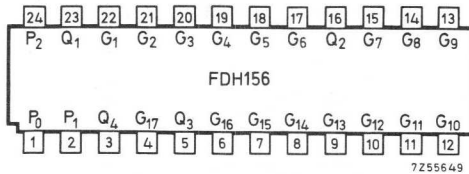
Power dissipation as a function of the supply voltages V_{P1} and V_{P2}



Propagation delay as a function of the supply voltages V_{P1} and V_{P2}

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

FIXED LOGIC ARRAY

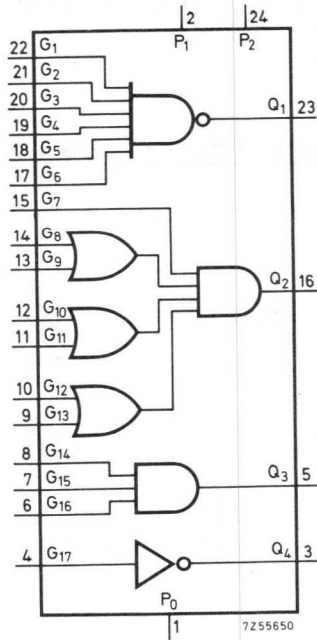


P₀ and metal lid on bottom of the package connected

QUICK REFERENCE DATA

| | | | |
|--------------------------------------------------------|---------------------------------|------------|----|
| Supply voltage | V _{P1} | -24 to -28 | V |
| Operating ambient temperature | T _{amb} | -55 to +85 | °C |
| Average propagation delay C _L = 50 pF | t _{pd} | typ. 150 | ns |
| D.C. noise margin | M _H , M _L | > 1.0 | V |
| Power dissipation f = 1 MHz; C _L = 50 pF | P _{tot} | typ. 160 | mW |

PACKAGE OUTLINE 24 lead ceramic dual in-line (See General Section)



GENERAL DESCRIPTION

The FDH156 contains all the logic functions shown in the diagram and described in the logic functions below. It is intended to perform logic functions in all MOS digital systems. The output voltage swing is determined by the output buffer supply voltage (V_{P2}).

All inputs are protected against over-voltage caused by static charges.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|-----------------------------------------------------------------------------|-----------|-------------|------------------|
| Voltage on all inputs, outputs and supply terminals with reference to P_0 | | +0.5 to -30 | V |
| Power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$ | P_{tot} | max. 1 | W |
| Junction temperature | T_j | max. 150 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | -65 to +150 | $^\circ\text{C}$ |
| Total current through terminal P_2 | $-I_{P2}$ | max. 40 | mA |
| Output current (per output) | $\pm I_Q$ | max. 20 | mA |

THERMAL RESISTANCE

| | | | | |
|--------------------------|---------------|---|-----|--------------------|
| From junction to ambient | $R_{th\ j-a}$ | = | 125 | $^\circ\text{C/W}$ |
|--------------------------|---------------|---|-----|--------------------|

LOGIC FUNCTIONS

Positive logic

$$Q_1 = \overline{G_1} \cdot G_2 \cdot G_3 \cdot G_4 \cdot G_5 \cdot G_6$$

$$Q_2 = G_7 \cdot (G_8 + G_9) \cdot (G_{10} + G_{11}) \cdot (G_{12} + G_{13})$$

$$Q_3 = G_{14} \cdot G_{15} \cdot G_{16}$$

$$Q_4 = \overline{G_{17}}$$

Negative logic

$$Q_1 = \overline{G_1 + G_2 + G_3 + G_4 + G_5 + G_6}$$

$$Q_2 = G_7 + (G_8 \cdot G_9) + (G_{10} \cdot G_{11}) + (G_{12} \cdot G_{13})$$

$$Q_3 = \overline{G_{14} + G_{15} + G_{16}}$$

$$Q_4 = \overline{G_{17}}$$

CHARACTERISTICS

Test conditions: $V_{P1} = -24$ to -28 V; $V_{P2} = -12$ to -14 V (see note 1); $T_{amb} = -55$ to $+85$ °C; $P_0 =$ grounded; standard load: 50 pF in parallel with 1 M Ω to P_0 .

| | Symbol | min. typ. ¹⁾ max. | | | Conditions and references |
|-------------------------------------------------|--------------------|------------------------------|-----|------|------------------------------------------------------------------------------------------------------------------------------|
| Input logic levels | | | | | |
| HIGH | V_{GH} | -2 | 0 | +0.3 | V |
| LOW | V_{GL} | -28 | - | -9 | V |
| Output levels | | | | | |
| HIGH | V_{QH} | -1.0 | - | 0 | V |
| LOW | V_{QL} | -14 | - | -10 | V |
| Input capacitance | C_G | - | 5 | 7 | pF bias: $V_G=0$; $f = 1$ MHz |
| Input leakage current | $-I_{GL}$ | - | - | 1 | μ A $\left\{ \begin{array}{l} V_G=-15V; T_{amb}=25^\circ C \\ \text{all other terminals at } V_{P0} \end{array} \right.$ |
| Output resistance | | | | | |
| HIGH | R_{QH} | - | 1 | - | k Ω $V_Q = -1$ V |
| LOW | R_{QL} | - | 2 | - | k Ω $V_Q = -10$ V |
| Supply currents | | | | | |
| $-I_{P1}$ | | - | 4.6 | 6.5 | mA $\left. \begin{array}{l} f = 1 \text{ MHz}; T_{amb} = 25^\circ C \\ \text{see note 2} \end{array} \right\}$ |
| $-I_{P2}$ | | - | 2.3 | 3.0 | mA |
| Output transition times: | | | | | |
| fall time | t_{THL} | - | 150 | - | ns |
| rise time | t_{TLH} | - | 150 | - | ns |
| Delay times (fall and rise times) | | | | | |
| G \rightarrow Q ₁ | t_{DHL}, t_{DLH} | - | 175 | 300 | ns $\left. \begin{array}{l} \\ \\ \end{array} \right\} \text{see note 3}$ |
| G \rightarrow Q ₂ ; Q ₃ | t_{DHL}, t_{DLH} | - | 150 | 250 | ns |
| G \rightarrow Q ₄ | t_{DHL}, t_{DLH} | - | 125 | 250 | ns |

Note 1: V_{P2} is independent of circuit operation and is used for output LOW only.

Note 2: Output buffer supply current is almost entirely dependent on the external load.

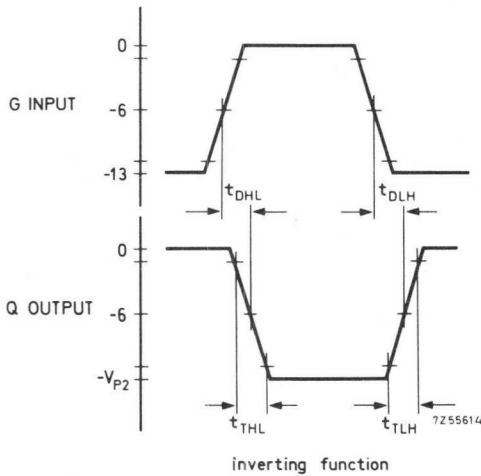
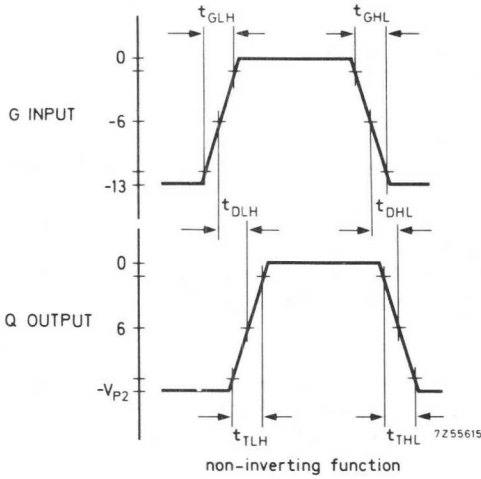
The value shown is for a load: 50 pF in parallel with 1 M Ω to P_0 .

Note 3: Delays are measured at -6 V levels of input and output signals.
(see also timing diagram on page 5)

¹⁾ All typ. values are measured at: $T_{amb} = 25$ °C ; $V_{P1} = -26$ V; $V_{P2} = -13$ V.

CHARACTERISTICS (continued)

TIMING DIAGRAMS



Measurements performed under the following conditions:

$$V_{P1} = -24 \text{ to } -28 \text{ V}; V_{P2} = -12 \text{ to } -14 \text{ V}; t_{GLH} = t_{GHL} = 150 \text{ ns.}$$

Note: The indicated points on the vertical axis are specified in the glossary of terms.

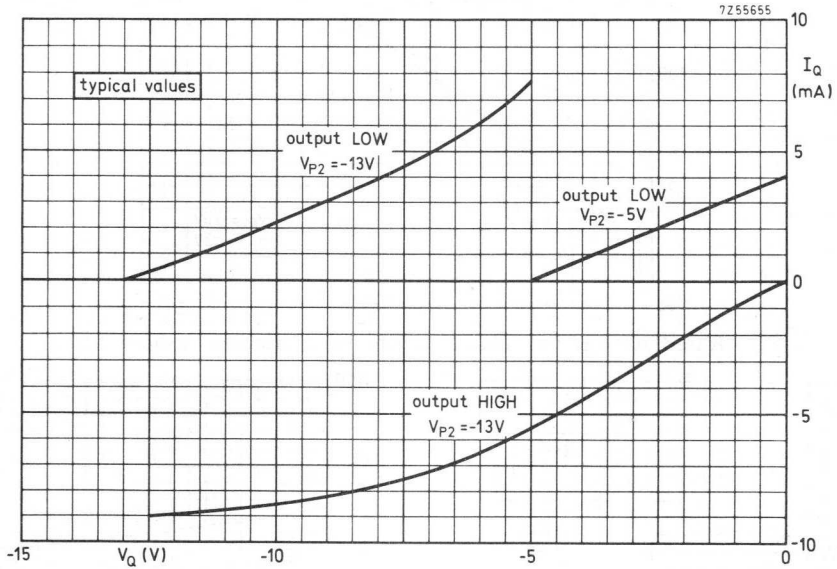
CHARACTERISTICS (continued)

GLOSSARY OF TERMS

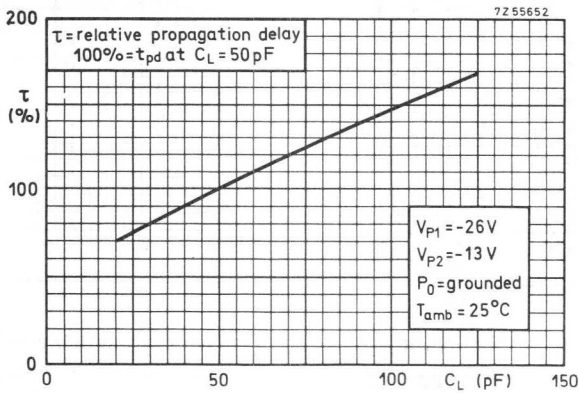
1. Input signal rise time: t_{GLH}
The time between the 90% and 10% voltage points as the input pulse goes from LOW to HIGH.
2. Input signal fall time: t_{GHL}
The time between the 10% and 90% voltage points as the input pulse goes from HIGH to LOW.
3. Rise delay time: t_{DLH}
The delay between the time the input arrives at -6 V point and the time the output passes -6 V when going from LOW to HIGH.
4. Fall delay time: t_{DHL}
The delay between the time the input arrives at -6 V point and the time the output passes -6 V when going from HIGH to LOW.
5. Output rise transition time: t_{TLH}
The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
6. Output fall transition time: t_{THL}
The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.

OUTPUT BUFFER DESCRIPTION

The FDH156 utilizes push-pull output buffers which exhibit the V_Q versus I_Q output curves, for both HIGH and LOW output, shown below.

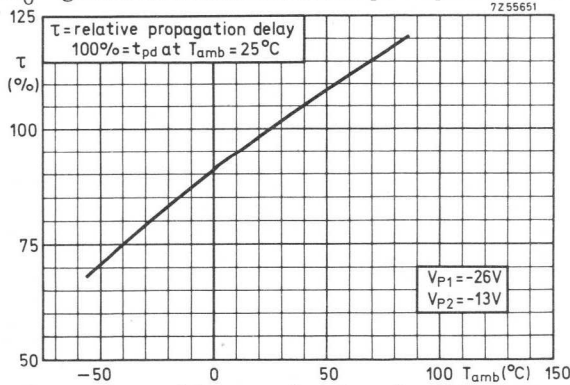


TYPICAL PERFORMANCE at load: C_L in parallel with $1 M\Omega$ to P_0 .

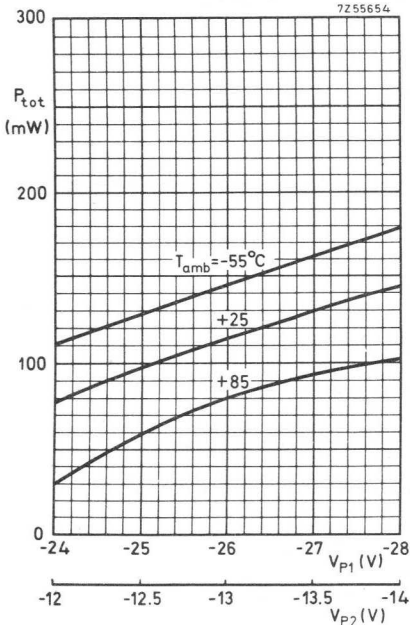


TYPICAL PERFORMANCE (continued)

Test conditions: $P_O =$ grounded; standard load: 50 pF in parallel with 1 M Ω to P_O .

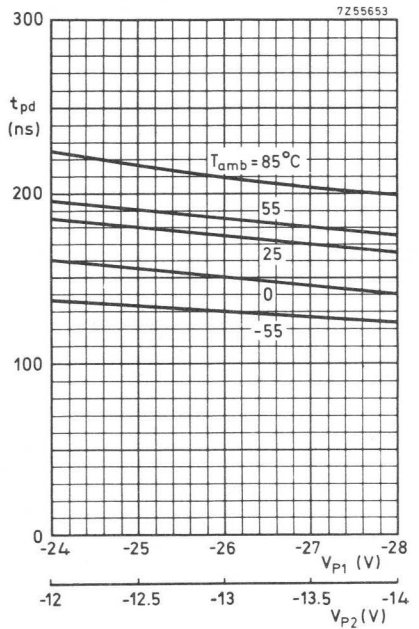


Rated propagation delay as a function of ambient temperature.



Power dissipation as a function of the supply voltages V_{P1} and V_{P2}

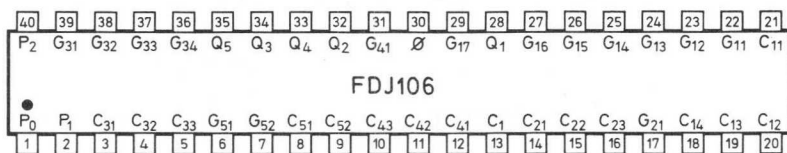
Note: output buffer power dissipation not included, since it is entirely dependent of loading conditions



Propagation delay of Q_2 (slowest output) as a function of the supply voltages V_{P1} and V_{P2} .

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

REGISTER ARRAY



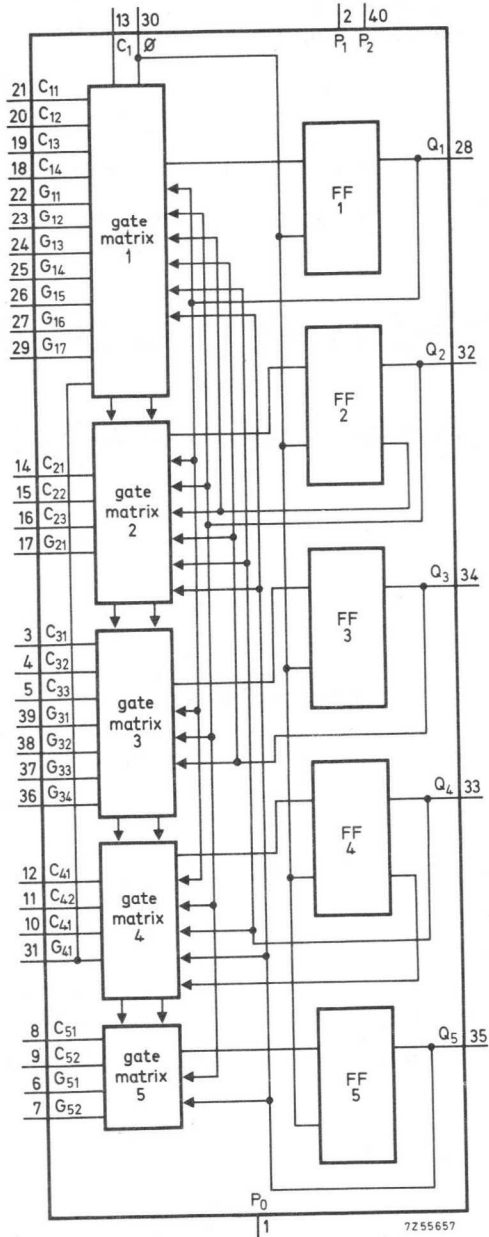
7255656

P_0 and metal lid on top of the package are connected.

QUICK REFERENCE DATA

| | | | |
|--------------------------------------------------------|------------|------------|-------------|
| Supply voltage | V_{P1} | -24 to -28 | V |
| Operating ambient temperature | T_{amb} | -55 to +85 | $^{\circ}C$ |
| Cycle time | | typ. 400 | ns |
| Propagation delay time at $C_L = 50$ pF | t_{pd} | typ. 150 | ns |
| D. C. noise margin | M_H, M_L | > 1.0 | V |
| Power dissipation $f_{\phi} = 1$ MHz; $C_L = 50$ pF | $P_{tot.}$ | typ. 180 | mW |

PACKAGE OUTLINE : 40 lead ceramic dual in-line (See General Section)



GENERAL DESCRIPTION

The FDJ106 is an array of 5 flip-flops, designed to act as a synchronous bit slice of a CPU.

Each of the 5 D-type flip-flops has at least one external input and output, as well as individually controlled transfer and input SELECT logic.

The input gating matrix can therefore enable transfers from external inputs or from other registers in the same array.

The register array contains one bit of each of the five main registers in most computers:

- FF1 - accumulator
- FF2 - memory data register
- FF3 - multiplier/quotient register
- FF4 - program counter
- FF5 - instruction register

All inputs are protected against over-voltage caused by static charge.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|-----------------------------------------------------------------------------|------------|-------------|------------------|
| Voltage on all inputs, outputs and supply terminals with reference to P_0 | | +0.5 to -30 | V |
| Power dissipation up to $T_{amb} = 25^\circ\text{C}$ | $P_{tot.}$ | max. 1 | W |
| Junction temperature | T_j | max. 150 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | -65 to +150 | $^\circ\text{C}$ |
| Total current through terminal P_2 | $-I_{P2}$ | max. 40 | mA |
| Current per output | $\pm I_Q$ | max. 20 | mA |

THERMAL RESISTANCE

| | | | |
|--------------------------|---------------|-------|--------------------|
| From junction to ambient | $R_{th\ j-a}$ | = 125 | $^\circ\text{C/W}$ |
|--------------------------|---------------|-------|--------------------|



LOGIC FUNCTION

REGISTER INPUT SELECTION TABLE

The FDJ106 outputs will conform to the following input transfer function table. With the given set of control inputs, including C_1 , which is common to all gate matrices, each flip-flop will have at its D-input the signal shown in the table below.

With the control inputs established, the output of each register will assume the state of its input after the positive going edge of ϕ .

| control input (for any gate matrix) | | | | Flip-flop inputs | | | | | | | | | | |
|-------------------------------------------|----------|----------|----------|------------------|----------|----------|----------|----------|-------------|------------------|----------|------------------|----------|--|
| | | | | C_1 : HIGH | | | | | C_1 : LOW | | | | | |
| C_{n4} | C_{n3} | C_{n2} | C_{n1} | FF1 | FF2 | FF3 | FF4 | FF5 | FF1 | FF2 | FF3 | FF4 | FF5 | |
| L | L | L | L | H | | | | | | G_{41} | | | | |
| L | L | L | H | G_{17} | | | | | | G_{17} | | | | |
| L | L | H | L | G_{16} | | | | | | G_{16} | | | | |
| L | L | H | H | G_{15} | | | | | | G_{15} | | | | |
| L | H | L | L | G_{14} | | | | | | G_{14} | | | | |
| L | H | L | H | G_{13} | | | | | | G_{13} | | | | |
| L | H | H | L | G_{12} | | | | | | G_{12} | | | | |
| L | H | H | H | G_{11} | | | | | | G_{11} | | | | |
| H | L | L | L | H | H | G_{34} | H | | Q_1 | $\overline{Q_2}$ | G_{34} | $\overline{Q_4}$ | | |
| H | L | L | H | H | H | G_{33} | H | | Q_1 | H | G_{33} | H | | |
| H | L | H | L | Q_5 | Q_5 | G_{32} | G_{41} | | Q_1 | G_{21} | G_{32} | L | | |
| H | L | H | H | Q_4 | Q_{21} | G_{31} | H | | Q_1 | Q_2 | G_{31} | Q_4 | | |
| H | H | L | L | $\overline{Q_2}$ | Q_4 | H | Q_1 | G_{52} | Q_1 | Q_2 | Q_3 | Q_4 | G_{52} | |
| H | H | L | H | Q_2 | Q_1 | Q_2 | Q_2 | G_{51} | Q_1 | Q_2 | Q_3 | Q_4 | G_{51} | |
| H | H | H | L | Q_3 | Q_3 | Q_1 | Q_5 | Q_2 | Q_1 | Q_2 | Q_3 | Q_4 | Q_5 | |
| H | H | H | H | Q_1 | Q_2 | Q_3 | Q_4 | Q_5 | Q_1 | Q_2 | Q_3 | Q_4 | Q_5 | |

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

CHARACTERISTICS

Test conditions: $V_{P1} = -24$ to -28 V; $V_{P2} = -12$ to -14 V; $T_{amb} = -55$ to $+85$ °C;
 $P_0 =$ grounded; standard load: 50 pF in parallel with 1 M Ω to P_0 .

| DRIVE REQUIREMENTS | Symbol | min. | typ. ¹⁾ | max. | Conditions and references |
|-----------------------------------------------------|---------------------------------|------|--------------------|------|---------------------------|
| Data and control input logic levels (except C_1) | | | | | |
| HIGH | V_{GH}, V_{CH} | -2 | - | +0.3 | V |
| LOW | V_{GL}, V_{CL} | -28 | - | -9 | V |
| C_1 input levels | | | | | |
| HIGH | V_{C1H} | -2 | - | 0.3 | V |
| LOW | V_{C1L} | -28 | - | -24 | V |
| Clock pulse width | $t_{\phi L}$ | 0.25 | - | 1.0 | μ s |
| Clock pulse transition times | $t_{\phi LH},$ $t_{\phi HL}$ | - | - | 0.1 | μ s |
| Clock pulse voltage levels: HIGH | $V_{\phi H}$ | -2 | - | +0.3 | V |
| LOW | $V_{\phi L}$ | -28 | -26 | -24 | V |

} see timing diagram on page 7.

¹⁾ All typical values are measured at: $V_{P1} = -26$ V; $V_{P2} = -13$ V; $T_{amb} = 25$ °C.

CHARACTERISTICS (continued)

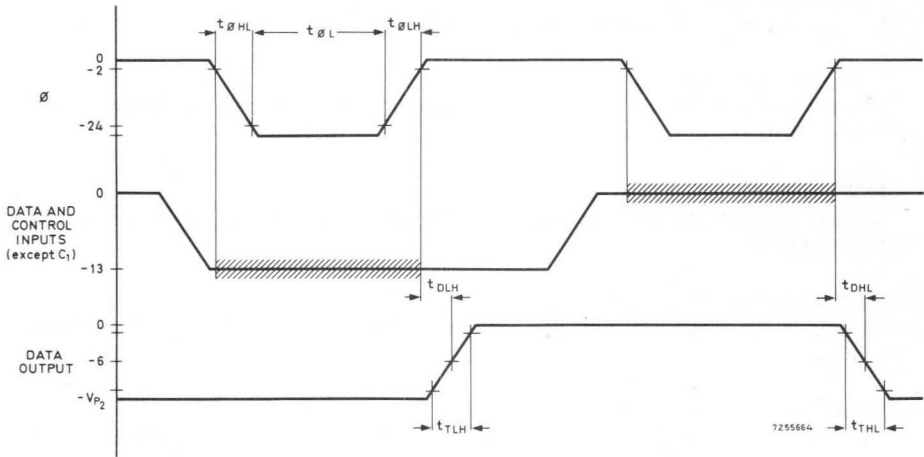
Test conditions: $V_{P1} = -24$ to -28 V; $V_{P2} = -12$ to -14 V; $T_{amb} = -55$ to $+85$ °C;
 P_0 = grounded; standard load: 50 pF in parallel with 1 M Ω to P_0 .

| | Symbol | min. | typ. ¹⁾ | max. | Conditions and references |
|--------------------------------------------------------|--------------------|------|--------------------|------|-------------------------------------------------------------------------------------------|
| Output logic levels | | | | | |
| HIGH | V_{QH} | -1.0 | - | 0 | V |
| LOW | V_{QL} | -14 | - | -10 | V |
| Input capacitance data and control (except C_1) | C_G, C_C | - | 4 | 7.5 | pF {bias: $V_G = V_C = 0$ V f = 1 MHz |
| C_1 | C_{C1} | - | 7 | 10 | pF bias: $V_{C1} = 0$ V; f = 1 MHz |
| clock input | C_ϕ | - | 20 | 25 | pF bias: $V_\phi = 0$ V; f = 1 MHz |
| Input leakage current data and control (except C_1) | $-I_{GL}, -I_{CL}$ | - | - | 1 | μ A {bias: $V_G = V_C = -15$ V; $T_{amb} = 25$ °C; all other terminals at V_{P0} |
| C_1 | $-I_{C1L}$ | - | - | 100 | μ A {bias: $V_{C1} = -28$ V; $T_{amb} = 25$ °C; all other terminals at V_{P0} |
| clock input | $-I_{\phi L}$ | - | - | 100 | μ A {bias: $V_\phi = -28$ V; $T_{amb} = 25$ °C; all other terminals at V_{P0} |
| Output resistance | | | | | |
| HIGH | R_{QH} | - | 1.0 | - | k Ω $V_Q = -1$ V |
| LOW | R_{QL} | - | 1.0 | - | k Ω $V_Q = -10$ V |
| Supply currents | $-I_{P1}$ | - | 6.0 | 10.0 | mA f = 1 MHz; $T_{amb} = 25$ °C |
| | $-I_{P2}$ | - | 1.6 | 2.5 | mA f = 1 MHz; $T_{amb} = 25$ °C |
| Output transition times: | | | | | |
| fall time | t_{THL} | - | 150 | - | ns |
| rise time | t_{TLH} | - | 150 | - | ns |
| Delay times: | | | | | |
| fall time | t_{DHL} | - | 150 | 300 | ns |
| rise time | t_{DLH} | - | 150 | 300 | ns |

¹⁾ All typical values are measured at: $V_{P1} = -26$ V; $V_{P2} = -13$ V; $T_{amb} = 25$ °C.

CHARACTERISTICS (continued)

TIMING DIAGRAMS

Note:

The indicated points on the vertical axis are specified in the glossary of terms.

Timing diagram notes:

1. Data and control inputs must remain valid for the shaded interval to ensure proper entry.
2. C_1 may be switched in the same manner as all other inputs, providing it completes its switching transition before input G_{41} becomes LOW, for any given clock pulse.

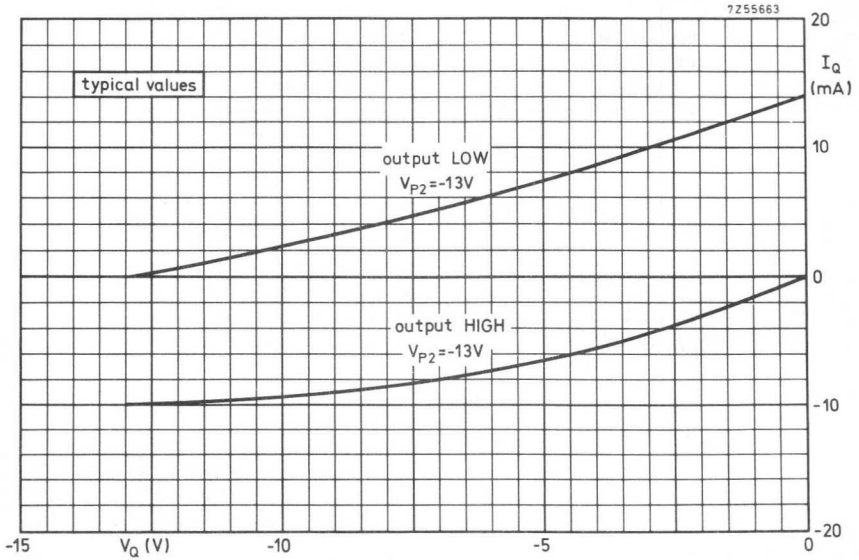
CHARACTERISTICS (continued)

GLOSSARY OF TERMS

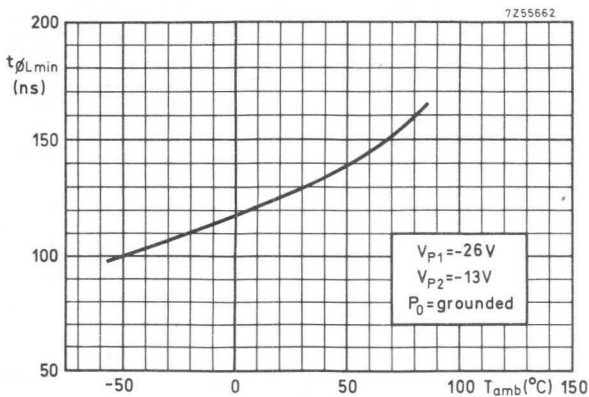
1. Clock pulse width: $t_{\phi L}$
The time for which the clock pulse is LOW; $V_{\phi} \leq -24$ V.
2. Clock pulse rise time: $t_{\phi LH}$
The time between the -24 V and -2 V voltage points as the clock pulse goes from LOW to HIGH.
3. Clock pulse fall time: $t_{\phi HL}$
The time between the -2 V and -24 V voltage points as the clock pulse goes from HIGH to LOW.
4. Output rise transition time: t_{TLH}
The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
5. Output fall transition time: t_{THL}
The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
6. Fall delay time: t_{DHL}
The delay between the time the positive going edge of the clock pulse arrives at -2 V and the output -6 V voltage point as the output goes from HIGH to LOW.
7. Rise delay time: t_{DLH}
The delay between the time the positive going edge of the clock pulse arrives at -2 V and the output -6 V voltage point as the output goes from LOW to HIGH.

OUTPUT BUFFER DESCRIPTION

The FDJ106 utilizes push-pull output buffers which exhibit the V_Q versus I_Q output curves, for both HIGH and LOW output, shown below.

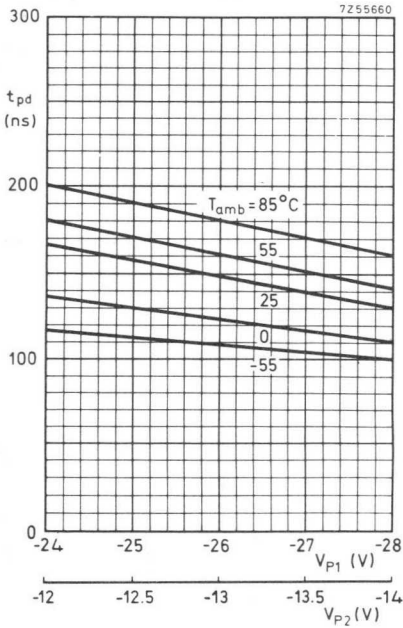
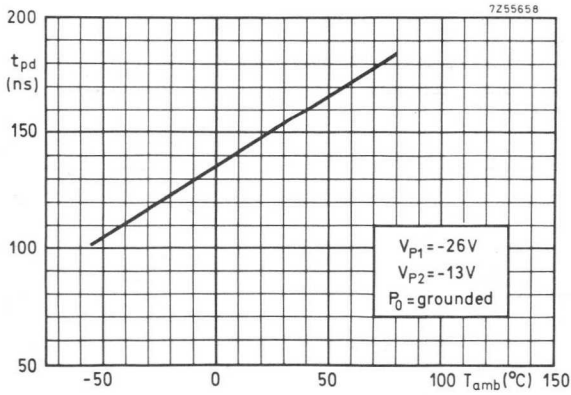


TYPICAL PERFORMANCE

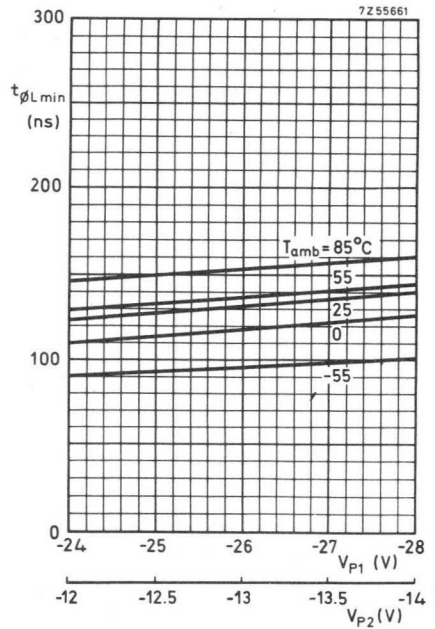


TYPICAL PERFORMANCE (continued)

Test conditions: $P_0 =$ grounded; standard load: 50 pF in parallel with 1 M Ω to P_0 .



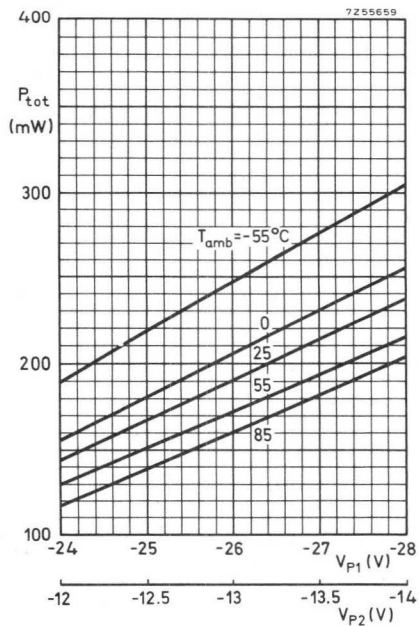
Propagation delay as a function of the supply voltages V_{P1} and V_{P2}



Minimum clock pulse width as a function of the supply voltages V_{P1} and V_{P2}

TYPICAL PERFORMANCE (continued)

Test conditions: $P_0 =$ grounded; standard load: 50 pF in parallel with 1 M Ω to P_0 .



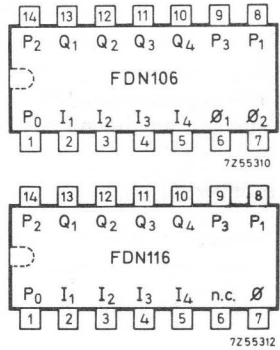
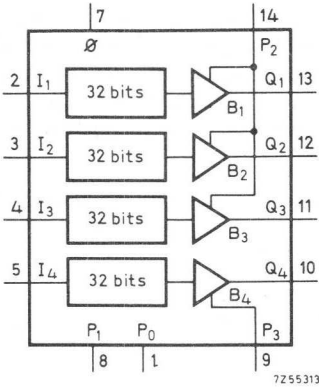
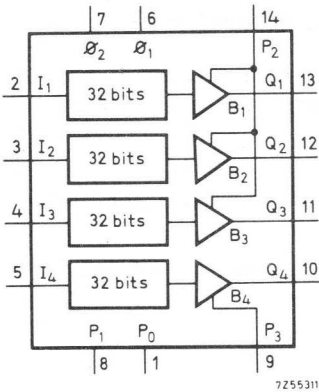
Power dissipation as a function of the supply voltages V_{P1} and V_{P2}

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

QUADRUPLE 32-BIT DYNAMIC SHIFT REGISTERS

FDN106

FDN116



P₀ and metal package bottom are connected.

QUICK REFERENCE DATA

| | | |
|--------------------------------------------|---------------------------------|---------------|
| Supply voltage | V _{P1} | -24 to -28 V |
| D. C. noise margin | M _L ; M _H | > 1 V |
| Clock rate: FDN106 | f _φ | 0.01 to 3 MHz |
| FDN116 | f _φ | 0.01 to 1 MHz |
| Power consumption per bit at 1 MHz: FDN106 | P _{av} | typ. 0.6 mW |
| FDN116 | P _{av} | typ. 1.0 mW |
| Power dissipation | P _{tot} | max. 300 mW |
| Operating ambient temperature | T _{amb} | -55 to +85 °C |

PACKAGE OUTLINE: 14 lead metal-ceramic dual in-line (See General Section)

GENERAL DESCRIPTION

The FDN106 and FDN116 packages comprise 4 separate 32-bit shift registers that can be used independently or can be externally connected to make registers up to 128-bits long. Clock and power lines are common to all four registers. The output buffers are bi-directional, low impedance NRZ ¹⁾, that by suitable biasing will directly drive MOS, DTL or TTL loads or, because **they have** separate supply voltages (V_{P2} ; V_{P3}), a combination of MOS and bipolar. V_{P2} and V_{P3} are output buffer voltages **only**, and the output LOW signal is independent of the width and amplitude of the clock pulse.

The FDN106 uses a two-phase external clock, has low power dissipation and will operate at high speed.

The FDN116 uses a single phase external clock, and is for applications not calling for the low power economy and high speed of the FDN106.

With the FDN106; FDN116; the FDN126; FDN136 (variable length 1 to 64-bit dynamic shift registers) and the FDN146; FDN156 (256-bit dynamic shift registers) shift registers of **any length** can be built from off-the shelf parts.

→ **RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|-------------------------------------------------------------------------------------------------|--------------------|-------------|----------------------|
| Voltages on all data inputs, clock inputs, outputs and supply terminals with reference to P_0 | | +0.5 to -30 | V |
| Power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$ | P_{tot} | max. | 800 mW |
| Junction temperature | T_j | max. | 150 $^\circ\text{C}$ |
| Storage temperature | T_{stg} | -65 to +150 | $^\circ\text{C}$ |
| Total current through terminals P_2 and P_3 | $-I_{P2}, -I_{P3}$ | max. | 40 mA |
| Output current (per output) | $\pm I_Q$ | max. | 20 mA |

→ **THERMAL RESISTANCE**

| | | | |
|--------------------------|---------------|---|------------------------|
| From junction to ambient | $R_{th\ j-a}$ | = | 156 $^\circ\text{C/W}$ |
|--------------------------|---------------|---|------------------------|

¹⁾ Non return to zero.

CHARACTERISTICS at $T_{amb} = -55$ to $+85$ °C

| | Symbol | Type number | min. | typ. | max. | Conditions and references |
|---------------------------|--------------------|--------------|--------|------|--------------|-----------------------------------------|
| Clock rate | f_{ϕ} | FDN106 | 0.01 | - | 3 MHz | |
| | f_{ϕ} | FDN116 | 0.01 | - | 1 MHz | |
| Clock pulse width | $t_{\phi 1L}$ | FDN106 | 0.125 | - | 25 μ s | } see timing diagram for parameter def. |
| | $t_{\phi 2L}$ | FDN106 | 0.125 | - | 25 μ s | |
| | $t_{\phi L}$ | FDN116 | 0.50 | - | 50 μ s | |
| Clock pulse fall time | $t_{\phi HL}$ | | - | - | 0.10 μ s | see note 1, 2 |
| Clock pulse rise time | $t_{\phi LH}$ | | - | - | 0.10 μ s | see note 2 |
| Clock delay time | $t_{\phi 1\phi 2}$ | FDN106 | 0 | - | 25 μ s | |
| Clock delay time | $t_{\phi 2\phi 1}$ | FDN106 | 0 | - | 25 μ s | |
| Clock pulse space | $t_{\phi H}$ | FDN116 | 0.50 | - | 50 μ s | |
| Clock pulse voltage level | HIGH | | -2 | 0 | +0.3 V | |
| | LOW | $V_{\phi H}$ | | | | |
| | | $V_{\phi L}$ | FDN106 | -28 | -26 | -24 V |
| | $V_{\phi L}$ | FDN116 | -28 | -12 | -9 V | |
| Data input logic levels | HIGH | | -1.5 | 0 | +0.3 V | |
| | LOW | | -28 | -12 | -9 V | |
| Data lead time | $t_{\ell I}$ | FDN106 | 10 | - | - ns | |
| | $t_{\ell I}$ | FDN116 | 20 | - | - ns | |
| Data hold time | t_{hI} | FDN116 | 75 | - | - ns | |

Note 1

The fall time specified for the FDN116 is to ensure that output data will meet the input hold time requirements of other shift registers, when more shift registers operate in series from a common clock. If a register does not drive other registers the clock pulse fall time may be longer.

Note 2

For FDN106 above $f_{\phi} = 1.54$ MHz $t_{\phi 1Lmin}$ and $t_{\phi 2Lmin}$ determine the maximum value of $t_{\phi HL}$ and $t_{\phi LH}$.

CHARACTERISTICS

Test conditions: $V_{P1} = -24\text{ V to } -28\text{ V}$; $V_{P2} = -12\text{ V to } -14\text{ V}$; $T_{amb} = -55\text{ to } +85\text{ }^\circ\text{C}$; $P_0 = \text{grounded}$;
standard load of $20\text{ k}\Omega$ in parallel with 50 pF to P_0

| | Symbol | Type number | min. | typ. | max. | Conditions and references |
|--------------------------------------------|--------------------------|-----------------|--------|------|-------------------|--------------------------------------------------------------------------------------------------------------|
| ELECTRICAL DATA | | | | | | |
| Output levels | | | | | | |
| HIGH | V_{QH} | | -0.5 | - | 0 V | |
| LOW | V_{QL} | | -14 | - | -10 V | |
| Data input capacitance | C_I | | - | 2 | 3.5 pF | bias: $V_I = 0\text{ V}$; $f = 1\text{ MHz}$ |
| Clock input capacitance | $C_{\phi 1}, C_{\phi 2}$ | FDN106 | - | 38 | 50 pF | } bias: $V_{\phi} = 0\text{ V}$; $f = 1\text{ MHz}$ bias: $V_{\phi} = -26\text{ V}$; $f = 1\text{ MHz}$ |
| | C_{ϕ} | FDN116 | - | 6 | 8 pF | |
| | $C_{\phi 1}, C_{\phi 2}$ | FDN106 | - | 28 | 37 pF | |
| Leakage currents: | | | | | | |
| Data input currents | $-I_{IL}$ | | - | - | 1 μA | $V_I = -15\text{ V}$; all other terminals at V_{P0} ; $T_{amb} = 25\text{ }^\circ\text{C}$ |
| Clock input current | $-I_{\phi L}$ | | - | - | 100 μA | $V_{\phi} = -28\text{ V}$; all other terminals at V_{P0} ; $T_{amb} = 25\text{ }^\circ\text{C}$ |
| Output resistance | | | | | | |
| HIGH | R_{QH} | | - | 220 | 500 Ω | $V_{P2} = V_{P3} = -5\text{ V}$ |
| LOW | R_{QL} | | - | 220 | 500 Ω | |
| Drive capability (see note 1) | V_{QL} | | - | -10 | -8 V | $R_L = 4\text{ k}\Omega$ reference to P_0 |
| | V_{QL} | | - | -4.7 | -4.4 V | $V_{P2} = V_{P3} = -5\text{ V}$; $R_L = 4\text{ k}\Omega$ reference to P_0 |
| Power supply current drain (see note 2) | $-I_{P2}, -I_{P3}$ | | - | 3.0 | 3.5 mA | $V_{P2} = V_{P3} = -13\text{ V}$; $f_{\phi} = 1\text{ MHz}$; $T_{amb} = 25\text{ }^\circ\text{C}$ |
| | $-I_{P1}$ | FDN106 | - | 2.0 | 4.0 mA | $V_{P1} = -26\text{ V}$; $f_{\phi} = 1\text{ MHz}$; $T_{amb} = 25\text{ }^\circ\text{C}$ |
| | $-I_{P1}$ | FDN116 | - | 5.0 | 7.0 mA | |
| Output transition times: | | | | | | |
| fall time | t_{THL} | | - | 100 | - ns | |
| rise time | t_{TLH} | | - | 100 | - ns | |
| Delay times: | fall time | t_{DHL} | FDN106 | - | 70 | - ns |
| | | t_{DHL} | FDN116 | - | 300 | - ns |
| | rise time | t_{DLH} | FDN106 | - | 70 | - ns |
| | | t_{DLH} | FDN116 | - | 300 | - ns |
| | | $t_{\gamma LH}$ | | - | - | - ns |
| D. C. noise margin | M_L, M_H | | 1 | - | - V | |

CHARACTERISTICS (continued)Note 1 (see page 4)

The maximum capacitive load that can be driven depends only on the speed desired and the power dissipation allowable. See the output buffer description on page 8 for further information on output drive capability.

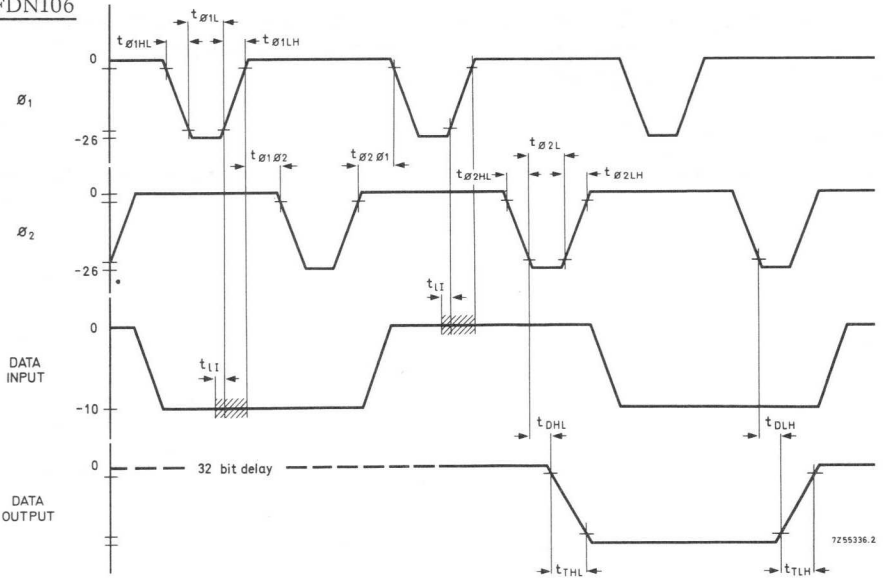
Note 2 (see page 4)

The output buffer power supply currents (I_{P2} , I_{P3}) are almost entirely dependent on the external load.

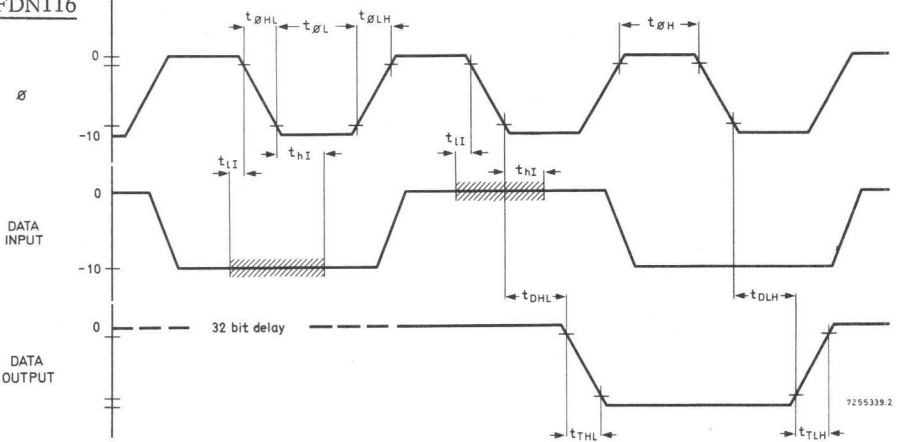


CHARACTERISTICS (continued)
TIMING DIAGRAMS

FDN106



FDN116



Notes

1. The indicated points on the vertical axes are specified in the glossary of terms.
2. Input data must remain valid during the shaded interval to ensure proper entry into the register.

CHARACTERISTICS (continued)GLOSSARY OF TERMS

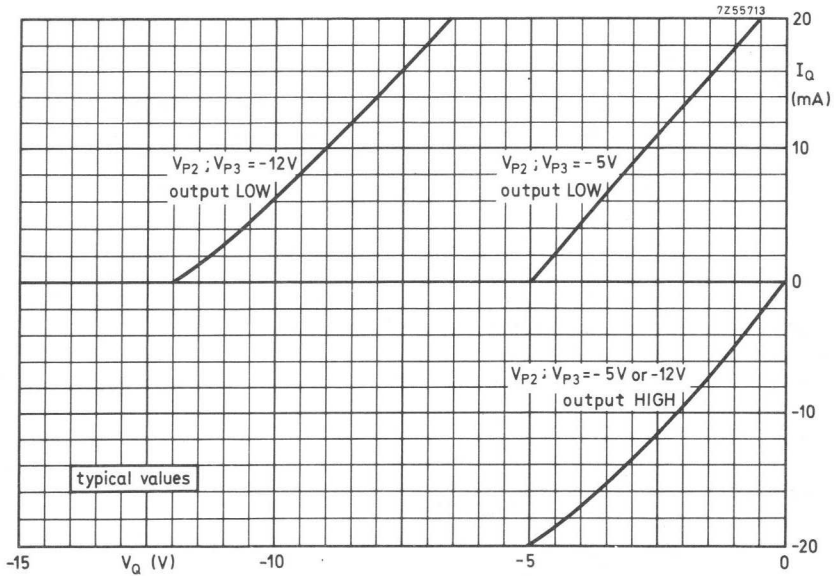
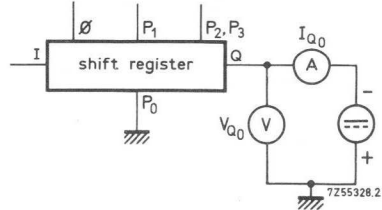
1. Clock pulse width: $t_{\phi L}$
The time for which the clock pulse is LOW: FDN106; $V_{\phi L} \leq -24 \text{ V}$
FDN116; $V_{\phi L} \leq -9 \text{ V}$
2. Clock pulse fall time: $t_{\phi HL}$
The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock delay time: $t_{\phi 1 \phi 2}$, $t_{\phi 2 \phi 1}$ (FDN106)
The least allowable time between the end of the ϕ_1 (or ϕ_2) clock pulse and the start of the ϕ_2 (or ϕ_1) clock pulse, defined at -2 V .
5. Clock pulse space: $t_{\phi H}$ (FDN116)
The minimum time between the end of a clock pulse (ϕ) and the start of the next, defined at -2 V .
6. Data lead time: $t_{\phi I}$
FDN106: The time before the 90% point on the clock pulse ϕ_1 for which the voltage at the data input must be at its specified logic level in order to ensure that the data will be entered in the register.
FDN116: The time before the 10% point on the clock pulse for which the voltage at the data input must be at its specified logic level in order to ensure that the data will be entered in the register.
7. Data hold time: t_{hI} (FDN116)
The time after the clock pulse ϕ reaches LOW for which the input data must remain stable to guarantee that it will be entered into the register.
8. Output fall transition time: t_{THL}
The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
9. Output rise transition time: t_{TLH}
The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
10. Fall delay time: t_{DHL}
FDN106: The delay between the clock pulse ϕ_2 reaching LOW and the output beginning to change from HIGH to LOW.
FDN116: The delay between the clock pulse ϕ reaching LOW and the output beginning to change from HIGH to LOW.
11. Rise delay time: t_{DLH}
FDN106: The delay between the clock pulse ϕ_2 reaching LOW and the output beginning to change from LOW to HIGH.
FDN116: The delay between the clock pulse ϕ reaching LOW and the output beginning to change from LOW to HIGH.

OUTPUT BUFFER DESCRIPTION

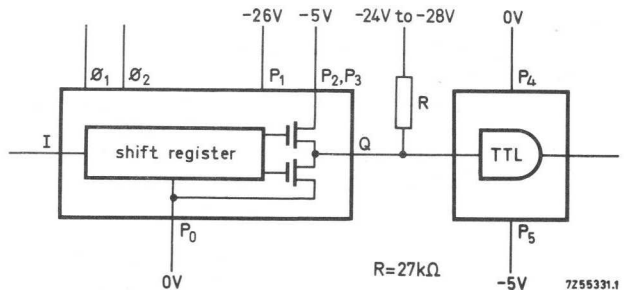
- 1. The curves below are typical output buffer voltage-current characteristics for the FDN106 and FDN116. They show V_Q versus I_Q for the bias V_{P2} and V_{P3} at -5 V and -12 V , for both HIGH and LOW output.

Note: When operating with high output current levels, the maximum power rating must not be exceeded.

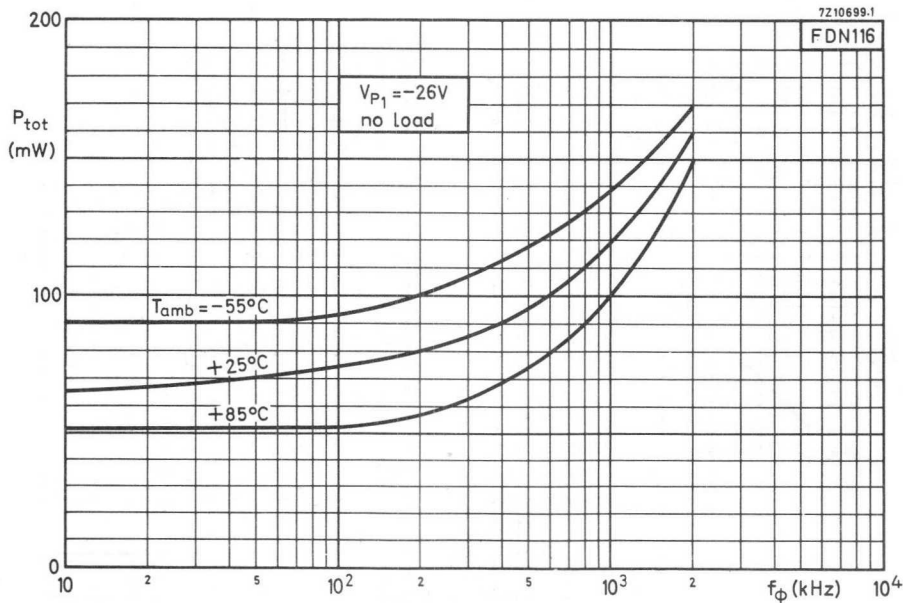
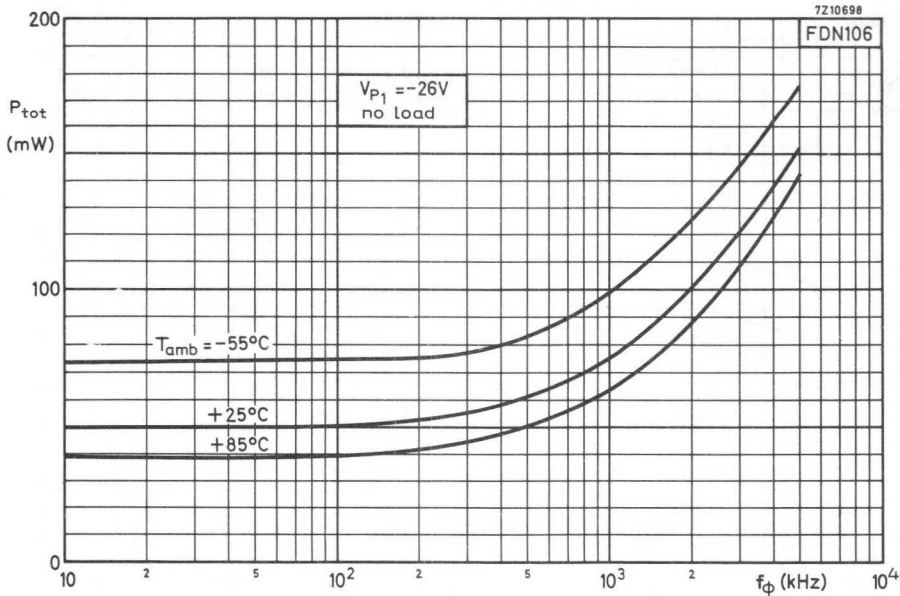
The circuit shown may be used to obtain output curves for other values of V_{P2} and V_{P3} .



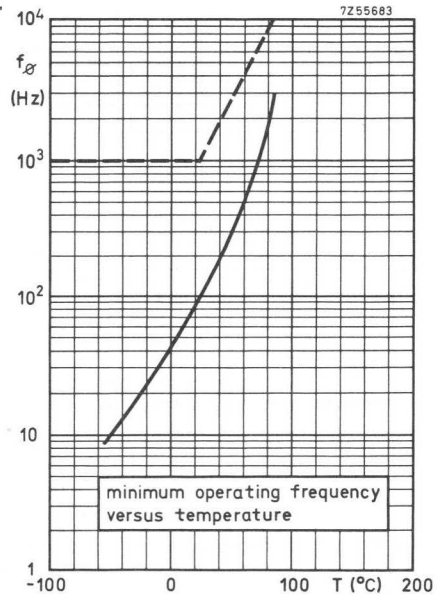
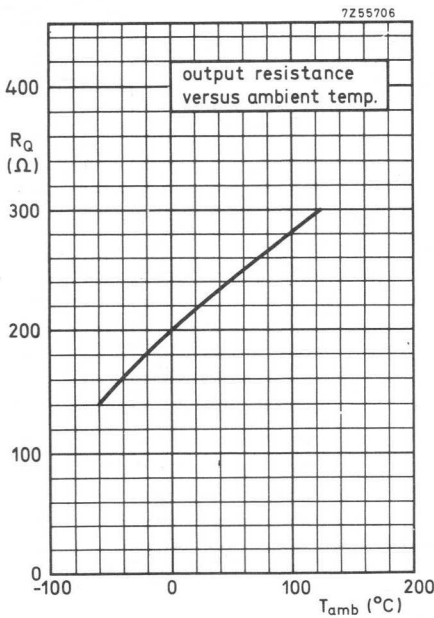
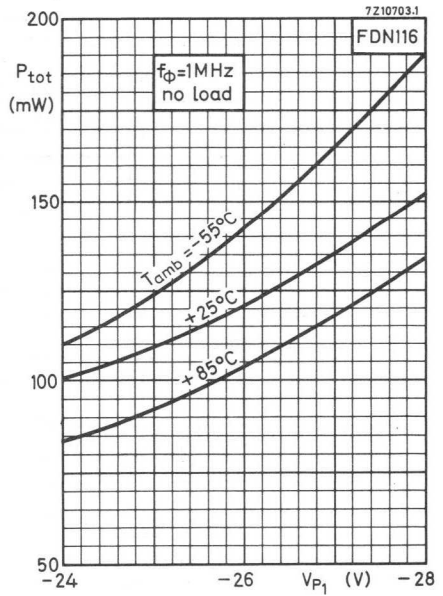
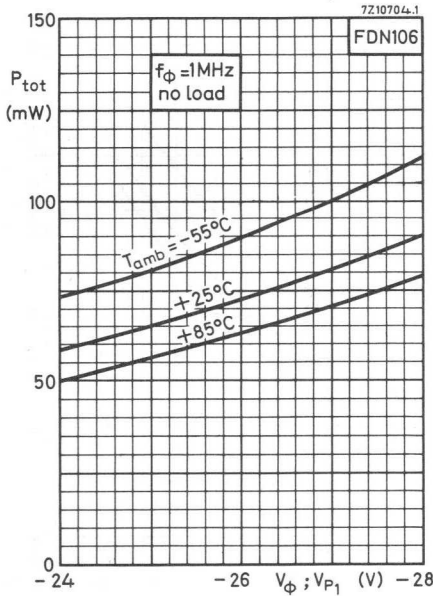
- 2. The bias arrangement shown is suitable for driving TTL or DTL loads direct.



TYPICAL PERFORMANCE

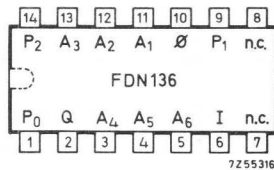
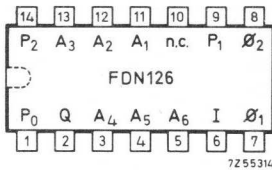
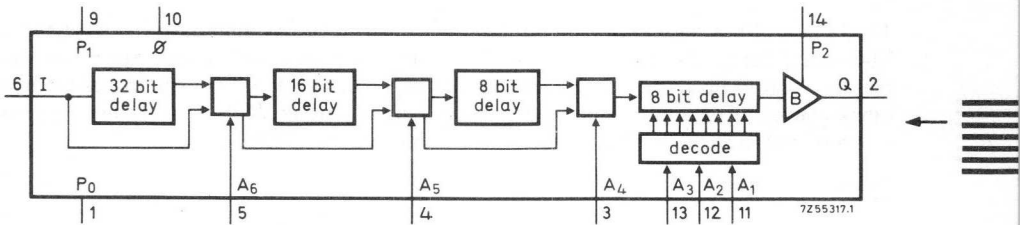
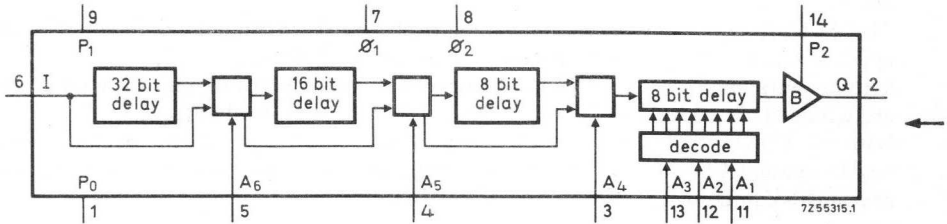


TYPICAL PERFORMANCE (continued)



The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

VARIABLE LENGTH 1 TO 64-BIT DYNAMIC SHIFT REGISTERS



P₀ and metal package bottom are connected.

QUICK REFERENCE DATA

| | | |
|-------------------------------|---------------------------------|---------------|
| Supply voltage | V _{P1} | -24 to -28 V |
| D.C. noise margin | M _L ; M _H | > 1 V |
| Clock rate: FDN126 FDN136 | f _φ | 0.01 to 3 MHz |
| | f _φ | 0.01 to 1 MHz |
| Operating ambient temperature | T _{amb} | -55 to +85 °C |

PACKAGE OUTLINE : 14 lead metal-ceramic dual in-line (See General Section)

GENERAL DESCRIPTION

The FDN126 and FDN136 are unique in that the bit length of both registers can be set from 1 to 64 bits by appropriate choice of the logic state of 6 control inputs. The same input and output leads are used, the control inputs determine the number of register stages connected between them.

The FDN126 is essentially for high speed operation and needs a 2 phase external clock.

The FDN136 needs only a low level single phase external clock; it is suitable for applications that do not demand speeds in excess of 1 MHz.

Both circuits use a bi-directional low impedance output buffer which, when appropriately biased, is capable of driving MOS or DTL and TTL loads direct.

With the FDN126; FDN136, the FDN106; FDN116 (quadruple 32-bit dynamic shift registers) and FDN146; FDN156 (256 bit dynamic shift registers) shift registers of any length can be built from off-the-shelf parts.

REGISTER LENGTH CONTROL

The length of the register is controlled by applying binary signals to lines A1 to A6. The actual length is one more than the binary sum (see table). The length control bits are gated in at ϕ_1 . The length of the register is set up approximately $2 \mu s + 2$ clock cycles after application of the control signals. (one clock cycle is one ϕ_1 pulse + one ϕ_2 pulse for the FDN126 and one ϕ pulse for the FDN136)

Table (examples)

| weight: 32 | 16 | 8 | 4 | 2 | 1 | register length |
|----------------|----------------|----------------|----------------|----------------|----------------|-----------------|
| A ₆ | A ₅ | A ₄ | A ₃ | A ₂ | A ₁ | |
| H | H | H | H | H | H | 1-bit |
| H | H | H | H | H | L | 2-bits |
| H | H | H | L | H | L | 6-bits |
| L | H | H | H | H | H | 33-bits |
| L | L | L | L | L | L | 64-bits |

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages on all data inputs, clock inputs, outputs,

control inputs and supply terminals with reference to P₀ +0.5 to -30 V

Power dissipation up to T_{amb} = 25 °C P_{tot} max. 800 mW

Junction temperature T_j max. 150 °C

Storage temperature T_{stg} -65 to +150 °C

Total current through terminal P₂ -I_{P2} max. 20 mA

Output current (per output) ±I_Q max. 20 mA

THERMAL RESISTANCE

From junction to ambient R_{th j-a} = 156 °C/W

DRIVE REQUIREMENTS

| | Symbol | Type number | min. | typ. | max. | Conditions and references | |
|------------------------------------|--------------------|-----------------|--------|------|--------------|-----------------------------------------|--|
| Clock rate | f_{ϕ} | FDN126 | 0.01 | - | 3 MHz | | |
| | f_{ϕ} | FDN136 | 0.01 | - | 1 MHz | | |
| Clock pulse width | $t_{\phi 1L}$ | FDN126 | 0.1 | - | 1.0 μ s | } see timing diagram for parameter def. | |
| | $t_{\phi 2L}$ | FDN126 | 0.125 | - | 1.0 μ s | | |
| | $t_{\phi L}$ | FDN136 | 0.50 | - | 50 μ s | | |
| Clock pulse fall time | $t_{\phi HL}$ | | - | - | 0.10 μ s | see note 1, 2 | |
| Clock pulse rise time | $t_{\phi LH}$ | | - | - | 0.10 μ s | see note 2 | |
| Clock delay time | $t_{\phi 1\phi 2}$ | FDN126 | 0 | - | 49 μ s | | |
| Clock delay time | $t_{\phi 2\phi 1}$ | FDN126 | 0 | - | 49 μ s | | |
| Clock pulse space | $t_{\phi H}$ | FDN136 | 0.50 | - | 50 μ s | | |
| Clock pulse voltage level | HIGH | | -2 | 0 | +0.3 V | | |
| | LOW | $V_{\phi L}$ | FDN126 | -28 | -26 | -24 V | |
| | | $V_{\phi L}$ | FDN136 | -28 | -12 | -9 V | |
| Data and control input logic level | HIGH | $V_{IH}:V_{AH}$ | -1.5 | 0 | +0.3 V | | |
| | LOW | $V_{IL}:V_{AL}$ | -28 | -12 | -9 V | | |
| Data lead time | $t_{\ell I}$ | FDN126 | 20 | - | - ns | | |
| | $t_{\ell I}$ | FDN136 | 75 | - | - ns | | |
| Data hold time | t_{hI} | FDN136 | 75 | - | - ns | | |

Note

The clock pulse fall time specified for the FDN136 is to ensure that output data will meet the input hold time requirements of other shift registers, when more shift registers operate in series from a common clock. If a register does not drive other registers, the clock pulse rise and fall times may be longer.

Note 2

For FDN126 above $f_{\phi} = 1.6$ MHz $t_{\phi 1Lmin}$ and $t_{\phi 2Lmin}$ determine the maximum value of $t_{\phi HL}$ and $t_{\phi LH}$.

CHARACTERISTICS

Test conditions: $V_{P1} = -24\text{ V}$ to -28 V ; $V_{P2} = -12$ to -14 V ; $T_{amb} = -55$ to $+85\text{ }^\circ\text{C}$; $P_0 = \text{grounded}$;
standard load of $20\text{ k}\Omega$ in parallel with 50 pF to P_0

| | Symbol | Type number | min. | typ. | max. | Conditions and references |
|--------------------------------------------|--------------------------|-------------|--------|------|-------------------|----------------------------------------------------------------------------------------------------------------------|
| ELECTRICAL DATA | | | | | | |
| Output levels | | | | | | |
| HIGH | V_{QH} | | -0.5 | - | 0 V | |
| LOW | V_{QL} | | -14 | - | -10 V | |
| Data input capacitance | C_I | | - | 2 | 3.5 pF | bias: $V_I = 0\text{ V}$; $f_\phi = 1\text{ MHz}$ |
| Clock input capacitance | $C_{\phi 1}, C_{\phi 2}$ | FDN126 | - | 22 | 30 pF | } bias: $V_\phi = 0\text{ V}$; $f_\phi = 1\text{ MHz}$ } bias: $V_\phi = -26\text{ V}$; $f_\phi = 1\text{ MHz}$ |
| | C_ϕ | FDN136 | - | 6 | 8 pF | |
| | $C_{\phi 1}, C_{\phi 2}$ | FDN126 | - | 14 | 20 pF | |
| <u>Leakage currents:</u> | | | | | | |
| Data input current | $-I_{IL}$ | | - | - | 1 μA | $V_I = -15\text{ V}$; all other terminals at V_{P0} ; $T_{amb} = 25\text{ }^\circ\text{C}$ |
| Clock input current | $-I_{\phi L}$ | FDN126 | - | - | 100 μA | $V_\phi = -28\text{ V}$; all other terminals at V_{P0} ; $T_{amb} = 25\text{ }^\circ\text{C}$ |
| | $-I_{\phi L}$ | FDN136 | - | - | 1 μA | $V_\phi = -15\text{ V}$; all other terminals at V_{P0} ; $T_{amb} = 25\text{ }^\circ\text{C}$ |
| <u>Output resistance:</u> | | | | | | |
| HIGH | R_{QH} | | - | 220 | 500 Ω | $V_{P2} = -5\text{ V}$ |
| LOW | R_{QL} | | - | 220 | 500 Ω | |
| Drive capability (see note 1) | V_{QL} | | - | -10 | -8 V | $R_L = 4\text{ k}\Omega$ reference to P_0 |
| | V_{QL} | | - | -4.7 | -4.4 V | $V_{P2} = -5\text{ V}$; $R_L = 4\text{ k}\Omega$ reference to P_0 |
| Power supply current drain (see note 2) | $-IP_2$ | | - | 0.8 | 1.0 mA | $V_{P2} = -13\text{ V}$; $f_\phi = 1\text{ MHz}$ $T_{amb} = 25\text{ }^\circ\text{C}$ |
| | $-IP_1$ | FDN126 | - | 2.5 | 5.0 mA | $V_{P1} = -26\text{ V}$; $f_\phi = 1\text{ MHz}$ $T_{amb} = 25\text{ }^\circ\text{C}$ |
| | $-IP_1$ | FDN136 | - | 3.0 | 6.0 mA | |
| <u>Output transition times:</u> | | | | | | |
| fall time | t_{THL} | | - | 80 | - ns | |
| rise time | t_{TLH} | | - | 80 | - ns | |
| <u>Delay times:</u> | fall time { | t_{DHL} | FDN126 | - | 70 | - ns |
| | | t_{DHL} | FDN136 | - | 300 | - ns |
| | rise time { | t_{DLH} | FDN126 | - | 70 | - ns |
| | | t_{DLH} | FDN136 | - | 300 | - ns |
| D. C. noise margin | $M_{L,MH}$ | | 1 | - | - V | |

CHARACTERISTICS (continued)Note 1 (see page 4)

The maximum capacitive load that can be driven depends only on the speed desired and the power dissipation allowable. See the output buffer description on page 8 for further information on output drive capability.

Note 2 (see page 4)

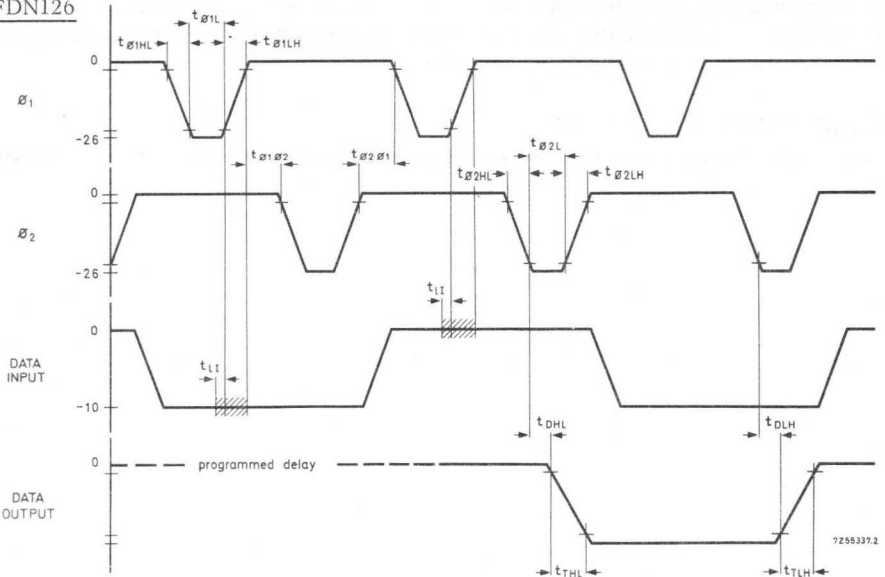
The output buffer power supply current I_{p2} is almost entirely dependent on the external load.



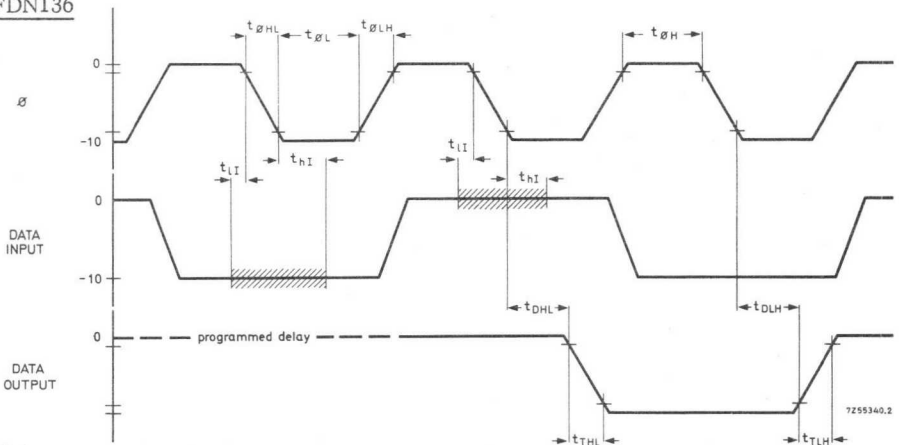
CHARACTERISTICS (continued)

TIMING DIAGRAMS

FDN126



FDN136



Notes

1. The indicated points on the vertical axes are specified in the glossary of terms.
2. During a continuous series of LOW signals the data output may return momentarily to zero once every clock cycle, i. e. when the register output normally changes signal. The data output should be not sampled during this period.
3. Input data must remain valid during the shaded interval to ensure proper entry into the register.

CHARACTERISTICS (continued)

GLOSSARY OF TERMS

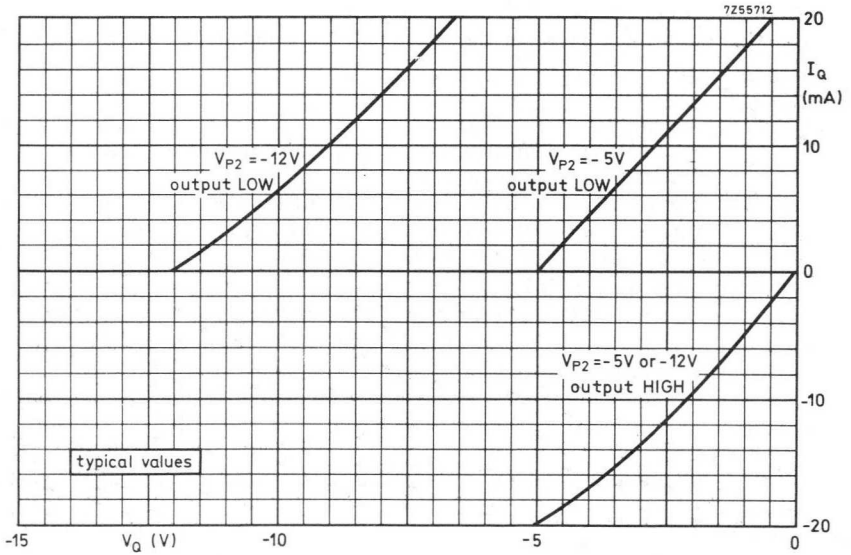
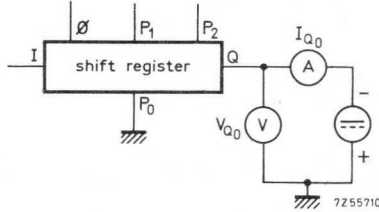
1. Clock pulse width: $t_{\phi L}$
The time for which the clock pulse is LOW: FDN126; $V_{\phi L} \leq -24$ V
FDN136; $V_{\phi L} \leq -9$ V
2. Clock pulse fall time: $t_{\phi HL}$
The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock delay time: $t_{\phi 1 \phi 2}$; $t_{\phi 2 \phi 1}$ (FDN126)
The least allowable time between the end of the ϕ_1 (or ϕ_2) clock pulse and the start of the ϕ_2 (or ϕ_1) clock pulse, defined at -2 V.
5. Clock pulse space: $t_{\phi H}$ (FDN136)
The minimum time between the end of a clock pulse (ϕ) and the start of the next, defined at -2 V.
6. Data lead time: $t_{\ell I}$
FDN126: The time before the 90% point on the clock pulse ϕ_1 for which the voltage at the data input must be at its specified logic level in order to ensure that the data will be entered in the register.
FDN136: The time before the 10% point on the clock pulse for which the voltage at the data input must be at its specified logic level in order to ensure that the data will be entered in the register.
7. Data hold time: t_{hI} (FDN136)
The time after the clock pulse ϕ reaches LOW for which the input data must remain stable to guarantee that it will be entered into the register.
8. Output fall transition time: t_{THL}
The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
9. Output rise transition time: t_{TLH}
The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
10. Fall delay time: t_{DHL}
FDN126: The delay between the clock pulse ϕ_2 reaching LOW and the output beginning to change from HIGH to LOW.
FDN136: The delay between the clock pulse ϕ reaching LOW and the output beginning to change from HIGH to LOW.
11. Rise delay time: t_{DLH}
FDN126: The delay between the clock pulse ϕ_2 reaching LOW and the output beginning to change from LOW to HIGH.
FDN136: The delay between the clock pulse ϕ reaching LOW and the output beginning to change from LOW to HIGH.

OUTPUT BUFFER DESCRIPTION

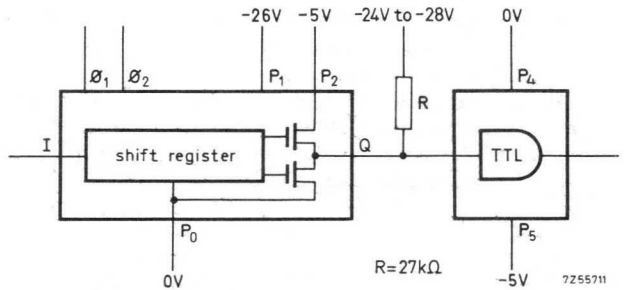
- 1. The curves below are typical output buffer voltage-current characteristics for the FDN126 and FDN136. They show V_Q versus I_Q for the bias V_{P2} at $-5V$ and $-12V$, for both HIGH and LOW output.

Note: When operating with high output current levels, the maximum power rating must not be exceeded.

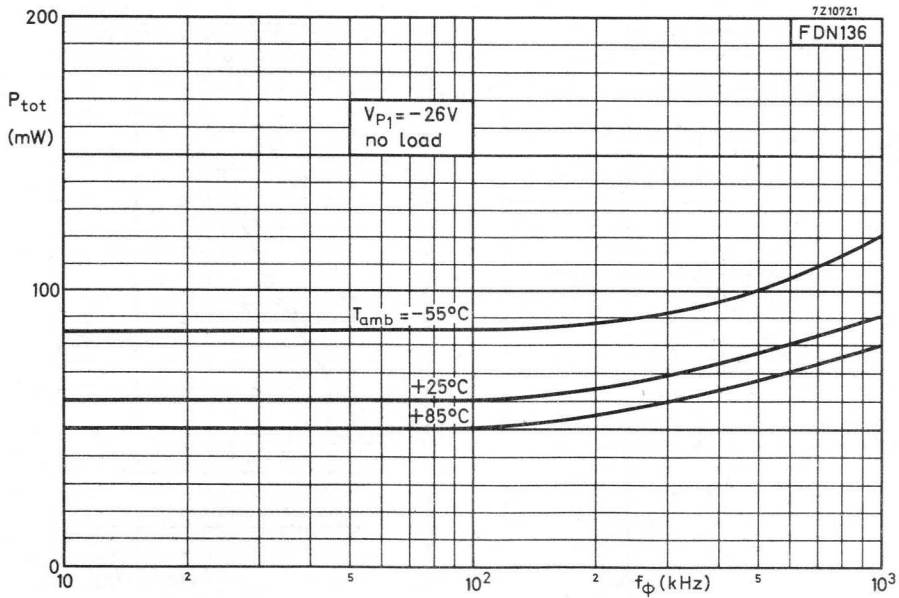
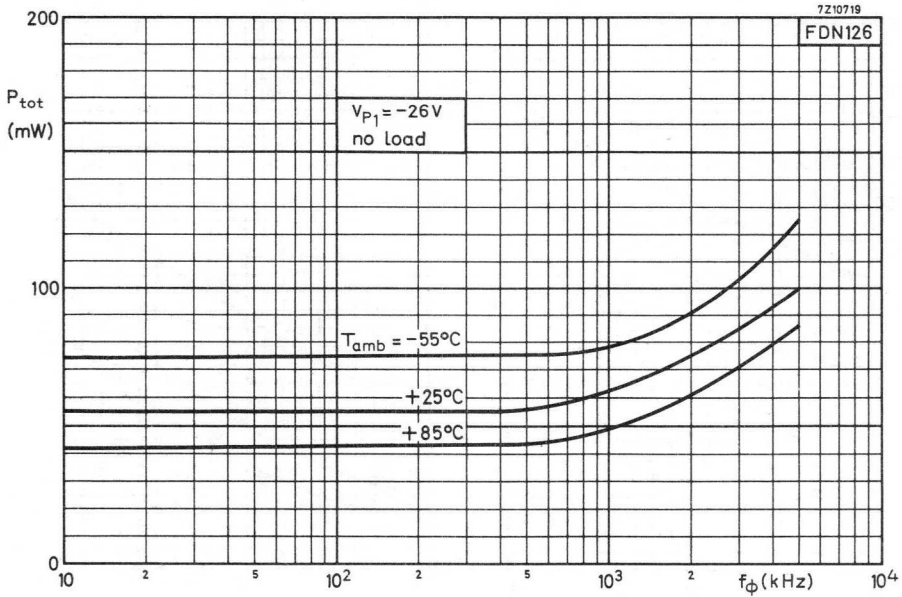
The circuit shown may be used to obtain output curves for other values of V_{P2} .



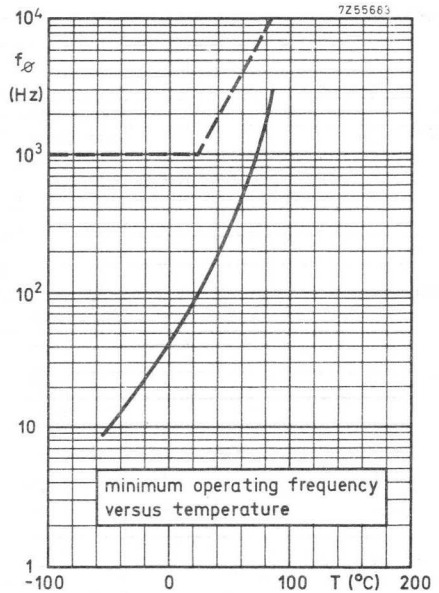
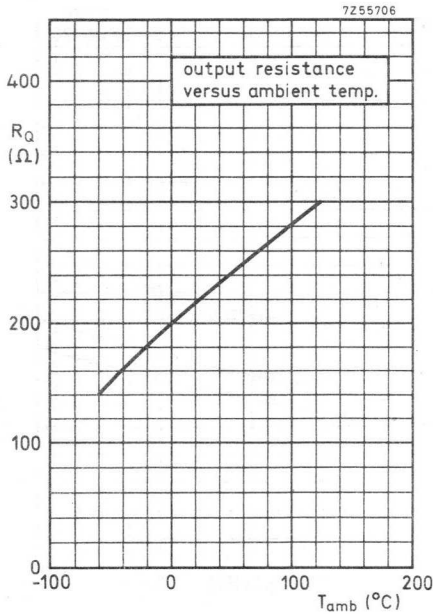
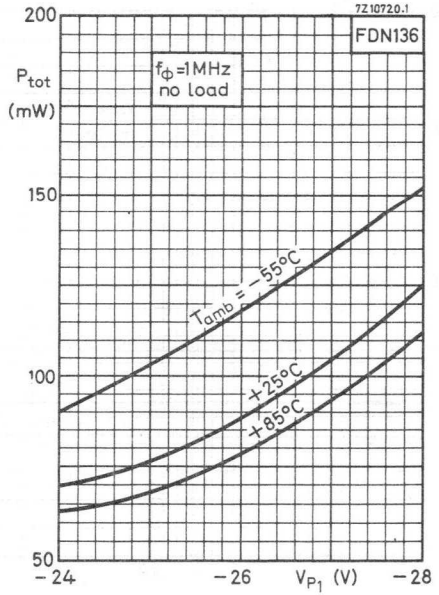
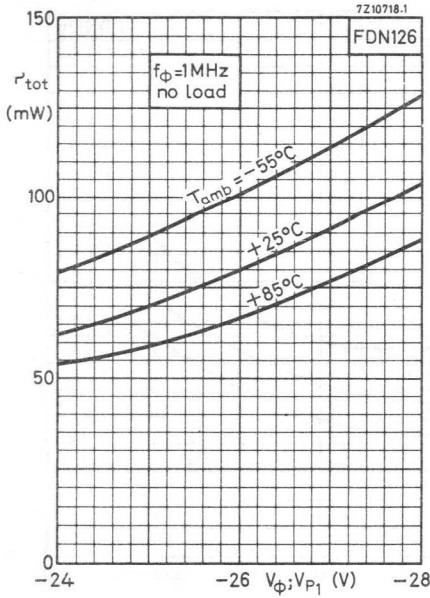
- 2. The bias arrangement shown is suitable for driving TTL or DTL loads direct.



TYPICAL PERFORMANCE

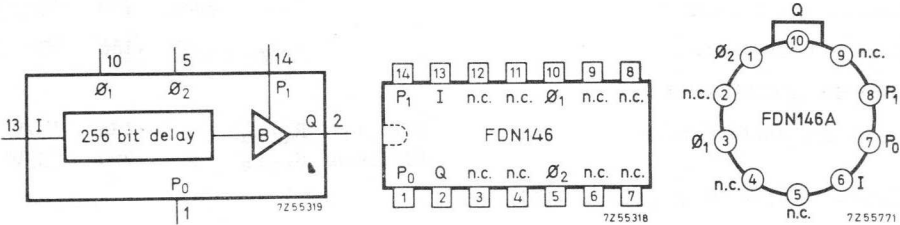


TYPICAL PERFORMANCE (continued)



The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

256-BIT DYNAMIC SHIFT REGISTER



Pin numbers refer to FDN146 only
 FDN146 : P₀ connected to metal bottom
 FDN146A: P₀ connected to metal case

QUICK REFERENCE DATA

| | | | |
|-------------------------------------|------------------|------------|----------|
| D.C. noise margin | M _L | > | 1 V |
| Clock rate | f _Ø | 0.01 to 3 | MHz |
| Power consumption per bit at 10 kHz | P _{av} | < | 0.002 mW |
| 1 MHz | P _{av} | < | 0.2 mW |
| 3 MHz | P _{av} | < | 0.6 mW |
| Power dissipation | P _{tot} | max. | 300 mW |
| Operating ambient temperature | T _{amb} | -55 to +85 | °C |

GENERAL DESCRIPTION

The FDN146(A) contains one continuous 256-bit shift register with one serial input and one serial output. It dissipates very little power and uses a two-phase external clock. The device has a low impedance push-pull output buffer which, when appropriately biased is capable of interfacing direct with MOS, DTL, TTL and other loads. The buffer supply terminal P₁ is a separate supply which determines the output LOW signal only. This provides an output level that is independent of both the amplitude and width of the clock pulse. With the FDN146(A), the FDN106 (a quadruple 32-bit shift register) and FDN126 (a variable length 1 to 64 bit shift register) shift registers of any length can be built from off-the-shelf parts.

PACKAGE OUTLINE: FDN146: 14 lead metal-ceramic dual in-line (See General Section)
 FDN146A: TO-100 (See General Section)

→ **RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages on all data inputs, clock inputs, outputs and supply terminals with reference to P₀ +0.5 to -30 V

Power dissipation up to T_{amb} = 25 °C

FDN146 : P_{tot} max. 800 mW
FDN146A: P_{tot} max. 625 mW

Junction temperature T_j max. 150 °C

Storage temperature T_{stg} -65 +156 °C

→ **THERMAL RESISTANCE**

From junction to ambient
FDN146 : R_{th j-a} = 156 °C/W
FDN146A: R_{th j-a} = 200 °C/W

CHARACTERISTICS at T_{amb} = -55 to +85 °C

| | Symbol | min. | typ. | max. | Conditions and references |
|---------------------------|--------------------------------------|----------------|------|------------------|------------------------------------------------|
| Clock rate | f _φ | 0.01 | - | 3 MHz | } see timing diagram for parameter definitions |
| Clock pulse width | t _{φ1L} t _{φ2L} | 0.125 0.125 | - | 1.0 μs 1.0 μs | |
| Clock pulse fall time | t _{φHL} | - | - | 0.10 μs | } see note 2 |
| Clock pulse rise time | t _{φLH} | - | - | 0.10 μs | |
| Clock delay time | t _{φ1φ2} | 0 | - | 49 μs | } see note 1 |
| Clock delay time | t _{φ2φ1} | 0 | - | 49 μs | |
| Clock pulse voltage level | | | | | } see note 1 |
| HIGH | V _{φH} | -2 | 0 | +0.3 V | |
| LOW | V _{φL} | -28 | -27 | -26 V | |
| Data input logic levels | | | | | } see note 1 |
| HIGH | V _{IH} | -1.5 | 0 | +0.3 V | |
| LOW | V _{IL} | -28 | -12 | -9 V | |
| Data lead time | t _{φI} | 10 | - | - ns | |

Note 1

The FDN146(A) can be supplied in versions that will operate with -24 V to -28 V clock pulse LOW signal range.

→ Note 2

Above f_φ = 1.54 MHz t_{φ1Lmin} and t_{φ2Lmin} determine the maximum value of t_{φHL} and t_{φLH}.

CHARACTERISTICS (continued)

Test conditions: $V_{P1} = -12\text{ V to } -14\text{ V}$; $T_{\text{amb}} = -55\text{ to } +85\text{ }^\circ\text{C}$; $P_0 = \text{grounded}$;
standard load: 50 pF in parallel with 20 k Ω to P_0

| | Symbol | min. | typ. | max. | Conditions and references |
|--------------------------------------------|--------------------------|-----------|------|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <u>ELECTRICAL DATA</u> | | | | | |
| <u>Output levels</u> | | | | | |
| HIGH | V_{QH} | -0.5 | - | 0 V | |
| LOW | V_{QL} | -14 | - | -10 V | |
| Data input capacitance | C_I | - | 2 | 3.5 pF | bias: $V_I = 0\text{ V}$; $f_\phi = 1\text{ MHz}$ |
| Clock input capacitance | $C_{\phi 1}, C_{\phi 2}$ | - | 70 | 80 pF | bias: $V_\phi = 0\text{ V}$; $f_\phi = 1\text{ MHz}$ |
| | $C_{\phi 1}, C_{\phi 2}$ | - | 45 | 55 pF | bias: $V_\phi = -26\text{ V}$; $f_\phi = 1\text{ MHz}$ |
| <u>Leakage currents:</u> | | | | | |
| Data input current | $-I_{IL}$ | - | - | 1 μA | $\left\{ \begin{array}{l} V_I = -15\text{ V}; \text{ all other} \\ \text{terminals at } V_{P0}; \\ T_{\text{amb}} = 25\text{ }^\circ\text{C} \end{array} \right.$ |
| Clock input current | $-I_{\phi L}$ | - | - | 100 μA | $\left\{ \begin{array}{l} V_\phi = -28\text{ V}; \text{ all other} \\ \text{terminals at } V_{P0}; \\ T_{\text{amb}} = 25\text{ }^\circ\text{C} \end{array} \right.$ |
| <u>Output resistance</u> | | | | | |
| HIGH | R_{QH} | - | 250 | 500 Ω | $V_{P1} = -5\text{ V}$ |
| LOW | R_{QL} | - | 120 | 300 Ω | |
| Drive capability see note 1 | V_{QL} | - | -4.8 | -4.6 V | $\left\{ \begin{array}{l} V_{P1} = -5\text{ V}; R_L = 4\text{ k}\Omega \\ \text{reference to } P_0 \end{array} \right.$ |
| Power supply current drain (see note 2) | $-I_{P1}$ | - | 1.0 | 1.5 mA | $\left\{ \begin{array}{l} V_{P1} = -13\text{ V}; f_\phi = 1\text{ MHz} \\ T_{\text{amb}} = 25\text{ }^\circ\text{C} \end{array} \right.$ |
| <u>Output transition times:</u> | | | | | |
| fall time | t_{THL} | - | 70 | - ns | |
| rise time | t_{TLH} | - | 70 | - ns | |
| <u>Delay times:</u> | fall time | t_{DHL} | - | 70 | - ns |
| | rise time | t_{DLH} | - | 70 | - ns |
| D.C. noise margin | $M_L; M_H$ | 1 | - | - V | |

Note 1

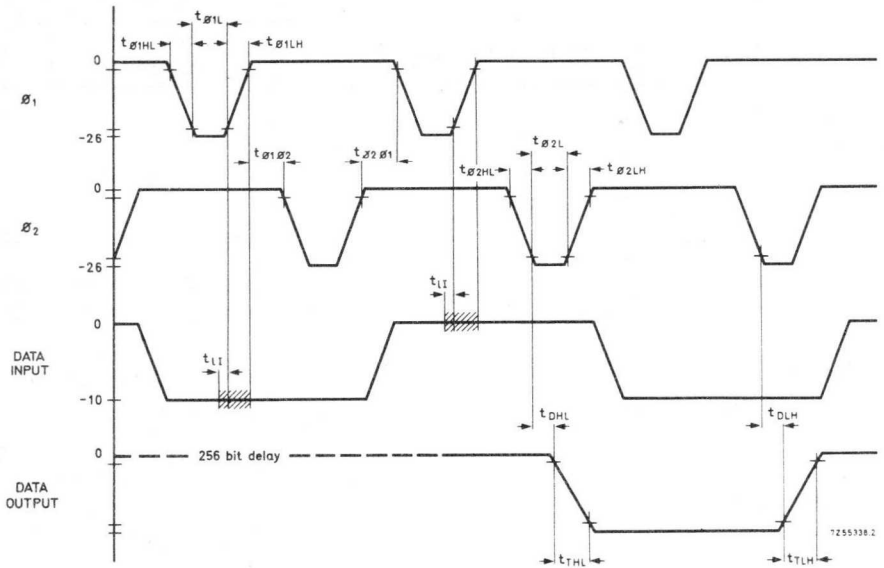
The maximum capacitive load that can be driven depends only on the speed desired and the power dissipation allowable. See the output buffer description on pages 6 and 7 for further information on output drive capability.

Note 2

The output buffer power supply current I_{P1} is almost entirely dependent on the external load. The value shown is for a standard load of 1 M Ω , 50 pF load.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Notes

1. The indicated points on the vertical axis are specified in the glossary of terms.
2. Input data must remain valid during the shaded interval to ensure proper entry into the register.

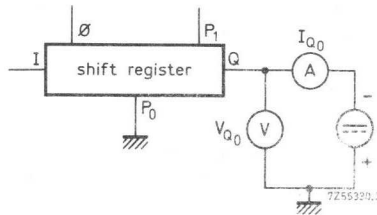
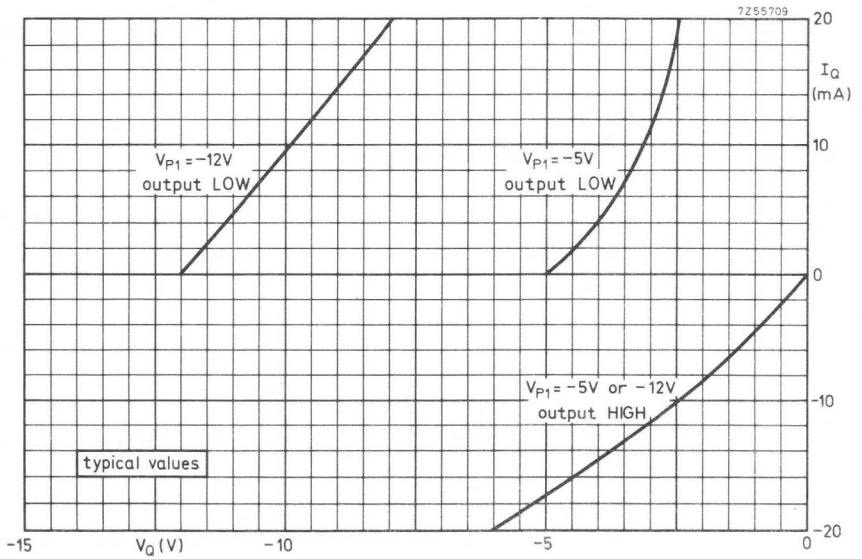
CHARACTERISTICS (continued)GLOSSARY OF TERMS

1. Clock pulse width: $t_{\phi L}$
The time for which the clock pulse is LOW: $V_{\phi L} \leq -26 \text{ V}$
2. Clock pulse fall time: $t_{\phi HL}$
The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock delay time: $t_{\phi 1 \phi 2}$, $t_{\phi 2 \phi 1}$
The least allowable time between the end of the ϕ_1 (or ϕ_2) clock pulse and the start of the ϕ_2 (or ϕ_1) clock pulse, defined at -2 V .
5. Data lead time: $t_{\ell 1}$
The time before the 90% point on the clock pulse ϕ_1 for which the voltage at the data input must be at its specified logic level in order to ensure that the data will be entered in the register.
6. Output fall transition time: t_{THL}
The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
7. Output rise transition time: t_{TLH}
The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
8. Fall delay time: t_{DHL}
The delay between the clock pulse ϕ_2 reaching LOW and the output beginning to change from HIGH to LOW.
9. Rise delay time: t_{DLH}
The delay between the clock pulse ϕ_2 reaching LOW and the output beginning to change from LOW to HIGH.

OUTPUT BUFFER DESCRIPTION

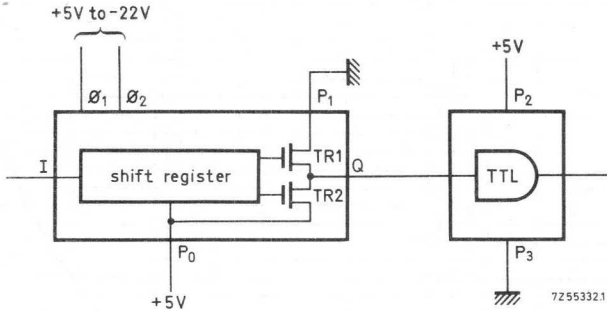
- The curves below are typical output buffer voltage-current characteristics for the FDN146(A). They show V_Q versus I_Q for the bias V_{P1} at -5 V and -12 V , for both HIGH and LOW output. The circuit shown may be used to obtain output curves for other values of V_{P1} .

Note: When operating with high output current levels, the maximum power rating must not be exceeded.



OUTPUT BUFFER DESCRIPTION (continued)

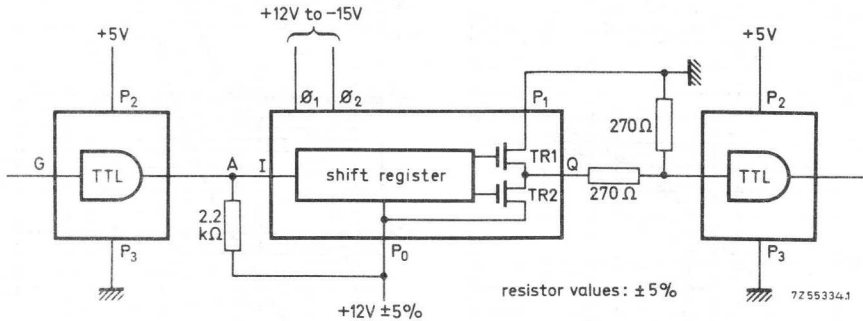
2. Biasing circuit A may be used to drive TTL or DTL loads direct. The MOS input logic levels must be referenced to V_{P0} . TR1 and TR2 are the push-pull output driver transistors of the FDN146.



Biasing circuit A

3. Biasing circuit B allows the MOS device to be interfaced with TTL or DTL at both the input and output using only passive interface components.

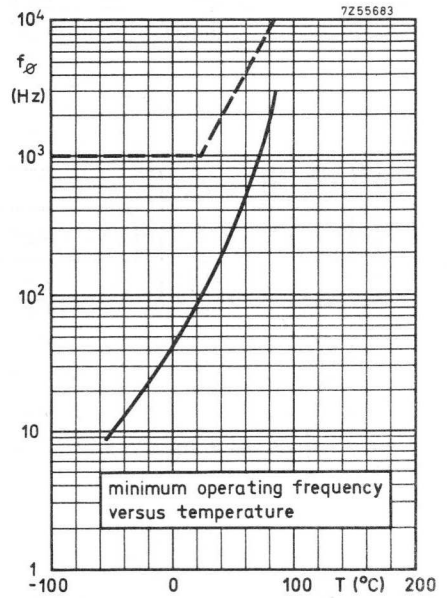
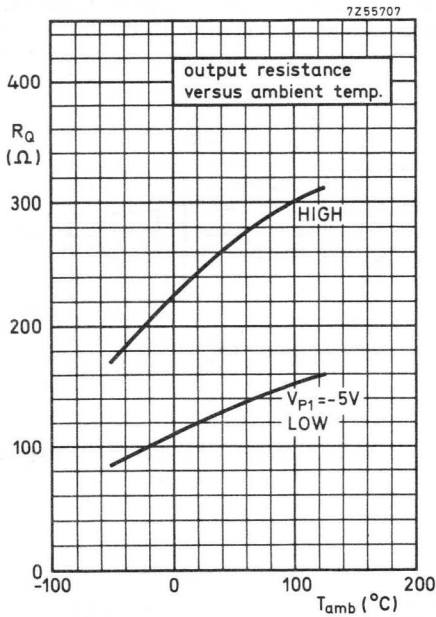
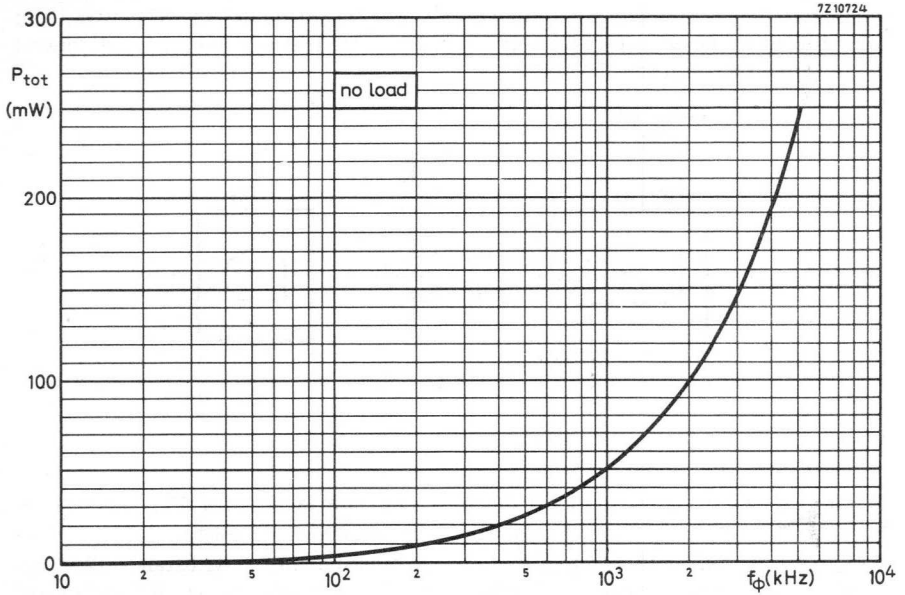
Note that the TTL or DTL integrated circuit must be able to withstand +12 V applied to the output lead (point A), most non- R_C type gates of our FC series and most FJ gates satisfy this requirement. Special open collector FJ gates (FJH301, 311, 321) have a minimum output breakdown voltage guarantee of 15 V.



Biasing circuit B

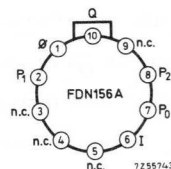
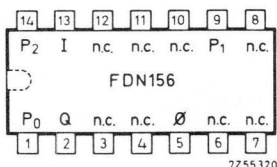
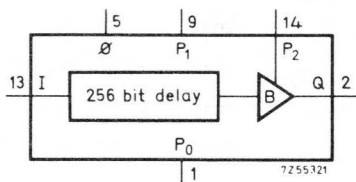
4. To drive MOS loads direct, the bias V_{P1} should be between -12 and -14 V to P_0 .

TYPICAL PERFORMANCE



The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

256-BIT DYNAMIC SHIFT REGISTER



Pin numbers refer to FDN156 only

FDN156 : P₀ connected to the metal bottom
 FDN156A: P₀ connected to the metal case

QUICK REFERENCE DATA

| | | | |
|-------------------------------------------|-----------|------------|--------|
| Supply voltage | V_{P1} | -26 to -28 | V |
| D.C. noise margin | M_L | > | 1 V |
| | M_H | > | 1.5 V |
| Clock rate | f_ϕ | 0.01 to 1 | MHz |
| Power consumption per bit at $f = 10$ kHz | P_{av} | < | 0.2 mW |
| | P_{av} | < | 0.6 mW |
| Operating ambient temperature | T_{amb} | -55 to +85 | °C |

GENERAL DESCRIPTION

The FDN156A contains one 256-bit shift register with one serial input and one serial output. It dissipates very little power and uses a one-phase external clock. The device has a low impedance push-pull output buffer which, when appropriately biased is capable of interfacing direct with MOS, DTL, TTL and other loads.

The buffer supply terminal P₂ is a separate supply which determines the output LOW signal only. This provides an output level that is independent of both the amplitude and width of the clock pulse.

With the FDN156A, the FDN116 (a quadruple 32-bit shift register) and FDN136 (a variable length 1 to 64-bit shift register) shift registers of any length can be built from off-the-shelf parts.

PACKAGE OUTLINE: FDN156: 14 lead metal-ceramic dual in-line (See General Section)
 FDN156A: TO-100 (See General Section)

→ **RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC134)

| | | | |
|----------------------------------------------------------------------------------------------------------|---------------------------|-------------|--------|
| Voltages on all data inputs, clock inputs, outputs and supply terminals with reference to P ₀ | | +0.5 to -30 | V |
| Power dissipation up to T _{amb} = 25 °C | FDN156 : P _{tot} | max. | 800 mW |
| | FDN156A: P _{tot} | max. | 625 mW |
| Junction temperature | T _j | max. | 150 °C |
| Storage temperature | T _{stg} | -65 to +150 | °C |
| Total current through terminal P ₂ | -I _{P2} | max. | 20 mA |
| Output current (per output) | ±I _Q | max. | 20 mA |

→ **THERMAL RESISTANCE**

| | | | |
|--------------------------|------------------------------|---|----------|
| From junction to ambient | FDN156 : R _{th j-a} | = | 156 °C/W |
| | FDN156A: R _{th j-a} | = | 200 °C/W |

CHARACTERISTICS at T_{amb} = -55 to +85 °C

| | Symbol | min. | typ. | max. | Conditions and references |
|---------------------------|------------------|------|------|---------|----------------------------------------------|
| Clock rate | f _φ | 0.01 | - | 1 MHz | See timing diagram for parameter definitions |
| Clock pulse width | t _{φL} | 0.5 | - | 50 μs | |
| Clock pulse fall time | t _{φHL} | - | - | 0.10 μs | |
| Clock pulse rise time | t _{φLH} | - | - | 0.10 μs | |
| Clock pulse space | t _{φH} | 0.5 | - | 50 μs | |
| Clock pulse voltage level | | | | | See note 1 |
| HIGH | V _{φH} | -2 | 0 | +0.3 V | |
| LOW | V _{φL} | -28 | -12 | -9 V | |
| Data input logic levels | | | | | |
| HIGH | V _{IH} | -2 | 0 | +0.3 V | |
| LOW | V _{IL} | -28 | -12 | -9 V | |
| Data lead time | t _{ℓI} | 20 | - | - ns | |
| Data hold time | t _{hI} | 75 | - | - ns | |
| Supply voltages | V _{P1} | -28 | -26 | -24 V | f _φ ≤ 750 kHz |
| | V _{P1} | -28 | -27 | -26 V | f _φ ≤ 750 kHz |
| | V _{P2} | -28 | - | +0.3 V | |

→ **Note 1**

The fall time specified for the FDN156(A) is to ensure that output data will meet the input hold time requirements of other shift registers, when more shift registers operate in series from a common clock. If a register does not drive other registers the clock pulse fall time may be longer.

CHARACTERISTICS (continued)

Test conditions: $V_{P1} = -26$ V to -28 V; $V_{P2} = -12$ V to -14 V; $T_{amb} = -55$ to $+85$ °C;
 $P_0 =$ grounded; standard load: 50 pF in parallel with 20 k Ω to P_0 .

| | Symbol | min. | typ. | max. | Conditions and references |
|--------------------------------------------|---------------|------|------|--------------|--------------------------------------------------------------------------|
| <u>ELECTRICAL DATA</u> | | | | | |
| Output levels | | | | | |
| HIGH | V_{QH} | -0.5 | - | 0 V | |
| LOW | V_{QL} | -14 | - | -10 V | |
| Data input capacitance | C_I | - | 2 | 3.5 pF | bias: $V_I = 0$ V; $f_\phi = 1$ MHz |
| Clock input capacitance | C_ϕ | - | 6 | 10 pF | bias: $V_\phi = 0$ V; $f_\phi = 1$ MHz |
| <u>Leakage currents</u> | | | | | |
| Data input currents | $-I_{IL}$ | - | - | 1 μ A | $V_I = -15$ V; all other terminals at V_{P0} ; $T_{amb} = 25$ °C |
| Clock input current | $-I_{\phi L}$ | - | - | 100 μ A | $V_\phi = -28$ V; all other terminals at V_{P0} ; $T_{amb} = 25$ °C |
| <u>Output resistance</u> | | | | | |
| HIGH | R_{QH} | - | 250 | 500 Ω | |
| LOW | R_{QL} | - | 250 | 500 Ω | $V_{P2} = -5$ V |
| Drive capability (see note 1) | V_{QL} | - | -4.8 | -4.6 V | $V_{P2} = -5$ V; $R_L = 4$ k Ω to reference P_0 |
| Power supply current drain (see note 2) | $-I_{P2}$ | - | 1.0 | 1.5 mA | $V_{P2} = -13$ V; $f_\phi = 1$ MHz; $T_{amb} = 25$ °C |
| | $-I_{P1}$ | - | 5.0 | 8.0 mA | $V_{P1} = -27$ V; $f_\phi = 1$ MHz; $T_{amb} = 25$ °C |
| <u>Output transition times:</u> | | | | | |
| fall time | t_{THL} | - | 100 | - ns | |
| rise time | t_{TLH} | - | 100 | - ns | |
| <u>Delay times:</u> | | | | | |
| fall time | t_{DHL} | - | 300 | - ns | |
| rise time | t_{DLH} | - | 300 | - ns | |
| D. C. noise margin | M_L | 1 | - | - V | |
| | M_H | 1.5 | - | - V | |

Note 1

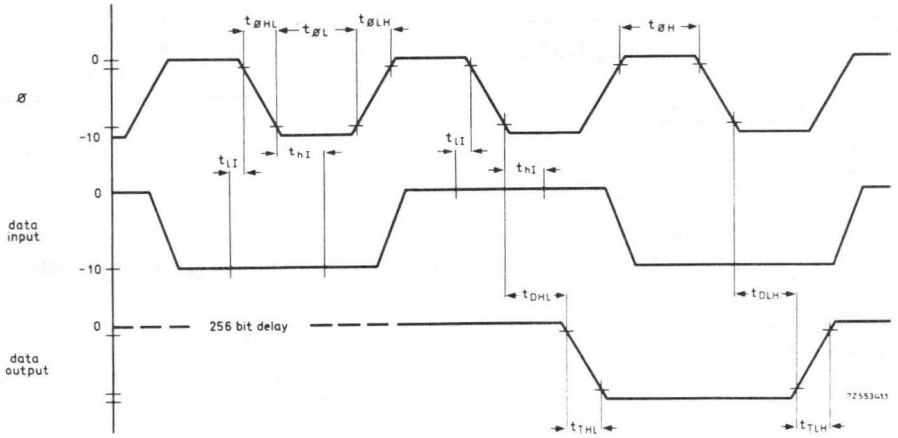
The maximum capacitive load that can be driven depends only on the speed desired and the power dissipation allowable. See the output buffer description on pages 5 and 6 for further information on output drive capability.

Note 2

The output buffer power supply current I_{P2} is almost entirely dependent on the external load.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Notes

1. The indicated points on the vertical axis are specified in the glossary of terms.

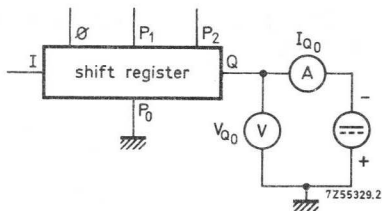
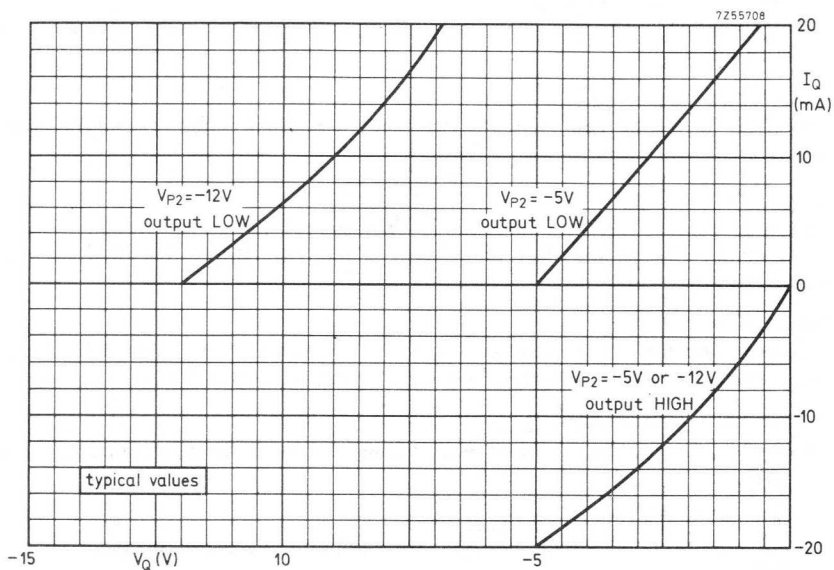
CHARACTERISTICS (continued)GLOSSARY OF TERMS

1. Clock pulse width: $t_{\phi L}$
The time for which the clock pulse is LOW: $V_{\phi L} \leq -9 \text{ V}$.
2. Clock pulse fall time: $t_{\phi HL}$
The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock pulse space: $t_{\phi H}$
The least allowable time between the end of a clock pulse (ϕ) and the start of the next.
5. Data lead time: $t_{\ell I}$
The time before the 10% point on the clock pulse for which the voltage at the data input must be at its specified logic level in order to ensure that the data will be entered in the register.
6. Data hold time: t_{hI}
The time after the clock pulse ϕ reaches LOW for which the input data must remain stable in order to ensure that the data will be entered in the register.
7. Output fall transition time: t_{THL}
The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
8. Output rise transition time: t_{TLH}
The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
9. Fall delay time: t_{DHL}
The delay between the clock pulse ϕ reaching LOW and the output beginning to change from HIGH to LOW.
10. Rise delay time: t_{DLH}
The delay between the clock pulse ϕ reaching LOW and the output beginning to change from LOW to HIGH.

OUTPUT BUFFER DESCRIPTION

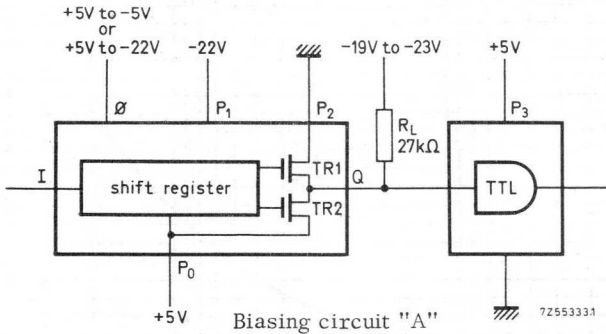
1. The curves below are typical output buffer voltage-current characteristics for the FDN156. They show V_Q versus I_Q for the bias V_{P1} at -5 V and -12 V , for both HIGH and LOW output. The circuit shown may be used to obtain output curves for other values of V_{P2} .

Note: When operating with high output current levels, the maximum power rating must not be exceeded.

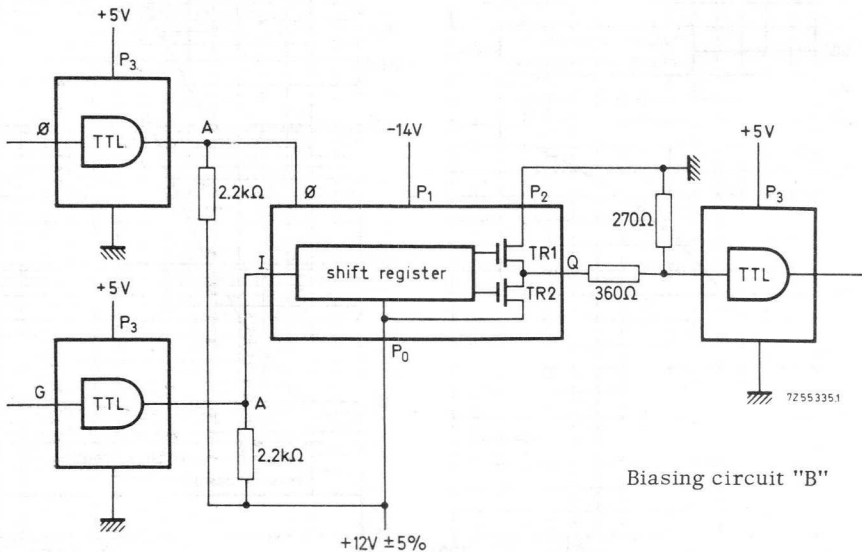


OUTPUT BUFFER DESCRIPTION

2. Biasing circuit "A" may be used to drive TTL or DTL loads direct. The MOS input logic levels must be referenced to V_{P0} . TR1 and TR2 are the push-pull output driver transistor of the FDN156.

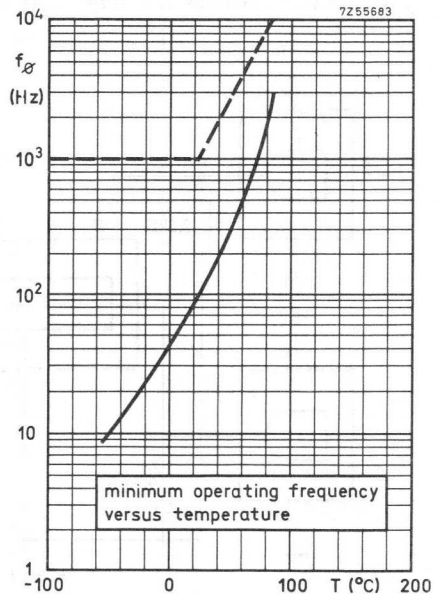
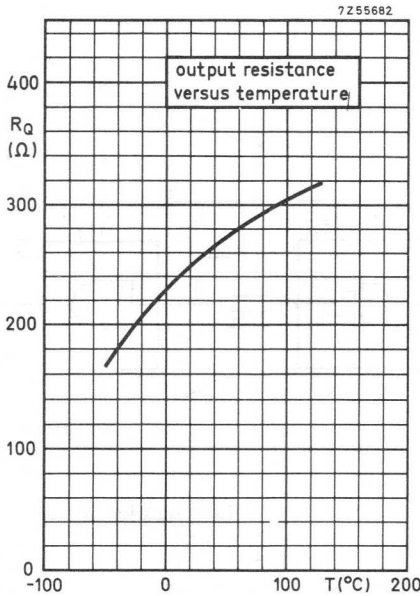
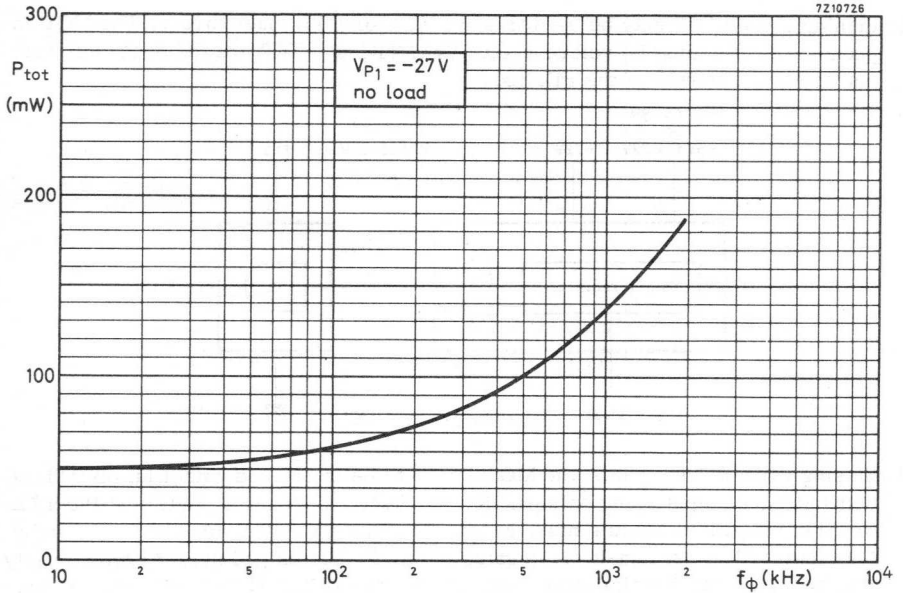


3. Biasing circuit "B" allows the MOS device to be interfaced with TTL or DTL at both input and output using only passive interface components. Note that the TTL or DTL integrated circuit must be able to withstand +10 V applied to the output lead (point A), most non- R_C type gates of our FC series and most FJ gates satisfy this requirement. Special open collector FJ gates (FJH301; 311; 321) have a minimum output breakdown voltage guarantee of 15 V.



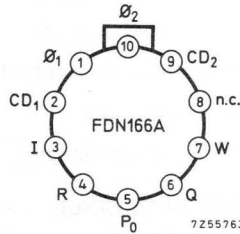
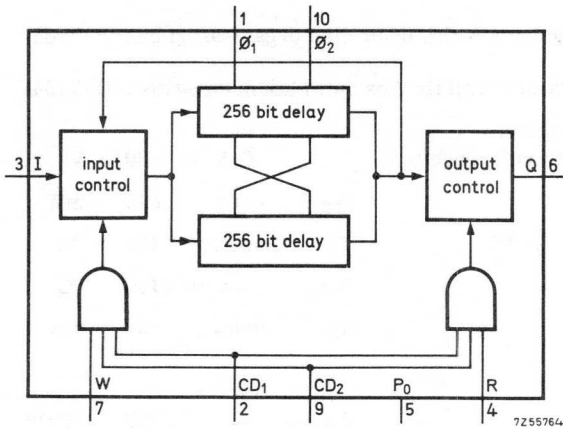
4. To drive MOS loads direct, the bias V_{P1} should be between -12 and -14 V to P_0 .

TYPICAL PERFORMANCE



The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

512-BIT RECIRCULATING DYNAMIC SERIAL MEMORY



P₀ connected to the metal case

QUICK REFERENCE DATA

| | | | |
|-------------------------------|------------|------------|-----|
| Clock rate | f_{ϕ} | 0.005 to 5 | MHz |
| Data rate | f_D | 0.01 to 5 | MHz |
| Power consumption per bit | | | |
| at 1 MHz data rate | P_{av} | 0.07 | mW |
| at 5 MHz data rate | P_{av} | 0.35 | mW |
| Operating ambient temperature | T_{amb} | -55 to +85 | °C |

•PACKAGE OUTLINE : TO-100 (See General Section)

GENERAL DESCRIPTION

The FDN166A consists of two 256-bit 2-phase dynamic shift registers, with internal multiplexing and recirculation circuitry.¹⁾

Data is written into and read from the device at both ϕ_1 and ϕ_2 , so that the data rate is twice the clock rate. The chip disable (CD) inputs allow selection of one-out-of-many circuits in larger memories. Both CD inputs have to be in the HIGH state to activate the device. Data will be written in when W, CD₁, and CD₂ are in the HIGH state; at all other times the device is in the recirculation mode. The output is active only when R, CD₁ and CD₂ are in the HIGH state; so that the outputs of more devices can be wired-OR.

With the FDN166A large serial memories with a drum-like organisation can be made.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage on all data inputs, clock inputs,

| | | |
|---------------------------------------------------------------|-----------------------|----------------|
| outputs and supply terminals with reference to P ₀ | +0.5 to -30 | V |
| Power dissipation | P _{tot} max. | 625 mW |
| Junction temperature up to T _{amb} = 25 °C | T _j max. | 150 °C |
| Storage temperature | T _{stg} | -65 to +150 °C |
| Output current (per output) | ±I _Q max. | 20 mA |

THERMAL RESISTANCE

| | | |
|--------------------------|-----------------------|----------|
| From junction to ambient | R _{th j-a} = | 200 °C/W |
|--------------------------|-----------------------|----------|

Note

All terminals are protected against over-voltage due to static charges.

¹⁾ External behaviour: 512-bit shift register.

DRIVE REQUIREMENTS at $T_{amb} = -55$ to $+85$ °C; P_0 is grounded

| | Symbol | min. | typ. | max. | Conditions and references |
|---------------------------------------------|--------------------------------------|------|------|-------------|---------------------------|
| Clock rate | f_{ϕ} | 0.05 | - | 1.5 MHz | $V_{\phi L} = -23$ V |
| | | 0.05 | - | 2.5 MHz | $V_{\phi L} = -26$ V |
| Clock pulse width | $t_{\phi L}$ | 0.28 | - | 10 μ s | $V_{\phi L} = -23$ V |
| | | 0.16 | - | 10 μ s | $V_{\phi L} = -26$ V |
| Clock pulse rise time | $t_{\phi LH}$ | - | - | 100 ns | |
| Clock pulse fall time | $t_{\phi HL}$ | - | - | 100 ns | |
| Clock delay | $t_{\phi 1\phi 2}, t_{\phi 2\phi 1}$ | 0 | - | 100 μ s | |
| Clock pulse voltage levels | | | | | |
| HIGH | $V_{\phi H}$ | -2 | - | +0.3 V | |
| LOW | $V_{\phi L}$ | -28 | - | -23 V | |
| Data input logic levels | | | | | |
| HIGH | $V_{IH}, V_{CDH}, V_{RH}, V_{WH}$ | -1 | - | +0.3 V | |
| LOW | $V_{IL}, V_{CDL}, V_{RL}, V_{WL}$ | -28 | - | -9 V | |
| Data lead time for I, W, R and CD inputs | t_{ℓ} | 50 | - | - ns | |

CHARACTERISTICS at $T_{amb} = -55$ to $+85$ °C; P_0 grounded

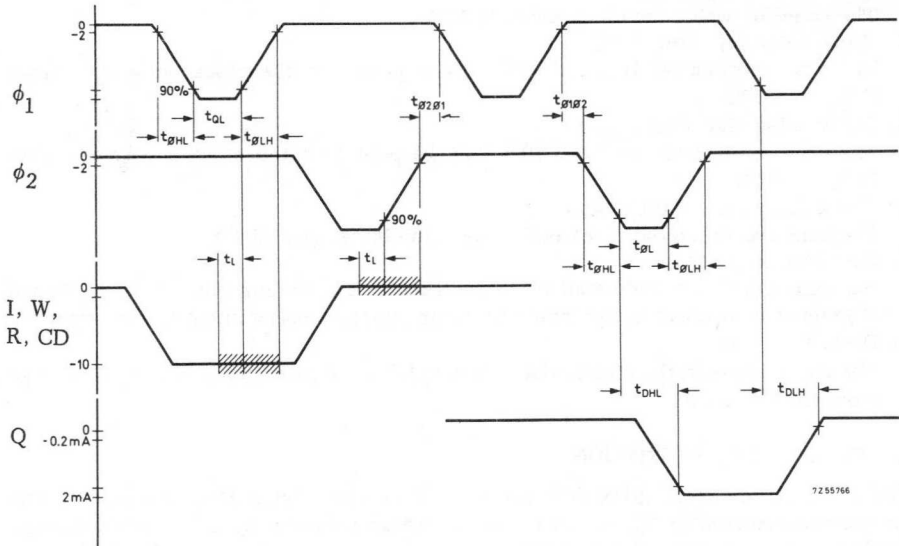
| | Symbol | min. | typ. | max. | Conditions and references |
|----------------------------|--------------------|------|------|--------------|------------------------------------------------------------------------|
| Data rate | f_D | 0.01 | - | 3 MHz | $V_{\phi L} = -23$ V |
| | f_D | 0.01 | - | 5 MHz | $V_{\phi L} = -26$ V |
| Output current | | | | | |
| HIGH | $-I_{QH}$ | 2 | - | - mA | $V_Q = -5$ V; see note |
| LOW | $-I_{QL}$ | - | - | 10 μ A | $V_Q = -15$ V |
| <u>Capacitances</u> | | | | | |
| I, R, W and CD inputs | C_I | - | 2.3 | 3.5 pF | $V_I = 0$ V; $f = 1$ MHz |
| Clock input capacitance | C_ϕ | - | 95 | 110 pF | $V_\phi = 0$ V; $f = 1$ MHz |
| Output capacitance | C_Q | - | 2.0 | 2.5 pF | $V_Q = 0$ V; $f = 1$ MHz |
| Leakage currents | | | | | |
| I, R, W and CD inputs | $-I_I$ | - | - | 1 μ A | $V_I = -15$ V; $T_{amb} = 25$ °C all other terminals at V_{P0} |
| Clock inputs | $-I_\phi$ | - | - | 100 μ A | $V_\phi = -28$ V; $T_{amb} = 25$ °C all other terminals at V_{P0} |
| Output resistance | | | | | |
| HIGH | R_{QH} | - | - | 1 k Ω | $V_Q = -5$ V See note |
| Delay times | | | | | |
| Clock input to data output | t_{DHL}, t_{DLH} | - | - | 110 ns | |

Note.

The specified output current is measured immediately after the delay time t_{DLH} . In a steady HIGH state the output resistance decreases to less than 1 k Ω .

CHARACTERISTICS (continued)

TIMING DIAGRAM

Note

Data inputs (I, W, R, CD_1 and CD_2) must remain valid for the shaded interval to ensure proper entry.

When CD_1, CD_2 and R are HIGH during this time, the output circuit will be active during the succeeding clock pulse.

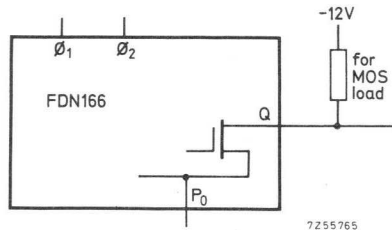
CHARACTERISTICS

GLOSSARY OF TERMS

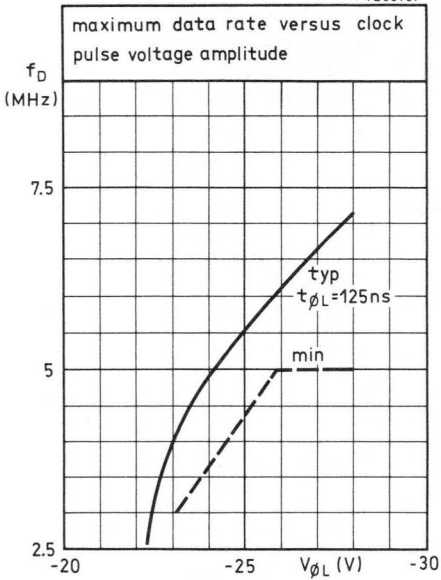
1. Clock pulse width: $t_{\phi L}$
The time for which the clock pulse is LOW.
2. Clock pulse fall time: $t_{\phi HL}$
The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock delay time: $t_{\phi 1\phi 2}$, $t_{\phi 2\phi 1}$
The time for which the clock pulses are simultaneously HIGH.
5. Data lead time: t_{ℓ}
The time before the indicated point on the clock pulse for which I, R, W, CD₁ and CD₂ must be present at the inputs to ensure correct entry into the memory.
6. Delay time: t_D
The delay between the clock pulse reaching LOW and the output beginning to change from LOW to HIGH.

OUTPUT BUFFER DESCRIPTION

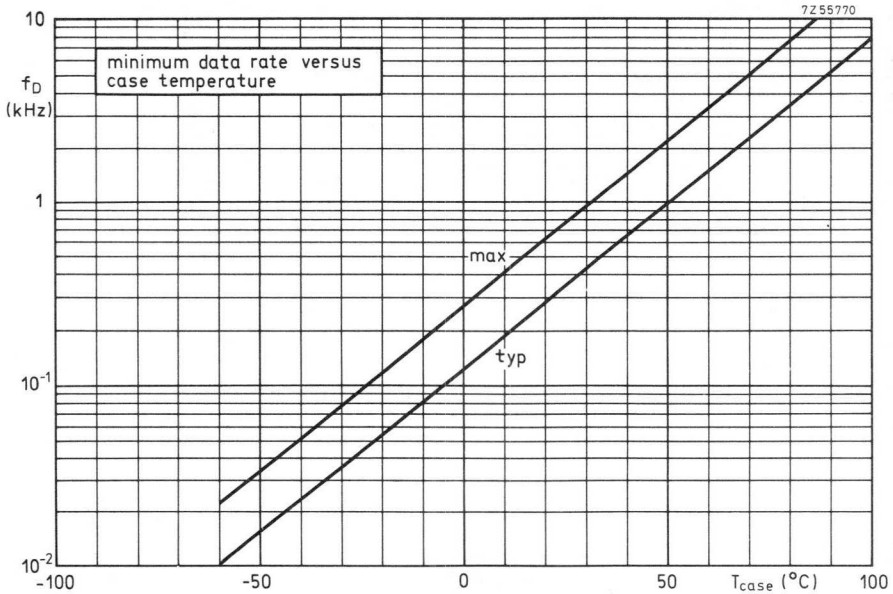
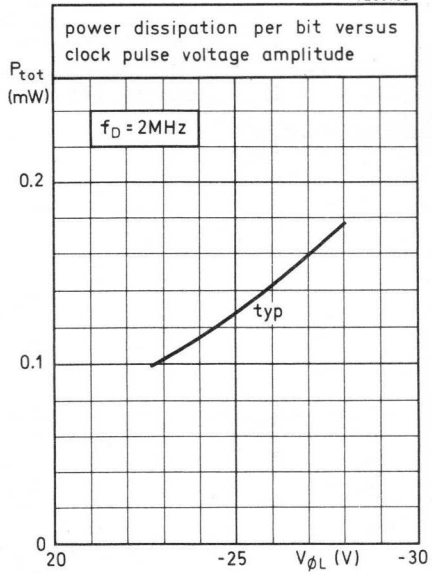
The output buffer of the FDN166A consists of an open drain MOS transistor. The source is connected to P₀, the drain to the output terminal Q. The use of this type of output allows wired-OR-ing of the outputs in expanded memories. The buffer can simply be interfaced with TTL or with other MOS circuits. In the latter case only one resistor is required; which value depends on the load capacitance and the speed desired.

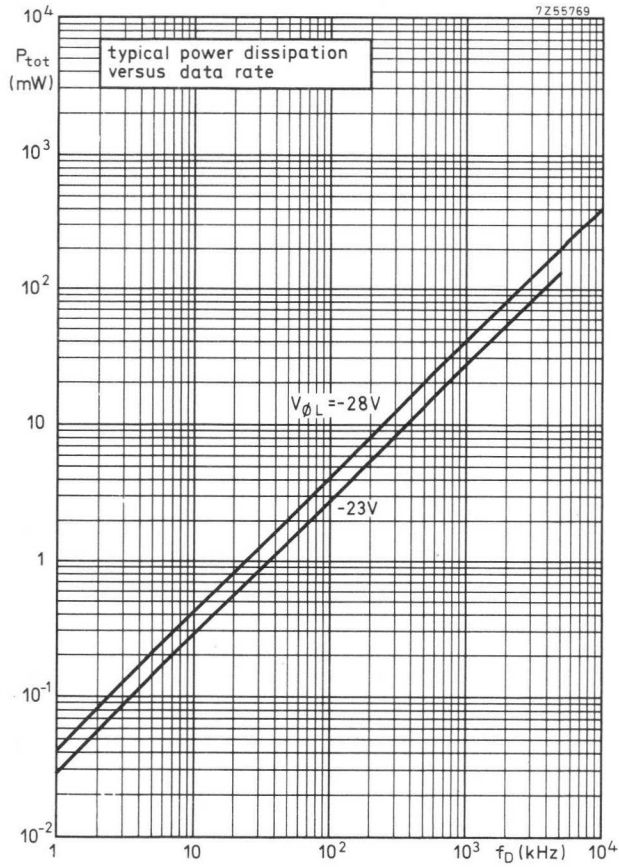


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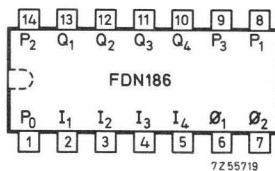
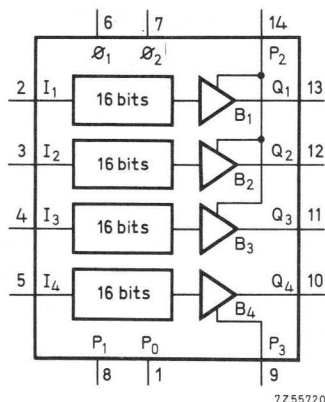
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The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

QUADRUPLE 16-BIT DYNAMIC SHIFT REGISTER



P₀ and metal package bottom are connected.

QUICK REFERENCE DATA

| | | |
|------------------------------------|---------------------------------|---------------|
| Supply voltage | V _{P1} | -24 to -28 V |
| D. C. noise margin | M _L ; M _H | > 1 V |
| Clock rate | f _φ | 0.01 to 3 MHz |
| Power consumption per bit at 1 MHz | P _{av} | typ. 1.2 mW |
| Operating ambient temperature | T _{amb} | -55 to +85 °C |

PACKAGE OUTLINE : 14 lead metal -ceramic dual in-line (See General Section)

GENERAL DESCRIPTION

The FDN186 package comprises 4 separate 16-bit shift registers that can be used independently or can be externally connected to make registers up to 64-bits long. Clock and power lines are common to all four registers. The output buffers are bi-directional, low impedance NRZ ¹⁾, that by suitable biasing will directly drive MOS, DTL or TTL loads or, because they have separate output voltages (V_{P2} ; V_{P3}), a combination of MOS and bipolar. V_{P2} and V_{P3} are output buffer voltages only, and the output signal is independent of the width and amplitude of the clock pulse.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage on all data inputs, clock inputs, outputs
and supply terminals with reference to P_0

+0,5 to -30 V

Power dissipation up to $T_{amb} = 25^{\circ}\text{C}$

P_{tot} max. 800 mW

Junction temperature

T_j max. 150 $^{\circ}\text{C}$

Storage temperature

T_{stg} -65 to +150 $^{\circ}\text{C}$

Total current through terminals P_2 and P_3

$-I_{P2}$, $-I_{P3}$ max. 40 mA

Output current (per output)

$\pm I_Q$ max. 20 mA

THERMAL RESISTANCE

From junction to ambient

$R_{th\ j-a} = 156^{\circ}\text{C/W}$

Note

The device is protected against over-voltage caused by static charges.

¹⁾ Non return to zero.

CHARACTERISTICS at $T_{amb} = -55$ to $+85^{\circ}\text{C}$

| | Symbol | min. | typ. | max. | Conditions and references |
|---------------------------|--------------------|--------------|------|--------------------|-----------------------------------------|
| Clock rate | f_{ϕ} | 0.01 | - | 3 MHz | } see timing diagram for parameter def. |
| Clock pulse width | $t_{\phi 1L}$ | 0.125 | - | 1 μs | |
| | $t_{\phi 2L}$ | 0.125 | - | 1 μs | |
| Clock pulse fall time | $t_{\phi HL}$ | - | - | 0.10 μs | see note 1 |
| Clock pulse rise time | $t_{\phi LH}$ | - | - | 0.10 μs | see note 1 |
| Clock delay times | $t_{\phi 1\phi 2}$ | 0 | - | 49 μs | |
| | $t_{\phi 2\phi 1}$ | 0 | - | 49 μs | |
| Clock pulse voltage level | | | | | |
| | HIGH | $V_{\phi H}$ | -2 | 0 | +0.3 V |
| | LOW | $V_{\phi L}$ | -28 | -26 | -24 V |
| Data input logic level | | | | | |
| | HIGH | V_{IH} | -1.5 | 0 | +0.3 V |
| | LOW | V_{IL} | -28 | -12 | -9 V |
| Data lead time | $t_{\ell I}$ | 10 | - | - | ns |

1) Above $f_{\phi} = 1.54\text{MHz}$ $t_{\phi 1Lmin}$ and $t_{\phi 2Lmin}$ determine the maximum value of $t_{\phi HL}$ and $t_{\phi LH}$.

CHARACTERISTICS (continued)

Test conditions: $V_{P1} = -24$ V to -28 V; $V_{P2} = V_{P3} = -12$ V to -14 V; $T_{amb} = -55$ to $+85$ °C; P_0 = grounded; standard load: 50 pF in parallel with 20 k Ω to P_0

| | Symbol | min. | typ. | max. | Conditions and references |
|---------------------------------------------------------|--------------------------|-----------|------|--------------|-------------------------------------------------------------------------|
| <u>ELECTRICAL DATA</u> | | | | | |
| Output levels | | | | | |
| HIGH | V_{QH} | -0.5 | - | 0 V | |
| LOW | V_{QL} | -14 | - | -10 V | |
| Data input capacitance | C_I | - | 2 | 3.5 pF | bias: $V_I = 0$ V; $f = 1$ MHz |
| Clock input capacitance | $C_{\phi 1}, C_{\phi 2}$ | - | 19 | 25 pF | bias: $V_{\phi} = 0$ V; $f = 1$ MHz |
| | $C_{\phi 1}, C_{\phi 2}$ | - | 14 | 18 pF | bias: $V_{\phi} = -26$ V; $f = 1$ MHz |
| <u>Leakage currents:</u> | | | | | |
| Data input currents | I_{IL} | - | - | 1 μ A | $V_I = -15$ V; all other terminals at V_{P0} ; $T_{amb} = 25$ °C |
| Clock input current | $I_{\phi L}$ | - | - | 100 μ A | $V_{\phi} = -28$ V; all other terminals at V_{P0} ; $T_{amb} = 25$ °C |
| <u>Output resistance</u> | | | | | |
| HIGH | R_{QH} | - | 300 | 600 Ω | $V_{P2} = V_{P3} = -5$ V |
| LOW | R_{QL} | - | 250 | 500 Ω | |
| Drive capability (see note 1 on page 5) | V_{QL} | - | -10 | -8 V | $R_L = 4$ k Ω reference to P_0 |
| | V_{QL} | - | -4.7 | -4.4 V | $V_{P2} = V_{P3} = -5$ V; $R_L = 4$ k Ω reference to P_0 |
| Power supply current drain (see note 2 on page 5) | I_{P1} | - | 2.0 | 3.0 mA | $V_{P1} = -26$ V; $f = 1$ MHz $T_{amb} = 25$ °C |
| | I_{P2}, I_{P3} | - | 2.4 | 3.0 mA | $V_{P2} = V_{P3} = -13$ V; $f = 1$ MHz $T_{amb} = 25$ °C |
| <u>Output transition times:</u> | | | | | |
| fall time | t_{THL} | - | 100 | - ns | |
| rise time | t_{TLH} | - | 100 | - ns | |
| <u>Delay times:</u> | fall time | t_{DHL} | - | 80 | - ns |
| | rise time | t_{DLH} | - | 80 | - ns |
| D.C. noise margin | M_L, M_H | 1 | - | - V | |

CHARACTERISTICS (continued)Note 1 (see page 4)

The maximum capacitive load that can be driven depends only on the speed desired and the power dissipation allowable. See the output buffer description on page 8 for further information on output drive capability.

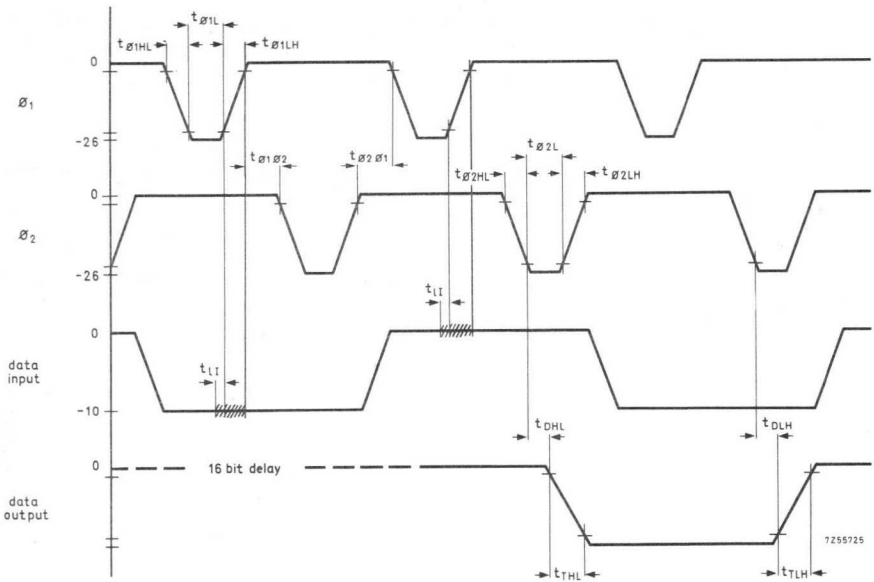
Note 2 (see page 4)

The output buffer power supply currents (I_{P2} , I_{P3}) are almost entirely dependent on the external load.



CHARACTERISTICS (continued)

TIMING DIAGRAM



Timing diagram note:

Input data must remain valid for the shaded interval to ensure proper entry into the register.

Note

The indicated points on the vertical axes are specified in the glossary of terms.

CHARACTERISTICS (continued)GLOSSARY OF TERMS

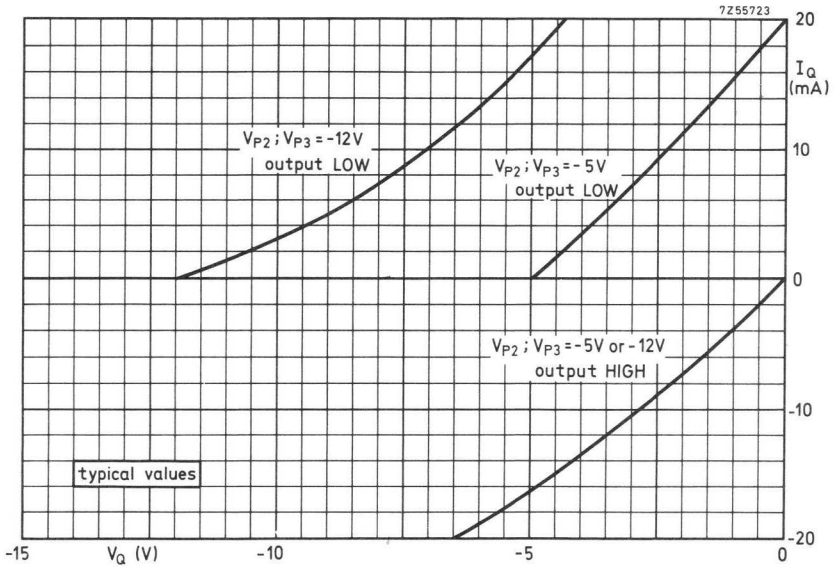
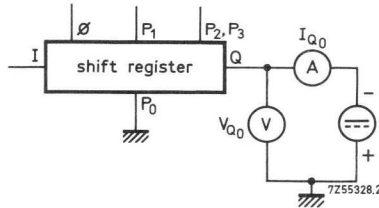
1. Clock pulse width: $t_{\phi L}$
The time for which the clock pulse is LOW: $V_{\phi L} \leq -24 \text{ V}$
2. Clock pulse fall time: $t_{\phi HL}$
The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock delay time: $t_{\phi 1\phi 2}$, $t_{\phi 2\phi 1}$
The time between the end of the ϕ_1 (or ϕ_2) clock pulse and the start of the ϕ_2 (or ϕ_1) clock pulse, defined at -2 V .
5. Data lead time: $t_{\ell I}$
The time before the 90% point on the clock pulse ϕ_1 for which the voltage at the input must be at its specified logic level in order to ensure that the data will be entered in the register.
6. Output fall transition time: t_{THL}
The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
7. Output rise transition time: t_{TLH}
The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
8. Fall delay time: t_{DHL}
The delay between the clock pulse ϕ_2 reaching LOW and the output beginning to change from HIGH to LOW.
9. Rise delay time: t_{DLH}
The delay between the clock pulse ϕ_2 reaching LOW and the output beginning to change from LOW to HIGH.

OUTPUT BUFFER DESCRIPTION

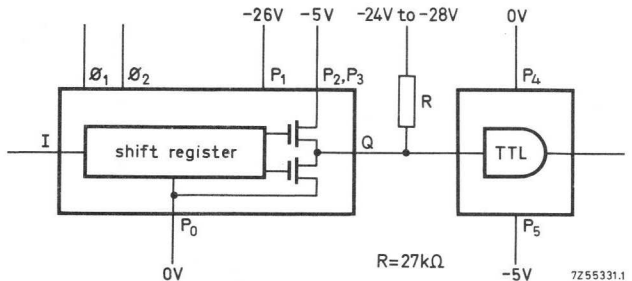
- The curves below are typical output buffer voltage-current characteristics for the FDN186. They show V_Q versus I_Q for the V_{P2} and V_{P3} at -5 V and -12 V , for both HIGH and LOW output.

Note: When operating with high output current levels, the maximum power rating must not be exceeded.

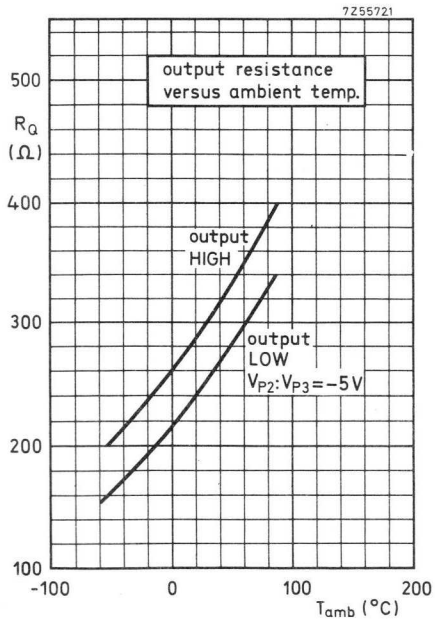
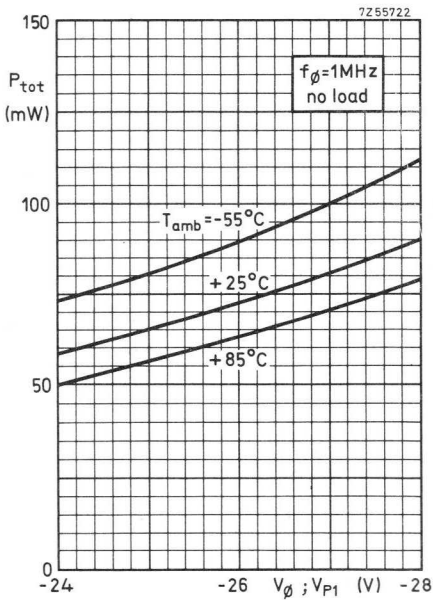
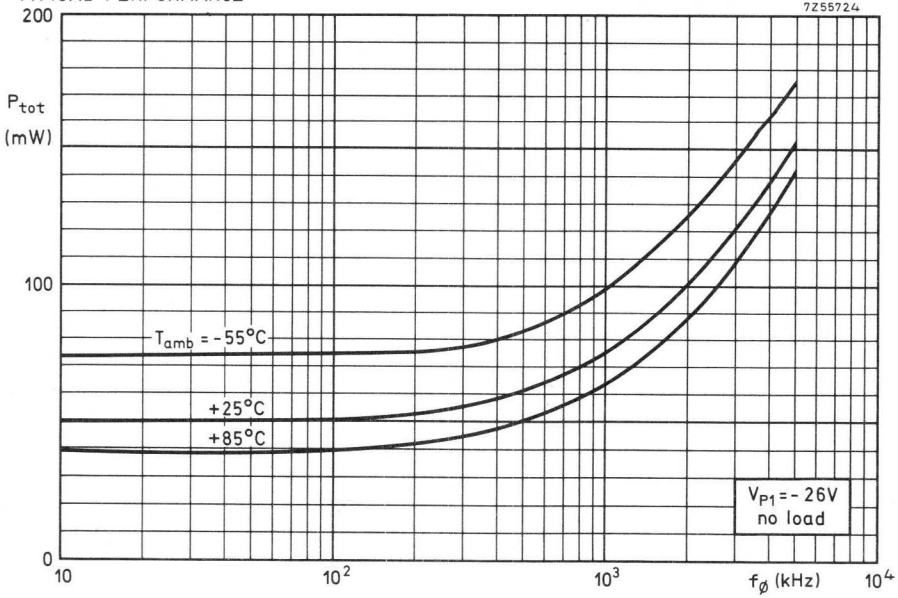
The circuit shown may be used to obtain output curves for other values of V_{P2} and V_{P3} .



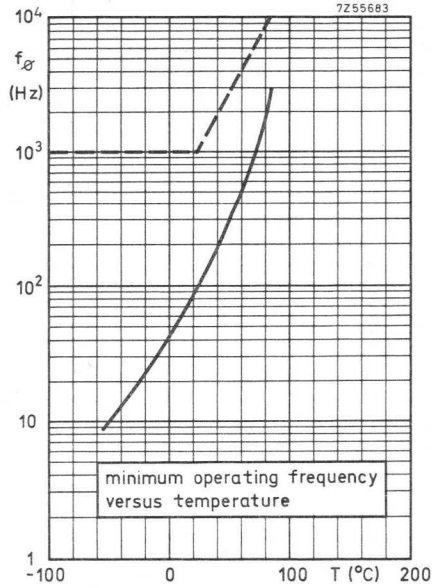
- The bias arrangement shown is suitable for driving TTL or DTL loads direct.



TYPICAL PERFORMANCE

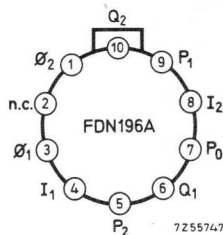
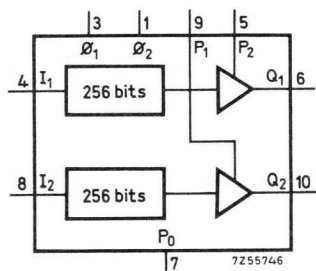


TYPICAL PERFORMANCE (continued)



The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

DUAL 256-BIT DYNAMIC SHIFT REGISTER



P_0 connected to metal case

QUICK REFERENCE DATA

| | | | |
|--------------------------------------------------|------------|------------|--------------------|
| Clock rate | f_ϕ | 0.01 to 3 | MHz |
| Power consumption per bit at $f_\phi = 3$ MHz | P_{av} | typ. 0.36 | mW |
| Operating ambient temperature | T_{amb} | -55 to +85 | $^{\circ}\text{C}$ |
| D. C. noise margin | $M_H; M_L$ | > | 1 V |

PACKAGE OUTLINE: TO-100 (See General Section)

GENERAL DESCRIPTION

The FDN196A consists of two 256-bit 2-phase dynamic shift registers, with common clock lines.

The device has two low impedance push-pull output buffers, with separate supply voltages. Thus the two outputs may be independently biased to drive a bipolar load or other MOS circuits.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|------------------------------------------------------------------------------------------------------------|-------------------------------------|------|-------------|----|
| Voltage on all data inputs, clock inputs, outputs and supply terminals with reference to P ₀ | | +0.5 | -30 | V |
| Power dissipation up to T _{amb} = 25 °C | P _{tot} | max. | 625 | mW |
| Junction temperature | T _j | max. | 150 | °C |
| Storage temperature | T _{stg} | | -65 to +150 | °C |
| Total current through terminals P ₁ , P ₂ | -I _{P1} , -I _{P2} | max. | 20 | mA |
| Output current (per output) | ±I _Q | max. | 20 | mA |

THERMAL RESISTANCE

| | | | | |
|--------------------------|---------------------|---|-----|------|
| From junction to ambient | R _{th j-a} | = | 200 | °C/W |
|--------------------------|---------------------|---|-----|------|

Note

All terminals are protected against over-voltage due to static charges.

DRIVE REQUIREMENTS at $T_{amb} = -55$ to $+85$ °C; P_0 is grounded

| | Symbol | min. | typ. | max. | Conditions and references |
|----------------------------|--------------------------------------|-------|------|------|---------------------------|
| Clock rate | f_{ϕ} | 0.01 | - | 3 | MHz |
| Clock pulse width | $t_{\phi 1L}$ | 0.125 | - | 5.0 | μs |
| | $t_{\phi 2L}$ | 0.125 | - | 5.0 | μs |
| Clock pulse rise time | $t_{\phi LH}$ | - | - | 0.5 | μs |
| Clock pulse fall time | $t_{\phi HL}$ | - | - | 0.5 | μs |
| Clock delay | $t_{\phi 1\phi 2}, t_{\phi 2\phi 1}$ | 0 | - | 45 | μs |
| Clock pulse voltage levels | | | | | |
| HIGH | $V_{\phi H}$ | -2 | 0 | +0.3 | V |
| LOW | $V_{\phi L}$ | -28 | -26 | -24 | V |
| Data input logic levels | | | | | |
| HIGH | V_{IH} | -2 | 0 | +0.3 | V |
| LOW | V_{IL} | -28 | -12 | -9 | V |
| Data lead time | $t_{\ell I}$ | 10 | - | - | ns |
| Buffer supply voltages | $-V_{P1}, -V_{P2}$ | 0 | - | 14 | V |

CHARACTERISTICS

Test conditions: $V_{P1} = V_{P2} = -12$ to -14 V; $T_{amb} = -55$ to $+85$ °C; P_0 = grounded
standard load: 50 pF in parallel with 20 k Ω to P_0 .

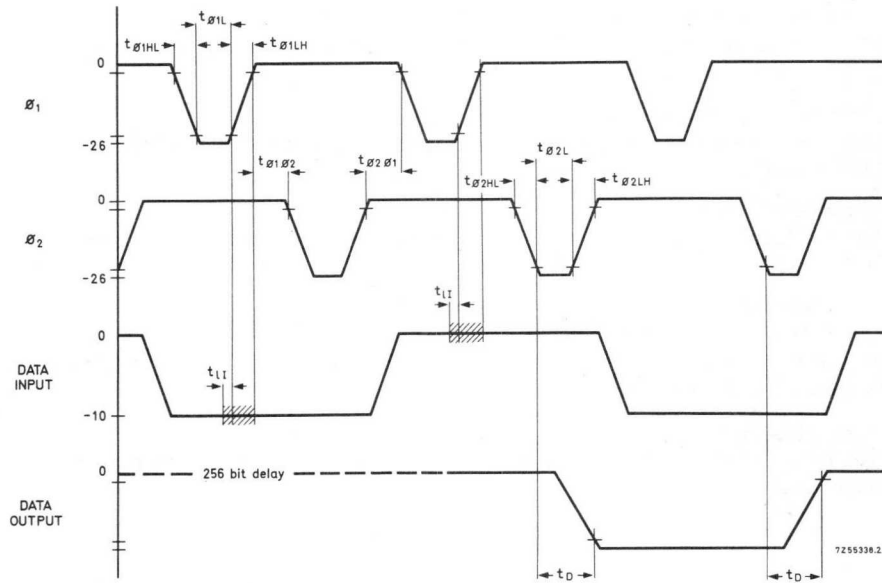
| ELECTRICAL DATA | Symbol | min. | typ. | max. | Conditions and references |
|--------------------------|--------------------------|------|-------|--------------|-------------------------------------------------------------------------|
| Output levels | | | | | |
| HIGH | V_{QH} | -0.5 | - | 0 V | |
| LOW | V_{QL} | -14 | - | -10 V | |
| Data input capacitance | C_I | - | 2 | 3.5 pF | $V_I = 0$ V; $f = 1$ MHz |
| Clock input capacitances | $C_{\phi 1}, C_{\phi 2}$ | - | 90 | 110 pF | $V_{\phi} = 0$ V; $f = 1$ MHz |
| | | - | 60 | 80 pF | $V_{\phi} = -26$ V; $f = 1$ MHz |
| <u>Leakage currents</u> | | | | | |
| Data input current | $-I_{IL}$ | - | - | 1 μ A | $V_I = -15$ V; all other terminals at P_0 ; $T_{amb} = 25$ °C |
| Clock input current | $-I_{\phi L}$ | - | - | 100 μ A | $V_{\phi} = -28$ V; all other terminals at P_0 ; $T_{amb} = 25$ °C |
| <u>Output resistance</u> | | | | | |
| HIGH | R_{QH} | - | 250 | 500 Ω | |
| LOW | R_{QL} | - | 150 | 300 Ω | $V_{P1}, V_{P2} = -5$ V |
| Supply currents | $-I_{P1}, -I_{P2}$ | - | -0.68 | -1.0 mA | $V_{P1}, V_{P2} = -13$ V $f = 1$ MHz; $T_{amb} = 25$ °C See note |
| <u>Delay time</u> | | | | | |
| Clock to output | t_D | - | 135 | 275 ns | |

Note

The output buffer power supply current is almost entirely dependent on the external load. The value shown is for a load of 50 pF in parallel with 1 M Ω to P_0 .

CHARACTERISTICS (continued)

TIMING DIAGRAM



Notes

1. The indicated points on the vertical axis are specified in the glossary of terms.
2. With the FDN196A the data inputs must also remain valid for the $t_{\phi LH}$.
3. Data inputs must remain valid for the shaded interval to ensure proper entry into the register.

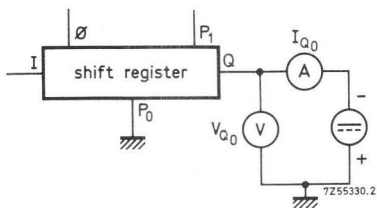
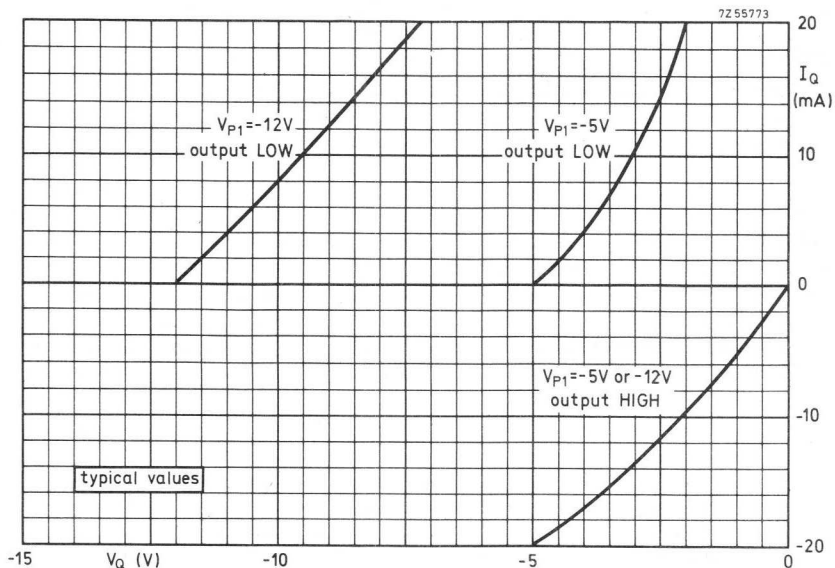
CHARACTERISTICS (continued)GLOSSARY OF TERMS

1. Clock pulse width: $t_{\phi L}$
The time for which the clock pulse is LOW: $V_{\phi L} \leq -26 \text{ V}$
2. Clock pulse fall time: $t_{\phi HL}$
The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock delay time: $t_{\phi 1\phi 2}$, $t_{\phi 2\phi 1}$
The last allowable time between the end of the ϕ_1 (or ϕ_2) clock pulse and the start of the ϕ_2 (or ϕ_1) clock pulse, defined at -2 V .
5. Data lead time: t_{lI}
The time before the 90% point on the clock pulse ϕ_1 for which the voltage at the data input must be at its specified logic level in order to ensure that the data will be entered in the register.
6. Delay time: t_D
The delay between the clock pulse ϕ_2 reaching LOW and the output reaching its logic level.

OUTPUT BUFFER DESCRIPTION

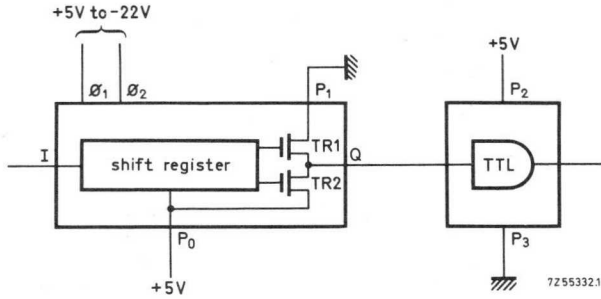
1. The curves below are typical output buffer voltage-current characteristics for the FDN196A. They show V_Q versus I_Q for the bias V_{P1} at -5 V and -12 V, for both HIGH and LOW output. The circuit shown may be used to obtain LOW output curves for other values of V_{P1} .

Note: When operating with high output current levels, the maximum power rating must not be exceeded.



OUTPUT BUFFER DESCRIPTION (continued)

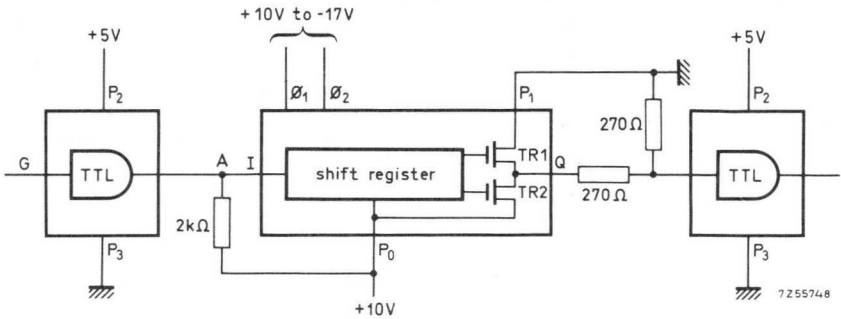
2. Biasing circuit A may be used to drive TTL or DTL loads direct. The MOS input logic levels must be referenced to V_{P0} . TR1 and TR2 are the push-pull output driver transistors of the FDN146.



Biasing circuit A

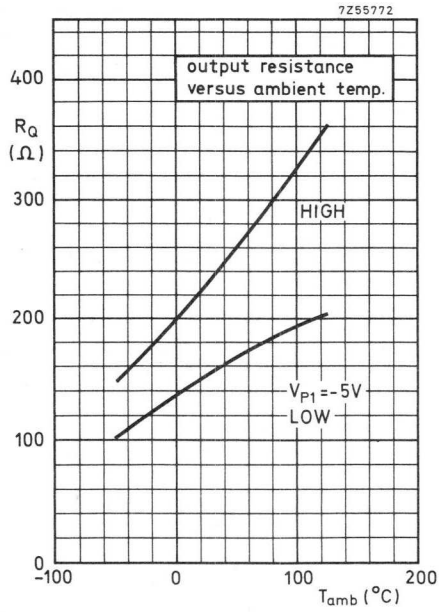
3. Biasing circuit B allows the MOS device to be interfaced with TTL or DTL at and output using only passive interface components.

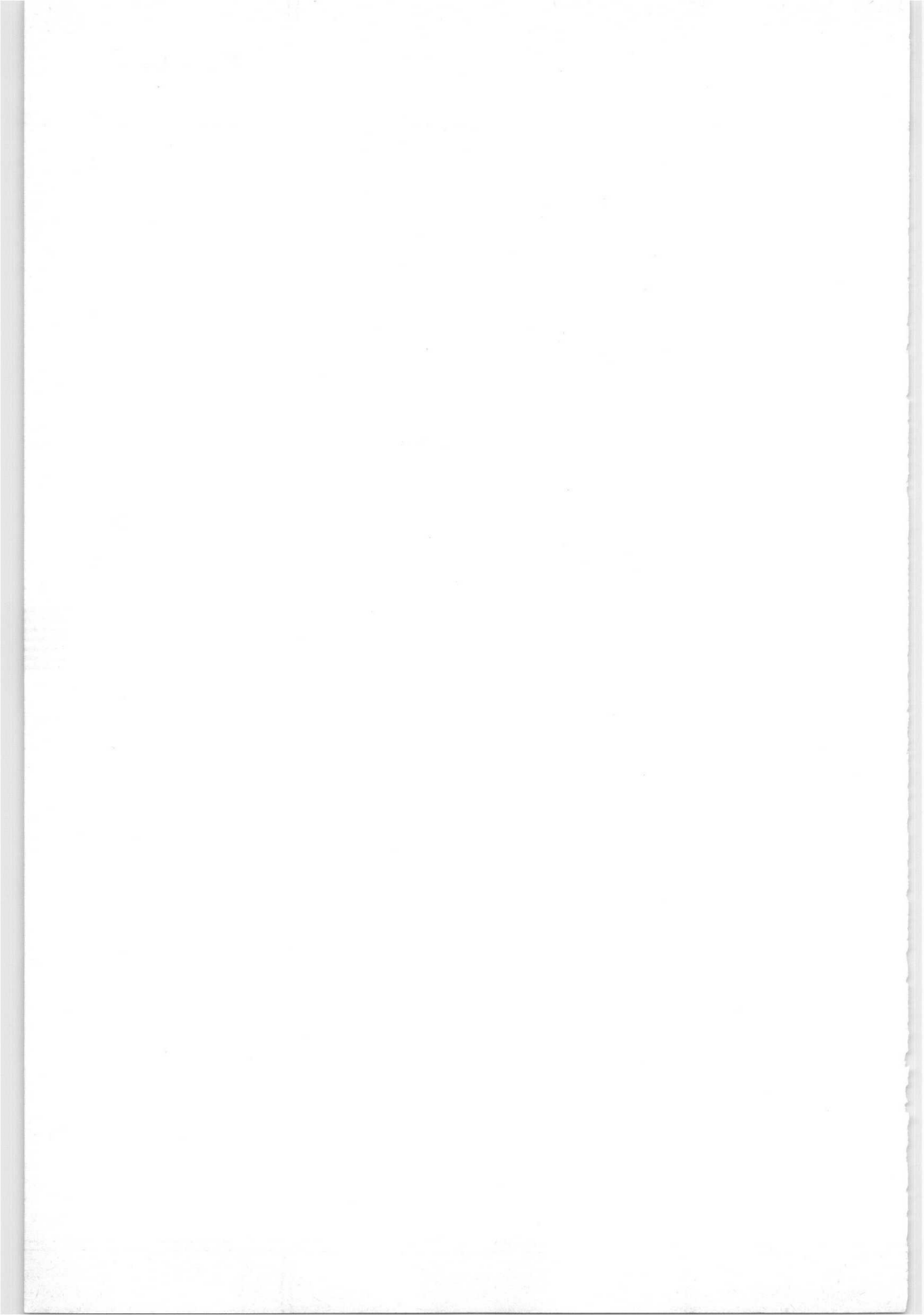
Note that the TTL or DTL integrated circuit must be able to withstand +10 V applied to the output lead (point A), most circuits of our FC series and most FJ gates satisfy this requirement. Some open collector FJ gates have a minimum output breakdown voltage guarantee of 15 V.



Biasing circuit B

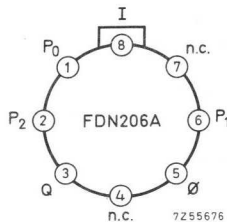
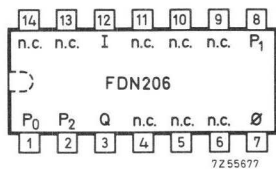
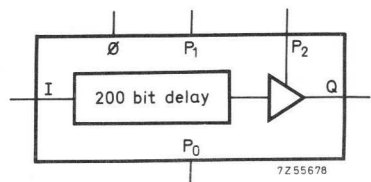
4. To drive MOS loads direct, the bias V_{P1} should be between -12 and -14 V to P_0 .





The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

200-BIT DYNAMIC SHIFT REGISTER



FDN206 : P₀ connected to the metal bottom
FDN206A: P₀ connected to the metal case

QUICK REFERENCE DATA

| | | | |
|------------------------------------------------|------------|------------|--------|
| Supply voltage | V_{P1} | -26 to -28 | V |
| D. C. noise margin | $M_L; M_H$ | > | 1 V |
| Clock rate | f_ϕ | 0.01 to 1 | MHz |
| Power consumption per bit at $f_\phi = 10$ kHz | P_{av} | < | 0.2 mW |
| | P_{av} | < | 0.6 mW |
| Operating ambient temperature | T_{amb} | -55 to +85 | °C |

PACKAGE OUTLINES : FDN206 ; 14 lead dual in-line (See General Section)
FDN206A; TO-99 (See General Section)

GENERAL DESCRIPTION

The FDN206 contains one 200-bit shift register with one serial input and one serial output. It dissipates little power and uses a one-phase external clock. The device has a low impedance push-pull output buffer which, when appropriately biased is capable of interfacing direct with MOS, DTL, TTL and other loads.

The buffer supply terminal P₂ is a separate supply which determines the output LOW signal only. This provides an output level that is independent of both the amplitude and width of the clock pulse.

With the FDN206, the FDN116 (a quadruple 32-bit shift register) and FDN136 (a variable length 1 to 64-bit shift register) shift registers of any required length can be built from off-the-shelf parts.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages on all data inputs, clock inputs, outputs
and supply terminals with reference to P₀

| | | | | |
|--------------------------------------------------|---------------------------|-------------|-----|----|
| | | +0.5 to | -30 | V |
| Power dissipation up to T _{amb} = 25 °C | FDN206 : P _{tot} | max. | 800 | mW |
| | FDN206A: P _{tot} | max. | 625 | mW |
| Junction temperature | T _j | max. | 150 | °C |
| Storage temperature | T _{stg} | -65 to +150 | | °C |
| Total current through terminal P ₂ | -I _{p2} | max. | 40 | mA |
| Output current (per output) | ±I _Q | max. | 20 | mA |

THERMAL RESISTANCE

| | | | | |
|--------------------------|------------------------------|---|-----|------|
| From junction to ambient | FDN206 : R _{th j-a} | = | 156 | °C/W |
| | FDN206A: R _{th j-a} | = | 200 | °C/W |

CHARACTERISTICS at $T_{amb} = -55$ to $+85$ °C

| | Symbol | min. | typ. | max. | Conditions and references |
|---------------------------|---------------|------|------|--------------|----------------------------------------------------------|
| Clock rate | f_{ϕ} | 0.01 | - | 1 MHz | See timing diagram for parameter definitions See note |
| Clock pulse width | $t_{\phi L}$ | 0.45 | - | 50 μ s | |
| Clock pulse fall time | $t_{\phi HL}$ | - | - | 0.10 μ s | |
| Clock pulse rise time | $t_{\phi LH}$ | - | - | 0.10 μ s | |
| Clock pulse space | $t_{\phi H}$ | 0.45 | - | 50 μ s | |
| Clock pulse voltage level | | | | | |
| HIGH | $V_{\phi H}$ | -2 | 0 | +0.3 V | $f_{\phi} \leq 750$ kHz $f_{\phi} > 750$ kHz |
| LOW | $V_{\phi L}$ | -28 | -12 | -9 V | |
| Data input logic levels | | | | | |
| HIGH | V_{IH} | -2 | 0 | +0.3 V | |
| LOW | V_{IL} | -28 | -12 | -9 V | |
| Data lead time | $t_{\ell I}$ | 20 | - | - ns | |
| Data hold time | t_{hI} | 75 | - | - ns | |
| Supply voltages | V_{P1} | -28 | -26 | -24 V | |
| | V_{P1} | -28 | -27 | -26 V | |
| | V_{P2} | -28 | - | +0.3 V | |

Note

The fall time specified for the FDN206 is to ensure that output data will meet the input hold time requirements of other shift registers, when more shift registers are operating in series from a common clock. If a register does not drive other registers the clock fall time may be longer.

CHARACTERISTICS (continued)

Test conditions: $V_{P1} = -26$ V to -28 V; $V_{P2} = -12$ V to -14 V; $T_{amb} = -55$ to $+85$ °C;
 $P_0 =$ grounded; standard load; 50 pF in parallel with 20 k Ω to P_0 .

| | Symbol | min. | typ. | max. | Conditions and references |
|----------------------------------|---------------|------|------|--------------|-----------------------------------------------------------------------|
| <u>ELECTRICAL DATA</u> | | | | | |
| Output levels | | | | | |
| HIGH | V_{QH} | -0.5 | - | 0 V | |
| LOW | V_{QL} | -14 | - | -10 V | |
| Data input capacitance | C_I | - | 2 | 3.5 pF | bias: $V_I = 0$ V; $f_\phi = 1$ MHz |
| Clock input capacitance | C_ϕ | - | 6 | 10 pF | bias: $V_\phi = 0$ V; $f_\phi = 1$ MHz |
| <u>Leakage currents</u> | | | | | |
| Data input currents | $-I_{IL}$ | - | - | 1 μ A | $V_I = -15$ V; all other terminals at V_{P0} ; $T_{amb} = 25$ °C |
| Clock input current | $-I_{\phi L}$ | - | - | 100 μ A | $V_\phi = -28$ V; all other terminals at V_{P0} ; $T_{amb} = 25$ °C |
| <u>Output resistance-</u> | | | | | |
| HIGH | R_{QH} | - | 250 | 500 Ω | |
| LOW | R_{QL} | - | 250 | 500 Ω | $V_{P2} = -5$ V |
| Drive capability (see note 1) | V_{QL} | - | -4.8 | -4.6 V | $V_{P2} = -5$ V; $R_L = 4$ k Ω to reference P_0 |
| Supply current (see note 2) | $-I_{P2}$ | - | 1.0 | 1.5 mA | $V_{P2} = -13$ V; $f_\phi = 1$ MHz; $T_{amb} = 25$ °C |
| | $-I_{P1}$ | - | 5.0 | 8.0 mA | $V_{P1} = -27$ V; $f_\phi = 1$ MHz; $T_{amb} = 25$ °C |
| <u>Output transition times:</u> | | | | | |
| fall time | t_{THL} | - | 100 | - ns | |
| rise time | t_{TLH} | - | 100 | - ns | |
| <u>Delay times:</u> | | | | | |
| fall time | t_{DHL} | - | 300 | - ns | |
| rise time | t_{DLH} | - | 300 | - ns | |
| D. C. noise margin | M_L | 1 | - | - V | |
| | M_H | 1.5 | - | - V | |

Note 1

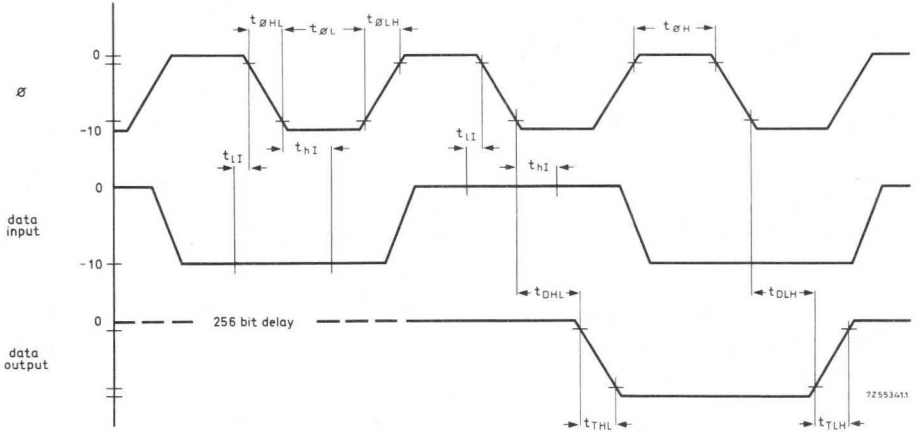
The maximum capacitive load that can be driven depends only on the speed desired and the power dissipation allowable. See the output buffer description on pages 7 and 8 for further information on output drive capability.

Note 2

The output buffer supply current I_{P2} is almost entirely dependent on the external load.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Note

The indicated points on the vertical axis are specified in the glossary of terms.

CHARACTERISTICS (continued)

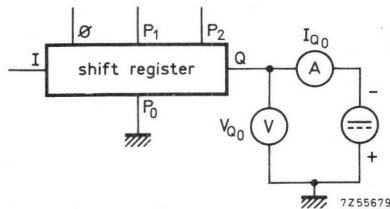
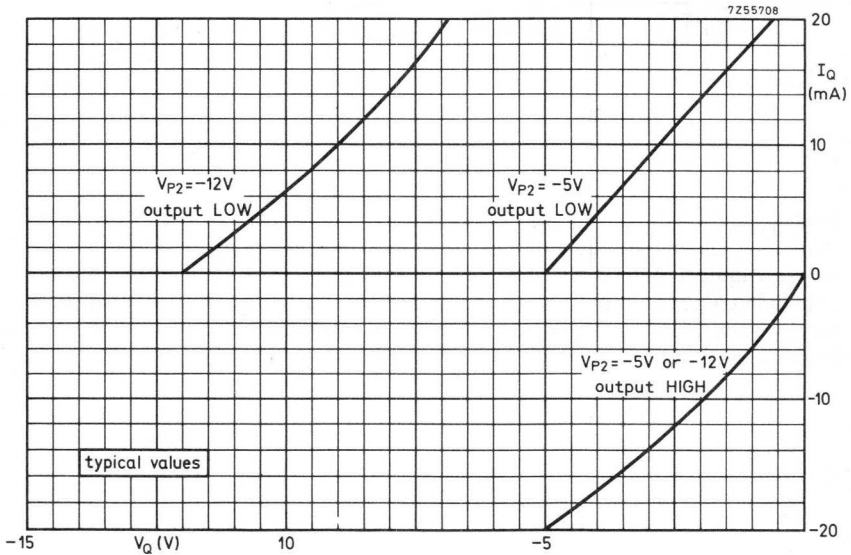
GLOSSARY OF TERMS

1. Clock pulse width: $t_{\phi L}$
The time for which the clock pulse is LOW: $V_{\phi L} \leq -9$ V.
2. Clock pulse fall time: $t_{\phi HL}$
The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock pulse space: $t_{\phi H}$
The least allowable time between the end of one clock pulse (ϕ) and the start of the next.
5. Data lead time: $t_{\ell I}$
The time before the 10% point on the clock pulse for which the voltage at the data input must be at its specified logic level in order to ensure that the data will be entered in the register.
6. Data hold time: $t_{\ell H}$
The time after the clock pulse ϕ reaches LOW for which the input data must remain stable to guarantee that it will be entered in the register.
7. Output fall transition time: t_{THL}
The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
8. Output rise transition time: t_{TLH}
The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
9. Fall delay time: t_{DHL}
The delay between the clock pulse ϕ reaching LOW and the output beginning to change from HIGH to LOW.
10. Rise delay time: t_{DLH}
The delay between the clock pulse ϕ reaching LOW and the output beginning to change from LOW to HIGH.

OUTPUT BUFFER DESCRIPTION

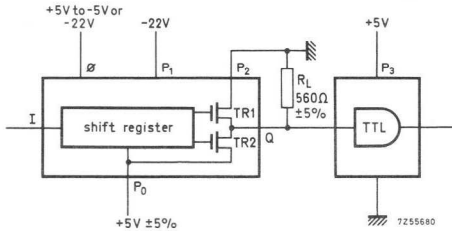
- The curves below are typical output buffer voltage-current characteristics for the FDN206. They show V_Q versus I_Q for the bias V_{P1} at -5 V and -12 V , for both HIGH and LOW output. The circuit shown may be used to obtain LOW output curves for other values of V_{P2} .

Note: When operating with high output current levels, the maximum power rating must not be exceeded.



OUTPUT BUFFER DESCRIPTION (continued)

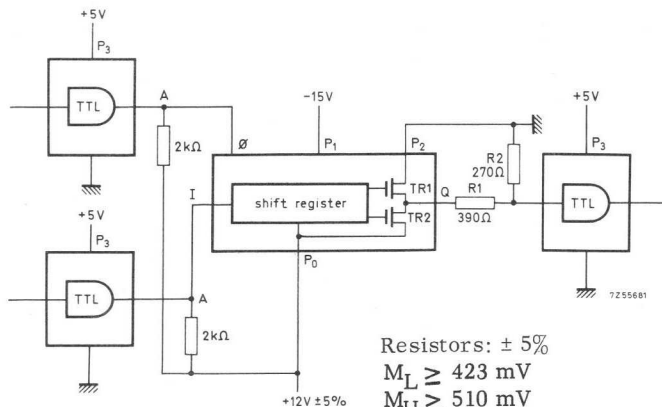
2. Biasing circuit A may be used to drive TTL or DTL loads direct. The MOS input logic levels must be referenced to V_{P0} . TR1 and TR2 are the push-pull output driver transistors of the FDN206.



$M_L \geq 368 \text{ mV}$
 $M_H \geq 458 \text{ mV}$
 Steady HIGH state
 dissipation $\leq 13 \text{ mW}$

Biasing circuit A

3. Biasing circuit B allows the MOS device to be interfaced with TTL or DTL at both input and output using only passive interface components. Note that the TTL or DTL integrated circuit must be able to withstand +10 V applied to the output lead (point A); most non- R_C type circuits of our FC series and most FJ gates satisfy this requirement. Some open collector FJ gates have a minimum output break-down voltage guarantee of 15 V (FJH301; FJH311; FJH321).

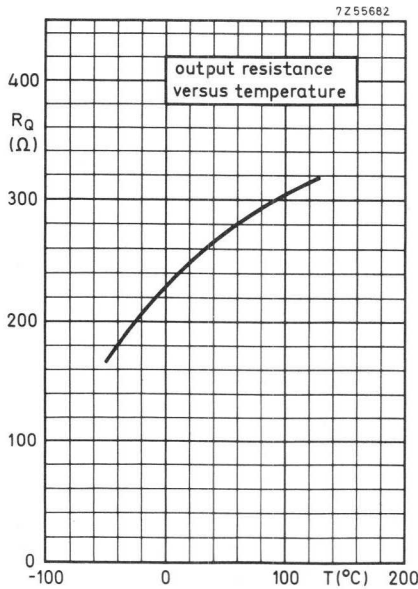
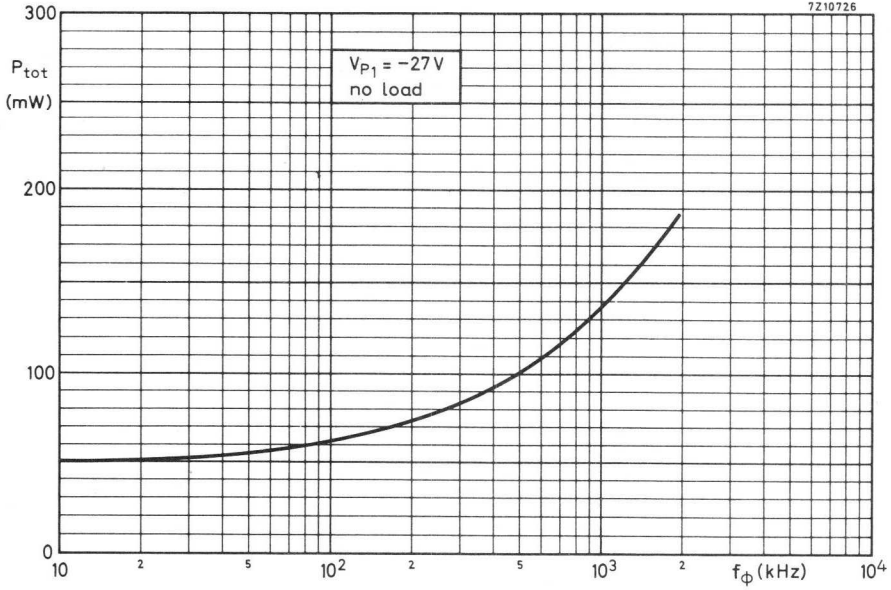


Resistors: $\pm 5\%$
 $M_L \geq 423 \text{ mV}$
 $M_H \geq 510 \text{ mV}$
 Steady HIGH state
 dissipation $\leq 55 \text{ mW}$

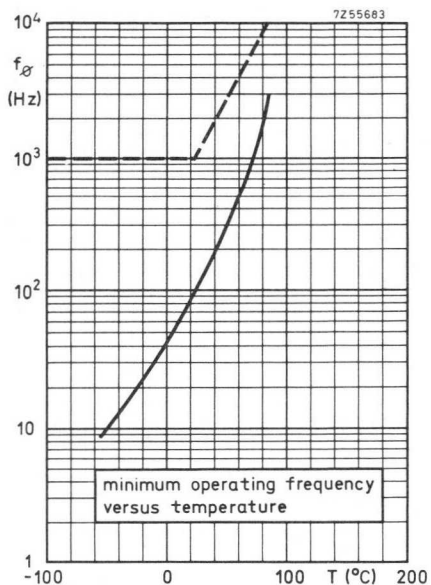
Biasing circuit B

4. To drive MOS loads direct, the bias V_{P0} should be between -12 and -14 V to P_0 .

TYPICAL PERFORMANCE

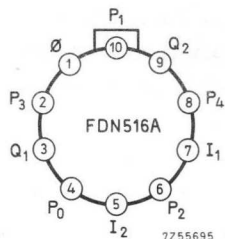
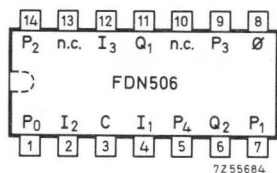
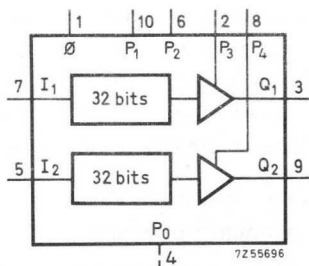
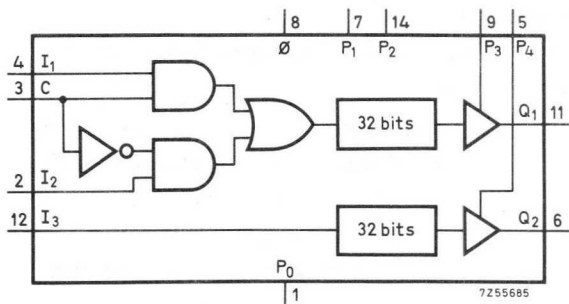


TYPICAL PERFORMANCE (continued)



The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

DUAL 32-BIT STATIC REGISTER



P₀ connected to the metal bottom

P₀ connected to the metal case

QUICK REFERENCE DATA

| | | | |
|-------------------------------------------------------|---------------------------------|------------|------|
| Supply voltages | V _{P1} | -24 to -28 | V |
| | V _{P2} | -12 to -14 | V |
| Clock frequency | f _φ | 0 to 1.5 | MHz |
| Power consumption per bit at f _φ = 1.5 MHz | P _{av} | typ. | 2 mW |
| Operating ambient temperature | T _{amb} | -55 to +85 | °C |
| D.C. noise margin | M _H , M _L | > | 1 V |

PACKAGE OUTLINE: FDN506; 14 lead ceramic dual in-line (See General Section)
FDN516A; TO-100 (See General Section)

GENERAL DESCRIPTION

The FDN506 and FDN516A are dual 32-bit static shift registers. They require a single phase, low voltage, external clock signal, and may be operated down to d. c. without loss of stored information. Both devices utilize common power and clock lines; the output buffer supplies are separated to facilitate independent biasing for MOS or TTL load drive.

The FDN506 contains the gating, external SELECT command and data inputs for selection of two independent data streams.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | |
|-------------------------------------------------------------------------------------------------------------|-------------------------------------|----------------|
| Voltages on all data inputs, clock inputs, outputs and supply terminals with reference to P ₀ | | +0.5 to -30 V |
| Power dissipation up to T _{amb} = 25 °C | { FDN506 P _{tot} | max. 800 mW |
| | { FDN516A P _{tot} | max. 625 mW |
| Junction temperature | T _j | max. 150 °C |
| Storage temperature | T _{stg} | -65 to +150 °C |
| Total current through terminals P ₃ , P ₄ | -I _{p3} , -I _{p4} | max. 40 mA |
| Output current (per output) | ±I _Q | max. 20 mA |

THERMAL RESISTANCE

| | | | |
|--------------------------|-----------------------------|---|----------|
| From junction to ambient | FDN506 R _{th j-a} | = | 156 °C/W |
| | FDN516A R _{th j-a} | = | 200 °C/W |

CHARACTERISTICS at $T_{amb} = -55$ to $+85$ °C

| | Symbol | min. | typ. | max. | Conditions and references |
|--------------------------------|--------------------------|------|------|--------------|----------------------------------------------------------|
| Clock rate | f_{ϕ} | 0 | - | 1.5 MHz | See timing diagram for parameter definitions See note |
| Clock pulse width | $t_{\phi H}$ | 0.24 | - | 50 μ s | |
| Clock pulse fall time | $t_{\phi HL}$ | - | - | 0.10 μ s | |
| Clock pulse rise time | $t_{\phi LH}$ | - | - | 1.0 μ s | |
| Clock pulse space | $t_{\phi L}$ | 0.36 | - | - μ s | |
| Clock pulse voltage level | | | | | |
| HIGH | $V_{\phi H}$ | -2 | 0 | +0.3 V | |
| LOW | $V_{\phi L}$ | -28 | -12 | -9 V | |
| Data/select input logic levels | | | | | |
| HIGH | V_{IH}, V_{CH} | -2 | 0 | +0.3 V | |
| LOW | V_{IL}, V_{CL} | -28 | -12 | -9 V | |
| Data/select lead time | $t_{\ell I}, t_{\ell C}$ | 50 | - | - | |
| Data/select hold time | t_{hI}, t_{hC} | 100 | - | - | |

Note:

The fall time specified for the FDN506 and FDN516A is to ensure that output data will meet the input hold time requirements of other registers, when more shift registers are operating in series from a common clock. If a register does not drive other registers the clock fall times may be longer.

CHARACTERISTICS (continued)

Test conditions: $V_{P1} = -24 \text{ V to } -28 \text{ V}$; $V_{P2} = V_{P3} = V_{P4} = -12 \text{ V to } -14 \text{ V}$;
 $T_{\text{amb}} = -55 \text{ to } +85 \text{ }^\circ\text{C}$; $P_0 = \text{grounded}$; standard load: 50 pF
in parallel with $20 \text{ k}\Omega$ to P_0 .

| | Symbol | min. | typ. | max. | Conditions and references |
|---------------------------------|--------------------|------|------|-------------------|-----------------------------------------------------------------------------------------------------------------|
| <u>ELECTRICAL DATA</u> | | | | | |
| Output levels | | | | | |
| HIGH | V_{QH} | -0.5 | - | 0 V | |
| LOW | V_{QL} | -14 | - | -10 V | |
| Data/select input capacitance | C_I, C_C | - | 2 | 3.5 pF | bias: $V_I = V_C = 0 \text{ V}$; $f = 1 \text{ MHz}$ |
| Clock input capacitance | C_ϕ | - | 6 | 8 pF | bias: $V_\phi = 0 \text{ V}$; $f = 1 \text{ MHz}$ |
| <u>Leakage currents</u> | | | | | |
| Data/select input currents | $-I_{IL}, -I_{CL}$ | - | - | 1 μA | $V_I = V_C = -15 \text{ V}$; all other terminals at V_{P0} ; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ |
| Clock input current | $-I_{\phi L}$ | - | - | 100 μA | $V_\phi = -28 \text{ V}$; all other terminals at V_{P0} ; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ |
| <u>Output resistance</u> | | | | | |
| HIGH | R_{QH} | - | 360 | 600 Ω | $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ |
| LOW | R_{QL} | - | 220 | 500 Ω | $V_{P3} = V_{P4} = -5 \text{ V}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ |
| | R_{QL} | - | 330 | - Ω | $V_{P3} = V_{P4} = -10 \text{ V}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ |
| Drive capability (See note 1) | V_{QL} | - | -10 | -8 V | $R_L = 4 \text{ k}\Omega$ to reference P_0 |
| Supply current (See note 2) | V_{QL} | - | -4.7 | -4.4 V | $V_{P3} = V_{P4} = -5 \text{ V}$; $R_L = 4 \text{ k}\Omega$ to reference P_0 |
| | $-I_{P2}$ | - | 4.0 | 6.0 mA | $V_{P2} = -13 \text{ V}$; $f = 1.5 \text{ MHz}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ |
| | $-I_{P1}$ | - | 3.0 | 4.5 mA | $V_{P1} = -26 \text{ V}$; $f = 1.5 \text{ MHz}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ |
| <u>Output transition times:</u> | | | | | |
| fall time | t_{THL} | - | 80 | - ns | |
| rise time | t_{TLH} | - | 80 | - ns | |
| Delay times: fall time | t_{DHL} | - | 260 | - ns | |
| rise time | t_{DLH} | - | 260 | - ns | |
| D.C. noise margin | M_L | 1.0 | - | - V | |
| | M_H | 1.5 | - | - V | |

Note 1

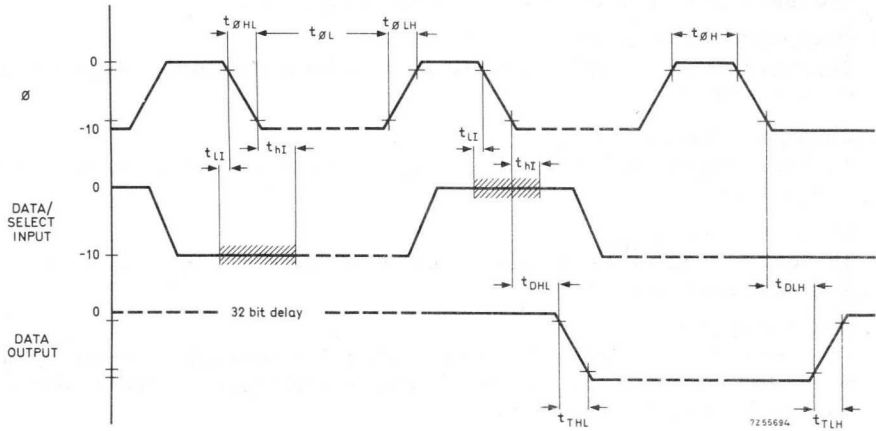
The maximum capacitive load that can be driven depends only on the speed desired and the power dissipation allowable. See the output buffer description on pages 5 and 6 for further information on output drive capability.

Note 2

The output buffer power supply current is almost entirely dependent on the external load.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Notes:

1. Clock pulse ϕ is normally kept LOW.
2. The data and select inputs must remain valid for the shaded interval to ensure proper selection and entry of input data.
3. Data is kept in the register for arbitrarily long periods by keeping the clock LOW.

CHARACTERISTICS (continued)

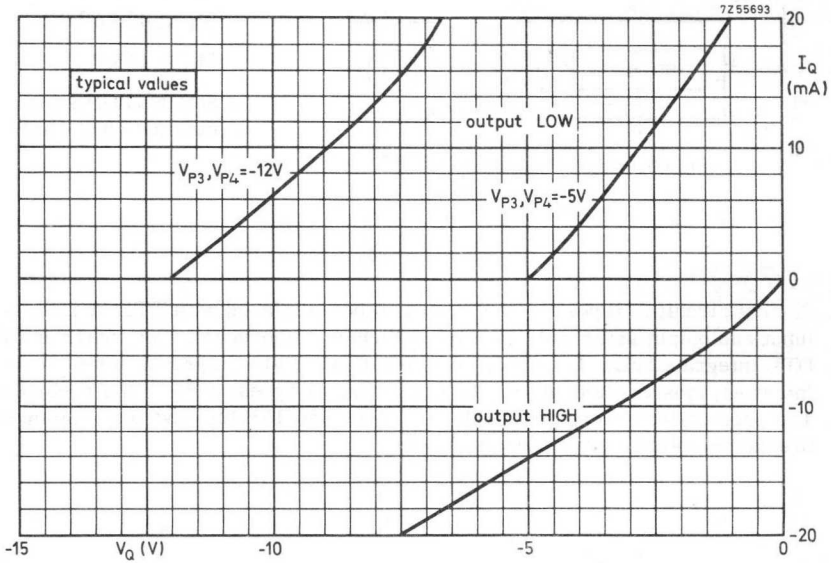
GLOSSERY OF TERMS

1. Clock pulse width: $t_{\phi H}$
The time for which the clock pulse is HIGH: $V_{\phi H} \geq -2 V$
2. Clock pulse fall time: $t_{\phi HL}$
The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock pulse space: $t_{\phi L}$
The least allowable time between the end of one clock pulse (ϕ) and the start of the next, measured at $-9 V$.
5. Data lead time: $t_{\ell L}$
The time before the $-2 V$ point on the clock pulse for which the voltage at the data/select input must be at its specified logic level in order to ensure that the data will be entered in the register.
6. Data hold time: t_{hL}
The time after the clock pulse ϕ reaches LOW ($-9 V$) for which the data/select inputs must remain stable in order to ensure that the data will be entered in the register.
7. Output fall transition time: t_{THL}
The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
8. Output rise transition time: t_{TLH}
The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
9. Fall delay time: t_{DHL}
The delay between the clock pulse ϕ reaching LOW and the output beginning to change from HIGH to LOW.
10. Rise delay time: t_{DLH}
The delay between the clock pulse ϕ reaching LOW and the output beginning to change from LOW to HIGH.

OUTPUT BUFFER DESCRIPTION

1. The curves below are typical output buffer voltage-current characteristics for the FDN506 and FDN516A.

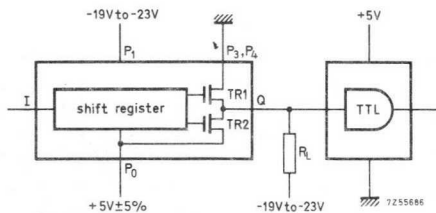
The output buffer supply voltages may be varied between 0 and -14 V according to the output voltage swing required. It does not affect the operating speed of the register.

Note

When operating with high output current levels, the maximum power rating must not be exceeded.

OUTPUT BUFFER DESCRIPTION (continued)

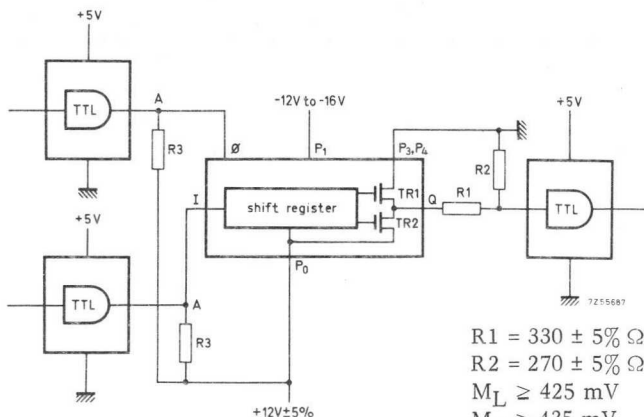
2. Biasing circuit A may be used to drive TTL or DTL loads direct. The MOS input logic levels must be referenced to V_{P0} . TR1 and TR2 are the push-pull output driver transistors of the FDN506 and FDN516A.



$R_L = 22 \pm 5\% \text{ k}\Omega$
 $M_L \geq 450 \text{ mV}$
 $M_H \geq 1.5 \text{ V}$
 Steady HIGH state
 dissipation $< 1 \text{ mW}$

Biasing circuit A

3. Biasing circuit B allows the MOS device to be interfaced with TTL or DTL at both input and output using only passive interface components. Note that the TTL or DTL integrated circuit must be able to withstand +12 V applied to the output lead (point A), most circuits of our FC series (non- R_C types) satisfy this requirement. The open collector FJ gates FJH301, FJH311 and FJH321 have a minimum output breakdown voltage guarantee of 15 V.



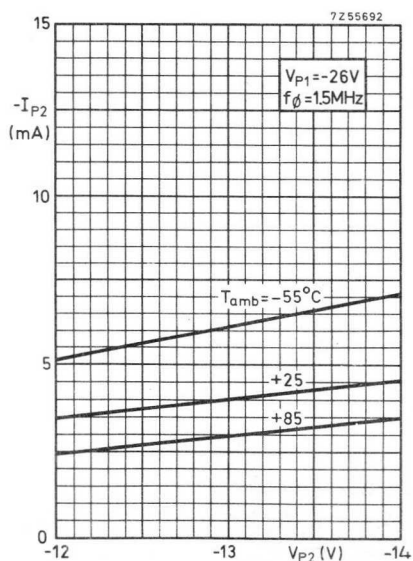
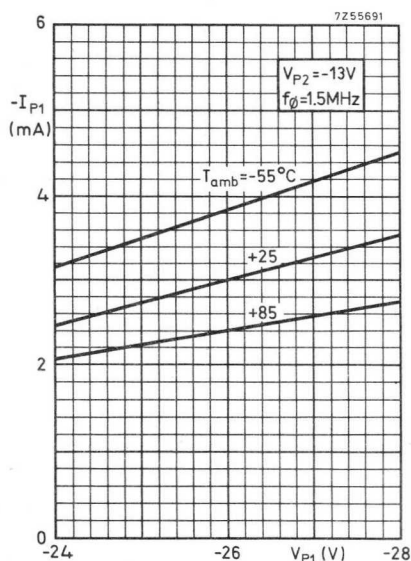
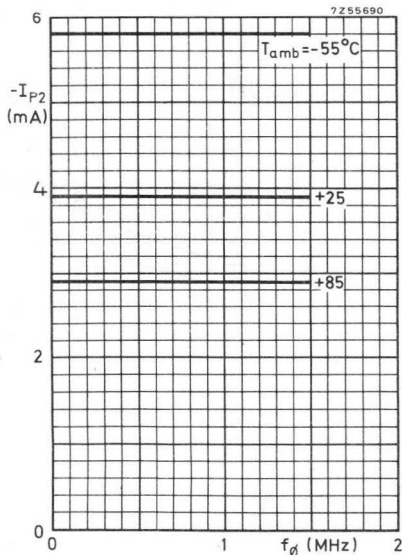
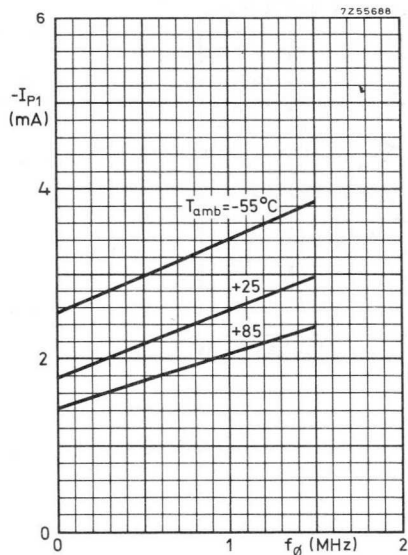
$R_1 = 330 \pm 5\% \Omega$
 $R_2 = 270 \pm 5\% \Omega$
 $M_L \geq 425 \text{ mV}$
 $M_H \geq 435 \text{ mV}$
 Steady HIGH state
 dissipation $\leq 63 \text{ mW}$

Biasing circuit B

4. To drive MOS loads direct, the bias V_{P3} and V_{P4} should be between -12 and -14 V to P_0 .

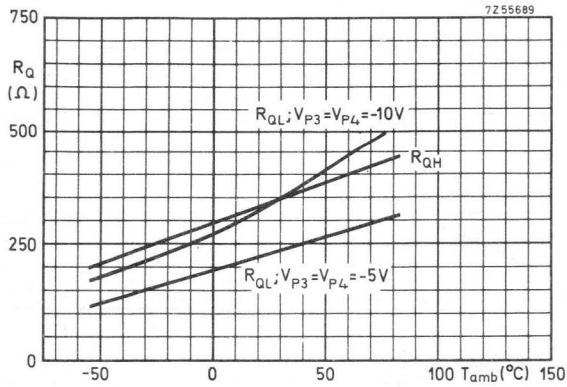
TYPICAL PERFORMANCE at $P_0 =$ grounded; standard load : 50 pF in parallel with 20 k Ω to P_0 .

Test condition: $V_{P1} = -26$ V; $V_{P2} = -13$ V



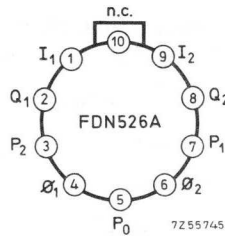
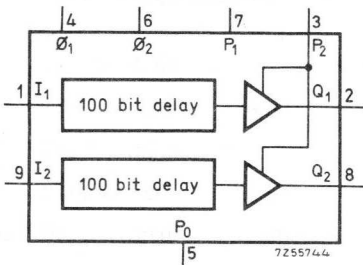
TYPICAL PERFORMANCE (continued)

Test conditions: $P_0 = \text{grounded}$; $V_{P1} = -26 \text{ V}$; $V_{P2} = -13 \text{ V}$



The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

DUAL 100-BIT STATIC SHIFT REGISTER



P₀ connected to metal case

QUICK REFERENCE DATA

| | | | |
|----------------------------------------------------|------------|------------|-------------|
| Clock rate | f_{ϕ} | 0 to 3 | MHz |
| Supply voltage | V_{P1} | -24 to -28 | V |
| Power consumption per bit at $f_{\phi} = 3$ MHz | P_{av} | typ. 2 | mW |
| Operating ambient temperature | T_{amb} | -55 to +85 | $^{\circ}C$ |
| D. C. noise margin | M_H, M_L | > 1 | V |

PACKAGE OUTLINE: TO-100 (See General Section)

GENERAL DESCRIPTION

The FDN526A is a monolithic dual 100-bit shift register. The two shift registers have each one serial input and output. They operate from common clocks and supply lines. The device has low impedance push-pull output buffers, which, when appropriately biased, are capable of interfacing direct with MOS, TTL, DTL and other loads. The buffer supply terminal P₂ is a separate supply which determines the output LOW signal only. This provides an output level that is independent of supply voltage V_{P1}, the amplitude and width of the clock pulses. All inputs, outputs, supply terminals and clock inputs are protected against static voltages.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|------------------------------------------------------------------------------------------------------------|------------------|-------------|----|
| Voltage on all data inputs, clock inputs, outputs and supply terminals with reference to P ₀ | | +0.5 to -30 | V |
| Power dissipation up to T _{amb} = 25 °C | P _{tot} | max. 625 | mW |
| Junction temperature | T _j | max. 150 | °C |
| Storage temperature | T _{stg} | -65 to +150 | °C |
| Total current through terminal P ₂ | -I _{P2} | max. 40 | mA |
| Output current (per output) | ±I _Q | max. 20 | mA |

THERMAL RESISTANCE

| | | | | |
|--------------------------|---------------------|---|-----|------|
| From junction to ambient | R _{th j-a} | = | 200 | °C/W |
|--------------------------|---------------------|---|-----|------|

DRIVE REQUIREMENTS at $T_{amb} = -55$ to $+85^{\circ}\text{C}$; $P_0 = \text{grounded}$

| | Symbol | min. | typ. | max. | Conditions and references | |
|---------------------------------|--------------------------------------|------|------|------|---------------------------|-------------------------------------|
| Clock rate | f_{ϕ} | 0 | - | 2 | MHz | $V_{P1}, V_{\phi L} = -24\text{ V}$ |
| | | 0 | - | 3 | MHz | $V_{P1}, V_{\phi L} = -26\text{ V}$ |
| Clock pulse width ¹⁾ | $t_{\phi 1L}$ | 0.2 | - | 10 | μs | $V_{P1}, V_{\phi L} = -24\text{ V}$ |
| | | 0.1 | - | 10 | μs | $V_{P1}, V_{\phi L} = -26\text{ V}$ |
| | $t_{\phi 2L}$ | 0.2 | - | - | μs | $V_{P1}, V_{\phi L} = -24\text{ V}$ |
| | | 0.15 | - | - | μs | $V_{P1}, V_{\phi L} = -26\text{ V}$ |
| Clock pulse rise time | $t_{\phi LH}$ | - | - | 0.5 | μs | |
| Clock pulse fall time | $t_{\phi HL}$ | - | - | 0.5 | μs | |
| Clock delay | $t_{\phi 1\phi 2}, t_{\phi 2\phi 1}$ | 0 | - | - | μs | |
| Clock pulse voltage levels | | | | | | |
| HIGH | $V_{\phi H}$ | -2 | - | +0.3 | V | |
| LOW | $V_{\phi L}$ | -28 | -26 | -24 | V | |
| Data input logic levels | | | | | | |
| HIGH | V_{IH} | -2.0 | 0 | +0.3 | V | |
| LOW | V_{IL} | -28 | -12 | -9 | V | |
| Data lead time | $t_{\ell I}$ | 20 | - | - | ns | |

¹⁾ See timing diagram on page 5.

CHARACTERISTICS

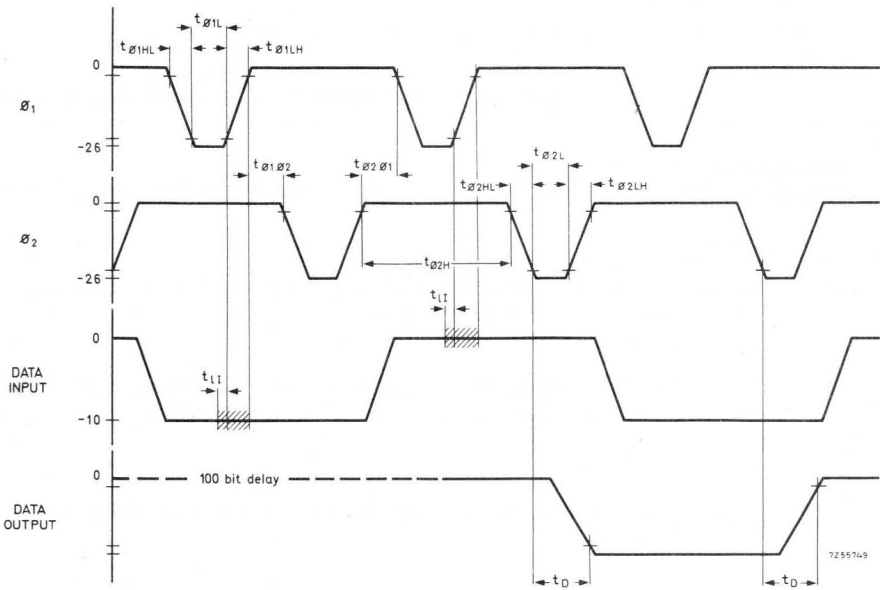
Test conditions: $V_{P1} = -24$ to -28 V; $V_{P2} = -12$ to -14 V; $T_{amb} = -55$ to $+85$ °C;
 P_0 = grounded; standard load: 25 pF in parallel with 20 k Ω to P_0 .

| | Symbol | min. | typ. ¹⁾ | max. | Conditions and references |
|--------------------------|--------------------------|------|--------------------|--------------|-----------------------------------------------------------------------------------------------------------------------------|
| <u>Output levels</u> | | | | | |
| HIGH | V_{QH} | -1 | - | 0 V | |
| LOW | V_{QL} | -14 | - | -10 V | |
| Data input capacitance | C_I | - | 2 | 3.5 pF | $V_I = 0$ V; $f = 1$ MHz |
| Clock input capacitances | $C_{\phi 1}, C_{\phi 2}$ | - | 17 | 25 pF | $V_{\phi} = 0$ V; $f = 1$ MHz |
| | $C_{\phi 1}, C_{\phi 2}$ | - | 15 | 22 pF | $V_{\phi} = -26$ V; $f = 1$ MHz |
| <u>Leakage currents</u> | | | | | |
| Data input current | $-I_{IL}$ | - | - | 1 μ A | $\left\{ \begin{array}{l} V_I = -15$ V; $T_{amb} = 25$ °C \\ \text{all other terminals at } V_{P0} \end{array} \right. |
| Clock input current | $-I_{\phi L}$ | - | - | 100 μ A | $\left\{ \begin{array}{l} V_{\phi} = -28$ V; $T_{amb} = 25$ °C \\ \text{all other terminals at } V_{P0} \end{array} \right. |
| <u>Output resistance</u> | | | | | |
| HIGH | R_{QH} | - | 400 | 750 Ω | $V_Q = -1$ V |
| Drive capability | V_{QL} | - | -11.3 | -8 V | $R_L = 4$ k Ω to P_0 ; $V_{P2} = -5$ V |
| <u>Supply currents</u> | | | | | |
| | $-I_{P1}$ | - | 1.1 | 1.8 mA | $\left\{ \begin{array}{l} V_{P1} = -26$ V; $f = 1$ MHz \\ $T_{amb} = 25$ °C; $R_L = 1$ M Ω \end{array} \right. |
| | $-I_{P2}$ | - | 9.3 | 18 mA | $\left\{ \begin{array}{l} V_{P2} = -13$ V; $f = 1.5$ MHz \\ $T_{amb} = 25$ °C; $R_L = 1$ M Ω \end{array} \right. |
| <u>Delay times</u> | | | | | |
| Clock to output | t_D | - | 150 | 275 ns | |
| D.C. noise margin | M_H, M_L | 1 | - | - V | |

¹⁾ Typical values measured at: $V_{P1} = -26$ V; $V_{P2} = -13$ V; $V_{\phi L} = -26$ V; $T_{amb} = 25$ °C.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Notes

1. Data inputs must remain valid for the shaded interval to ensure proper entry into the register.
2. For d.c. operation ϕ_2 should be kept LOW.

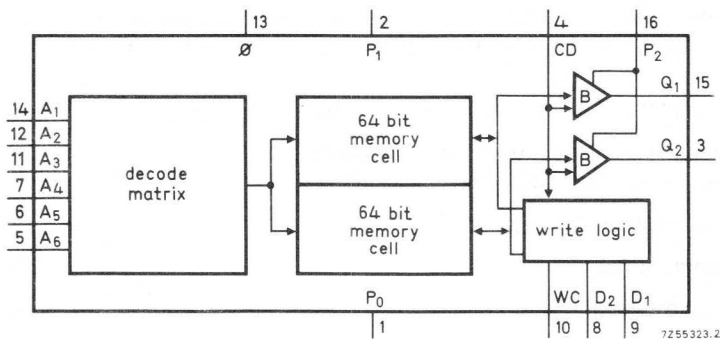
CHARACTERISTICS (continued)

GLOSSARY OF TERMS

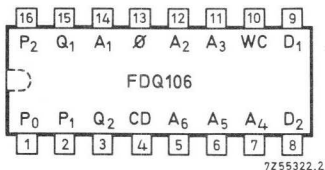
1. Clock pulse width: $t_{\phi L}$
The time for which the clock pulse is LOW: $V_{\phi L} = -26 \text{ V}$
2. Clock pulse space: $t_{\phi 2H}$
The time for which the clock pulse ϕ_2 is HIGH ($V_{\phi} > -2 \text{ V}$).
3. Clock pulse fall time: $t_{\phi HL}$
The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
4. Clock pulse rise time: $t_{\phi LH}$
The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
5. Clock delay time: $t_{\phi 1\phi 2}$, $t_{\phi 2\phi 1}$
The least allowable time between the end of the ϕ_1 (or ϕ_2) clock pulse and the start of the ϕ_2 (or ϕ_1) clock pulse, defined at -2 V .
6. Data lead time: $t_{\ell I}$
The time before the 90% point on the clock pulse for which the voltage at the data input must be at its specified logic level in order to ensure that the data will be entered in the register.
7. Delay time: t_D
The delay between the clock pulse reaching LOW and the output reaching its logic level.

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

READ/WRITE RANDOM ACCESS MEMORY, 128-BIT, 64 WORD, 2 BITS PER WORD



WC = write control; CD = chip disable



P₀ and metal package bottom are connected

QUICK REFERENCE DATA

| | | |
|----------------------------------------------|--------------------|---------------|
| Supply voltage | V _{P1} | -26 to -28 V |
| Standby power per bit (required clock power) | | typ. 3 μW |
| Total power consumption at 1 MHz read-rate | P _{tot} | typ. 135 mW |
| Read access time | t _{AR} | < 1 μs |
| D.C. noise margin | M _{L, MH} | > 1 V |
| Data read rate | f _{DR} | < 1 MHz |
| Data write rate | f _{DW} | < 1 MHz |
| Operating ambient temperature | T _{amb} | -55 to +85 °C |

PACKAGE OUTLINE: 16 lead metal-ceramic dual in-line (See general section)

GENERAL DESCRIPTION

The FDQ106 is a monolithic, 128 bit random access read/write memory. It is organized as two 64 bit memories with 6 common single-rail address inputs and two separate outputs; it is used as a 64 word, 2-bits per word memory. It requires a single-phase clock strobe pulse to refresh the data stored in all the memory cells simultaneously and to change the data stored in a cell in the write mode.

It also incorporates a chip disable that inhibits both data inputs and output buffers for expanded memory applications. The memory is activated in the write mode by applying a write control pulse; at all other times it is in the read mode.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|----------------------------------------------------------------------------------------------------------|------------------|-------------|--------|
| Voltage on all data inputs, clock inputs, outputs and supply terminals, with reference to P ₀ | | +0.5 to -30 | V |
| Power dissipation up to T _{amb} = 25 °C | P _{tot} | max. | 800 mW |
| Junction temperature | T _j | max. | 150 °C |
| Storage temperature | T _{stg} | -65 to +150 | °C |
| Total current through terminal P ₂ | -I _{P2} | max. | 40 mA |
| Output current (per output) | ±I _Q | max. | 20 mA |

THERMAL RESISTANCE

| | | | |
|--------------------------|---------------------|---|----------|
| From junction to ambient | R _{th j-a} | = | 156 °C/W |
|--------------------------|---------------------|---|----------|

CHARACTERISTICS at $T_{amb} = -55$ to $+85$ °C

| | Symbol | min. | typ. | max. | Conditions and references |
|-------------------------------------------------------------|---------------------------|------|------|-------------|------------------------------------------------|
| Data read rate | f_{DR} | - | - | 1 MHz | { see timing diagram for parameter definitions |
| Data write rate | f_{DW} | - | - | 1 MHz | |
| Strobe rate | f_{ϕ} | 0.01 | - | 1 MHz | |
| Strobe pulse width | $t_{\phi H}$ | 0.08 | - | 5 μs | |
| Write control pulse width | t_{WL} | 0.5 | - | 10 μs | |
| Write control and strobe pulse rise time: { fall time: { | t_{WLH} | - | - | 0.1 μs | |
| | $t_{\phi LH}$ | - | - | 0.1 μs | |
| | t_{WHL} | - | - | 0.1 μs | |
| | $t_{\phi HL}$ | - | - | 0.1 μs | |
| Write control and strobe pulse voltage levels: | | | | | |
| HIGH | $V_{WH}; V_{\phi H}$ | -2 | 0 | +0.3 V | |
| LOW | $V_{WH}; V_{\phi L}$ | -28 | -27 | -26 V | |
| Address, data, and chip disable input logic levels: | | | | | |
| HIGH | V_{AH}, V_{DH}, V_{CDH} | -2 | 0 | +0.3 V | |
| LOW | V_{AL}, V_{DL}, V_{CDL} | -28 | -12 | -9 V | |
| Write address lead time | t_{lWA} | 0.35 | - | - μs | |
| Strobe address lead time | $t_{l\phi A}$ | 0.76 | - | - μs | |
| Strobe write lead time | $t_{lW\phi HL}$ | 0.40 | - | - μs | |



CHARACTERISTICS (continued)

Test conditions: $V_{P1} = -26 \text{ V to } -28 \text{ V}$; $V_{P2} = -12 \text{ V to } -14 \text{ V}$; $T_{amb} = -55 \text{ to } +85^\circ\text{C}$;
 $P_0 = \text{grounded}$; standard load: 50 pF in parallel with 50 k Ω to P_0 .

| | Symbol | min. | typ. | max. | Conditions and references |
|--------------------------------------------|------------------------------|------|------|------|------------------------------------------------------------------------------------------|
| <u>ELECTRICAL DATA</u> | | | | | |
| Read access time | t_{AR} | 0.2 | 0.5 | 1.0 | μs |
| Data output logic levels | | | | | |
| HIGH | V_{QH} | -1.0 | - | 0 | V |
| LOW | V_{QL} | -14 | - | -10 | V |
| Address and data input capacitance | C_A, C_D | - | 4.5 | 6.0 | pF bias: $V_A; V_D = 0 \text{ V}$; $f_\phi = 1 \text{ MHz}$ |
| Chip disable input capacitance | C_{CD} | - | 7.0 | 9.0 | pF bias: $V_{CD} = 0 \text{ V}$; $f_\phi = 1 \text{ MHz}$ |
| Strobe input capacitance | C_ϕ | - | 56 | 68 | pF bias: $V_\phi = 0 \text{ V}$; $f_\phi = 1 \text{ MHz}$ |
| | C_ϕ | - | 28 | 35 | pF bias: $V_\phi = -26 \text{ V}$; $f_\phi = 1 \text{ MHz}$ |
| Write control input capacitance | C_W | - | 7.9 | 9.2 | pF bias: $V_{WC} = 0 \text{ V}$; $f_\phi = 1 \text{ MHz}$ |
| | C_W | - | 5.8 | 7.0 | pF bias: $V_{WC} = -26 \text{ V}$; $f_\phi = 1 \text{ MHz}$ |
| Data output capacitance | C_Q | - | 3.5 | 4.5 | pF bias: $V_Q = 0 \text{ V}$; $f_\phi = 1 \text{ MHz}$ |
| <u>Leakage currents:</u> | | | | | |
| Address, data, chip disable input currents | $-I_{AL}, -I_{DL}, -I_{CDL}$ | - | - | 1 | μA { bias: $V_A; V_D; V_{CD} = -15 \text{ V}$; see note 2 |
| Strobe and write control input currents | $-I_{\phi L}, -I_{WL}$ | - | - | 100 | μA { bias: $V_\phi; V_{WC} = -28 \text{ V}$; all see note 2 |
| Output leakage current | $-I_Q$ | - | - | 10 | μA ($V_Q = 10 \text{ V}$; $CD = \text{LOW}$ $T_{amb} = 25^\circ\text{C}$ |
| <u>Output resistances:</u> | | | | | |
| HIGH | R_{QH} | - | 250 | 600 | Ω $V_{P2} = -5 \text{ V}$ |
| LOW | R_{QL} | - | 250 | 600 | Ω $V_{P1} = -28 \text{ V}$ |
| Power supply current | | | | | |
| <u>drain:</u> at V_{P1} | $-I_{P1}$ | - | 4.5 | 7.5 | mA $f_\phi = 1 \text{ MHz}$ $T_{amb} = 25^\circ\text{C}$ |
| at V_{P2} (see note 1) | $-I_{P2}$ | - | 0.8 | 1.0 | mA $f_\phi = 1 \text{ MHz}$ $T_{amb} = 25^\circ\text{C}$ |
| <u>Output transition times:</u> | | | | | |
| fall time | t_{THL} | - | 100 | - | ns |
| rise time | t_{TLH} | - | 100 | - | ns |
| D. C. noise margin | M_L, M_H | 1 | - | - | V |

Notes

- I_{P2} is almost entirely dependent on the external load.
- $T_{amb} = 25^\circ\text{C}$; all other terminals at V_{P0}

CHARACTERISTICS (continued)STAND-BY POWER CONSIDERATIONS

If the FDQ106 is to be kept in stand-by condition with all d. c. power to it shut off, the stored data can be preserved by maintaining a 10 kHz strobe clock rate.

Since essentially all d. c. power dissipation is in the address input inverters, decode circuits and output buffers, the power required to preserve the stored data is limited to reactive strobe power and whatever leakage current occurs at the strobe input lead. Since the reactive strobe power is frequency dependent, the lowest allowable frequency should be used for stand-by operation. A strobe frequency of less than 10 kHz may be used if the ambient temperature is less than +85 °C.

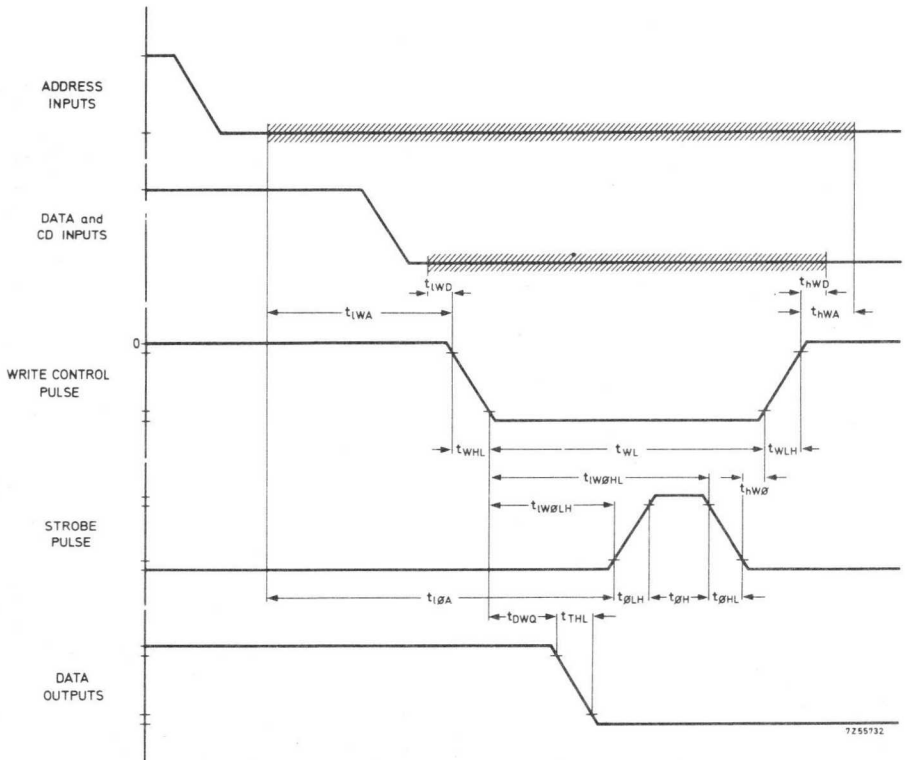
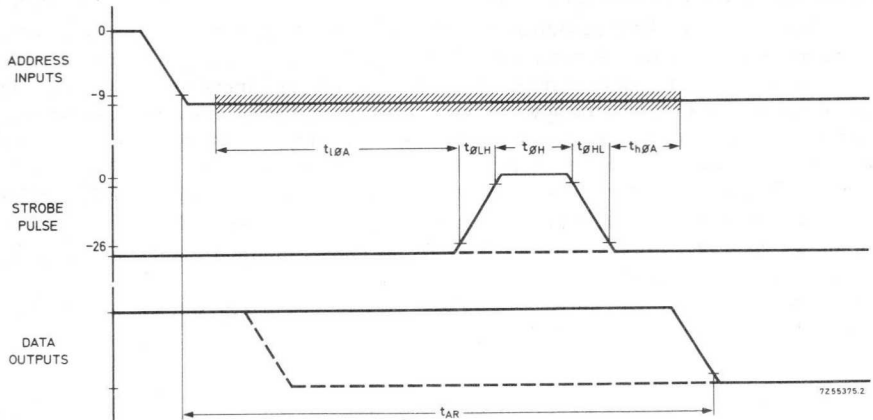
D.C. power may be switched on and off only at those moments when a change of address is also allowable.

After re-application of d. c. power, a series of about 10 strobe pulses is required before the circuit is fully operational.



CHARACTERISTICS (continued)

TIMING DIAGRAM



CHARACTERISTICS (continued)

Timing diagram notes

1. To avoid destroying data in non-addressed memory cells, the address inputs must not be made to change state during the shaded intervals in the timing diagrams.
2. When the CD input is LOW, the WRITE logic is inoperative and the output is floating. The CD input affects the output directly, with a propagation delay of about 100 ns. It may change state any time except during the shaded interval in the timing diagram.
3. No strobe pulse is required during a READ cycle; however, a minimum strobe frequency of 10 kHz is required and strobe pulses may occur during READ cycles if the requirement of note 1 is observed.
4. To write into the device, a WRITE control pulse and a strobe pulse are required, and the CD input must be HIGH.
During a WRITE cycle the memory outputs are active and the new data will appear at the outputs after $t_{DWQ} (\leq 200 \text{ ns})$.
However, data is actually written into the memory cell by the trailing edge of the strobe pulse.
5. Whether they are in READ or WRITE cycles, all memory cells are simultaneously refreshed during a strobe pulse. No cycling through addresses is required.
6. If the address inputs remain unchanged, the data outputs appear as d.c. levels, no return to zero.

GLOSSARY OF TERMS

1. Strobe pulse width: $t_{\phi H}$
The time for which the strobe pulse is in the HIGH state (ϕ is nominally LOW)
2. Write control pulse width: t_{WL}
The time for which the WRITE control pulse is LOW ($V_{WL} \leq -26 \text{ V}$)
3. Pulse fall time: $t_{\phi HL}$ and $t_{\phi HL}$
The time between the 10% and 90% voltage points as the pulse goes from HIGH to LOW.
4. Pulse rise time: $t_{\phi LH}$ and $t_{\phi LH}$
The time between the 90% and 10% voltage points as the pulse goes from LOW to HIGH.
5. Strobe address lead time: $t_{\ell \phi A}$
The time before the 10% strobe pulse voltage point for which the address must be present.
6. Write address lead time: $t_{\ell WA}$
The time before the 10% write control pulse voltage point for which the address must be present.
7. Write data lead time: $t_{\ell WD}$
The time before the 10% write control pulse voltage point for which the data must be present at the data inputs ($t_{\ell WD} \geq 0$)
8. Read access time: t_{AR}
After the address inputs reach the correct level, the time that elapses before the outputs start to change state.

CHARACTERISTICS (continued)

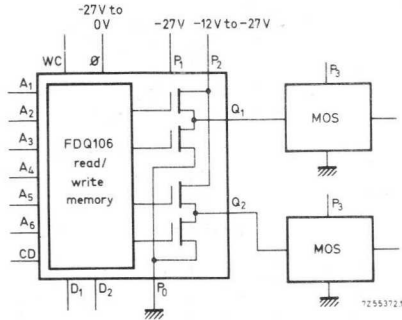
9. Write-pulse-to-output propagation time: t_{DWQ}
After the write control pulse reaches the LOW state, the time that elapses before the outputs start to change state.
10. Output fall transition time: t_{THL}
The time between the 10 % and 90 % voltage points as the output goes from HIGH to LOW.
11. Output rise transition time: t_{TLH}
The time between the 90 % and 10 % voltage points as the output goes from LOW to HIGH.
12. Write address and write data hold times: t_{hWA} and t_{hWD}
The time for which the write control pulse must be in the HIGH state before the address or inputs may change state ($t_{hWA} \geq 0$ and $t_{hWD} \geq 0$).
13. Strobe address hold time: $t_{h\phi A}$
The time for which the strobe pulse must be LOW before the address may change state ($t_{h\phi A} \geq 0$).
14. Write control-strobe pulse lead times: $t_{\ell W\phi LH}$ and $t_{\ell W\phi HL}$
The time before the 10 % voltage point on the strobe pulse leading edge, or the 90 % voltage point on the strobe pulse trailing edge, for which the write control pulse must be in the LOW state ($t_{\ell W\phi LH} \geq 0$; $t_{\ell W\phi HL} \geq 400$ ns).
15. Write control-strobe pulse hold time: $t_{hW\phi}$
The time after the strobe pulse has returned to LOW for which the write control pulse remain LOW ($t_{hW\phi} \geq 0$).

OUTPUT BUFFER DESCRIPTION

The output buffers used on the FDQ106 are identical to these used on the FDN106, FDN116, FDN126 and FDN136 dynamic shift registers. The V_Q versus I_Q characteristics shown in the data sheets for these shift registers also apply, therefore, to the FDQ106. The V_p supply voltage may be varied between 0 and $-28V$ according to the load requirements.

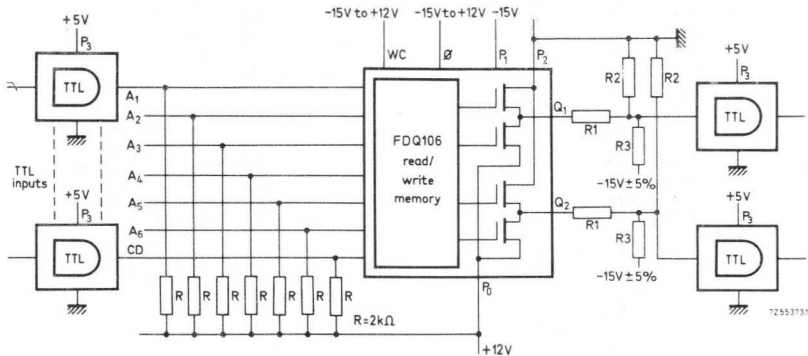
1. Biasing circuit A may be used to drive MOS loads.

Normal MOS input signals must drive the address and other input signals in accordance with the specified electrical characteristics.



Biasing circuit A

2. Biasing circuit B allows the MOS device to be interfaced with TTL or DTL at both data inputs and data outputs. Note that the TTL or DTL integrated circuit must be able to withstand $+12V$ applied to the output lead, most of our FC gates ¹⁾ and FJ gates ¹⁾ satisfy this requirement. Some open collector FJ gates have a minimum output breakdown voltage guarantee of $15V$. ⁽¹⁾ non-RC types

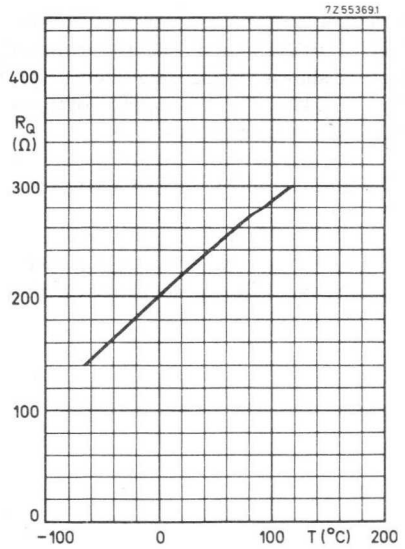
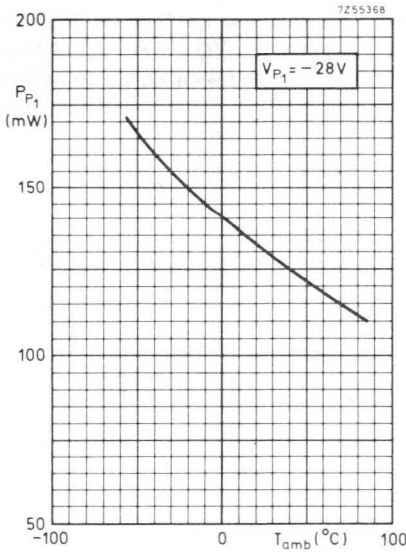


| | |
|---------------------------|--------------------------------------------------------------------------------------------------------------------------|
| Fan-out = 1 | |
| $R1 = 1.2\text{ k}\Omega$ | $\left. \begin{aligned} M_H &= 600\text{ mV} \\ M_L &= 750\text{ mV} \\ P_{HIGH} &= 13\text{ mW} \end{aligned} \right\}$ |
| $R2 = 1\text{ k}\Omega$ | |
| $R3 = 10\text{ k}\Omega$ | |

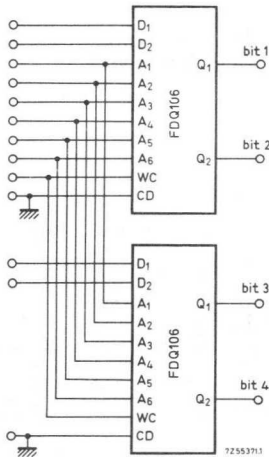
| | |
|---------------------------|--------------------------------------------------------------------------------------------------------------------------|
| Fan-out = 2 | |
| $R1 = 560\ \Omega$ | $\left. \begin{aligned} M_H &= 450\text{ mV} \\ M_L &= 500\text{ mV} \\ P_{HIGH} &= 41\text{ mV} \end{aligned} \right\}$ |
| $R2 = 1\text{ k}\Omega$ | |
| $R3 = 4.7\text{ k}\Omega$ | |

Biasing circuit B

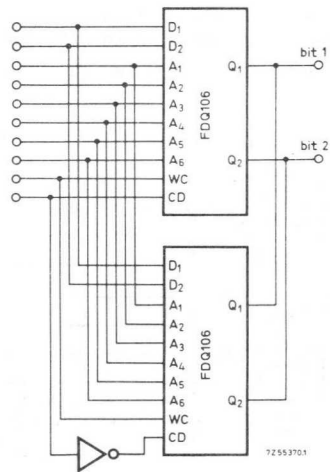
TYPICAL PERFORMANCE



EXPANDED MEMORIES



64 word, 4 bits per word



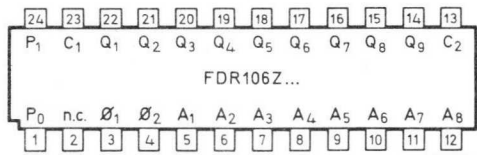
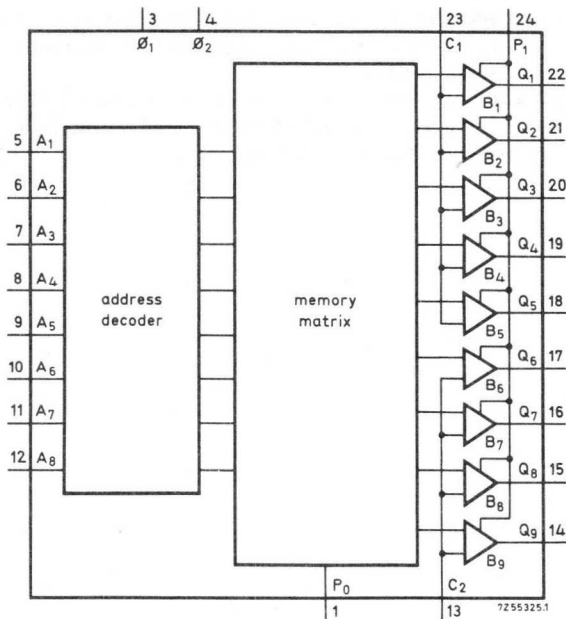
128 word, 2 bits per word

A LOW state at the chip **disable** input will cause both push-pull output buffers to turn off. In the off state, the output impedance of the output transistors becomes very high (approximately 5 MΩ) making it possible to use wired-or configurations with other FDQ106 outputs.

Chip disable also inhibits write, which allows common bussing of data input lines.

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

READ ONLY MEMORY, 256 WORD, 9 BITS PER WORD



QUICK REFERENCE DATA

| | | | |
|-----------------------------------------|------------|------------|--------------|
| Read access time | t_{AR} | max. | 1 μ s |
| Clock rate | f_{ϕ} | max. | 1 MHz |
| Power dissipation at $f_{\phi} = 1$ MHz | P_{ϕ} | typ. | 90 mw |
| D.C. noise margin | M_L, M_H | > | 1 V |
| Operating ambient temperature | T_{amb} | -55 to +85 | $^{\circ}$ C |

PACKAGE OUTLINE 24 lead ceramic dual in-line. (See General Section)

→ GENERAL DESCRIPTION

The FDR106Z is a monolithic 2304 bit read only memory. When ordering an FDR106Z the customer must send a bit pattern matrix (see example on pages 10 to 15) with the desired content. For performance evaluation, we can supply specimens of FDR106Z1, which is identical to the FDR106Z but contains a bit pattern of our own. The FDR106Z requires a two phase clock, but the outputs remain steady as long as the address remains unchanged. The normal configuration is as a 256 word, 9 bits per word, parallel output ROM. However, by means of two output inhibit controls it can be set up for 512 4-bit words.

The memory matrix is programmed with the aid of a mask pattern during manufacture. The only d.c. supply is the output buffer supply, which is variable and can be biased to drive bipolar output loads direct.



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134) ←

| | | | |
|--------------------------------------------------------------------------------------------------|-----------|-------------|--------------------|
| Voltages on all data inputs, clock inputs, outputs and supply terminals, with reference to P_0 | | +0.5 to -30 | V |
| Power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$ | P_{tot} | max. 1 | W |
| Junction temperature | T_j | max. 150 | $^{\circ}\text{C}$ |
| Storage temperature | T_{stg} | -65 to +150 | $^{\circ}\text{C}$ |
| Total current through terminal P_1 | $-I_{P1}$ | max. 40 | mA |
| Output current (per output) | $\pm I_Q$ | max. 20 | mA |

THERMAL RESISTANCE ←

| | | | | |
|--------------------------|---------------|---|-----|-----------------------------|
| From junction to ambient | $R_{th\ j-a}$ | = | 125 | $^{\circ}\text{C}/\text{W}$ |
|--------------------------|---------------|---|-----|-----------------------------|



CHARACTERISTICS at $T_{amb} = -55$ to $+85$ °C

| <u>ELECTRICAL DRIVE REQUIREMENTS</u> | Symbol | min. | typ. | max. | Conditions and references |
|------------------------------------------------------|--------------------|------------------|------|--------------|----------------------------------------------|
| Clock rate | f_{ϕ} | 0.01 | - | 1.0 MHz | |
| Clock pulse width | $t_{\phi 1L}$ | 0.50 | - | 5.0 μs | see timing diagram for parameter definitions |
| | $t_{\phi 2L}$ | 0.35 | - | 5.0 μs | |
| Clock pulse fall time | $t_{\phi HL}$ | - | - | 0.10 μs | see note |
| Clock pulse rise time | $t_{\phi LH}$ | - | - | 0.10 μs | see note |
| Clock delay time | $t_{\phi 1\phi 2}$ | 0 | - | 45 μs | |
| Clock delay time | $t_{\phi 2\phi 1}$ | 0 | - | 45 μs | |
| Clock input voltage level | | | | | |
| | HIGH | $V_{\phi H}$ | -2 | 0 | +0.3 V |
| LOW | $V_{\phi L}$ | -28 | -26 | -24 V | |
| Address input and output inhibit input logic levels: | | | | | |
| | HIGH | V_{AH}, V_{CH} | -2 | 0 | +0.3 V |
| LOW | V_{AL}, V_{CL} | -28 | -12 | -9 V | |

→ Note

At frequencies higher than 800 kHz, $t_{\phi 1Lmin}$ and $t_{\phi 2Lmin}$ will be determined by $t_{\phi LHmax}$ and $t_{\phi HLmax}$.

CHARACTERISTICS

Test conditions: $V_{P1} = -12\text{ V to }-14\text{ V}$; $T_{amb} = -55\text{ to }+85\text{ }^\circ\text{C}$; $P_0 = \text{grounded}$; standard load: 30 pF in parallel with $150\text{ k}\Omega$ to P_0 .

| ELECTRICAL DATA | Symbol | min. | typ. | max. | Conditions and references |
|-------------------------------------------------|--------------------------|------|------|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <u>Output levels:</u> | | | | | |
| HIGH | V_{QH} | -1 | - | 0 V | |
| LOW | V_{QL} | -14 | - | -10 V | |
| Address input capacitance | C_A | - | 3.2 | 4.0 pF | bias: $V_A = 0\text{ V}$; $f_\phi = 1\text{ MHz}$ |
| Output inhibit input capacitance | C_C | - | 5.0 | 6.0 pF | } bias: V_ϕ ; $V_C = 0\text{ V}$; $f_\phi = 1\text{ MHz}$ |
| Clock input capacitance | $C_{\phi 1}$ | - | 15 | 17 pF | |
| | $C_{\phi 2}$ | - | 18 | 21 pF | } bias: $V_\phi = -26\text{ V}$; $f_\phi = 1\text{ MHz}$ |
| | $C_{\phi 1}$ | - | 8.1 | 10.5 pF | |
| | $C_{\phi 2}$ | - | 11.2 | 14.5 pF | } bias: $V_Q = 0\text{ V}$; $f_\phi = 1\text{ MHz}$ |
| Output capacitance | C_Q | - | 4.0 | 5.0 pF | |
| <u>Leakage currents:</u> | | | | | |
| Address input and output inhibit input currents | $-I_{AL}$, $-I_{CL}$ | - | - | 1 μA | } $V_A = V_C = -15\text{ V}^1)$ $V_\phi = -28\text{ V}^1)$ $V_Q = -10\text{ V}$; $V_{C1} = V_{C2} = \text{LOW}$ $T_{amb} = 25\text{ }^\circ\text{C}$ |
| Clock input current | $-I_{\phi L}$ | - | - | 100 μA | |
| Output current | $-I_Q$ | - | - | 10 μA | |
| <u>Output resistance</u> | | | | | |
| HIGH | R_{QH} | - | 700 | - Ω | $V_{P1} = -5\text{ V}$ |
| LOW | R_{QL} | - | 300 | - Ω | |
| Clock power dissipation (see note 1) | $P_{\phi 1}, P_{\phi 2}$ | - | 36 | - mW | } $f_\phi = 1\text{ MHz}$ $V_{P1} = -13\text{ V}$ $f_\phi = 1\text{ MHz}$ $T_{amb} = 25\text{ }^\circ\text{C}$ |
| Input current (See note 2) | $-I_{P1}$ | - | 4.8 | - mA | |
| <u>Output transition times:</u> | | | | | |
| fall time | t_{THL} | - | 100 | - ns | |
| rise time | t_{TLH} | - | 350 | - ns | |
| <u>Delay times:</u> fall time | t_{DHL} | - | 20 | - ns | |
| rise time | t_{DLH} | - | 20 | - ns | |
| D. C. noise margin | M_L, M_H | 1 | - | - V | |

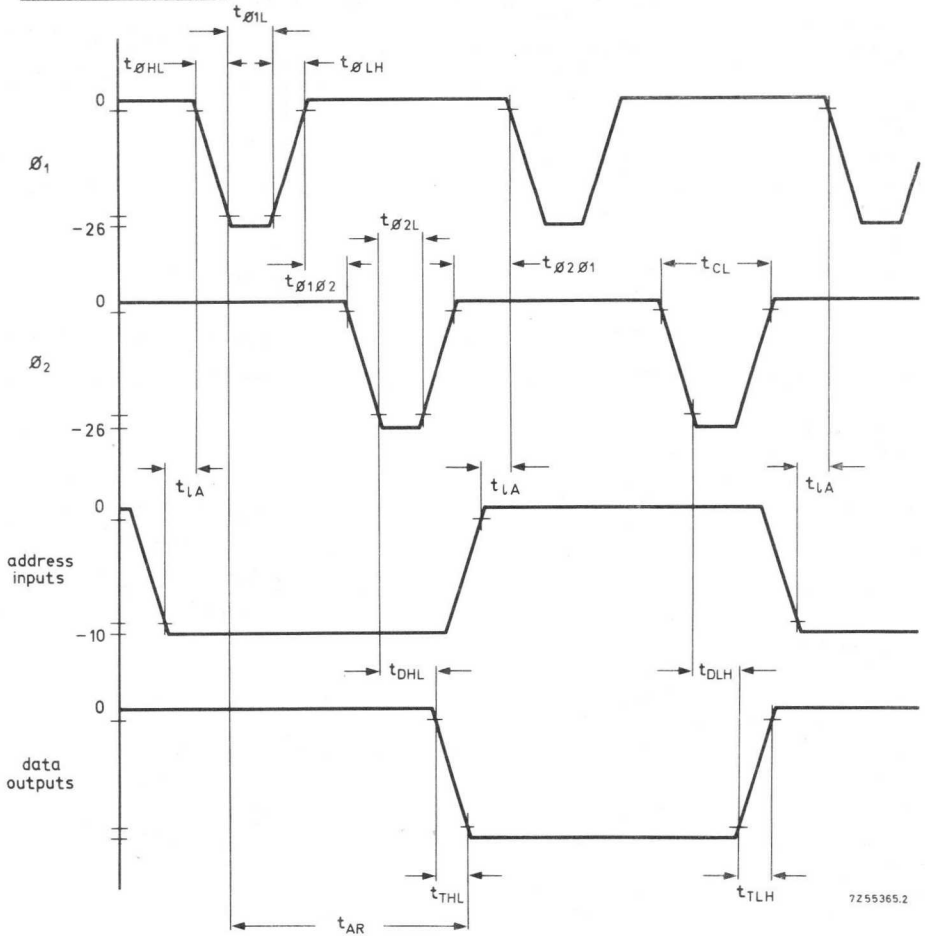
Note 1: No d. c. power is dissipated in the decoder or memory matrix; the quoted power dissipation is a. c. only.

Note 2: I_{P1} is almost entirely dependent on the external load.

¹⁾ $T_{amb} = 25\text{ }^\circ\text{C}$; all other terminals at V_{P0} .

CHARACTERISTICS (continued)

TIMING DIAGRAM



Address and output inhibit timing requirements:

1. Address input signals are clocked into the memory during ϕ_1 , and must remain present throughout ϕ_1 . Address lead time (t_{LA}) must be ≥ 0 .
2. Output inhibit signals act without delay. If output signals are to be read during phase 1, output inhibit signals must be delayed with respect to their associated address until phase 2 (t_{CL}).
3. The output signals remain steady for as many clock cycles as the address and output inhibit signals remain unchanged.

Note:

The indicated points on the vertical axis are specified in the glossary of terms.

CHARACTERISTICS (continued)

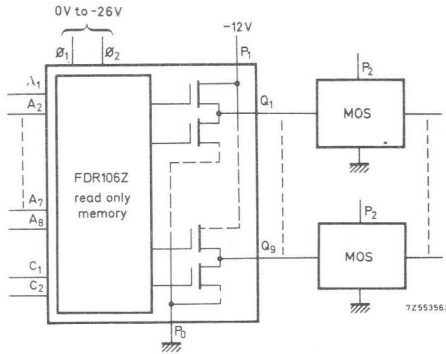
GLOSSARY OF TERMS

1. Clock pulse width: $t_{\phi L}$
The time for which the clock pulse is LOW; $V_{\phi} \leq -24 \text{ V}$
2. Clock pulse fall time: $t_{\phi HL}$
The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock delay time: $t_{\phi 1 \phi 2}$; $t_{\phi 2 \phi 1}$
The least allowable time between the end of the ϕ_1 (or ϕ_2) clock pulse and the start of the ϕ_2 (or ϕ_1) clock pulse, defined at -2 V .
5. Fall delay time: t_{DHL}
After the clock pulse ϕ_2 reaches LOW, the time that elapses before the output starts to change from HIGH to LOW.
6. Rise delay time: t_{DLH}
After the clock pulse ϕ_2 reaches LOW, the time that elapses before the output starts to change from LOW to HIGH.
7. Output fall transition time: t_{THL}
The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
8. Output rise transition time: t_{TLH}
The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
9. Output inhibit time: t_{CL}
The minimum time that the output inhibit signal must be present during ϕ_2 in order to inhibit the output, defined at -2 V .
10. Read access time: t_{AR}
The time between the 90% point on the negative going edge of the clock pulse ϕ_1 and the time at which the output is present, defined at 90%.

OUTPUT BUFFER DESCRIPTION

The only d.c. supply required is V_{P1} , the push-pull output buffer supply. V_{P1} may be varied between 0 and -28 V according to the output voltage swing required. It does not affect the operating speed of the memory.

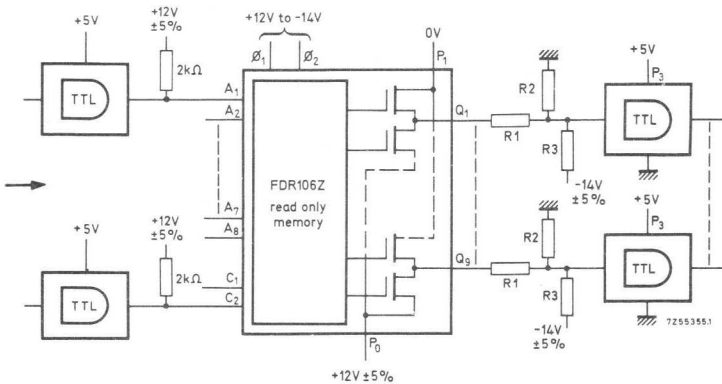
1. Biasing circuit A is used when driving MOS loads. Normal MOS input signals must drive the address and inhibit inputs.



Biasing circuit A

2. Biasing circuit B is used when driving TTL or DTL loads direct from each output buffer.

Note the neither active nor passive interface components are required. The circuit assumes MOS input excursions from $+5\text{ V}$ (V_{P0}) to $\leq 4\text{ V}$.



- $R_1 = 910\ \Omega$
- $R_2 = 1.8\ \text{k}\Omega$
- $R_3 = 8.2\ \text{k}\Omega$
- all resistors: $\pm 5\%$
- $M_L = 600\ \text{mV}$
- $M_H = 460\ \text{mV}$
- $P_{\text{totHIGH}} < 200\ \text{mW}$ per output

Biasing circuit B.

Note: The negative voltage is $26\text{ V} \pm 5\%$ below V_{P0} .

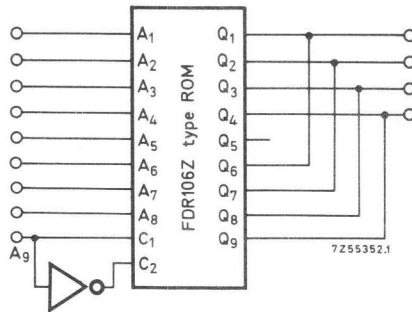
WIRED-OR APPLICATIONS

Use of wired-or output capability:

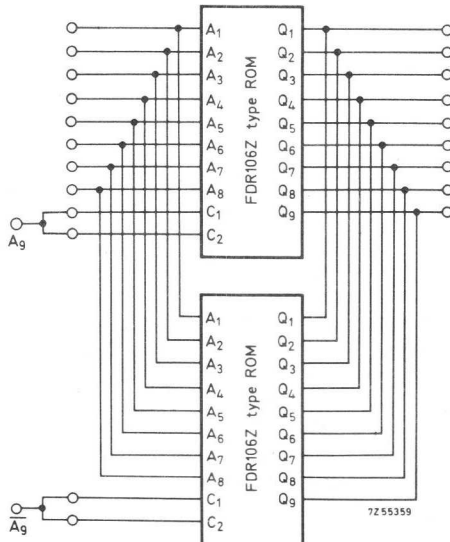
Applying a LOW signal to the output inhibit leads will cause both of the push pull output transistors associated with each output driver to turn off. Their output impedances are then very high (about 5 MΩ) and they can be wired-or with other ROM output buffers without affecting the output drive capability of any buffer operating in the low impedance mode¹⁾. C₁ controls output buffers 1 to 5, and C₂ controls output buffers 6 to 9. This output inhibit wired-or capability makes it possible to use the FDR106Z type ROM in many different applications, such as those shown here.

Note that the terminals A₉ and \bar{A}_9 although shown as address inputs, must actually be output inhibit signals synchronous with the addressed data word rather than the address.

ROM
512 word
4 bits



ROM
512 word
9 bits



¹⁾ Except for the effect of leakage current and capacitive load.

PROCEDURE FOR ORDERING A SPECIAL BIT PATTERN

To ensure accuracy when ordering a special bit pattern for a Read Only Memory (ROM) mask, customers should make use of the form on page 12. Four forms are needed for 256 word memories. The completed forms enable us to transfer any desired bit pattern into a standard ROM without error. After receipt of the forms our procedure is as follows:

1. An IBM card is punched for each row of each sheet of the form. (If he prefers to do so, the customer may punch his own cards and supply them to us, provided their format is identical with that of the forms).
2. The punched card are incorporated in a computer program that originates the following:
 - a duplicate of the ordered bit pattern, for verification.
 - a control tape for programming final electrical testing of the customers's ROM.
 - a control tape embodying the ordered pattern of ones and zeros to govern the movement of the automatic plotter used in mask making.
3. The computer print-out is checked against the original order forms; a copy is also sent to the customer for his verification and signature.
4. Upon receipts of the customer's signed verification, full scale masks embodying the desired pattern are made.

INSTRUCTION FOR COMPLETING THE FORMS**A. Customer block: ON EACH FORM**

Enter Name, Date and Authorized Signature in the spaces provided.

B. The ADDRESS INPUTS and CONTENTS

Each page of the ROM Bit Pattern Form is laid out for 64 consecutive words; 16 in each of the four columns (00, 01, 10 and 11).

1. ADDRESS INPUTS

- a) There are nine Address Inputs; the right-hand bit is always bit 1 and is the least significant bit; the left-hand bit is bit 9, it is the most significant. The Address Input leads on the ROM package are labelled A₁, A₂, etc., to correspond.
- b) The states of bits 1 to 4 are listed consecutively down the page. The state of bits 5 and 6 are at the head of each of four output columns. The Address Input of 64 consecutive words are thus uniquely specified on each page.
- c) Bit 7, 8, and 9 (or bits 7 and 8 only, for 256 word memories) specify sets of memory locations, 1 set of 64 words per page. These spaces should be filled by the customer using a consecutive full binary code. The first position on page 1 of your specification should be three (or two) zeros. ¹⁾ Memories of 256 words need 4 pages, of specifications.
- d) Only ones (1 = LOW) or zeros (0 = HIGH) should be used in completing the form except where, as with 256 word memories, column 9 is unused and is, therefore, left blank.

¹⁾ See example on page 12.

2. CONTENTS (DATA OUTPUTS)

- a) Each column has provision for words of 9 bits numbered 1 to 9, bit 1 is always the right-hand bit. The output leads of the ROM package are labelled Q1, Q2, etc., to correspond.
- b) The requisite bit pattern should be inserted under headings 1 to 9 using only ones (1 = LOW) and zeros (0 = HIGH).

3. AUTHORIZED SIGNATURE

Having completed the bit pattern, the customer should check that the forms are numbered, dated, and signed, as they constitute formal evidence of his request. In the event that the customer provides his own punched cards the signature on the computer duplicate will serve as formal evidence.



PHILIPS
Electronic Components
and Materials
Integrated Circuits

Read Only Memory Bit Pattern

FDR 106 Z...

page of

AUTHORIZED SIGNATURE

DATE

CUSTOMER NAME:

| ADDRESS INPUTS | | | | | | | | CONTENTS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|---|---|---|---|---|---|--|----------|----|----|----|---------|----|----|----|---------|----|----|----|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--|--|--|
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | | 00 | | | | 01 | | | | 10 | | | | 11 | | | | | | | | | | | | | | | | | | |
| 987654321 | | | | | | | | OUTPUTS | | | | OUTPUTS | | | | OUTPUTS | | | | OUTPUTS | | | | | | | | | | | | | | | | | | |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | | | |
| X | X | X | X | X | X | X | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | X | X | X | X | X | X | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | X | X | X | X | X | X | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | X | X | X | X | X | X | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | X | X | X | X | X | X | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | X | X | X | X | X | X | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | X | X | X | X | X | X | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | X | X | X | X | X | X | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | X | X | X | X | X | X | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | X | X | X | X | X | X | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | X | X | X | X | X | X | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | X | X | X | X | X | X | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | X | X | X | X | X | X | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | X | X | X | X | X | X | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Note: 1 = LOW; 0 = HIGH

APPLICATIONS

The bit patterns stored in the FDR106Z1 allow this ROM to perform the following functions:

1. STARBURST ALPHA-NUMERIC CHARACTER GENERATION

Generation of activating signals for 64 17-segment starburst pattern character using an ASCII input code (128 words).

2. STARBURST PATTERN GENERATION

Generation of x and y deflection signal to produce a 22 stroke starburst pattern on a CRT (22 words).

3. SEVEN SEGMENT DECODE NUMERIC BLANKING CHARACTER GENERATOR (16 WORDS)**4. SELECTRIC TO ASCII CODE CONVERSION**

Conversion of IBM selectric input/output writer keyboard code to ASCII code with even or odd parity (88 words).



PATTERN 1

STARBURST CHARACTER GENERATION

For a starburst character, 17 activating signals are used for the 17 segments of the pattern. Since only 9 output lines are available in the FDR106Z1, the complete bit pattern for each character must be stored in two 9-bit words; thus a total of 128 words are used for 64 characters. Fig. 1 shows the segments controlled by the output bits of the first (S) and second (T) word for each character. The S word contains 9 segment signals and the T word 8. The ninth bit of ROM T(T6) is not used. A logic 1 output signal (nominally -12 V) represents an activated (ON) segment signal. The starburst character generation function is selected by setting address bit A₈ to 0 V (V_{P0} or HIGH signals). S words are selected by setting address bit A₅ to 0 V (HIGH) and T words by setting address bit A₅ to -10 V (LOW).

Address bits A₁, A₂, A₃, A₄, A₆ and A₇ are used to select any one of the characters. The input character code is a subset of the standard ASCII 7 bit code derived by using ASCII bits b₁, b₂, b₃, b₄, b₅ and b₇ according to the following table:

| FDR106Z1 | |
|----------------|----------------|
| address input | ASCII bit |
| A ₁ | b ₄ |
| A ₂ | b ₃ |
| A ₃ | b ₂ |
| A ₄ | b ₁ |
| A ₆ | b ₅ |
| A ₇ | b ₇ |

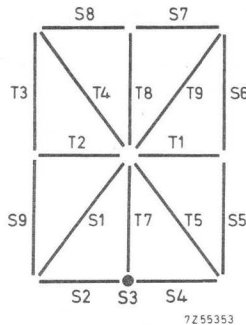


Fig. 1 Starburst pattern segments

PATTERN 1 (continued)

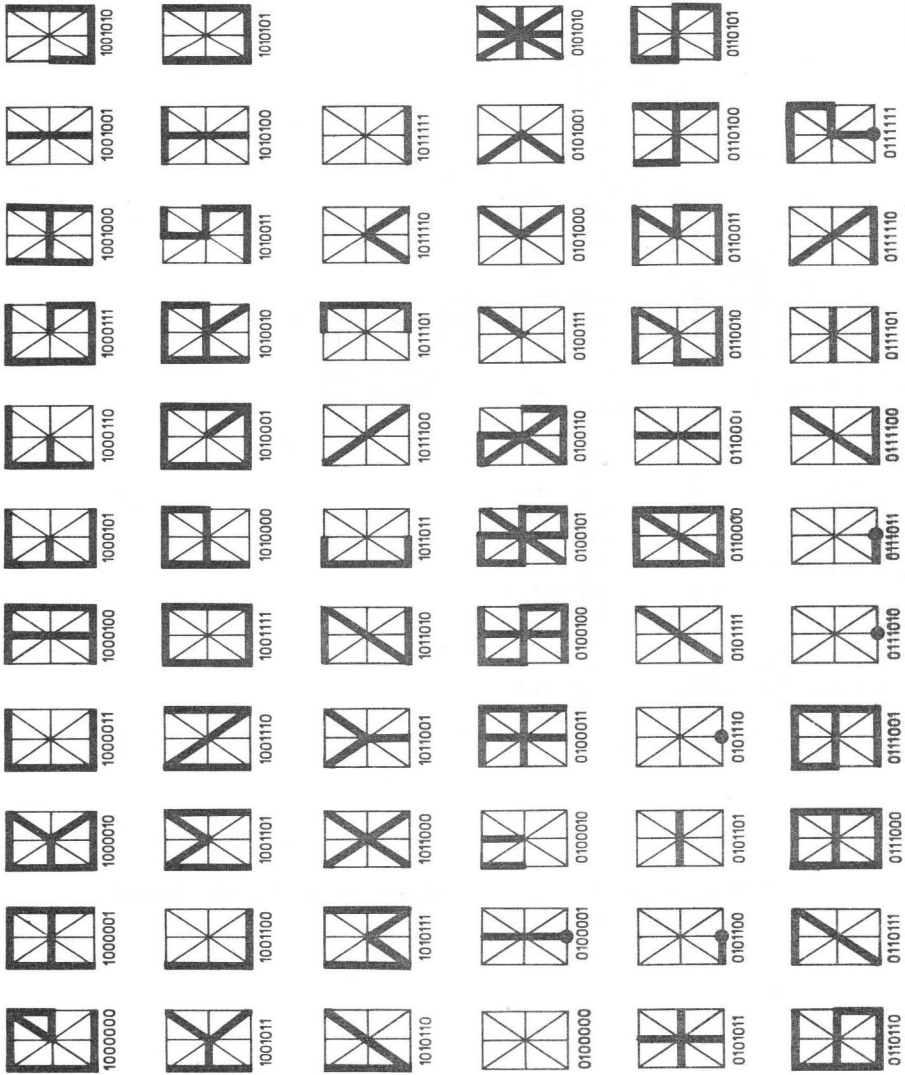


Fig. 2 Starburst character forms

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→ **PATTERN 1** (continued)

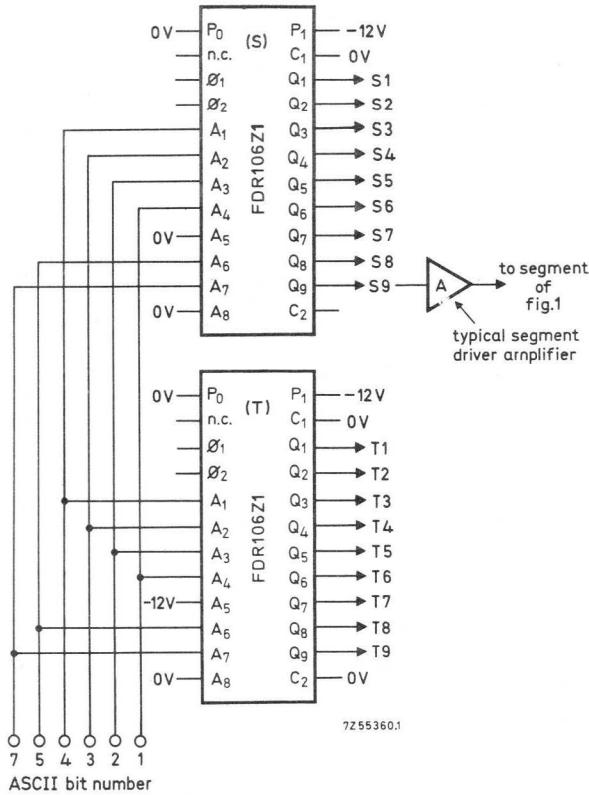


Fig. 3. Wiring diagram for segment activation of a 17 segment illuminated display

PATTERN 2

2.1 STARBURST STROKE PATTERNS GENERATION

In this configuration, the ROM is used to produce x and y deflection signals to generate the pattern of Fig. 4 on a CRT. For this purpose the FDR106Z1 is connected as shown in Fig. 5, with certain of the ROM outputs connected back to the address input lines¹⁾. Each word in this sequence contains (in addition to the x and y steering signal outputs for a CRT) the address of the next word of the group used for this function. One clock power is applied, the memory steps in turn to a next word of the group each clock period and will thus continuously cycle through the group, as shown in Fig. 6 where the address and contents (outputs) of each word are sequentially listed. The +x, -x, +y and -y signals are rate signals and must be integrated as shown in Figs. 7a, b and c to produce the x and y deflection signals for a CRT.

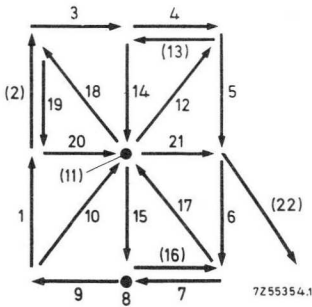


Fig. 4 Starburst stroke pattern

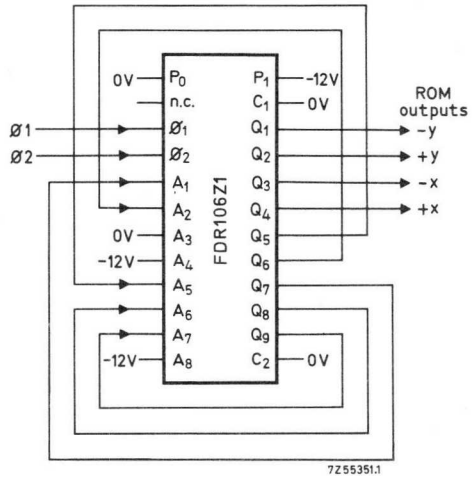


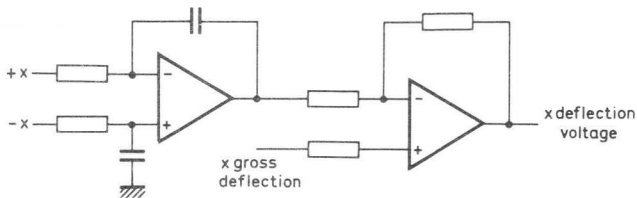
Fig. 5 Wiring diagram for starburst stroke pattern generator

¹⁾ In doing so, the ROM runs at the ϕ_1, ϕ_2 clock-rate through a sequence of 22 addresses.

PATTERN 2 (continued)

| Address bits | | | | | | | | Segment of Fig. 4 | ROM contents | | | | | | | | |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|-------------------------|--------------|----|----|----|---|---|---|---|---|
| A ₈ | A ₇ | A ₆ | A ₅ | A ₄ | A ₃ | A ₂ | A ₁ | | +x | -x | +y | -y | | | | | |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 2 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 3 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 4 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 5 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 6 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 7 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 9 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 10 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 11 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 12 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 13 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 14 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 15 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 16 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 17 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 18 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 19 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 20 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 21 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 22 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |

Fig. 6 Starburst pattern sequence



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Fig. 7a x integrator circuit:
identical circuit for y

Note: 1 = LOW; 0 = HIGH

PATTERN 2 (continued)

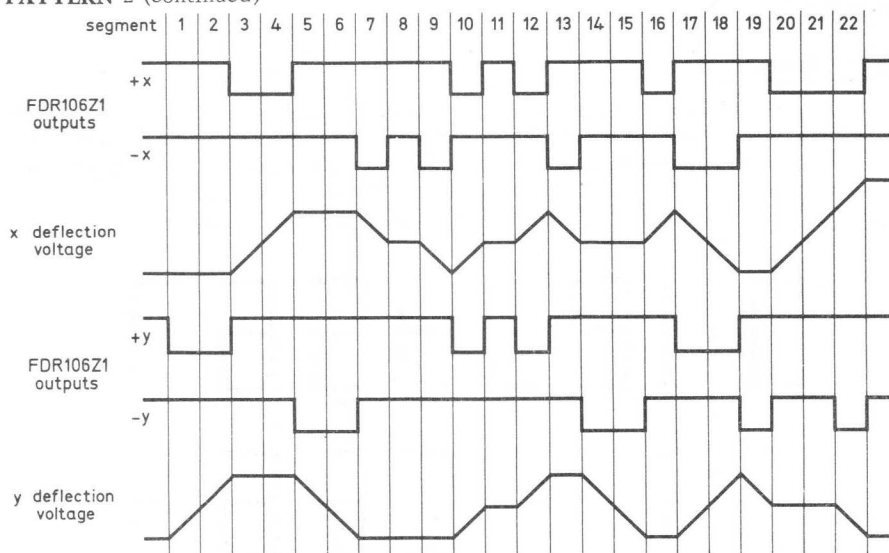


Fig. 7b and 7c x and y deflection signal generation

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2.2 Generation of blanking signal

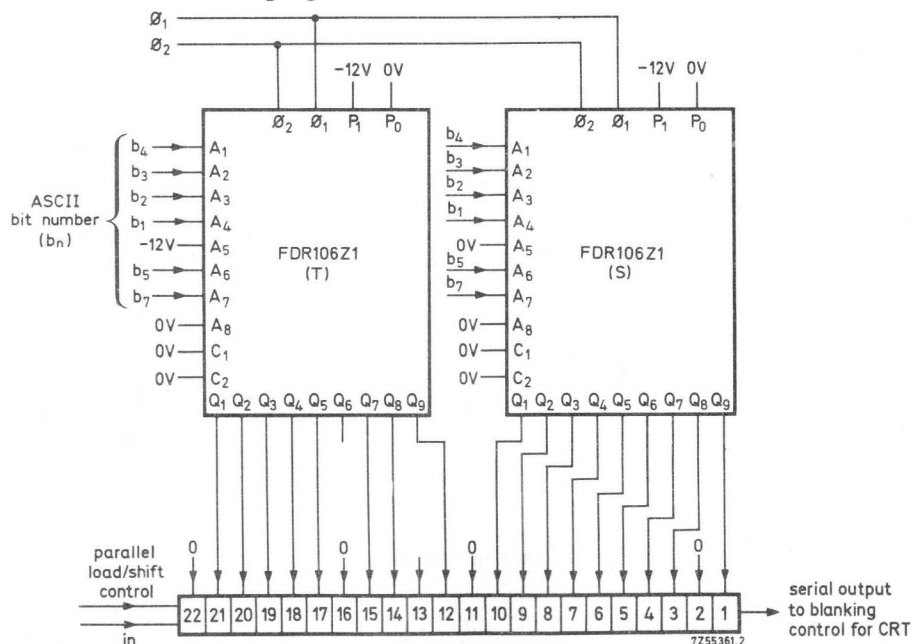


Fig. 8

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→ **PATTERN 3**

SEVEN SEGMENT DECODE

This portion of the FDR106Z1 generates seven driver signals, a zero indicator signal, and an "over-nine" indicator signal for a seven segment display device. The input code is BCD augmented by special characters. The segment activation patterns are shown, together with the BCD code at the ROM inputs, in Fig.9.

Fig.10 is the connection diagram for seven segment function configuration.

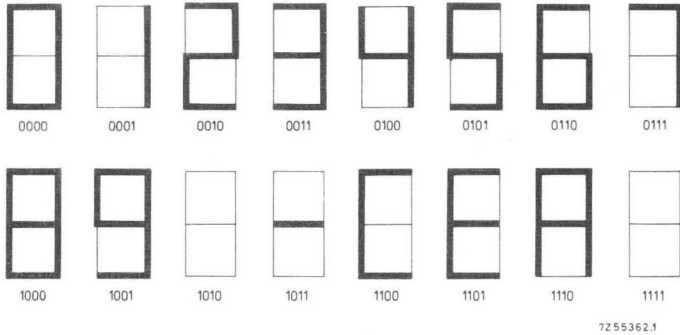


Fig. 9 Seven segment character forms and their binary input code (8421)

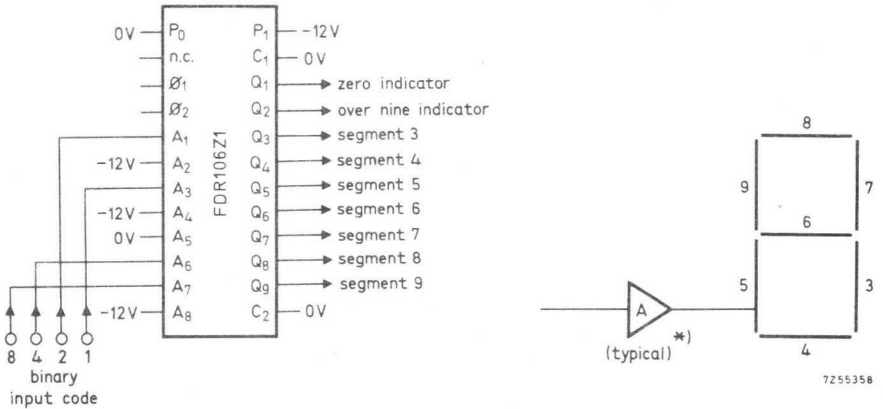


Fig. 10 Wiring diagram for a seven segment decode

*) Typical segment driver amplifier

PATTERN 4

SELECTRIC TO ASCII CODE CONVERTER

When used in the selectric to ASCII code converter configuration, the FDR106Z1 translates seven input line signals from a selectric input/output writer (correspondence model) to ASCII code with even or odd parity. Fig. 11 shows the wiring connections for this function. The connection of selectric contacts is shown for a machine with standard wiring. Selectric keyboards provide six signal lines (R₁, R₂, R_{2A}, R₅, T₁ and T₂) and a parity line which is not used in this application. The keyboard shift contact provides the seventh input line (A₇) to the FDR106Z1 (upper case is LOW, lower case is HIGH). Fig. 12 shows the selectric contact signals and FDR106Z1 address bits for which the code converter is patterned. The ASCII code for > is generated when the selectric ϵ key is depressed, and the code for < when the selectric \circ (degrees) key is depressed.

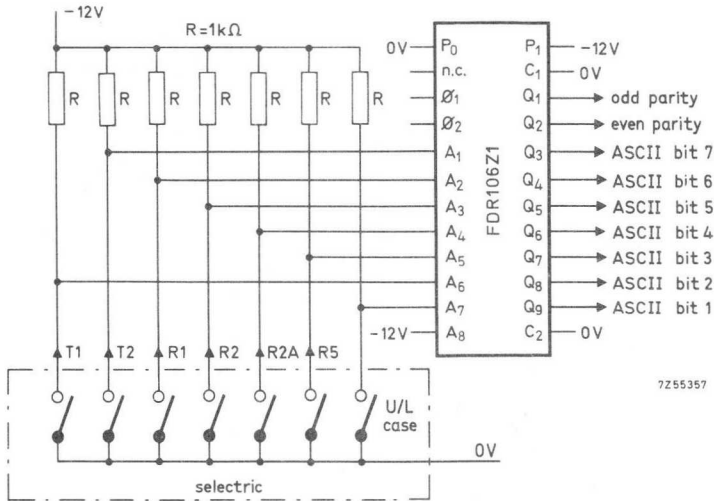


Fig. 11 Wiring diagram for selectric to ASCII code converter

SELECTRIC CODE

| FDR106Z1 address bit selectric contact | A7 | A6 | A1 | A2 | A3 | A4 | A5 | FDR106Z1 address bit selectric contact | A7 | A6 | A1 | A2 | A3 | A4 | A5 |
|-------------------------------------------------|------|----|----|----|----|-----|----|-------------------------------------------------|------|----|----|----|----|-----|----|
| character | case | T1 | T2 | R1 | R2 | R2A | R5 | character | case | T1 | T2 | R1 | R2 | R2A | R5 |
| A | U | 0 | 1 | 1 | 1 | 0 | 0 | W | U | 0 | 1 | 1 | 1 | 1 | 1 |
| a | L | 0 | 1 | 1 | 1 | 0 | 0 | w | L | 0 | 1 | 1 | 1 | 1 | 1 |
| B | U | 1 | 0 | 1 | 1 | 1 | 1 | X | U | 1 | 0 | 0 | 0 | 0 | 0 |
| b | L | 1 | 0 | 1 | 1 | 1 | 1 | x | L | 1 | 0 | 0 | 0 | 0 | 0 |
| C | U | 1 | 0 | 1 | 1 | 0 | 0 | Y | U | 1 | 1 | 0 | 1 | 1 | 1 |
| c | L | 1 | 0 | 1 | 1 | 0 | 0 | y | L | 1 | 1 | 0 | 1 | 1 | 1 |
| D | U | 1 | 0 | 0 | 1 | 0 | 0 | Z | U | 0 | 0 | 0 | 0 | 0 | 1 |
| d | L | 1 | 0 | 0 | 1 | 0 | 0 | z | L | 0 | 0 | 0 | 0 | 0 | 1 |
| E | U | 1 | 0 | 0 | 1 | 0 | 1 | (| U | 0 | 0 | 0 | 0 | 0 | 0 |
| e | L | 1 | 0 | 0 | 1 | 0 | 1 |) | L | 0 | 0 | 0 | 0 | 0 | 0 |
| F | U | 1 | 1 | 1 | 0 | 0 | 0 | @ | U | 0 | 0 | 1 | 0 | 0 | 1 |
| f | L | 1 | 1 | 1 | 0 | 0 | 0 | 2 | L | 0 | 0 | 1 | 0 | 0 | 1 |
| G | U | 1 | 1 | 0 | 0 | 0 | 0 | # | U | 0 | 0 | 1 | 0 | 0 | 0 |
| g | L | 1 | 1 | 0 | 0 | 0 | 0 | 3 | L | 0 | 0 | 1 | 0 | 0 | 0 |
| H | U | 1 | 0 | 0 | 1 | 1 | 1 | \$ | U | 0 | 0 | 0 | 1 | 1 | 0 |
| h | L | 1 | 0 | 0 | 1 | 1 | 1 | 4 | L | 0 | 0 | 0 | 1 | 1 | 0 |
| I | U | 0 | 1 | 1 | 1 | 0 | 1 | % | U | 0 | 0 | 0 | 1 | 0 | 1 |
| i | L | 0 | 1 | 1 | 1 | 0 | 1 | 5 | L | 0 | 0 | 0 | 1 | 0 | 1 |
| J | U | 1 | 1 | 0 | 0 | 0 | 1 | ¢ | U | 0 | 0 | 1 | 1 | 0 | 1 |
| j | L | 1 | 1 | 0 | 0 | 0 | 1 | 6 | L | 0 | 0 | 1 | 1 | 0 | 1 |
| K | U | 1 | 0 | 1 | 1 | 0 | 1 | & | U | 0 | 0 | 0 | 1 | 0 | 0 |
| k | L | 1 | 0 | 1 | 1 | 0 | 1 | 7 | L | 0 | 0 | 0 | 1 | 0 | 0 |
| L | U | 1 | 0 | 0 | 1 | 1 | 0 | * | U | 0 | 0 | 1 | 1 | 0 | 0 |
| l | L | 1 | 0 | 0 | 1 | 1 | 0 | 8 | L | 0 | 0 | 1 | 1 | 0 | 0 |
| M | U | 0 | 1 | 0 | 0 | 0 | 0 | (| U | 0 | 0 | 1 | 1 | 1 | 1 |
| m | L | 0 | 1 | 0 | 0 | 0 | 0 | 9 | L | 0 | 0 | 1 | 1 | 1 | 1 |
| N | U | 1 | 0 | 1 | 0 | 0 | 1 |) | U | 0 | 0 | 0 | 1 | 1 | 1 |
| n | L | 1 | 0 | 1 | 0 | 0 | 1 | 0 | L | 0 | 0 | 0 | 1 | 1 | 1 |
| O | U | 0 | 1 | 0 | 1 | 1 | 0 | - | U | 1 | 1 | 1 | 1 | 1 | 1 |
| o | L | 0 | 1 | 0 | 1 | 1 | 0 | - | L | 1 | 1 | 1 | 1 | 1 | 1 |
| P | U | 1 | 1 | 0 | 1 | 0 | 1 | + | U | 1 | 1 | 1 | 0 | 0 | 1 |
| p | L | 1 | 1 | 0 | 1 | 0 | 1 | = | L | 1 | 1 | 1 | 0 | 0 | 1 |
| Q | U | 1 | 1 | 1 | 1 | 0 | 1 | ° | U | 0 | 1 | 0 | 0 | 0 | 1 |
| q | L | 1 | 1 | 1 | 1 | 0 | 1 | ! | L | 0 | 1 | 0 | 0 | 0 | 1 |
| R | U | 0 | 1 | 0 | 1 | 0 | 0 | : | U | 1 | 1 | 0 | 1 | 0 | 0 |
| r | L | 0 | 1 | 0 | 1 | 0 | 0 | ; | L | 1 | 1 | 0 | 1 | 0 | 0 |
| S | U | 0 | 1 | 0 | 1 | 1 | 1 | " | U | 0 | 1 | 0 | 1 | 0 | 1 |
| s | L | 0 | 1 | 0 | 1 | 1 | 1 | , | L | 0 | 1 | 0 | 1 | 0 | 1 |
| T | U | 1 | 0 | 0 | 0 | 0 | 1 | ' | U | 1 | 1 | 1 | 1 | 0 | 0 |
| t | L | 1 | 0 | 0 | 0 | 0 | 1 | ' | L | 1 | 1 | 1 | 1 | 0 | 0 |
| U | U | 1 | 0 | 1 | 0 | 0 | 0 | | U | 0 | 1 | 1 | 0 | 0 | 1 |
| u | L | 1 | 0 | 1 | 0 | 0 | 0 | | L | 0 | 1 | 1 | 0 | 0 | 1 |
| V | U | 0 | 1 | 1 | 0 | 0 | 0 | ? | U | 1 | 1 | 0 | 1 | 1 | 0 |
| v | L | 0 | 1 | 1 | 0 | 0 | 0 | / | L | 1 | 1 | 0 | 1 | 1 | 0 |

Note: 1 = LOW; 0 = HIGH

COMPLETE FDR106Z1 BIT PATTERN

| ADDRESS INPUTS | | ROM CONTENTS | | | | | | | | | | | | | | | | | | |
|----------------|-----------------|---------------|---|---|---------------|---|---|---------------|---|---|---------------|---|---|---|---|---|---|---|---|---|
| | | 00 outputs | | | 01 outputs | | | 10 outputs | | | 11 outputs | | | | | | | | | |
| 8 | 7 6 5 4 3 2 1 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | |
| 1 | 0 0 X X 0 0 0 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2 | 0 0 X X 0 0 0 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3 | 0 0 X X 0 0 1 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 4 | 0 0 X X 0 0 1 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 5 | 0 0 X X 0 1 0 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 6 | 0 0 X X 0 1 0 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 7 | 0 0 X X 0 1 1 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 8 | 0 0 X X 0 1 1 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 9 | 0 0 X X 1 0 0 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 10 | 0 0 X X 1 0 0 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 11 | 0 0 X X 1 0 1 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 12 | 0 0 X X 1 0 1 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 13 | 0 0 X X 1 1 0 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 14 | 0 0 X X 1 1 0 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 15 | 0 0 X X 1 1 1 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 16 | 0 0 X X 1 1 1 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: 1 = LOW; 0 = HIGH



COMPLETE FDR106Z1 BIT PATTERN

| ADDRESS INPUTS | | ROM CONTENTS | | | | | | | | | | | | | | | | | | | | |
|----------------|-----------------|---------------|---|---|---------------|---|---|---------------|---|---|---------------|---|---|---|---|---|---|---|---|---|---|---|
| | | 00 outputs | | | 01 outputs | | | 10 outputs | | | 11 outputs | | | | | | | | | | | |
| 8 | 7 6 5 4 3 2 1 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | | | |
| 17 | 0 1 X X 0 0 0 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | |
| 18 | 0 1 X X 0 0 0 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 19 | 0 1 X X 0 0 1 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 20 | 0 1 X X 0 0 1 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 21 | 0 1 X X 0 1 0 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 22 | 0 1 X X 0 1 0 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 23 | 0 1 X X 0 1 1 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 24 | 0 1 X X 0 1 1 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 25 | 0 1 X X 1 0 0 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 26 | 0 1 X X 1 0 0 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 27 | 0 1 X X 1 0 1 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 28 | 0 1 X X 1 0 1 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 29 | 0 1 X X 1 1 0 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 30 | 0 1 X X 1 1 0 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 31 | 0 1 X X 1 1 1 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 32 | 0 1 X X 1 1 1 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: 1 = LOW; 0 = HIGH

COMPLETE FDR106Z1 BIT PATTERN (continued)

| ADDRESS INPUTS | ROM CONTENTS | | | | | | | | | | | | | | |
|-----------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| | 00 outputs | | | | 01 outputs | | | | 10 outputs | | | | 11 outputs | | |
| 8 7 6 5 4 3 2 1 | 9 8 7 6 5 4 3 2 1 | 0 0 1 1 0 1 1 0 | 1 0 1 1 1 0 1 1 0 | 0 1 0 1 1 1 1 1 0 | 9 8 7 6 5 4 3 2 1 | 0 1 0 1 1 1 1 1 0 | 0 0 0 0 1 0 0 0 1 | 1 0 0 0 0 1 0 0 1 | 0 0 0 1 1 1 1 0 1 | 9 8 7 6 5 4 3 2 1 | 0 0 0 1 1 1 1 0 1 | 0 0 1 1 1 1 1 0 1 | 0 0 1 0 1 1 1 0 1 | 0 0 1 0 1 1 1 0 1 | 0 0 1 0 1 1 1 0 1 |
| 33 | 1 0 X X 0 0 0 0 | 1 0 1 1 1 0 1 1 0 | 1 0 1 1 1 0 1 1 0 | 0 1 0 1 1 1 1 1 0 | 9 8 7 6 5 4 3 2 1 | 0 1 0 1 1 1 1 1 0 | 0 0 0 1 1 1 1 0 1 | 0 0 1 1 1 0 1 1 0 | 0 0 0 1 1 1 1 0 1 | 9 8 7 6 5 4 3 2 1 | 0 0 1 1 1 1 1 0 1 | 0 0 1 0 1 1 1 0 1 | 0 0 1 0 1 1 1 0 1 | 0 0 1 0 1 1 1 0 1 | 0 0 1 0 1 1 1 0 1 |
| 34 | 1 0 X X 0 0 0 1 | 1 0 1 1 0 1 1 1 0 | 1 0 1 1 0 1 1 1 0 | 0 1 0 0 0 1 0 0 1 | 9 8 7 6 5 4 3 2 1 | 1 0 0 0 0 1 0 0 1 | 1 0 0 0 0 1 0 0 1 | 1 1 1 0 0 1 1 1 0 | 1 1 1 0 0 1 1 1 0 | 9 8 7 6 5 4 3 2 1 | 0 1 0 1 0 1 1 1 0 | 0 1 0 1 0 1 1 1 0 | 0 1 0 1 0 1 1 1 0 | 0 1 0 1 0 1 1 1 0 | 0 1 0 1 0 1 1 1 0 |
| 35 | 1 0 X X 0 0 1 0 | 1 1 0 0 1 1 0 0 1 | 1 1 0 0 1 1 0 0 1 | 0 1 0 0 1 1 0 1 0 | 9 8 7 6 5 4 3 2 1 | 0 1 0 0 1 1 0 1 0 | 0 1 0 0 1 1 0 1 0 | 1 0 1 0 1 1 1 1 0 | 1 0 1 0 1 1 1 1 0 | 9 8 7 6 5 4 3 2 1 | 0 1 0 1 0 1 1 1 0 | 0 1 0 1 0 1 1 1 0 | 0 1 0 1 0 1 1 1 0 | 0 1 0 1 0 1 1 1 0 | 0 1 0 1 0 1 1 1 0 |
| 36 | 1 0 X X 0 0 1 1 | 0 1 1 0 1 1 1 1 0 | 0 1 1 0 1 1 1 1 0 | 0 1 1 1 0 1 0 0 1 | 9 8 7 6 5 4 3 2 1 | 0 1 1 1 0 1 0 0 1 | 0 1 1 1 0 1 0 0 1 | 0 1 1 0 0 1 1 0 1 | 0 1 1 0 0 1 1 0 1 | 9 8 7 6 5 4 3 2 1 | 0 1 0 0 1 1 0 1 0 | 0 1 0 0 1 1 0 1 0 | 0 1 0 0 1 1 0 1 0 | 0 1 0 0 1 1 0 1 0 | 0 1 0 0 1 1 0 1 0 |
| 37 | 1 0 X X 0 1 0 0 | 1 1 1 0 1 1 0 1 0 | 1 1 1 0 1 1 0 1 0 | 1 0 1 0 1 1 0 0 1 | 9 8 7 6 5 4 3 2 1 | 1 0 1 0 1 1 0 0 1 | 1 0 1 0 1 1 0 0 1 | 0 0 1 0 0 1 1 1 0 | 0 0 1 0 0 1 1 1 0 | 9 8 7 6 5 4 3 2 1 | 1 0 1 0 0 1 1 1 0 | 1 0 1 0 0 1 1 1 0 | 1 0 1 0 0 1 1 1 0 | 1 0 1 0 0 1 1 1 0 | 1 0 1 0 0 1 1 1 0 |
| 38 | 1 0 X X 0 1 0 1 | 0 1 0 0 1 1 1 0 1 | 0 1 0 0 1 1 1 0 1 | 1 1 1 0 0 1 0 0 1 | 9 8 7 6 5 4 3 2 1 | 1 1 1 0 0 1 0 0 1 | 1 1 1 0 0 1 0 0 1 | 1 1 0 1 1 1 0 1 0 | 1 1 0 1 1 1 0 1 0 | 9 8 7 6 5 4 3 2 1 | 0 0 0 0 1 1 1 1 0 | 0 0 0 0 1 1 1 1 0 | 0 0 0 0 1 1 1 1 0 | 0 0 0 0 1 1 1 1 0 | 0 0 0 0 1 1 1 1 0 |
| 39 | 1 0 X X 0 1 1 0 | 0 0 0 1 1 1 0 1 0 | 0 0 0 1 1 1 0 1 0 | 0 1 1 0 1 1 0 0 1 | 9 8 7 6 5 4 3 2 1 | 0 1 1 0 1 1 0 0 1 | 0 1 1 0 1 1 0 0 1 | 1 1 0 0 0 1 1 0 1 | 1 1 0 0 0 1 1 0 1 | 9 8 7 6 5 4 3 2 1 | 1 1 0 1 0 1 1 1 0 | 1 1 0 1 0 1 1 1 0 | 1 1 0 1 0 1 1 1 0 | 1 1 0 1 0 1 1 1 0 | 1 1 0 1 0 1 1 1 0 |
| 40 | 1 0 X X 0 1 1 1 | 1 0 0 0 0 1 1 1 0 | 1 0 0 0 0 1 1 1 0 | 1 0 0 1 0 1 1 1 0 | 9 8 7 6 5 4 3 2 1 | 1 0 0 1 0 1 1 1 0 | 1 0 0 1 0 1 1 1 0 | 0 0 1 1 0 1 0 1 0 | 0 0 1 1 0 1 0 1 0 | 9 8 7 6 5 4 3 2 1 | 1 0 0 0 1 1 1 0 1 | 1 0 0 0 1 1 1 0 1 | 1 0 0 0 1 1 1 0 1 | 1 0 0 0 1 1 1 0 1 | 1 0 0 0 1 1 1 0 1 |
| 41 | 1 0 X X 1 0 0 0 | 0 0 1 0 0 0 1 0 0 | 0 0 1 0 0 0 1 0 0 | 0 0 0 0 0 0 0 0 0 | 9 8 7 6 5 4 3 2 1 | 0 0 0 0 0 0 0 0 0 | 0 0 0 0 0 0 0 0 0 | 1 0 1 1 0 0 0 1 0 | 1 0 1 1 0 0 0 1 0 | 9 8 7 6 5 4 3 2 1 | 0 0 0 0 1 0 1 0 0 | 0 0 0 0 1 0 1 0 0 | 0 0 0 0 1 0 1 0 0 | 0 0 0 0 1 0 1 0 0 | 0 0 0 0 1 0 1 0 0 |
| 42 | 1 0 X X 1 0 0 1 | 0 1 1 0 0 1 0 1 0 | 0 1 1 0 0 1 0 1 0 | 0 1 0 0 1 0 0 0 1 | 9 8 7 6 5 4 3 2 1 | 0 1 0 0 1 0 0 0 1 | 0 1 0 0 1 0 0 0 1 | 0 1 1 1 1 0 0 0 0 | 0 1 1 1 1 0 0 0 0 | 9 8 7 6 5 4 3 2 1 | 0 0 1 0 1 0 0 0 1 | 0 0 1 0 1 0 0 0 1 | 0 0 1 0 1 0 0 0 1 | 0 0 1 0 1 0 0 0 1 | 0 0 1 0 1 0 0 0 1 |
| 43 | 1 0 X X 1 0 1 0 | 1 1 1 0 1 1 1 0 1 | 1 1 1 0 1 1 1 0 1 | 0 1 1 0 1 1 0 0 0 | 9 8 7 6 5 4 3 2 1 | 0 1 1 0 1 1 0 0 0 | 0 1 1 0 1 1 0 0 0 | 1 0 1 1 0 0 1 0 0 | 1 0 1 1 0 0 1 0 0 | 9 8 7 6 5 4 3 2 1 | 0 0 0 1 1 1 0 0 0 | 0 0 0 1 1 1 0 0 0 | 0 0 0 1 1 1 0 0 0 | 0 0 0 1 1 1 0 0 0 | 0 0 0 1 1 1 0 0 0 |
| 44 | 1 0 X X 1 0 1 1 | 0 1 1 1 1 1 0 0 0 | 0 1 1 1 1 1 0 0 0 | 0 1 0 1 1 0 0 1 0 | 9 8 7 6 5 4 3 2 1 | 0 1 0 1 1 0 0 1 0 | 0 1 0 1 1 0 0 1 0 | 1 1 0 1 1 1 1 0 0 | 1 1 0 1 1 1 1 0 0 | 9 8 7 6 5 4 3 2 1 | 1 0 1 1 1 1 0 1 0 | 1 0 1 1 1 1 0 1 0 | 1 0 1 1 1 1 0 1 0 | 1 0 1 1 1 1 0 1 0 | 1 0 1 1 1 1 0 1 0 |
| 45 | 1 0 X X 1 1 0 0 | 0 0 1 0 1 1 0 1 0 | 0 0 1 0 1 1 0 1 0 | 0 0 0 0 1 1 0 0 1 | 9 8 7 6 5 4 3 2 1 | 0 0 0 0 1 1 0 0 1 | 0 0 0 0 1 1 0 0 1 | 0 0 1 1 0 1 1 0 1 | 0 0 1 1 0 1 1 0 1 | 9 8 7 6 5 4 3 2 1 | 0 0 0 1 0 1 1 1 0 | 0 0 0 1 0 1 1 1 0 | 0 0 0 1 0 1 1 1 0 | 0 0 0 1 0 1 1 1 0 | 0 0 0 1 0 1 1 1 0 |
| 46 | 1 0 X X 1 1 0 1 | 1 1 1 1 0 1 1 0 1 | 1 1 1 1 0 1 1 0 1 | 1 1 1 0 0 1 1 1 0 | 9 8 7 6 5 4 3 2 1 | 1 1 1 0 0 1 1 1 0 | 1 1 1 0 0 1 1 1 0 | 1 1 1 0 1 0 1 0 1 | 1 1 1 0 1 0 1 0 1 | 9 8 7 6 5 4 3 2 1 | 1 0 0 1 1 1 1 1 0 | 1 0 0 1 1 1 1 1 0 | 1 0 0 1 1 1 1 1 0 | 1 0 0 1 1 1 1 1 0 | 1 0 0 1 1 1 1 1 0 |
| 47 | 1 0 X X 1 1 1 0 | 0 0 1 0 0 0 1 0 0 | 0 0 1 0 0 0 1 0 0 | 1 0 0 0 1 1 0 0 1 | 9 8 7 6 5 4 3 2 1 | 1 0 0 0 1 1 0 0 1 | 1 0 0 0 1 1 0 0 1 | 1 1 0 1 0 1 1 0 0 | 1 1 0 1 0 1 1 0 0 | 9 8 7 6 5 4 3 2 1 | 0 1 0 0 0 1 1 1 0 | 0 1 0 0 0 1 1 1 0 | 0 1 0 0 0 1 1 1 0 | 0 1 0 0 0 1 1 1 0 | 0 1 0 0 0 1 1 1 0 |
| 48 | 1 0 X X 1 1 1 1 | 0 1 1 1 0 1 1 0 0 | 0 1 1 1 0 1 1 0 0 | 1 1 1 0 1 1 0 1 0 | 9 8 7 6 5 4 3 2 1 | 1 1 1 0 1 1 0 1 0 | 1 1 1 0 1 1 0 1 0 | 0 1 1 0 0 0 1 0 0 | 0 1 1 0 0 0 1 0 0 | 9 8 7 6 5 4 3 2 1 | 1 0 1 1 0 1 0 0 1 | 1 0 1 1 0 1 0 0 1 | 1 0 1 1 0 1 0 0 1 | 1 0 1 1 0 1 0 0 1 | 1 0 1 1 0 1 0 0 1 |

Note: 1 = LOW; 0 = HIGH



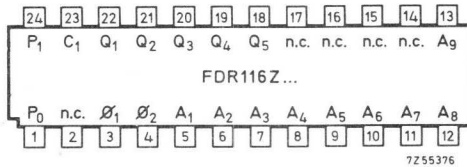
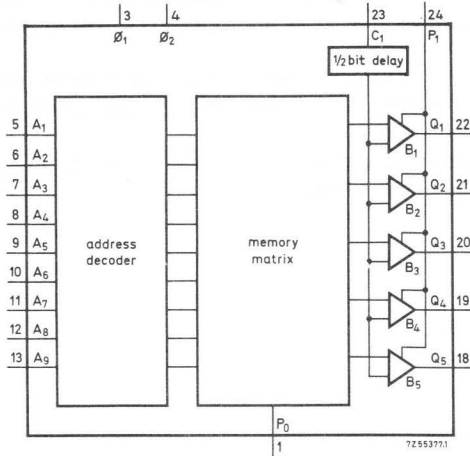
COMPLETE FDR106Z1 BIT PATTERN (continued)

| ADDRESS INPUTS | | ROM CONTENTS | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|---|---------------|---|---|---------------|---|---|---------------|---|---|---------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 00 outputs | | | 01 outputs | | | 10 outputs | | | 11 outputs | | | | | | | | | | | | | | |
| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | | | | | | | | | |
| 49 | 1 | 1 | X | X | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 50 | 1 | 1 | X | X | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 51 | 1 | 1 | X | X | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 52 | 1 | 1 | X | X | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 53 | 1 | 1 | X | X | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 54 | 1 | 1 | X | X | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 55 | 1 | 1 | X | X | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 56 | 1 | 1 | X | X | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 57 | 1 | 1 | X | X | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 58 | 1 | 1 | X | X | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 59 | 1 | 1 | X | X | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 60 | 1 | 1 | X | X | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 61 | 1 | 1 | X | X | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 62 | 1 | 1 | X | X | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 63 | 1 | 1 | X | X | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 64 | 1 | 1 | X | X | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Note: 1 = LOW; 0 = HIGH

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

READ-ONLY MEMORY, 512 WORD, 5 BITS PER WORD



QUICK REFERENCE DATA

| | | |
|-----------------------------------------|------------|---------------|
| Read access time | t_{AR} | max. 850 ns |
| Clock rate | f_{ϕ} | max. 1.2 MHz |
| Power dissipation at $f_{\phi} = 1$ MHz | P_{ϕ} | typ. 90 mw |
| D.C. noise margin | M_L, M_H | > 1 V |
| Operating ambient temperature | T_{amb} | -55 to +85 °C |

PACKAGE OUTLINE 24 lead metal-ceramic dual in-line (See General Section)

GENERAL DESCRIPTION

The FDR116Z is a monolithic 2560 bit read only memory. When ordering an FDR116Z the customer must send a bit pattern matrix with the desired content. For performance evaluation, we can supply specimens of FDR116Z1, which is identical to the FDR116Z but contains a bit pattern of our own. The FDR116Z requires a two phase clock, but the outputs remain steady as long as the address remains unchanged. The normal configuration is as a 512,word, 5 bits per word, parallel output ROM. An output inhibit control allows the use of multiple FDR116Z in a wired-OR configuration.

The memory matrix is programmed with the aid of a mask pattern during manufacture. The only d.c. supply is the output buffer supply, which is variable and can be biased to drive bipolar output loads direct.

The patterns permanently stored in the memory matrix of the FDR116Z1 are described in the following data sheets.



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134) ←

| | | | |
|-----------------------------------------------------------------------------------------------------------|------------------|-------------|----|
| Voltages on all data inputs, clock inputs, outputs and supply terminals, with reference to P ₀ | | +0.5 to -30 | V |
| Power dissipation up to T _{amb} = 25 °C | P _{tot} | max. 1 | W |
| Junction temperature | T _j | max. 150 | °C |
| Storage temperature | T _{stg} | -65 to +150 | °C |
| Total current through terminal P ₂ | -I _{P2} | max. 40 | mA |
| Output current (per output) | ±I _Q | max. 20 | mA |

THERMAL RESISTANCE

| | | | | |
|--------------------------|---------------------|---|-----|------|
| From junction to ambient | R _{th j-a} | = | 125 | °C/W |
|--------------------------|---------------------|---|-----|------|

CHARACTERISTICS at $T_{amb} = -55$ to $+85$ °C

| <u>ELECTRICAL DRIVE REQUIREMENTS</u> | Symbol | min. | typ. | max. | Conditions and references |
|------------------------------------------------------|--------------------|------------------|------|--------------|----------------------------------------------|
| Clock rate | f_{ϕ} | 0.1 | - | 1.2 MHz | see note |
| Clock pulse width | $t_{\phi 1L}$ | 0.50 | - | 1.0 μs | see timing diagram for parameter definitions |
| | $t_{\phi 2L}$ | 0.25 | - | 1.0 μs | |
| Clock pulse fall time | $t_{\phi HL}$ | - | - | 0.10 μs | see note |
| Clock pulse rise time | $t_{\phi LH}$ | - | - | 0.10 μs | |
| Clock delay time | $t_{\phi 1\phi 2}$ | 0 | - | 4.5 μs | |
| Clock delay time | $t_{\phi 2\phi 1}$ | 0 | - | 4.5 μs | |
| Clock input voltage level | | | | | |
| | HIGH | $V_{\phi H}$ | -2 | 0 | +0.3 V |
| LOW | $V_{\phi L}$ | -28 | -26 | -24 V | |
| Address input and output inhibit input logic levels: | | | | | |
| | HIGH | V_{AH}, V_{CH} | -2 | 0 | +0.3 V |
| LOW | V_{AL}, V_{CL} | -14 | -12 | -9 V | |

→ Note

At frequencies higher than 870 kHz, $t_{\phi 1Lmax}$ and $t_{\phi 2Lmin}$ will be determined by $t_{\phi LHmax}$ and $t_{\phi HLmax}$.

CHARACTERISTICS

Test conditions: $V_{P1} = -12\text{ V to } -14\text{ V}$; $T_{amb} = -55\text{ to } +85\text{ }^\circ\text{C}$; $P_0 = \text{grounded}$;
standard load: 30 pF in parallel with 150 k Ω to P_0 .

| <u>ELECTRICAL DATA</u> | Symbol | min. typ. max. | Conditions and references |
|-------------------------------------------------|--------------------|-----------------------|--------------------------------------------------------------------------------------------------------|
| Read access time | t_{AR} | - 750 850 ns | see note 1 |
| <u>Output levels:</u> | | | |
| HIGH | V_{QH} | -1 - 0 V | |
| LOW | V_{QL} | -14 - -10 V | |
| Address input capacitance | C_A | - 3.2 4.0 pF | bias: $V_A = 0\text{ V}$; $f_\phi = 1\text{ MHz}$ |
| Output inhibit input capacitance | C_C | - 3.2 4.0 pF | } bias: $V_C; V_\phi = 0\text{ V}$; $f_\phi = 1\text{ MHz}$ |
| Clock input capacitance | $C_{\phi 1}$ | - 21 30 pF | |
| | $C_{\phi 2}$ | - 13 18 pF | |
| | $C_{\phi 1}$ | - 13 18 pF | } bias: $V_\phi = -26\text{ V}$; $f_\phi = 1\text{ MHz}$ |
| | $C_{\phi 2}$ | - 7.4 10 pF | |
| <u>Leakage currents:</u> | | | |
| Address input and output inhibit input currents | $-I_{AL}, -I_{CL}$ | - - 1 μA | $V_A = V_C = -15\text{ V}$; all other terminals at V_{P0} ; $T_{amb} = 25\text{ }^\circ\text{C}$ |
| Clock input current | $-I_{\phi L}$ | - - 100 μA | $V_\phi = -28\text{ V}$; all other terminals at V_{P0} ; $T_{amb} = 25\text{ }^\circ\text{C}$ |
| <u>Output resistance</u> | | | |
| HIGH | R_{QH} | - 300 - Ω | $V_{P1} = -5\text{ V}$ |
| LOW | R_{QL} | - 170 - Ω | |
| Clock power dissipation (see note 2) | P_ϕ | - 36 - mW | $f_\phi = 1\text{ MHz}$ |
| Input current (see note 3) | $-I_{P1}$ | - 4.0 - mA | $V_{P1} = -13\text{ V}$ $f_\phi = 1\text{ MHz}$ $T_{amb} = 25\text{ }^\circ\text{C}$ |
| <u>Output transition times:</u> | | | |
| fall time | t_{THL} | - 100 - ns | |
| rise time | t_{TLH} | - 100 - ns | |
| <u>Delay times:</u> fall time | t_{DHL} | - 20 - ns | |
| rise time | t_{DLH} | - 20 - ns | |
| D. C. noise margin | M_L, M_H | 1 - - V | |

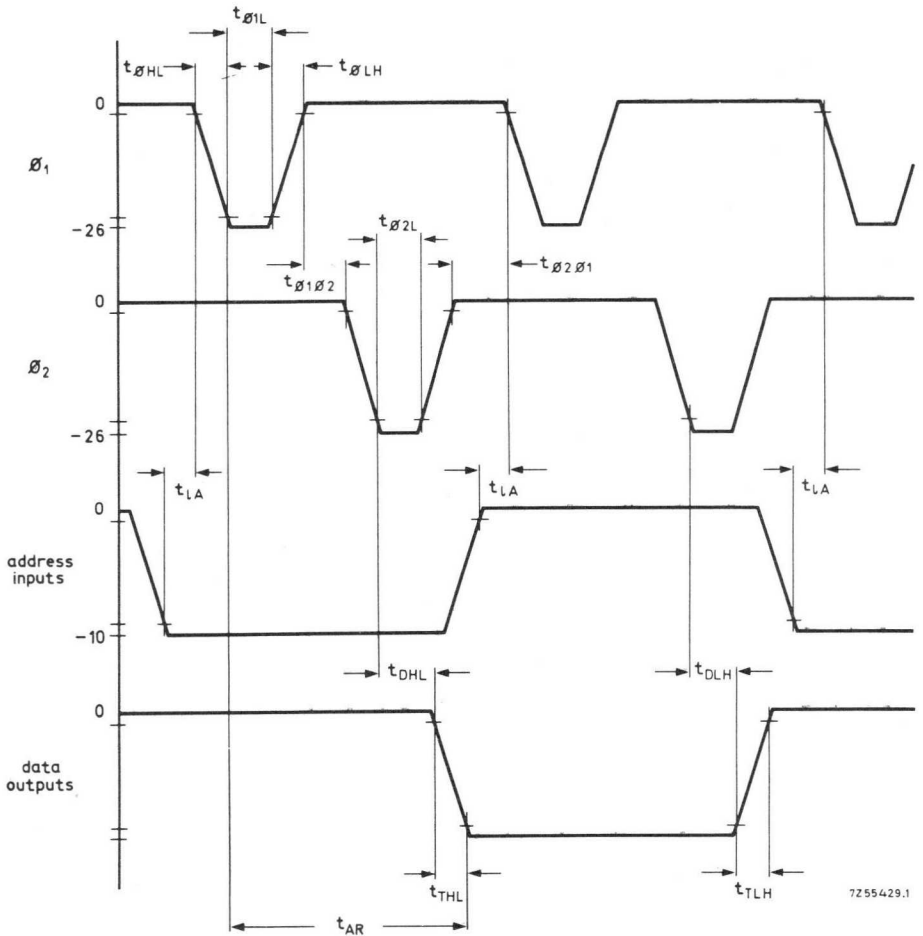
Note 1: The minimum access time assumes the summation of the rise time of ϕ_1 and the fall time of ϕ_2 is less than 40 ns.

Note 2: No d.c. power is dissipated in the decoder or memory matrix; the quoted power dissipation is a.c. only.

Note 3: I_{P1} is almost entirely dependent on the external load.

CHARACTERISTICS (continued)

TIMING DIAGRAM



7255429.1

Note

The indicated points on the vertical axis are specified in the glossary of terms.
Address and output inhibit timing requirements:

1. Address input (and output inhibit input) signals are clocked into the memory during ϕ_1 , and must remain present throughout ϕ_1 . Address lead time (t_{LA}) must be ≥ 0 .
2. The output signals remain steady for as many clock cycles as the address and output inhibit signals remain unchanged.

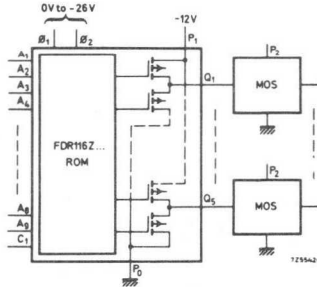
CHARACTERISTICS (continued)GLOSSARY OF TERMS

1. Clock pulse width: $t_{\phi L}$
The time for which the clock pulse is LOW; $V_{\phi} \leq -24$ V
2. Clock pulse fall time: $t_{\phi HL}$
The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock delay time: $t_{\phi 1\phi 2}$; $t_{\phi 2\phi 1}$
The least allowable time between the end of the ϕ_1 (or ϕ_2) clock pulse and the start of the ϕ_2 (or ϕ_1) clock pulse, defined at -2 V.
5. Fall delay time: t_{DHL}
After the clock pulse ϕ_2 reaches LOW, the time that elapses before the output starts to change from HIGH to LOW.
6. Rise delay time: t_{DLH}
After the clock pulse ϕ_2 reaches LOW, the time that elapses before the output starts to change from LOW to HIGH.
7. Output fall transition time: t_{THL}
The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
8. Output rise transition time: t_{TLH}
The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
9. Read access time: t_{AR}
The time between the 90% point on the negative going edge of the clock pulse ϕ_1 and the time at which the output is present, defined at 90%.

OUTPUT BUFFER DESCRIPTION

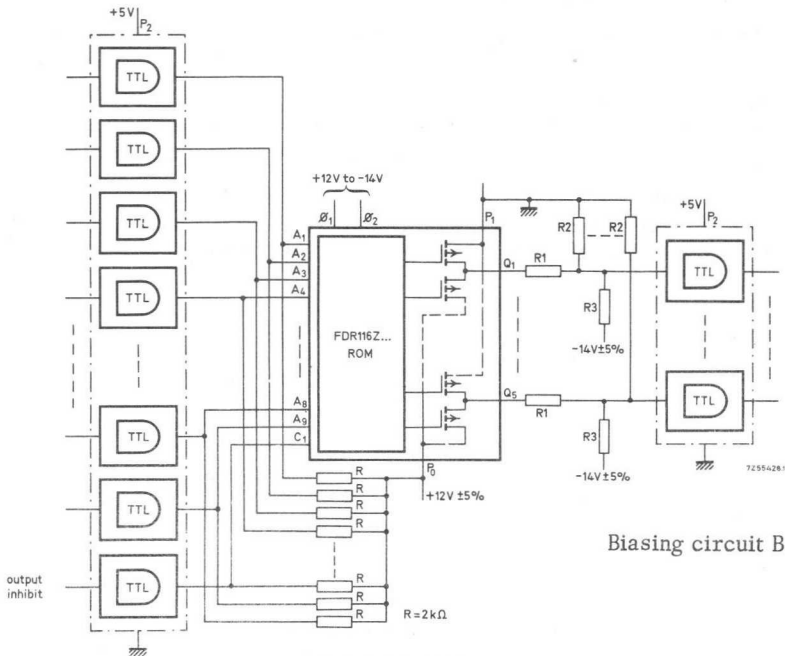
The only d.c. supply required is V_{P1} , the push-pull output buffer supply. V_{P1} may be varied between 0 and -28 V according to the output voltage swing required. It does not affect the operating speed of the memory.

1. Biasing circuit A is used when driving MOS loads. Normal MOS input signals must drive the address and inhibit inputs.



Biasing circuit A.

2. Biasing circuit B may be used to interface with TTL, both at the input and the output of the ROM. Note that no active interface devices are required. At the address and C inputs any TTL devices can be used that will sustain a minimum of $+12\text{ V}$ at their output terminals.

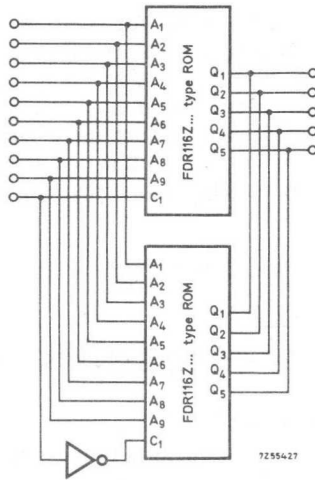


Biasing circuit B.

WIRED-OR APPLICATIONS

Use of wired-or output capability:

Applying a LOW signal to the output inhibit leads will cause both of the push pull output transistors associated with each output driver to turn off. Their output impedances are then very high (about 5 MΩ) and they can be wired-OR with other ROM output buffers without affecting the output drive capability of any buffer operating in the low impedance mode. This output inhibit wired-OR capability makes it possible to use the FDR116Z type ROM in many different applications, such as the one shown here.



1024 words, 5 bits per word ROM

PROCEDURE FOR ORDERING A SPECIAL BIT PATTERN

To ensure accuracy when ordering a special bit pattern for a Read Only Memory (ROM) mask, customers should make use of the form on page 12. Eight forms are needed for 512 word memories. The completed forms enable us to transfer any desired bit pattern into a standard ROM without error. After receipt of the forms our procedure is as follows:

1. An IBM card is punched for each row of each sheet of the form. (If he prefers to do so, the customer may punch his own cards and supply them to us, provided their format is identical with that of the forms).
2. The punched card are incorporated in a computer program that originates the following:
 - a duplicate of the ordered bit pattern, for verification.
 - a control tape for programming final electrical testing of the customers's ROM.
 - a control tape embodying the ordered pattern of ones and zeros to govern the movement of the automatic plotter used in mask making.
3. The computer print-out is checked against the original order forms; a copy is also sent to the customer for his verification and signature.
4. Upon receipts of the customer's signed verification, full scale masks embodying the desired pattern are made.

INSTRUCTION FOR COMPLETING THE FORMS**A. Customer block: ON EACH FORM**

Enter Name, Date and Authorized Signature in the spaces provided.

B. The ADDRESS INPUTS and CONTENTS

Each page of the ROM Bit Pattern Form is laid out for 64 consecutive words; 16 in each of the four columns (00, 01, 10 and 11).

1. ADDRESS INPUTS

- a) There are nine Address Inputs; the right-hand bit is always bit 1 and is the least significant bit; the left-hand bit is bit 9, it is the most significant. The Address Input leads on the ROM package are labelled A₁, A₂, etc., to correspond.
- b) The states of bits 1 to 4 are listed consecutively down the page. The state of bits 5 and 6 are at the head of each of four output columns. The Address Input of 64 consecutive words are thus uniquely specified on each page.
- c) Bit 7, 8 and 9 specify sets of memory locations, 1 set of 64 words per page. These spaces should be filled by the customer using a consecutive full binary code. The first position on page 1 of your specification should be three (or two) zeros. ¹⁾ Memories of 512 words need 8 pages, of specifications.
- d) Only ones (1 = LOW) or zeros (0 = HIGH) should be used in completing the form.

¹⁾ See example on page 12

PROCEDURE FOR ORDERING A SPECIAL BIT PATTERN (continued)**2. CONTENTS (DATA OUTPUTS)**

- a) Each column has provision for words of 10 bits numbered 1 to 10, bit 1 is always the right-hand bit. The output leads of the ROM package are labelled Q₁, Q₂, etc., to correspond.
- b) The requisite bit pattern should be inserted under headings 1 to 5 using only ones (1 = LOW) and zeros (0 = HIGH).

3. AUTHORIZED SIGNATURE

Having completed the bit pattern, the customer should check that the forms are numbered, dated, and signed, as they constitute formal evidence of his request. In the event that the customer provides his own punched cards the signature on the computer duplicate will serve as formal evidence.

CHARACTER GENERATION

The FDR116Z1 is meant for generating ASCII characters for display in a system in which each character is made up of seven 5-bit rows that are traced one at a time. It is capable of storing 64 different characters, each having its own 6-bit address.

To generate a line of characters for display, word addresses are applied in sequence to the WORD SELECT inputs A₁ to A₃ and character addresses to the CHARACTER SELECT inputs A₄ to A₉. First, the row to be traced is selected by applying its address (3 bits) to inputs A₁ to A₃; then the desired characters are selected by applying their addresses (6 bits each) to inputs A₄ to A₉. When one row in a line of characters has been traced, the next row is generated by applying a new word address (inputs A₁ to A₃) and repeating the same sequence of character addresses as before. After the sequence of character addresses has been repeated in conjunction with the word addresses for all seven rows, the full line of characters has been generated. Of the FDR116Z1, a selection is available, which has a maximum read rating of 1.67 MHz (cycle time 600 ns).



| | | OUTPUTS | | | |
|--------------------------------|----------------------------------------------------------------------|----------------|----------------|----------------|----------------|
| | | 05 Q4 Q3 Q2 Q1 | 05 Q4 Q3 Q2 Q1 | 05 Q4 Q3 Q2 Q1 | 05 Q4 Q3 Q2 Q1 |
| | | 00 | 01 | 10 | 11 |
| ASCII CHARACTER ADDRESS INPUTS | WORD SELECT INPUTS | | | | |
| A9 A8 A7 A6 A5 A4 X X | A3 A2 A1 | | | | |
| 0 0 0 X X 0 | 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1 | | | | |
| 0 0 0 X X 1 | 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1 | | | | |
| 0 0 1 X X 0 | 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1 | | | | |
| 0 0 1 X X 1 | 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1 | | | | |



| | | OUTPUTS | | | |
|--------------------------------|----------------------------------------------------------------------|----------------|----------------|----------------|----------------|
| | | 00 | 01 | 10 | 11 |
| | | Q5 Q4 Q3 Q2 Q1 | Q5 Q4 Q3 Q2 Q1 | Q5 Q4 Q3 Q2 Q1 | Q5 Q4 Q3 Q2 Q1 |
| | | ↑ | | | |
| ASCII CHARACTER ADDRESS INPUTS | WORD SELECT INPUTS | | | | |
| A9 A8 A7 A6 A5 A4 | A3 A2 A1 | | | | |
| \overline{X} X | | | | | |
| 0 1 0 X X 0 | 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1 | | | | |
| 0 1 0 X X 1 | 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1 | | | | |
| 0 1 1 X X 0 | 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1 | | | | |
| 0 1 1 X X 1 | 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1 | | | | |

| | | OUTPUTS | | | |
|--------------------------------|----------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------|
| | | 00 | 01 | 10 | 11 |
| ASCII CHARACTER ADDRESS INPUTS | WORD SELECT INPUTS | Q5 Q4 Q3 Q2 Q1 | Q5 Q4 Q3 Q2 Q1 | Q5 Q4 Q3 Q2 Q1 | Q5 Q4 Q3 Q2 Q1 |
| A9 A8 A7 A6 A5 A4 [X X] | A3 A2 A1 | 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 | 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 | 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 | 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 |
| 1 0 0 X X 0 | 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1 | 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 | 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 | 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 | 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 |
| 1 0 0 X X 1 | 0 0 0 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1 | 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 | 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 | 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 | 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 |
| 1 0 1 X X 0 | 0 0 0 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1 | 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 | 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 | 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 | 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 |
| 1 0 1 X X 1 | 0 0 0 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1 | 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 | 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 | 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 | 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 00000 |



| | | OUTPUTS | | | |
|--------------------------------|------------------------------------------------------------------|----------------|----|----|----|
| ASCII CHARACTER ADDRESS INPUTS | WORD SELECT INPUTS | Q5 Q4 Q3 Q2 Q1 | | | |
| | | 00 | 01 | 10 | 11 |
| A9 A8 A7 A6 A5 A4 ┌ X X | A3 A2 A1 000 001 010 011 100 101 110 111 | | | | |
| 1 1 0 X X 0 | 000 001 010 011 100 101 110 111 | | | | |
| 1 1 0 X X 1 | 000 001 010 011 100 101 110 111 | | | | |
| 1 1 1 X X 0 | 000 001 010 011 100 101 110 111 | | | | |
| 1 1 1 X X 1 | 000 001 010 011 100 101 110 111 | | | | |



ROM ORGANISATION

In this example, with the word select input address fixed, the ASCII character addresses are sequentially altered to produce one line of three different characters, left to right. After 8 sequential binary word select iterations using the same character address sequence, the complete line of characters is formed, including a SPACE line.

| A ₃ A ₂ A ₁ word select inputs | ASCII character address for R applied to A ₄ to A ₉ 0 1 0 0 1 0 | ASCII character address for O applied to A ₄ to A ₉ 0 0 1 1 1 1 | ASCII character address for M applied to A ₄ to A ₉ 0 0 1 1 0 1 |
|-----------------------------------------------------------------------|------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------|
| 0 0 0 | row ₁ → 0 0 0 0 0 | → 0 0 0 0 0 | → 0 0 0 0 0 |
| 0 0 1 | row ₂ → 1 1 1 1 0 | → 0 1 1 1 0 | → 1 0 0 0 1 |
| 0 1 0 | row ₃ → 1 0 0 0 1 | → 1 0 0 0 1 | → 1 1 0 1 1 |
| 0 1 1 | row ₄ → 1 0 0 0 1 | → 1 0 0 0 1 | → 1 0 1 0 1 |
| 1 0 0 | row ₅ → 1 1 1 1 0 | → 1 0 0 0 1 | → 1 0 1 0 1 |
| 1 0 1 | row ₆ → 1 0 1 0 0 | → 1 0 0 0 1 | → 1 0 0 0 1 |
| 1 1 0 | row ₇ → 1 0 0 1 0 | → 1 0 0 0 1 | → 1 0 0 0 1 |
| 1 1 1 | row ₈ → 1 0 0 0 1 | → 0 1 1 1 0 | → 1 0 0 0 1 |



1000

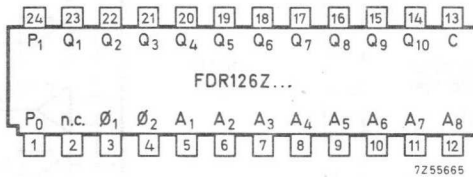
1000

1000

1000

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

READ ONLY MEMORY, 256 WORD, 10 BITS PER WORD

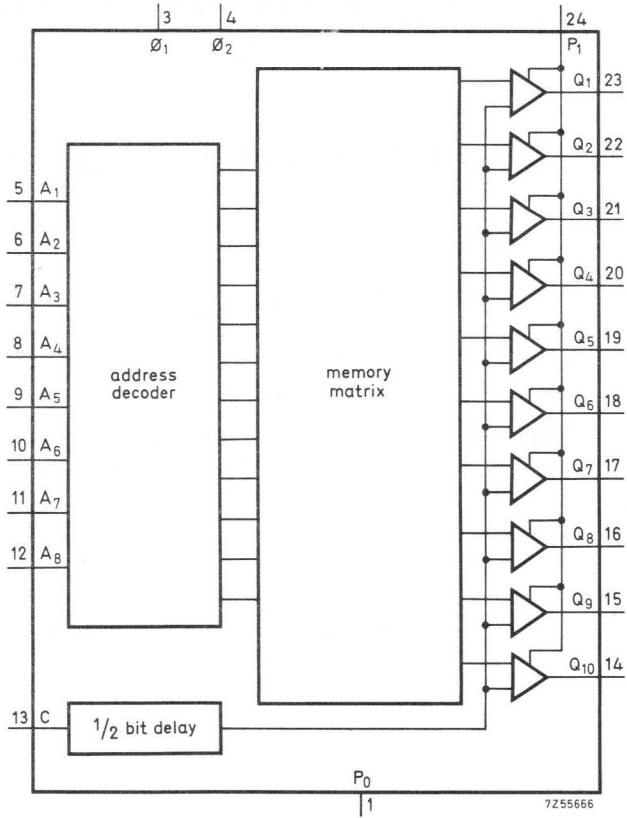


P₀ and metal package bottom are connected.

QUICK REFERENCE DATA

| | | | |
|---------------------------------------------|---------------------------------|------------|--------|
| Read access time | t _{AR} | max. | 1 μs |
| Clock rate | f _φ | 0.1 to | 1 MHz |
| Power dissipation at f _φ = 1 MHz | P _{av} | typ. | 100 mw |
| D. C. noise margin | M _H , M _L | > | 1.0 V |
| Operating ambient temperature | T _{amb} | -55 to +85 | °C |

PACKAGE OUTLINE 24 lead ceramic dual in-line. (See General Section)



GENERAL DESCRIPTION

The FDR126Z is a monolithic 2560 bit read only memory. When ordering an FDR126Z the customer must send a bit pattern matrix (see example on pages 12, 14 to 17) with the desired content. For performance evaluation, we can supply specimens of FDR126Z1, which is identical to the FDR126Z but contains a bit pattern of our own. The FDR126Z requires a two phase clock; the outputs remain steady as long as the address remains unchanged.

The memory matrix is programmed with the aid of a mask pattern during manufacture. The only d. c. supply is the output buffer supply, which is variable and can be biased to drive bipolar output loads direct.

The FDR126Z1 is a pre-programmed version of the FDR126Z READ-ONLY memory. It is intended to convert from ASCII to SELECTRIC line code and vice versa.

When 7-bit address of either code is applied to the inputs of the ROM, the corresponding 7-bits of the other code will appear at the outputs.

The three remaining outputs are used for parity and control code indications.

The electrical characteristics of the FDR126Z1 are equal to those of the FDR126Z.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages on all data inputs, clock inputs, outputs
and supply terminals, with reference to P₀

+0.5 to -30 V

Power dissipation up to T_{amb} = 25 °C

P_{tot} max. 1 W

Junction temperature

T_j max. 150 °C

Storage temperature

T_{stg} -65 to +150 °C

Total current through terminal P₁

-I_{P1} max. 40 mA

Output current (per output)

±I_Q max. 20 mA**THERMAL RESISTANCE**

From junction to ambient

R_{th j-a} = 125 °C/WNote

All terminals are protected against over-voltage caused by static charges.

CHARACTERISTICS at $T_{amb} = -55$ to $+85$ °C

| <u>ELECTRICAL DRIVE REQUIREMENTS</u> | Symbol | min. | typ. | max. | Conditions and references |
|------------------------------------------------------|--------------------------------|--------------|------|------|---------------------------|
| Clock rate | f_{ϕ} | 0.01 | - | 1.0 | MHz |
| Clock pulse width | $t_{\phi 1L}$ $t_{\phi 2L}$ | 0.60 0.25 | - | 5.0 | μs |
| Clock pulse fall time | $t_{\phi HL}$ | - | - | 0.10 | μs |
| Clock pulse rise time | $t_{\phi LH}$ | - | - | 0.10 | μs |
| Clock delay time | $t_{\phi 1\phi 2}$ | 0 | - | 45 | μs |
| Clock delay time | $t_{\phi 2\phi 1}$ | 0 | - | 45 | μs |
| Clock input voltage level | | | | | |
| HIGH | $V_{\phi H}$ | -2 | 0 | +0.3 | V |
| LOW | $V_{\phi L}$ | -28 | -26 | -24 | V |
| Address input and output inhibit input logic levels: | | | | | |
| HIGH | V_{AH}, V_{CH} | -2 | 0 | +0.3 | V |
| LOW | V_{AL}, V_{CL} | -28 | -12 | -9 | V |

see timing diagram for parameter definitions

CHARACTERISTICS (continued)

Test conditions: $V_{P1} = -12$ V to -14 V; $T_{amb} = -55$ to $+85$ °C; $P_0 =$ grounded; standard load: 30 pF in parallel with 150 k Ω to P_0 .

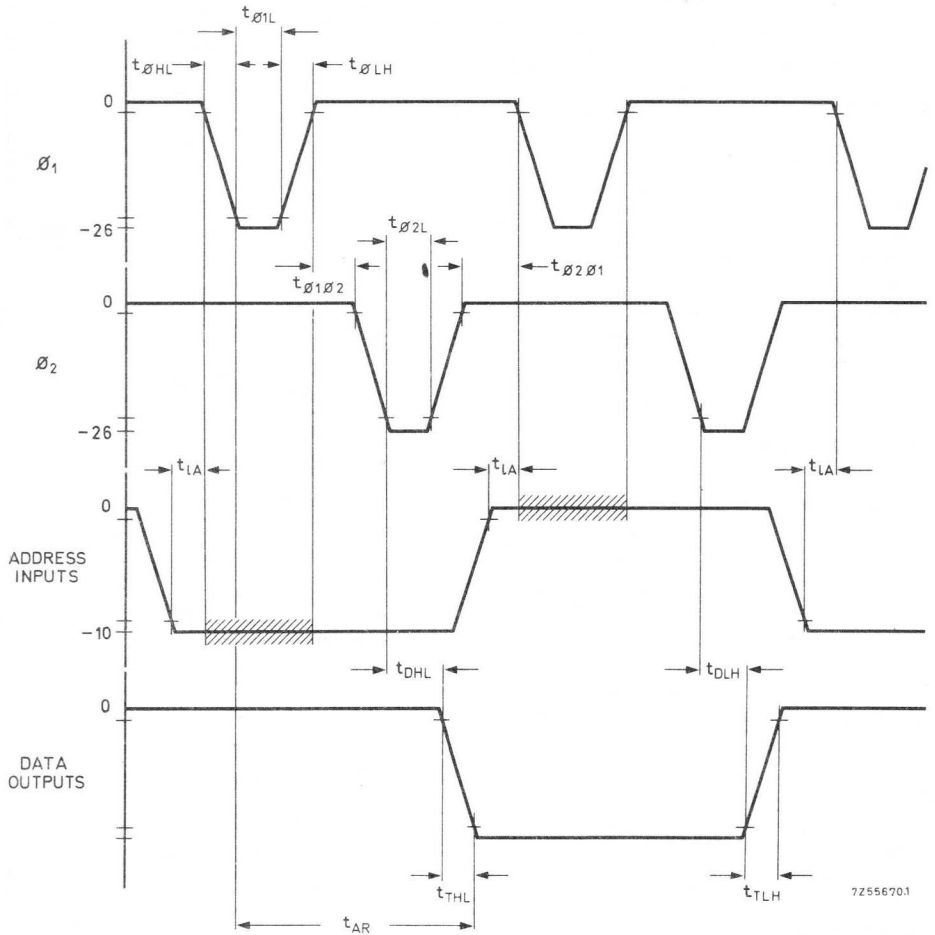
| ELECTRICAL DATA | Symbol | min. | typ. | max. | Conditions and references |
|------------------------------------------------------------|--------------------|------|------|------|------------------------------------------------------------------------------------|
| Read access time | t_{AR} | - | 0.75 | 1 | μ s |
| <u>Output levels:</u> | | | | | |
| HIGH | V_{QH} | -1 | - | 0 | V |
| LOW | V_{QL} | -14 | - | -10 | V |
| Address input capacitance | C_A | - | 3.6 | 5.0 | pF bias: $V_A = 0$ V; $f_\phi = 1$ MHz |
| Output inhibit input capacitance | C_C | - | 3.2 | 4.0 | pF |
| Clock input capacitance | $C_{\phi 1}$ | - | 19 | 30 | pF } bias: $V_C = V_\phi = 0$ V; $f_\phi = 1$ MHz |
| | $C_{\phi 2}$ | - | 20 | 30 | pF |
| | $C_{\phi 1}$ | - | 11 | 20 | pF } bias: $V_\phi = -26$ V; $f_\phi = 1$ MHz |
| | $C_{\phi 2}$ | - | 12 | 20 | pF |
| <u>Leakage currents:</u> | | | | | |
| Address input and output inhibit input currents | $-I_{AL}, -I_{CL}$ | - | - | 1 | μ A } $V_A = V_C = -15$ V; all other terminals at V_{P0} ; $T_{amb} = 25$ °C |
| Clock input current | $-I_{\phi L}$ | - | - | 100 | μ A } $V_\phi = -28$ V; all other terminals at V_{P0} ; $T_{amb} = 25$ °C |
| <u>Output resistance</u> | | | | | |
| HIGH | R_{QH} | - | 400 | - | Ω |
| LOW | R_{QL} | - | 300 | - | Ω $V_{P1} = -5$ V |
| Clock power dissipation (see note 1) ($\phi_1 + \phi_2$) | P_ϕ | - | 36 | - | mW } $f_\phi = 1$ MHz |
| Supply current (see note 2) | $-I_{P1}$ | - | 5.0 | - | mA } $V_{P1} = -13$ V |
| | | | | | } $f_\phi = 1$ MHz |
| | | | | | } $T_{amb} = 25$ °C |
| <u>Output transition times:</u> | | | | | |
| fall time | t_{THL} | - | 100 | - | ns |
| rise time | t_{TLH} | - | 100 | - | ns |
| Delay times: fall time | t_{DHL} | - | 20 | - | ns |
| rise time | t_{DLH} | - | 20 | - | ns |
| D. C. noise margin | M_L, M_H | 1 | - | - | V |

Note 1: No d. c. power is dissipated in the decoder or memory matrix; the quoted power dissipation is a. c. only.

Note 2: I_{P1} is almost entirely dependent on the external load.

CHARACTERISTICS (continued)

TIMING DIAGRAM



72556701

Address and output inhibit timing requirements:

1. Address and output inhibit signals are clocked into the memory during ϕ_1 , and must remain present throughout ϕ_1 . Address and output inhibit lead time (t_{LA}) must be ≥ 0 , during the shaded interval.
2. The output signals remain steady for as many clock cycles as the address and output inhibit signals remain unchanged.

Note:

The indicated points on the vertical axis are specified in the glossary of terms.

CHARACTERISTICS (continued)

GLOSSARY OF TERMS

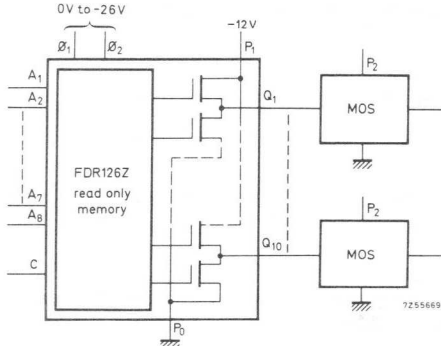
1. Clock pulse width: $t_{\phi L}$
The time for which the clock pulse is LOW; $V_{\phi} \leq -24$ V.
2. Clock pulse fall time: $t_{\phi HL}$
The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock delay time: $t_{\phi 1\phi 2}$; $t_{\phi 2\phi 1}$
The least allowable time between the end of the ϕ_1 (or ϕ_2) clock pulse and the start of the ϕ_2 (or ϕ_1) clock pulse, defined at -2 V.
5. Fall delay time: t_{DHL}
After the clock pulse ϕ_2 reaches LOW, the time that elapses before the output starts to change from HIGH to LOW.
6. Rise delay time: t_{DLH}
After the clock pulse ϕ_2 reaches LOW, the time that elapses before the output starts to change from LOW to HIGH.
7. Output fall transition time: t_{THL}
The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
8. Output rise transition time: t_{TLH}
The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
9. Output inhibit time: t_{CL}
The minimum time that the output inhibit signal must be present during ϕ_2 in order to inhibit the output, defined at -2 V.
10. Read access time: t_{AR}
The time between the 90% point on the leading edge of the clock pulse ϕ_1 and the time at which the output is present.



OUTPUT BUFFER DESCRIPTION

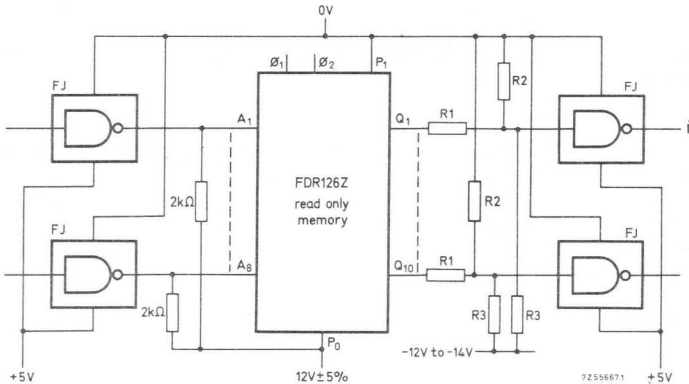
The only d. c. supply required is V_{P1} , the push-pull output buffer supply. V_{P1} may be varied between 0 and -28 V according to the output voltage swing required. It does not affect the operating speed of the memory.

1. Biasing circuit A is used when driving MOS loads. Normal MOS input signals must drive the address and inhibit inputs.



Biasing circuit A

2. Biasing circuit B is used when driving TTL loads direct from each output buffer. This circuit allows also to drive MOS circuits direct from TTL. For this purpose special TTL gates are available (FJH301, FJH311 and FJH321), with a guaranteed minimum output breakdown voltage of 15 V .



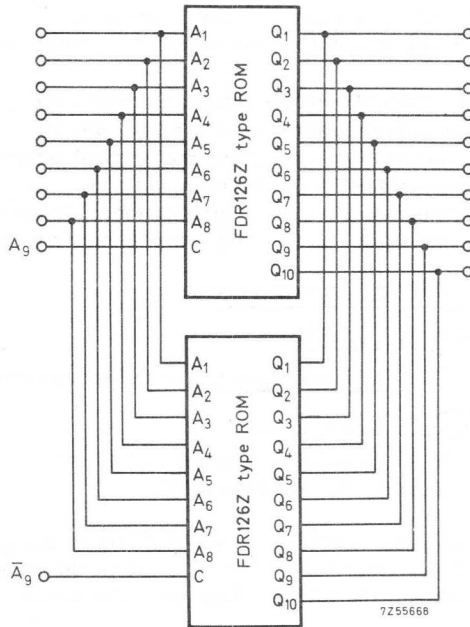
- $R1 = 820\ \Omega$
- $R2 = 820\ \Omega$
- $R3 = 12\ \text{k}\Omega$
- All resistors: $\pm 5\%$

Biasing circuit B

WIRED-OR APPLICATIONS

Use of wired-or output capability:

Applying a LOW signal to the output inhibit leads will cause both of the push pull output transistors associated with each output driver to turn off. Their output impedances are then very high (about 5 MΩ) and they can be wired-or with other ROM output buffers without affecting the output drive capability of any buffer operating in the low impedance mode. This output inhibit wired-or capability makes it possible to use the FDR126Z type ROM in many different applications, such as those shown here. Note that the terminals A₉ and \bar{A}_9 although shown as address inputs, must actually be output inhibit signals synchronous with the address.



PROCEDURE FOR ORDERING A SPECIAL BIT PATTERN

To ensure accuracy when ordering a special bit pattern for a Read Only Memory (ROM) mask, customers should make use of the form on page 12. Four forms are needed for 256 word memories. The completed forms enable us to transfer any desired bit pattern into a standard ROM without error. After receipt of the forms our procedure is as follows:

1. An IBM card is punched for each row of each sheet of the form. (If he prefers to do so, the customer may punch his own cards and supply them to us, provided their format is identical with that of the forms).
2. The punched card are incorporated in a computer program that originates the following:
 - a duplicate of the ordered bit pattern, for verification.
 - a control tape for programming final electrical testing of the customers's ROM.
 - a control tape embodying the ordered pattern of ones and zeros to govern the movement of the automatic plotter used in mask making.
3. The computer print-out is checked against the original order forms; a copy is also sent to the customer for his verification and signature.
4. Upon receipts of the customer's signed verification, full scale masks embodying the desired pattern are made and the unique type number suffix is assigned.

INSTRUCTION FOR COMPLETING THE FORMS**A. Customer block: ON EACH FORM**

Enter Name, Date and Authorized Signature in the spaces provided.

B. The ADDRESS INPUTS and CONTENTS

Each page of the ROM Bit Pattern Form is laid out for 64 consecutive words; 16 in each of the four columns (00, 01, 10 and 11).

1. ADDRESS INPUTS

- a) There are nine Address Inputs; the right-hand bit is always bit 1 and is the least significant bit; the left hand bit is bit 9, it is the most significant. The Address Input leads on the ROM package are labelled A₁, A₂, etc., to correspond.
- b) The states of bits 1 to 4 are listed consecutively down the page. The state of bits 5 and 6 are at the head of each of four output columns. The Address Input of 64 consecutive words are thus uniquely specified on each page.
- c) Bits 7, 8 and 9 (or bits 7 and 8 only, for 256 word memories) specify sets of memory locations, 1 set of 64 words per page. These spaces should be filled by the customer using a consecutive full binary code. The first position on page 1 of your specification should be three (or two) zeros. ¹⁾ Memories of 256 words need 4 pages, of specifications.
- d) Only ones (1 = LOW) or zeros (0 = HIGH) should be used in completing the form except where, as with 256 word memories, column 9 is unused and is, therefore, left blank.

¹⁾ See example on page 12.

2. CONTENTS (DATA OUTPUTS)

- a) Each column has provision for words of 10 bits numbered 1 to 10, bit 1 is always the right-hand bit. The output leads of the ROM package are labelled Q₁, Q₂, etc., to correspond.
- b) The requisite bit pattern should be inserted under headings 1 to 10 using only ones (1 = LOW) and zeros (0 = HIGH), except where a column is unused and is, therefore, left blank.

3. AUTHORIZED SIGNATURE

Having completed the bit pattern, the customer should check that the forms are numbered, dated, and signed, as they constitute formal evidence of his request. In the event that the customer provides his own punched cards the signature on the computer duplicate will serve as formal evidence.





PHILIPS
Electronic Components
and Microcircuits
Integrated Circuits

Read Only Memory Bit Pattern FDR 126 ...

page of

CUSTOMER NAME:

AUTHORIZED SIGNATURE

DATE

| ADDRESS INPUTS | | 00 | 01 | 10 | 11 |
|----------------|---|-------------|-------------|-------------|-------------|
| | | OUTPUTS | OUTPUTS | OUTPUTS | OUTPUTS |
| 9 | 8 | 10987654321 | 10987654321 | 10987654321 | 10987654321 |
| 7 | 6 | X X 0 0 0 0 | X X 0 0 0 0 | X X 0 0 0 0 | X X 0 0 0 0 |
| 5 | 4 | X X 0 0 0 1 | X X 0 0 0 1 | X X 0 0 0 1 | X X 0 0 0 1 |
| 3 | 2 | X X 0 0 1 0 | X X 0 0 1 0 | X X 0 0 1 0 | X X 0 0 1 0 |
| | 1 | X X 0 0 1 1 | X X 0 0 1 1 | X X 0 0 1 1 | X X 0 0 1 1 |
| | | X X 0 1 0 0 | X X 0 1 0 0 | X X 0 1 0 0 | X X 0 1 0 0 |
| | | X X 0 1 0 1 | X X 0 1 0 1 | X X 0 1 0 1 | X X 0 1 0 1 |
| | | X X 0 1 1 0 | X X 0 1 1 0 | X X 0 1 1 0 | X X 0 1 1 0 |
| | | X X 0 1 1 1 | X X 0 1 1 1 | X X 0 1 1 1 | X X 0 1 1 1 |
| | | X X 1 0 0 0 | X X 1 0 0 0 | X X 1 0 0 0 | X X 1 0 0 0 |
| | | X X 1 0 0 1 | X X 1 0 0 1 | X X 1 0 0 1 | X X 1 0 0 1 |
| | | X X 1 0 1 0 | X X 1 0 1 0 | X X 1 0 1 0 | X X 1 0 1 0 |
| | | X X 1 0 1 1 | X X 1 0 1 1 | X X 1 0 1 1 | X X 1 0 1 1 |
| | | X X 1 1 0 0 | X X 1 1 0 0 | X X 1 1 0 0 | X X 1 1 0 0 |
| | | X X 1 1 0 1 | X X 1 1 0 1 | X X 1 1 0 1 | X X 1 1 0 1 |
| | | X X 1 1 1 0 | X X 1 1 1 0 | X X 1 1 1 0 | X X 1 1 1 0 |
| | | X X 1 1 1 1 | X X 1 1 1 1 | X X 1 1 1 1 | X X 1 1 1 1 |

Note: 1 = LOW; 0 = HIGH

GENERAL DESCRIPTION of FDR126Z1

The FDR126Z1 is a version of the FDR126Z pre-programmed to convert from ASCII to SELECTRIC line code and vice versa.

When any 7-bit address of either code is presented to the input the FDR126Z1 will deliver the corresponding word at its output.

The direction of conversion is selected with the eighth address input.

The correspondence between code bits and inputs and outputs is shown in the table below.

| address input | ASCII bit | SELECTRIC bit | output |
|----------------|----------------|---------------|----------------|
| A ₁ | b ₁ | 1 | Q ₁ |
| A ₂ | b ₂ | 2 | Q ₂ |
| A ₃ | b ₃ | 4 | Q ₃ |
| A ₄ | b ₄ | 8 | Q ₄ |
| A ₅ | b ₅ | A | Q ₅ |
| A ₆ | b ₆ | B | Q ₆ |
| A ₇ | b ₇ | S | Q ₇ |

A₈ = LOW: conversion from SELECTRIC line code to ASCII.

A₈ = HIGH: conversion from ASCII to SELECTRIC line code.

Output Q₈ adds an odd parity bit to the 7-bit output code on Q₁ to Q₇ (see note).

Output Q₉ LOW indicates odd parity at the input.

Comparison of the Q₉ output with the parity bit added to the input word indicates whether or not the input code is correct.

If Q₁₀ is LOW, the word on outputs Q₁ to Q₇ is a line control code.

Note:

1 = LOW; 0 = HIGH



ASCII CODE

| ASCII CODE | | row | | | | | | |
|------------|----|-----|----|----|----|----|-----------|--|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | column | |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | NUL | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | DLE | |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | IL1 | |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | PRE2 | |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | SPACE | |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | SPACE1 | |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | DC1 | |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | RS2 | |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | DC2 | |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | PN1 | |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | DC3 | |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | RS1 | |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | DC4 | |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | PF1 | |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | ENQ | |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | UC2 | |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | ACK | |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | ETB | |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | LC1 | |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | P | |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | Q | |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | R | |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | R | |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | S | |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | S | |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | T | |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | T | |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | U | |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | U | |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | V | |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | V | |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | W | |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | W | |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | X | |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | Y | |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | Z | |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | [| |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 |] | |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | ^ | |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | _ | |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | backslash | |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | grave | |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | a | |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | a | |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | b | |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | b | |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | c | |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | c | |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | d | |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | d | |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | e | |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | e | |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | f | |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | f | |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | g | |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | g | |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | h | |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | h | |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | i | |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | i | |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | j | |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | j | |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | k | |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | k | |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | l | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | l | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | m | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | n | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | o | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | p | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | q | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | r | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | r | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | s | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | s | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | t | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | t | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | u | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | u | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | v | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | v | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | w | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | w | |

Note: 1 = LOW; 0 = HIGH

ASCII CODE (continued)

| b7 ↑ | b6 ↑ | b5 ↑ | column ↑ | | | | row ↓ | | | | | | | | | | | | |
|---------|---------|---------|-------------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| b4 ↑ | b3 ↑ | b2 ↑ | b1 ↑ | row ↓ | row ↓ | row ↓ | | row ↓ | row ↓ | row ↓ | row ↓ | row ↓ | row ↓ | row ↓ | row ↓ | row ↓ | row ↓ | row ↓ | row ↓ |
| 1 | 0 | 0 | 0 | | BS | CAN | ! | | | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | | HT | EM |) | | | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | | LF | SUB | * | | | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | | VT | ESC | + | | | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | | FF | FS | , | | | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | | CR | GS | - | | | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | | SO | RS | . | | | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | | SI | US | / | | | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |

Note: 1 = LOW; 0 = HIGH


SELETRIC LINE CODE TO ASCII CODE CORRESPONDENCE (continued)

| | S | | | B | | | A | | | 8 4 2 1 | | | | | | | |
|---------|-----|-----|-----|-----|-----|------|----|------|-----|---------|-----|----|------|-----|------|-----|----|
| | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | | | | | |
| | | | | | | | | | | | | | | | | | |
| | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | | | | | |
| | ↑ | ↑ | ↑ | ↑ | ↑ | ↑ | ↑ | ↑ | ↑ | ↑ | ↑ | ↑ | | | | | |
| | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | | | | | |
| | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | | | | | |
| | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | | | | | |
| | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | | | | | |
| | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | ↔ | | | | | |
| 1 0 0 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 0 0 1 | 0 | 0 | 1 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | | | | | | | |
| 1 0 1 0 | 4 | 4 | 0 | h | h | h | h | h | h | h | h | h | h | h | h | h | h |
| 1 0 1 1 | 9 | 9 | 9 | b | b | b | b | b | b | b | b | b | b | b | b | b | b |
| 1 1 0 0 | PN1 | DC2 | BY1 | SUB | LF1 | EOB1 | SO | EOT1 | UC1 | EOB1 | ETX | SO | EOT1 | UC1 | EOB1 | ETX | SO |
| 1 1 0 1 | RS1 | DC3 | LF1 | LF | BS1 | ETX | SO | EOT1 | UC1 | EOB1 | ETX | SO | EOT1 | UC1 | EOB1 | ETX | SO |
| 1 1 1 0 | PN1 | DC2 | BY1 | SUB | LF1 | EOB1 | SO | EOT1 | UC1 | EOB1 | ETX | SO | EOT1 | UC1 | EOB1 | ETX | SO |
| 1 1 1 1 | RS1 | DC3 | LF1 | LF | BS1 | ETX | SO | EOT1 | UC1 | EOB1 | ETX | SO | EOT1 | UC1 | EOB1 | ETX | SO |
| 1 0 0 0 | z | z | ① | RS | VT | RS | z | z | z | z | z | z | z | z | z | z | z |
| 1 0 0 1 | 0 | 0 | h | h | h | h | h | h | h | h | h | h | h | h | h | h | h |
| 1 0 1 0 | z | z | ① | RS | VT | RS | z | z | z | z | z | z | z | z | z | z | z |
| 1 0 1 1 | 9 | 9 | b | b | b | b | b | b | b | b | b | b | b | b | b | b | b |
| 1 1 0 0 | PN1 | DC2 | BY1 | SUB | LF1 | EOB1 | SO | EOT1 | UC1 | EOB1 | ETX | SO | EOT1 | UC1 | EOB1 | ETX | SO |
| 1 1 0 1 | RS1 | DC3 | LF1 | LF | BS1 | ETX | SO | EOT1 | UC1 | EOB1 | ETX | SO | EOT1 | UC1 | EOB1 | ETX | SO |
| 1 1 1 0 | PN1 | DC2 | BY1 | SUB | LF1 | EOB1 | SO | EOT1 | UC1 | EOB1 | ETX | SO | EOT1 | UC1 | EOB1 | ETX | SO |
| 1 1 1 1 | RS1 | DC3 | LF1 | LF | BS1 | ETX | SO | EOT1 | UC1 | EOB1 | ETX | SO | EOT1 | UC1 | EOB1 | ETX | SO |

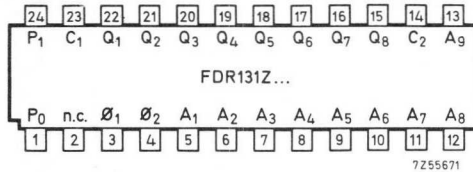
Note: 1 = LOW; 0 = HIGH



1000
1000
1000
1000
1000

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

READ ONLY MEMORY, 512 WORD, 8 BITS PER WORD

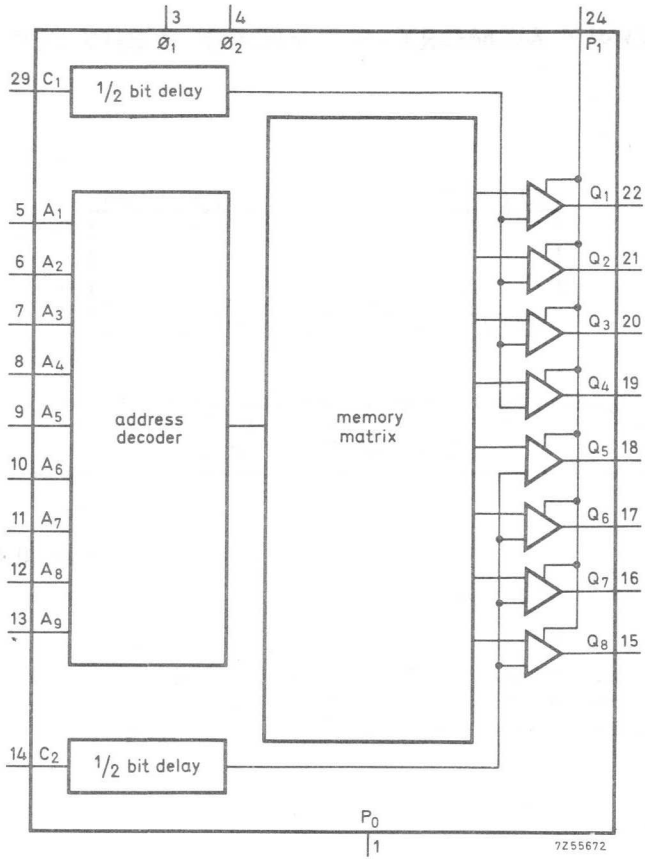


P₀ and metal lid on bottom of the package are connected

QUICK REFERENCE DATA

| | | | | |
|-------------------------------|---------------------------------|------|---------|-----|
| Read access time | t _{AR} | max. | 1.5 | μs |
| Clock rate | f _φ | max. | 0.66 | MHz |
| Power dissipation (MOS load) | P _{tot} | typ. | 100 | mW |
| D.C. noise margin | M _H , M _L | > | 1.0 | V |
| Operating ambient temperature | T _{amb} | | 0 to 70 | °C |

PACKAGE OUTLINE 24 lead ceramic dual in-line. (See page 18)



GENERAL DESCRIPTION

The FDR131Z is a monolithic 4096-bit READ-only memory (ROM) with a capacity of 512 words, 8 bits per word. With two output-inhibit control lines C₁ and C₂ it can also operate as a 1024-word, 4 bits per word memory. The memory matrix is given the desired content by means of a special mask. When ordering, customers have to complete a set of forms specifying the bit pattern to be associated with each address. The output-inhibit control make it possible to use several FDR131Z memories in wired-OR configuration.

The only d. c. supply is the output buffer supply (P₁), which may be adapted to interface direct with either MOS or bipolar DTL/TTL. All terminals of the FD circuits are effectively protected against over voltage caused by static charge.

A pre-programmed specimen of the FDR131Z is the FDR131Z1 given on page 14.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|-----------------------------------------------------------------------------------------------------------|------------------|-------------|----|
| Voltages on all data inputs, clock inputs, outputs and supply terminals, with reference to P ₀ | | +0.5 to -30 | V |
| Power dissipation up to T _{amb} = 25 °C | P _{tot} | max. 1 | W |
| Junction temperature | T _j | max. 150 | °C |
| Storage temperature | T _{stg} | -65 to +150 | °C |
| Total current through terminal P ₁ | -IP ₁ | max. 40 | mA |
| Output current (per output) | ±IQ | max. 20 | mA |

THERMAL RESISTANCE

| | | | | |
|--------------------------|---------------------|---|-----|------|
| From junction to ambient | R _{th j-a} | = | 125 | °C/W |
|--------------------------|---------------------|---|-----|------|

CHARACTERISTICS at $T_{amb} = 0$ to $+70$ °C

| <u>ELECTRICAL DRIVE REQUIREMENTS</u> | Symbol | min. | typ. | max. | Conditions and references |
|------------------------------------------------------|----------------------------------|--------------|------|----------------------------|----------------------------------------------|
| Clock rate | f_{ϕ} | 0.1 | - | 0.66 MHz | (see note) |
| Clock pulse width | $t_{\phi 1L}$ $t_{\phi 2L}$ | 0.90 0.35 | - | 2.0 μ s 2.0 μ s | see timing diagram for parameter definitions |
| Clock pulse rise time (ϕ_1, ϕ_2) | $t_{\phi LH}$ | - | - | 1.0 μ s | } See note |
| Clock pulse fall time | $t_{\phi 1HL}$ $t_{\phi 2HL}$ | 0.165 - | - | 1.0 μ s 1.0 μ s | |
| Clock delay time | $t_{\phi 1\phi 2}$ | 0 | - | 4.5 μ s | |
| Clock delay time | $t_{\phi 2\phi 1}$ | 0 | - | 4.5 μ s | |
| Clock input voltage level | | | | | |
| HIGH | $V_{\phi H}$ | -2 | 0 | +0.3 V | |
| LOW | $V_{\phi L}$ | -28 | -26 | -24 V | |
| Address input and output inhibit input logic levels: | | | | | |
| HIGH | V_{AH}, V_{CH} | -2 | 0 | +0.3 V | |
| LOW | V_{AL}, V_{CL} | -14 | -12 | -9 V | |

Note:

At frequencies higher than 191 kHz the maximum clock pulse rise and fall times will be determined by the minimum ϕ_1 and ϕ_2 pulse width.

CHARACTERISTICS

Test conditions: $V_{P1} = -12\text{ V to } -14\text{ V}$; $T_{amb} = 0\text{ to } +70\text{ }^\circ\text{C}$; $P_0 = \text{grounded}$; standard load: 30 pF in parallel with 150 k Ω to P_0 .

| <u>ELECTRICAL DATA</u> | Symbol | min. | typ. | max. | Conditions and references |
|------------------------------------------------------------|----------------------|------|------|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Read access time | t_{AR} | - | 1.2 | 1.5 μs | see note 1 |
| <u>Output levels:</u> | | | | | |
| HIGH | V_{QH} | -1 | - | 0 V | |
| LOW | V_{QL} | -14 | - | -10 V | |
| Address input and output inhibit input capacitances | C_A, C_C | - | 3.2 | 4.0 pF | { bias: $V_A = V_C = 0\text{ V}$; $f_\phi = 1\text{ MHz}$ |
| Clock input capacitance | $C_{\phi 1}$ | - | 18 | 22 pF | |
| | $C_{\phi 2}$ | - | 16 | 20 pF | |
| | $C_{\phi 1}$ | - | 11 | 14 pF | { bias: $V_\phi = -26\text{ V}$; $f_\phi = 1\text{ MHz}$ |
| | $C_{\phi 2}$ | - | 9.5 | 12 pF | |
| <u>Leakage currents:</u> | | | | | |
| Address input and output inhibit input currents | $-I_{ILL}, -I_{ICL}$ | - | - | 1 μA | { $V_A = V_C = -15\text{ V}$; all other terminals at V_{P0} ; $T_{amb} = 25\text{ }^\circ\text{C}$ $V_\phi = -28\text{ V}$; all other terminals at V_{P0} ; $T_{amb} = 25\text{ }^\circ\text{C}$ |
| Clock input current | $-I_{\phi L}$ | - | - | 100 μA | |
| <u>Output resistance</u> | | | | | |
| HIGH | R_{QH} | - | 500 | Ω | $V_{P1} = -5\text{ V}$ |
| LOW | R_{QL} | - | 350 | Ω | |
| Clock power dissipation (see note 2) ($\phi_1 + \phi_2$) | P_ϕ | - | 36 | mW | $f_\phi = 1\text{ MHz}$ |
| Supply current (see note 3) | $-I_{P1}$ | - | 4.0 | mA | { $V_{P1} = -13\text{ V}$ $f_\phi = 1\text{ MHz}$ $T_{amb} = 25\text{ }^\circ\text{C}$ |
| <u>Output transition times:</u> | | | | | |
| fall time | t_{THL} | - | 200 | ns | |
| rise time | t_{TLH} | - | 200 | ns | |
| <u>Delay times:</u> fall time | t_{DHL} | - | 20 | ns | |
| rise time | t_{DLH} | - | 20 | ns | |
| D.C. noise margin | M_L, M_H | 1 | - | V | |

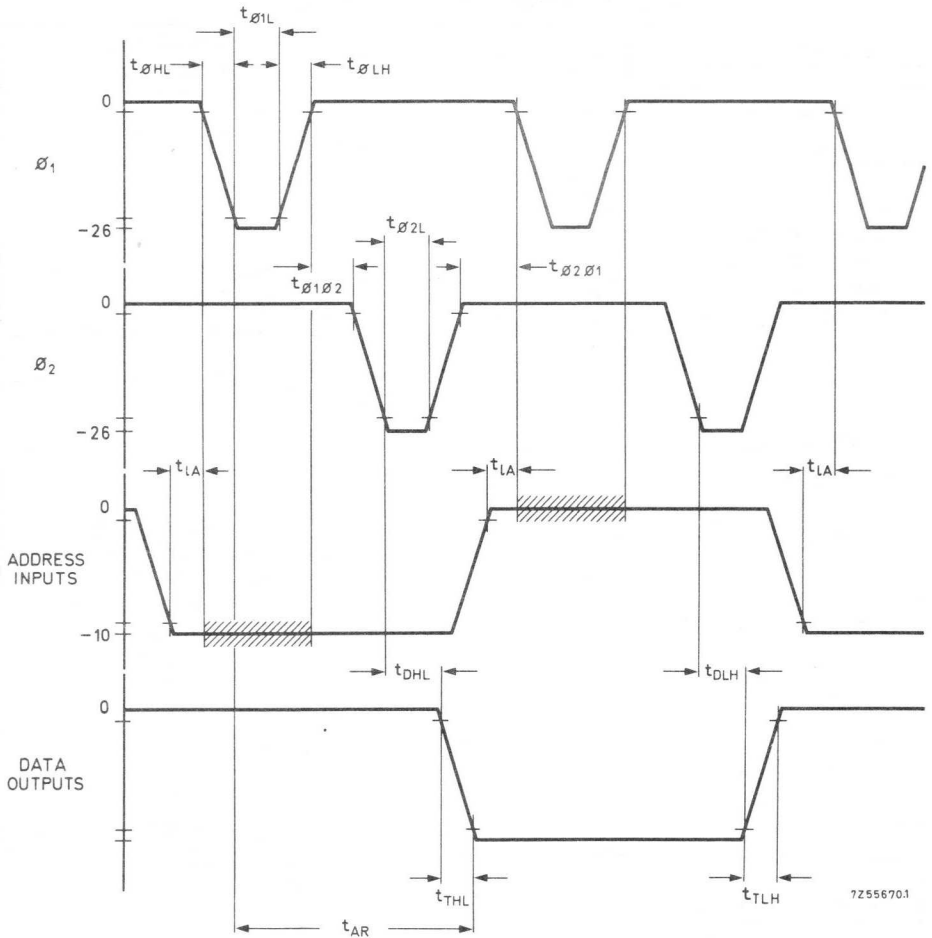
Note 1: Assuming the fall time of ϕ_1 and rise time of ϕ_2 is less than 40 ns.

Note 2: No d.c. power is dissipated in the decoder or memory matrix; the quoted power dissipation is a.c. only.

Note 3: I_{P1} is almost entirely dependent on the external load.

CHARACTERISTICS (continued)

TIMING DIAGRAM



72556701

Address and output inhibit requirements:

1. Address and output inhibit signals are clocked into the memory during ϕ_1 , and must remain present during the shaded interval. Address lead time (t_{lA}) must be ≥ 0 .
2. The output signals remain steady when the address and output inhibit signals remain unchanged.

Note:

The indicated points on the vertical axis are specified in the glossary of terms.

CHARACTERISTICS (continued)

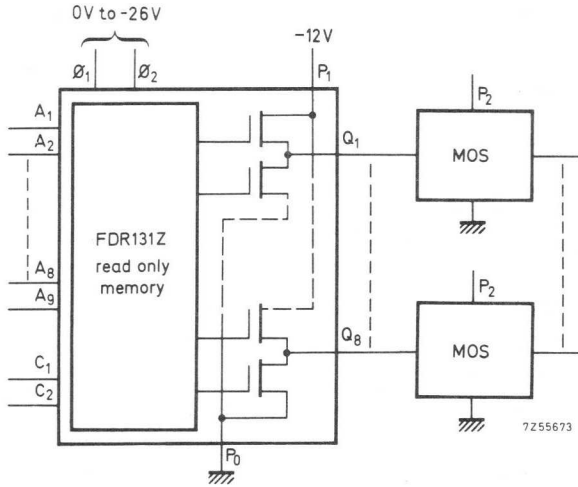
GLOSSARY OF TERMS

1. Clock pulse width: $t_{\phi L}$
The time for which the clock pulse is LOW; $V_{\phi} \leq -24$ V
2. Clock pulse fall time: $t_{\phi HL}$
The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock delay time: $t_{\phi 1\phi 2}$; $t_{\phi 2\phi 1}$
The least allowable time between the end of the ϕ_1 (or ϕ_2) clock pulse and the start of the ϕ_2 (or ϕ_1) clock pulse, defined at -2 V.
5. Fall delay time: t_{DHL}
After the clock pulse ϕ_2 reaches LOW, the time that elapses before the output start to change from HIGH to LOW.
6. Rise delay time: t_{DLH}
After the clock pulse ϕ_2 reaches LOW, the time that elapses before the output starts to change from LOW to HIGH.
7. Output fall transition time: t_{THL}
The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
8. Output rise transition time: t_{TLH}
The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
9. Read access time: t_{AR}
The time between the 90% point on the leading edge of the clock pulse ϕ_1 and the time at which the output is present, defined at 90%.

OUTPUT BUFFER DESCRIPTION

The only d.c. supply required is V_{P1} , the push-pull output buffer supply. V_{P1} may be varied between 0 and -28 V according to the output voltage swing required. It does not affect the operating speed of the memory.

1. Biasing circuit A is used when driving MOS loads. Normal MOS input signals must drive the address and inhibit inputs.

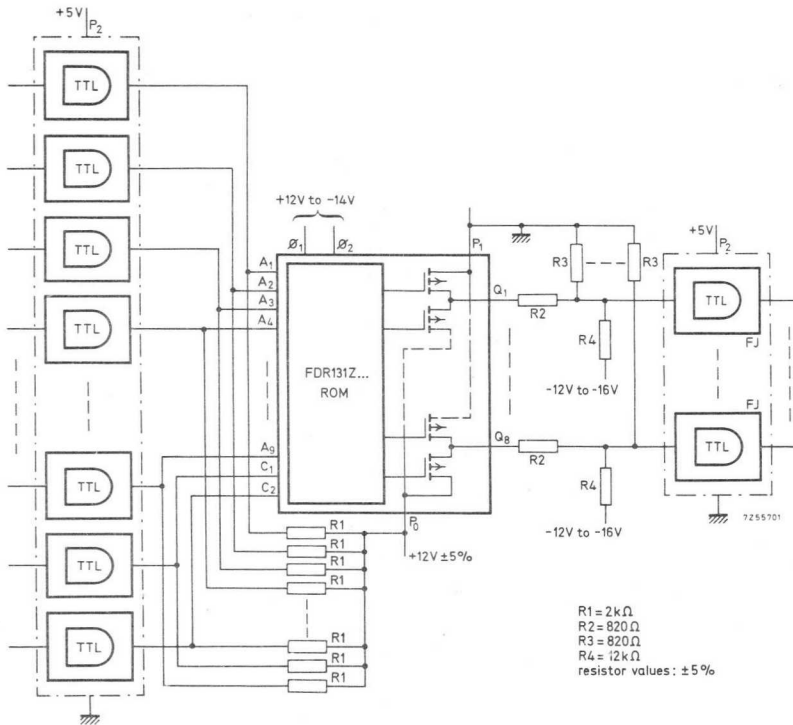


Biasing circuit A

OUTPUT BUFFER DESCRIPTION (continued)

2. Biasing circuit B is used to interface direct with TTL on both the inputs and outputs of the READ-only memory. No active interface components are required. The TTL circuits on the inputs of the ROM must be able to sustain at least +12V at their outputs.

The quadruple NAND gate FJH301 and the sextuple inverter FJH321 are especially manufactured with a guaranteed breakdown voltage of 15 V for this purpose.



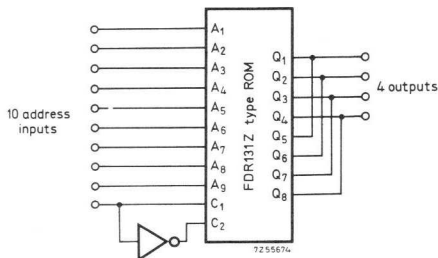
WIRED-OR APPLICATIONS

Use of wired-or output capability:

Applying a LOW signal to the output inhibit leads will cause both of the push pull output transistors associated with each output driver to turn off. Their output impedances are then very high (about 5 MΩ) and they can be wired-or with other ROM output buffers without affecting the output drive capability of any buffer operating in the low impedance mode. C₁ controls output buffers 1 to 4, and C₂ controls output buffers 5 to 8. This output inhibit wired-or capability makes it possible to use the FDR131Z type ROM in many different applications, such as those shown here.

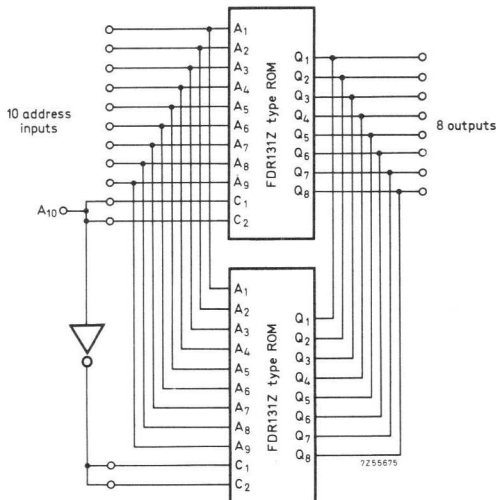
1024 words

4-bits per word



1024 words

8-bits per word



PROCEDURE FOR ORDERING A SPECIAL BIT PATTERN

To ensure accuracy when ordering a special bit pattern for a Read Only Memory (ROM) mask, customers should make use of the form on page 13. Eight forms are needed for 512 word memories. The completed forms enable us to transfer any desired bit pattern into a standard ROM without error. After receipt of the forms our procedure is as follows:

1. An IBM card is punched for each row of each sheet of the form. (If he prefers to do so, the customer may punch his own cards and supply them to us, provided their format is identical with that of the forms).
2. The punched cards are incorporated in a computer program that originates the following:
 - a duplicate of the ordered bit pattern, for verification.
 - a control tape for programming final electrical testing of the customer's ROM.
 - a control tape embodying the ordered pattern of ones and zeros to govern the movement of the automatic plotter used in mask making.
3. The computer print-out is checked against the original order forms; a copy is also sent to the customer for his verification and signature.
4. Upon receipts of the customer's signed verification, full scale masks embodying the desired pattern are made and the unique type number suffix is assigned.

INSTRUCTION FOR COMPLETING THE FORMSA. Customer block: ON EACH FORM

Enter Name, Date and Authorized Signature in the spaces provided.

B. The ADDRESS INPUTS and CONTENTS

Each page of the ROM Bit Pattern Form is laid-out for 64 consecutive words; 16 in each of the four columns (00, 01, 10 and 11).

1. ADDRESS INPUTS

- a) There are nine Address Inputs; the right-hand bit is always bit 1 and is the least significant bit; the left-hand bit is 9, it is the most significant. The Address Input leads on the ROM package are labelled A₁, A₂, etc., to correspond.
- b) The states of bits 1 to 4 are listed consecutively down the page. The state of bits 5 and 6 are at the head of each of four output columns. The Address Input of 64 consecutive words are thus uniquely specified on each page.
- c) Bit 7, 8, and 9 (or bits 7 and 8 only, for 256 word memories) specify sets of memory locations, 1 set of 64 words per page. These spaces should be filled by the customer using a consecutive full binary code. The first position on page 1 of your specification should be three (or two) zeros. ¹⁾ Memories of 256 words need 4 pages, of specifications.
- d) Only ones (1 = LOW) or zeros (0 = HIGH) should be used in completing the form except where, a column is unused and is, therefore, left blank.

¹⁾ See example on page 13

2. CONTENTS (DATA OUTPUTS)

- a) Each column has provision for words of 10 bits numbered 1 to 10, bit 1 is always the right-hand bit. The output leads of the ROM package are labelled Q₁, Q₂, etc., to correspond.
- b) The requisite bit pattern should be inserted under headings 1 to 10 using only ones (1 = LOW) and zeros (0 = HIGH), except where a column is unused and is, therefore, left blank.

3. AUTHORIZED SIGNATURE

Having completed the bit pattern, the customer should check that the forms are numbered, dated, and signed, as they constitute formal evidence of his request. In the event that the customer provides his own punched cards the signature on the computer duplicate will serve as formal evidence.



Read Only Memory Bit Pattern FDR 131 ...

page of

AUTHORIZED SIGNATURE

CUSTOMER NAME:

DATE

FD family

FDR131Z
FDR131Z1

| ADDRESS INPUTS | CONTENTS | | |
|----------------|-------------|-------------|-------------|
| | 00 | 01 | 10 |
| 987654321 | 10987654321 | 10987654321 | 10987654321 |
| X X 0 0 0 0 | | | |
| X X 0 0 0 1 | | | |
| X X 0 0 1 0 | | | |
| X X 0 0 1 1 | | | |
| X X 0 1 0 0 | | | |
| X X 0 1 0 1 | | | |
| X X 0 1 1 0 | | | |
| X X 0 1 1 1 | | | |
| X X 1 0 0 0 | | | |
| X X 1 0 0 1 | | | |
| X X 1 0 1 0 | | | |
| X X 1 0 1 1 | | | |
| X X 1 1 0 0 | | | |
| X X 1 1 0 1 | | | |
| X X 1 1 1 0 | | | |
| X X 1 1 1 1 | | | |

Note: 1 = LOW; 0 = HIGH



GENERAL DESCRIPTION of FDR131Z 1

The FDR131Z1 is a version of the FDR131Z pre-programmed to convert from ASCII to EBCDIC and vice versa.

When the standard 7-bit ASCII code plus parity is presented to address inputs A₁ to A₈, the FDR131Z1 will deliver the corresponding 8-bit EBCDIC code at its outputs, when the A₉ input is HIGH. Conversely, when the standard 8-bit EBCDIC code is presented to inputs A₁ to A₈, the corresponding ASCII code plus parity will be delivered at the outputs when A₉ is LOW. The code conversion circuits from ASCII to EBCDIC are provided in duplicate to accommodate either odd or even parity. The correspondence between code bits and inputs and outputs is shown in the tables below and on the following pages.

Conversion from ASCII to EBCDIC

| ASCII-bits | ROM inputs ¹⁾ | ROM outputs | EBCDIC-bit s |
|----------------------------------------|--------------------------|----------------|---------------------------|
| b ₁ (least significant bit) | A ₁ | Q ₁ | 7 (least significant bit) |
| b ₂ | A ₂ | Q ₂ | 6 |
| b ₃ | A ₃ | Q ₃ | 5 |
| b ₄ | A ₄ | Q ₄ | 4 |
| b ₅ | A ₅ | Q ₅ | 3 |
| b ₆ | A ₆ | Q ₆ | 2 |
| b ₇ (most significant bit) | A ₇ | Q ₇ | 1 |
| b ₈ (odd or even parity) | A ₈ | Q ₈ | 0 (most significant bit) |

Correspondence of ASCII(A) to EBCDIC(E) code

To find the 7-bit ASCII code for a particular symbol, (see table on page 15) write down the binary coded decimal number belonging to that symbol; e. g., the number belonging to the letter g is 103, which means that the corresponding binary digits for bits b₇ to b₁ of the ASCII code are 1100111.

¹⁾ Condition: A₉ is HIGH

Correspondence of ASCII(A) to EBCDIC(E) code (continued)

| | 0-15 | | 16-31 | | 32-47 | | 48-63 | | 64-79 | | 80-95 | | 96-111 | | 112-127 | |
|----|------|-----|-------|-----|-------|----|-------|---|-------|---|-------|---|--------|---|---------|-----|
| | A | E | A | E | A | E | A | E | A | E | A | E | A | E | A | E |
| 0 | NUL | NUL | DLE | DLE | SP | SP | 0 | 0 | @ | @ | P | P | \ | ↑ | p | p |
| 1 | SOH | SOH | DC1 | DC1 | ! | ! | 1 | 1 | A | A | Q | Q | a | a | q | q |
| 2 | STX | STX | DC2 | DC2 | " | " | 2 | 2 | B | B | R | R | b | b | r | r |
| 3 | ETX | ETX | DC3 | DC3 | # | # | 3 | 3 | C | C | S | S | c | c | s | s |
| 4 | EOT | EOT | DC4 | DC4 | \$ | \$ | 4 | 4 | D | D | T | T | d | d | t | t |
| 5 | ENQ | ENQ | NAK | NAK | % | % | 5 | 5 | E | E | U | U | e | e | u | u |
| 6 | ACK | ACK | SYN | SYN | & | & | 6 | 6 | F | F | V | V | f | f | v | v |
| 7 | BEL | BEL | ETB | EOB | / | ' | 7 | 7 | G | G | W | W | g | g | w | w |
| 8 | BS | BS | CAN | CAN | (| (| 8 | 8 | H | H | X | X | h | h | x | x |
| 9 | HT | HT | EM | EM |) |) | 9 | 9 | I | I | Y | Y | i | i | y | y |
| 10 | LF | LF | SUB | SUB | * | * | : | : | J | J | Z | Z | j | j | z | z |
| 11 | VT | VT | ESC | PRE | + | + | ; | ; | K | K | [| (| k | k | { | (|
| 12 | FF | FF | FS | IFS | , | , | < | < | L | L | \ | / | l | l | : | |
| 13 | CR | CR | GS | IGS | - | - | = | = | M | M |] |) | m | m |] |) |
| 14 | SO | SO | RS | IRS | . | . | > | > | N | N | ^ | ⌋ | n | n | ~ | ¢ |
| 15 | SI | SI | US | IUS | / | / | ? | ? | O | O | - | - | o | o | DEL | DEL |

Explanation of symbols

- | | |
|---------------------------|---------------------------------|
| NUL = null | DLE = data link escape |
| SOH = start of heading | DC1 to DC4 = device control |
| STX = start of text | NAK = negative acknowledge |
| ETX = end of text | SYN = synchronous idle |
| EOT = end of transmission | ETB = end of transmission block |
| ENQ = enquiry | CAN = cancel |
| ACK = acknowledge | EM = end of medium |
| BEL = bell | SUB = substitute |
| BS = backspace | ESC = escape |
| HT = horizontal tab | FS = file separator |
| FF = form-feed | GS = group separator |
| CR = carriage return | RS = record separator |
| SO = shift out | US = unit separator |
| SI = shift in | DEL = delete (rub out) |

The ASCII to EBCDIC characters for which there was no correspondence have been converted as follows:

| 128-ASCII | 256-EBCDIC | 128-ASCII | 256-EBCDIC |
|-----------|------------|-----------|------------|
| [| (| \ | ↑ 1) |
| \ | / | { | (|
|] |) | } |) |
| ^ | ⌋ | ~ | ¢ |

1) The EBCDIC to ASCII is ' to /

Conversion from EBCDIC to ASCII

When the standard 8-bit EBCDIC code is presented to inputs A₁ to A₈, the corresponding ASCII code plus parity will be delivered at the outputs when A₉ is LOW.

| EBCDIC-bits | ROM-inputs ¹⁾ | ROM-outputs | ASCII-bits |
|---------------------------|--------------------------|----------------|----------------------------------------|
| 7 (least significant bit) | A ₁ | Q ₁ | b ₁ (least significant bit) |
| 6 | A ₂ | Q ₂ | b ₂ |
| 5 | A ₃ | Q ₃ | b ₃ |
| 4 | A ₄ | Q ₄ | b ₄ |
| 3 | A ₅ | Q ₅ | b ₅ |
| 2 | A ₆ | Q ₆ | b ₆ |
| 1 | A ₇ | Q ₇ | b ₇ (most significant bit) |
| 0 (most significant bit) | A ₈ | Q ₈ | b ₈ (even parity) |

Correspondence of EBCDIC to ASCII code

| | 0-15 | | 16-31 | | 32-47 | | 48-63 | | 64-79 | | 80-95 | | 96-111 | | 112-127 | |
|----|------|-----|-------|-----|-------|-----|-------|-----|-------|----|-------|---|--------|---|---------|---|
| | E | A | E | A | E | A | E | A | E | A | E | A | E | A | E | A |
| 0 | NUL | NUL | DLE | DLE | DS | - | - | - | SP | SP | & | & | - | - | - | - |
| 1 | SOH | SOH | DC1 | DC1 | SOS | - | - | - | - | - | - | - | / | / | - | - |
| 2 | STX | STX | DC2 | DC2 | FS | - | SYN | SYN | - | - | - | - | - | - | - | - |
| 3 | ETX | ETX | DC3 | DC3 | - | - | - | - | - | - | - | - | - | - | - | - |
| 4 | PF | - | RES | - | BYP | - | PN | - | - | - | - | - | - | - | - | - |
| 5 | HT | HT | NL | - | LF | LF | RS | - | - | - | - | - | - | - | - | - |
| 6 | LC | - | BS | BS | EOB | ETB | VC | - | - | - | - | - | - | - | - | - |
| 7 | DEL | DEL | IL | - | PRE | ESC | EOT | EOT | - | - | - | - | - | - | - | - |
| 8 | - | - | CAN | CAN | - | - | - | - | - | - | - | - | - | - | - | - |
| 9 | - | - | EM | EM | - | - | - | - | - | - | - | - | - | - | - | - |
| 10 | SMM | - | CC | - | SM | - | - | - | ⌘ | - | ! | ! | - | - | : | : |
| 11 | VT | VT | - | - | - | - | - | - | . | . | ⌘ | ⌘ | , | , | # | # |
| 12 | FF | FF | IFS | FS | - | - | DC4 | DC4 | < | < | * | * | % | % | @ | @ |
| 13 | CR | CR | IGS | GS | ENQ | ENQ | NAK | NAK | (| (|) |) | - | - | , | / |
| 14 | SO | SO | IRS | RS | ACK | ACK | - | - | + | + | ; | ; | > | > | = | = |
| 15 | SI | SI | IUS | US | BEL | BEL | SUB | SUB | | : | ⌘ | - | ? | ? | " | " |

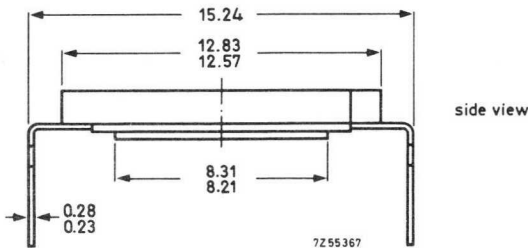
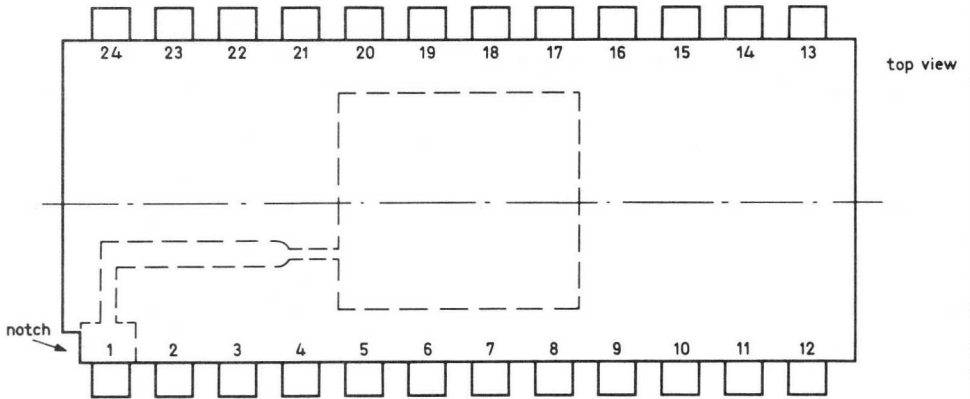
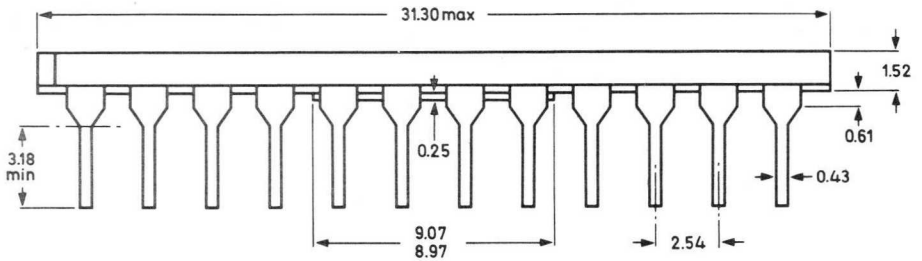
¹⁾ Condition: A₉ = LOW

Correspondence of EBCDIC to ASCII code (continued)

To find the 8-bit EBCDIC code for a particular symbol (see table below and on page 16), write down the decimal number belonging to that symbol; e. g. , the number belonging to the letter g is 135, which means the corresponding number for the bit positions 0 to 7 of the EBCDIC code is 10000111.

| 128-143 | | 144-159 | | 160-175 | | 176-191 | | 192-207 | | 208-223 | | 224-239 | | 240-255 | |
|---------|---|---------|---|---------|---|---------|---|---------|---|---------|---|---------|---|---------|---|
| E | A | E | A | E | A | E | A | E | A | E | A | E | A | E | A |
| - | - | - | - | - | - | - | - | - | - | - | - | - | - | 0 | 0 |
| a | a | j | j | - | - | - | - | A | A | J | J | - | - | 1 | 1 |
| b | b | k | k | s | s | - | - | B | B | K | K | S | S | 2 | 2 |
| c | c | l | l | t | t | - | - | C | C | L | L | T | T | 3 | 3 |
| d | d | m | m | u | u | - | - | D | D | M | M | U | U | 4 | 4 |
| e | e | n | n | v | v | - | - | E | E | N | N | V | V | 5 | 5 |
| f | f | o | o | w | w | - | - | F | F | O | O | W | W | 6 | 6 |
| g | g | p | p | x | x | - | - | G | G | P | P | X | X | 7 | 7 |
| h | h | q | q | y | y | - | - | H | H | Q | Q | Y | Y | 8 | 8 |
| i | i | r | r | z | z | - | - | I | I | R | R | Z | Z | 9 | 9 |
| - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |

PACKAGE OUTLINE 24 lead metal-ceramic dual in-line



Notes

1. Leads on opposite sides are designed to fit in holes 15.24 mm apart.
2. Pin 1 is marked by a notch and connected to the metal lid on the bottom of the package.

Linear integrated circuits



100
100
100
100
100
100
100
100

INTEGRATED CIRCUIT AMPLIFIER FOR IN THE EAR HEARING AID

Monolithic semiconductor integrated-circuit amplifier in a plastic envelope, primarily intended for in the ear hearing aids.

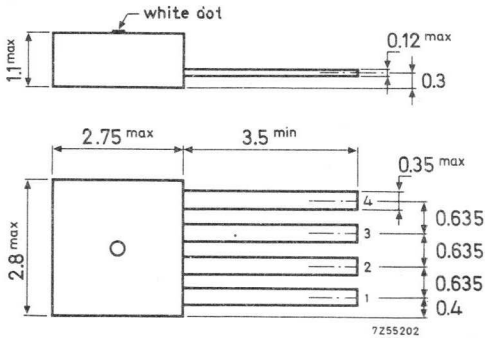
QUICK REFERENCE DATA

For meaning of symbols: see page 3 fig. 1.

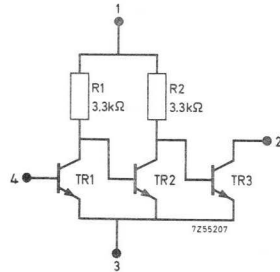
| | | | |
|------------------------------------------------------------|-----------|------|--------|
| Supply voltage | V_{1-3} | max. | 5 V |
| Output current | I_2 | max. | 5 mA |
| Total power dissipation up to $T_{amb} = 25^\circ\text{C}$ | P_{tot} | max. | 25 mW |
| In a practical circuit as given on page 3 fig. 1: | | | |
| Total supply current | I_{tot} | typ. | 1 mA |
| Transducer gain | G_{tr} | > | 75 dB |
| | | typ. | 80 dB |
| Power output at $d_{tot} = 10\%$ | P_o | > | 0.2 mW |
| Cut-off frequency (-3 dB) | f_c | > | 20 kHz |

PACKAGE OUTLINE

Dimensions in mm



CIRCUIT DIAGRAM



The sealing of the plastic envelope withstands the accelerated damp heat test of IEC recommendation 68-2 (test D, severity IV, 6 cycles).

RATINGS (Limiting values)¹⁾

(for meaning of symbols see page 3, fig. 1)

Voltages

| | | | |
|----------------|------------|------|-------------------|
| Supply voltage | V_{1-3} | max. | 5 V |
| Output voltage | V_{2-3} | max. | 5 V ²⁾ |
| Input voltage | $-V_{4-3}$ | max. | 5 V |

Currents

| | | | |
|----------------|-------|------|------|
| Output current | I_2 | max. | 5 mA |
| Input current | I_4 | max. | 5 mA |

Power dissipation

| | | | |
|--------------------------------------|-----------|------|-------|
| Total power dissipation (See page 6) | P_{tot} | max. | 25 mW |
|--------------------------------------|-----------|------|-------|

Temperatures

| | | | |
|---------------------|-----------|------------|-------|
| Storage temperature | T_{stg} | -20 to +80 | °C |
| Ambient temperature | T_{amb} | max. | 80 °C |

CHARACTERISTICS at $V_{1-3} = 1.3$ V and $T_{amb} = 25$ °C unless otherwise specified

I_2 see figure 1

| | | | |
|-----------------------------------------------------|-----------|------|---------|
| <u>Supply current</u> (no signal) | I_{tot} | < | 1.2 mA |
| | I_1 | typ. | 0.34 mA |
| <u>Transducer gain</u> ³⁾ at $f = 1$ kHz | G_{tr} | > | 75 dB |
| | | typ. | 80 dB |
| $V_{1-3} = 1.3$ V; $T_{amb} = -10$ °C | G_{tr} | typ. | 78 dB |
| $V_{1-3} = 1.1$ V; $T_{amb} = 25$ °C | G_{tr} | typ. | 76 dB |

¹⁾ Limiting values according to the Absolute Maximum System as defined in IEC publication 134.

²⁾ This value may be exceeded during inductive switch-off for transient energies < 10 μ Ws.

³⁾ The transducer gain is defined as the ratio of the output power in the load of $|Z| = 1.5$ k Ω and the available input power of the source with $R_S = 5$ k Ω

$$G_{tr} = \frac{P_o}{V_1^2/4R_S}$$

CHARACTERISTICS (continued)

at $V_{1-3} = 1.3 \text{ V}$ and $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ unless otherwise specified

I_2 see figure 1

Total distortion at $f = 1 \text{ kHz}$

$P_O = 100 \text{ } \mu\text{W}$ d_{tot} typ. 4 %
 $< 6 \text{ } \%$

$P_O = 200 \text{ } \mu\text{W}$ d_{tot} $< 10 \text{ } \%$

Noise figure at $R_S = 5 \text{ k}\Omega$

Bandwidth $f = 400 \text{ to } 3200 \text{ Hz}$ $F < 6 \text{ dB}$

Cut-off frequency (-3 dB)

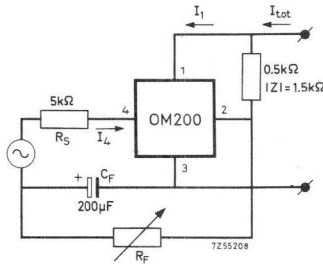
$f_c > 20 \text{ kHz}$

Value of R_F to adjust I_2 at 0.7 mA

$> 50 \text{ k}\Omega$
 R_F typ. $300 \text{ k}\Omega$
 $< 700 \text{ k}\Omega$

$I_2 = 0.7 \text{ mA}$,
 adjusted by means of R_F .
 $V_{1-3} = 1.3 \text{ V}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$.

Fig. 1



SOLDERING RECOMMENDATION

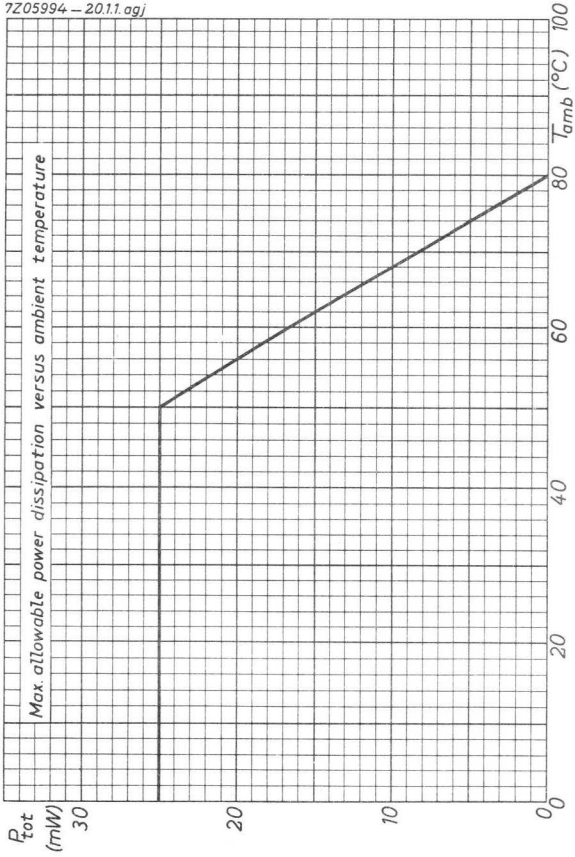
A: Iron soldering

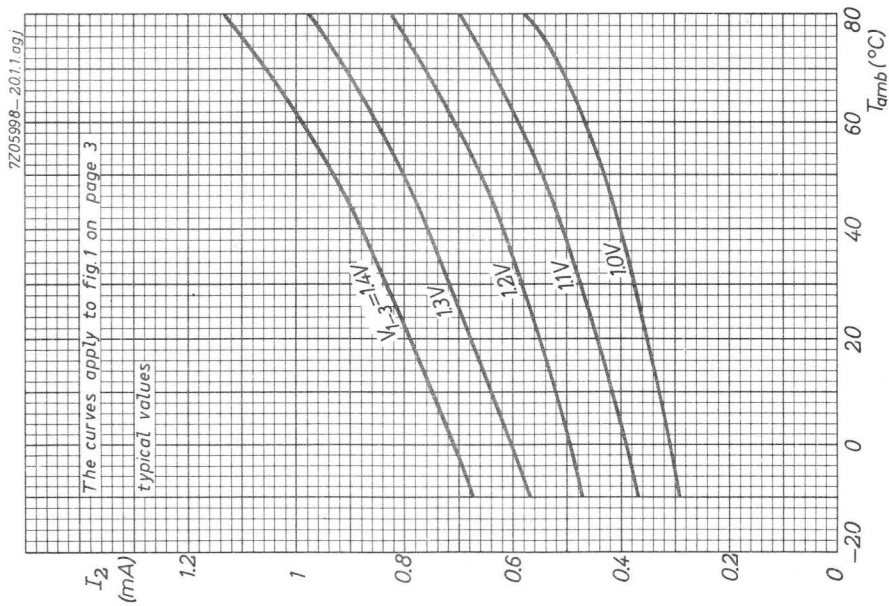
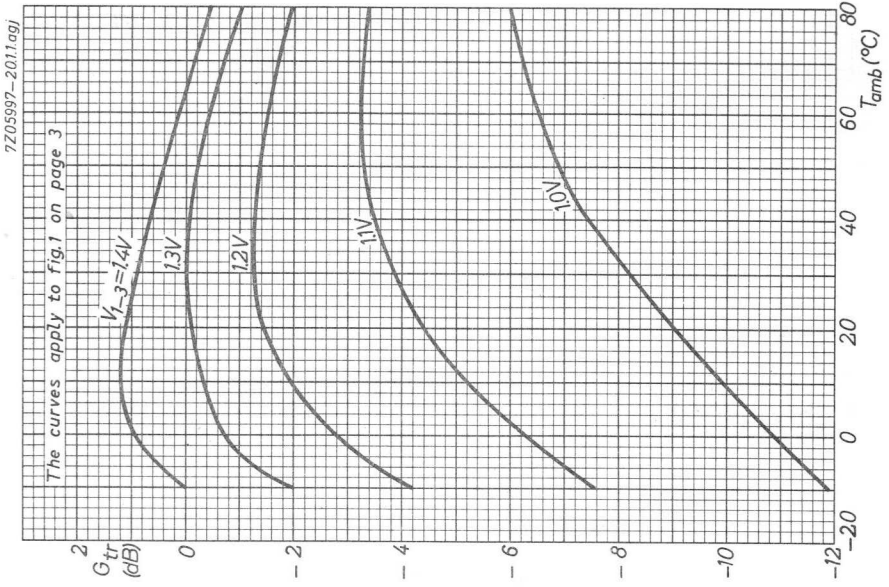
At a maximum iron temperature of $300 \text{ }^\circ\text{C}$ the maximum permissible soldering time is 3 seconds, provided the soldering spot is at least 0.5 mm from the seal and the leads are not soldered at the same time. Soldering in immediate subsequence is allowed.

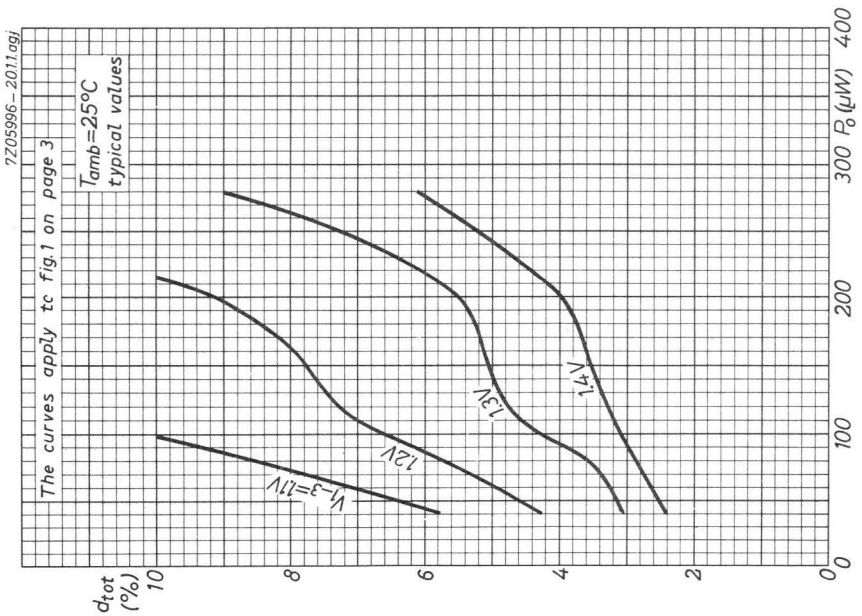
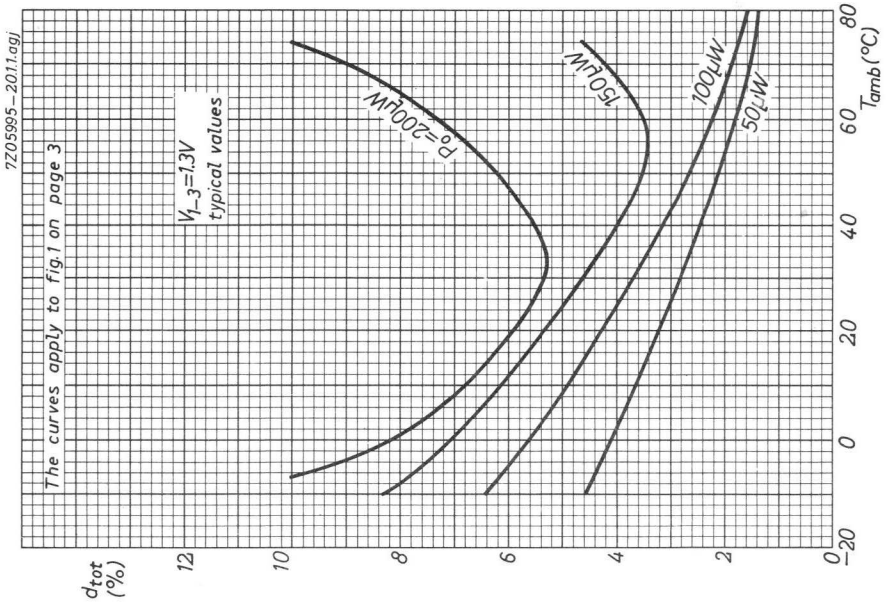
B: Dip soldering

At a maximum solder temperature of $250 \text{ }^\circ\text{C}$ the maximum permissible soldering time is 3 seconds, provided the soldering spot is at least 0.5 mm from the seal.

7Z05994 - 201.1.agj







LOW-LEVEL AMPLIFIER

The TAA263 is a semiconductor integrated amplifier in a 4-lead TO-72 metal envelope. It comprises a three-stage, direct coupled low-level amplifier for use from d.c. up to frequencies of 600 kHz.

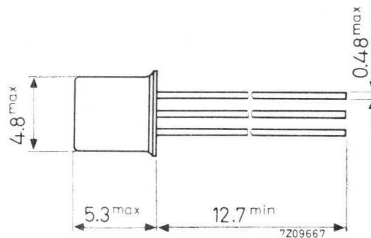
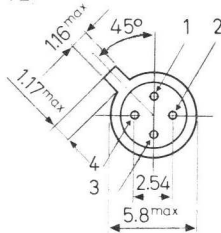
QUICK REFERENCE DATA

| | | | |
|----------------------------------|-----------|-------------|-------------|
| Supply voltage | V_B | max. | 8 V |
| Output voltage | V_{3-4} | max. | 7 V |
| Output current | I_3 | max. | 25 mA |
| Transducer gain at $P_O = 10$ mW | | | |
| $R_L = 150 \Omega$; $f = 1$ kHz | G_{tr} | typ. | 77 dB |
| Operating ambient temperature | T_{amb} | -20 to +100 | $^{\circ}C$ |

PACKAGE OUTLINE

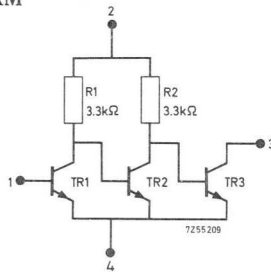
Dimensions in mm

TO-72



TAA263

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

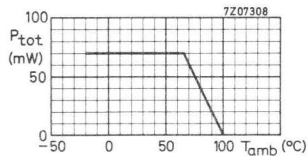
| | | | |
|----------------|------------|------|-----|
| Supply voltage | V_B | max. | 8 V |
| Output voltage | V_{3-4} | max. | 7 V |
| Input voltage | $-V_{1-4}$ | max. | 5 V |

Currents

| | | | |
|----------------|-------|------|-------|
| Output current | I_3 | max. | 25 mA |
| Input current | I_1 | max. | 10 mA |

Power dissipation

| | | | |
|------------------------------------------------------------|-----------|------|-------|
| Total power dissipation up to $T_{amb} = 65^\circ\text{C}$ | P_{tot} | max. | 70 mW |
|------------------------------------------------------------|-----------|------|-------|



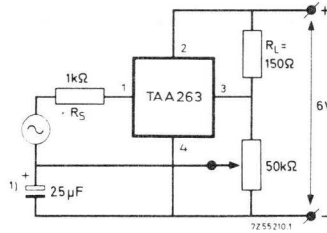
Temperatures

| | | |
|-------------------------------|-----------|----------------|
| Storage temperature | T_{stg} | -65 to +100 °C |
| Operating ambient temperature | T_{amb} | -20 to +100 °C |

CHARACTERISTICS

$T_{amb} = 25\text{ }^{\circ}\text{C}$

Test circuit:



Currents

| | | | |
|---------------------------------|-------------|------|-------|
| Output current | I_3 | typ. | 12 mA |
| Total current drain (no signal) | $I_2 + I_3$ | < | 16 mA |

Over-all small signal current gain

| | | | |
|--------------------|--------------------|------|----------------|
| $f = 1\text{ kHz}$ | $h_{f\text{ tot}}$ | typ. | $5 \cdot 10^5$ |
|--------------------|--------------------|------|----------------|

Transducer gain

| | | | |
|----------------------------------------|----------|------|-------|
| $f = 1\text{ kHz}; P_O = 10\text{ mW}$ | G_{tr} | > | 70 dB |
| | | typ. | 77 dB |

Output power at $f = 1\text{ kHz}; d_{tot} = 10\%$
 $d_{tot} = 5\%$

| | | |
|-------|---|-------|
| P_O | > | 10 mW |
| P_O | > | 8 mW |

Noise figure

| | | | |
|-----------------------------------------------|-----|------|--------|
| $f = 400\text{ Hz to } 6\text{ kHz}$ | F | typ. | 5 dB |
| | | < | 10 dB |
| $f = 450\text{ kHz}; \Delta f = 5\text{ kHz}$ | F | typ. | 2.7 dB |

¹⁾ $Z \leq 10\text{ }\Omega$ at $f = 1\text{ kHz}$

CHARACTERISTICS (continued)

 $T_{amb} = 25\text{ }^{\circ}\text{C}$ y parameters (point 4 common connection) $V_B = 6\text{ V}; I_3 = 3\text{ mA}; V_{3-4} = 4.2\text{ V}$ $f = 1\text{ kHz}$

Input admittance

 $y_i = g_i$ typ. 20 $\mu\Omega^{-1}$

Transfer admittance

 $y_f = g_f$ typ. 11 Ω^{-1}

Output admittance

 $y_o = g_o$ typ. 60 $\mu\Omega^{-1}$ $f = 450\text{ kHz}$

Input conductance

 g_i typ. 15 $\mu\Omega^{-1}$

Input capacitance

 C_i typ. 14 pF

Transfer admittance

 $|y_f|$ typ. 9.4 Ω^{-1}

Phase angle of transfer admittance

 φ_f typ. 125°

Output conductance

 g_o typ. 20 $\mu\Omega^{-1}$

Output capacitance

 C_o typ. 13 pF

GENERAL PURPOSE AMPLIFIER

The TAA293 is a general purpose integrated amplifier which can be applied in various audio and i.f. applications. Its configuration furthermore allows the use of the TAA293 in multivibrators, pulse amplifiers, trigger circuits, etc.

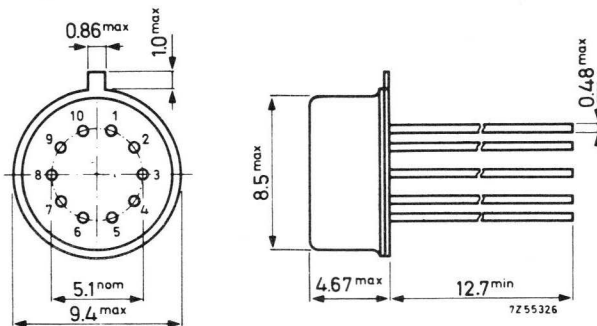
QUICK REFERENCE DATA

| | | | |
|------------------------------------------------------------------------------------------------|------------------|-----------|---------|
| Supply voltage | V ₇₋₄ | nom. +6.0 | V |
| Small signal current gain of first transistor I _g = 1 mA; V _{g-1} = 1 V | h _{fe} | typ. | 80 |
| Transducer gain | G _{tr} | typ. | 80 dB |
| Noise figure (30 to 15 000 Hz) | F | typ. | 6 dB |
| Frequency response (-3 dB) | | typ. | 600 kHz |
| Output power | P _o | > | 10 mW |

PACKAGE OUTLINE

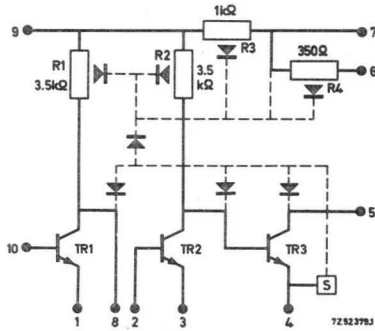
Dimensions in mm

TO-74; reduced height



TAA293

CIRCUIT DIAGRAM



Note:

The diodes drawn with dotted lines are the parasitic diodes formed by the P-N junction of the resistor-diffusions in the N-isle and of the N-isle to the P-substrate respectively. Taking account of the parasitic diodes one can prevent any unwanted effects due to their becoming conducting under certain conditions of d.c. potentials or signal voltages.

RATINGS Limiting values in Accordance with the Absolute Maximum System (IEC134)

Voltages

| | |
|------------|--------------------------|
| V_{9-1} | max. 7.0 V |
| V_{8-1} | max. 7.0 V |
| V_{8-10} | max. 7.0 V |
| V_{9-3} | max. 7.0 V |
| V_{9-4} | max. 7.0 V |
| V_{8-4} | max. 7.0 V |
| V_{7-4} | max. 7.0 V ¹⁾ |
| V_{6-4} | max. 7.0 V |
| V_{5-4} | max. 7.0 V |
| V_{1-10} | max. 6.0 V |
| V_{3-2} | max. 6.0 V |

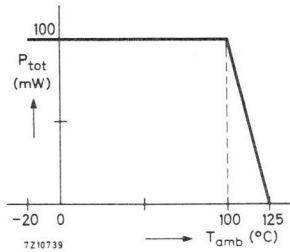
Currents

| | |
|----------|------------|
| I_5 | max. 40 mA |
| $-I_4$ | max. 40 mA |
| $-I_1$ | max. 20 mA |
| I_8 | max. 20 mA |
| $-I_3$ | max. 10 mA |
| I_{10} | max. 10 mA |
| I_2 | max. 10 mA |

→ ¹⁾ Pin 7 must be at the highest potential to avoid unwanted influence of the parasite diodes.

RATINGS (continued)

Total power dissipation



Temperatures

Storage temperature

T_{stg}

-20 to +125 $^{\circ}C$ ←

Ambient temperature

T_{amb}

-20 to +125 $^{\circ}C$

CHARACTERISTICS at $T_{amb} = 25^{\circ}C$; $V_{7-4} = 6 V$

Collector current

of the last transistor

I_5

typ. 12 mA

Small signal current gain

of first transistor

$I_8 = 1 mA$; $V_{8-1} = 1 V$

h_{fe}

> 30
typ. 80

Saturation voltages

$V_{7-1} = 6 V$; $R_{9-10} = 35 k\Omega$

$V_{8-1 sat}$

typ. 100 mV

$V_{7-4} = 6 V$; $R_4 = 2 k\Omega$; $V_{2-3} = 0$

$V_{5-4 sat}$

typ. 600 mV

Noise figure of first transistor

$I_1 = 100 \mu A$; $R_S = 2 k\Omega$; $V_{8-1} = 6 V$

F

typ. 6 dB

$B = 30 Hz$ to $15000 Hz$

< 10 dB

Transducer gain at $f = 1 kHz$

$P_O = 10 mW$

G_{tr}

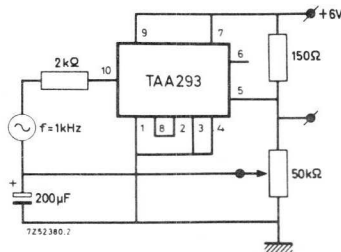
> 70 dB
typ. 80 dB

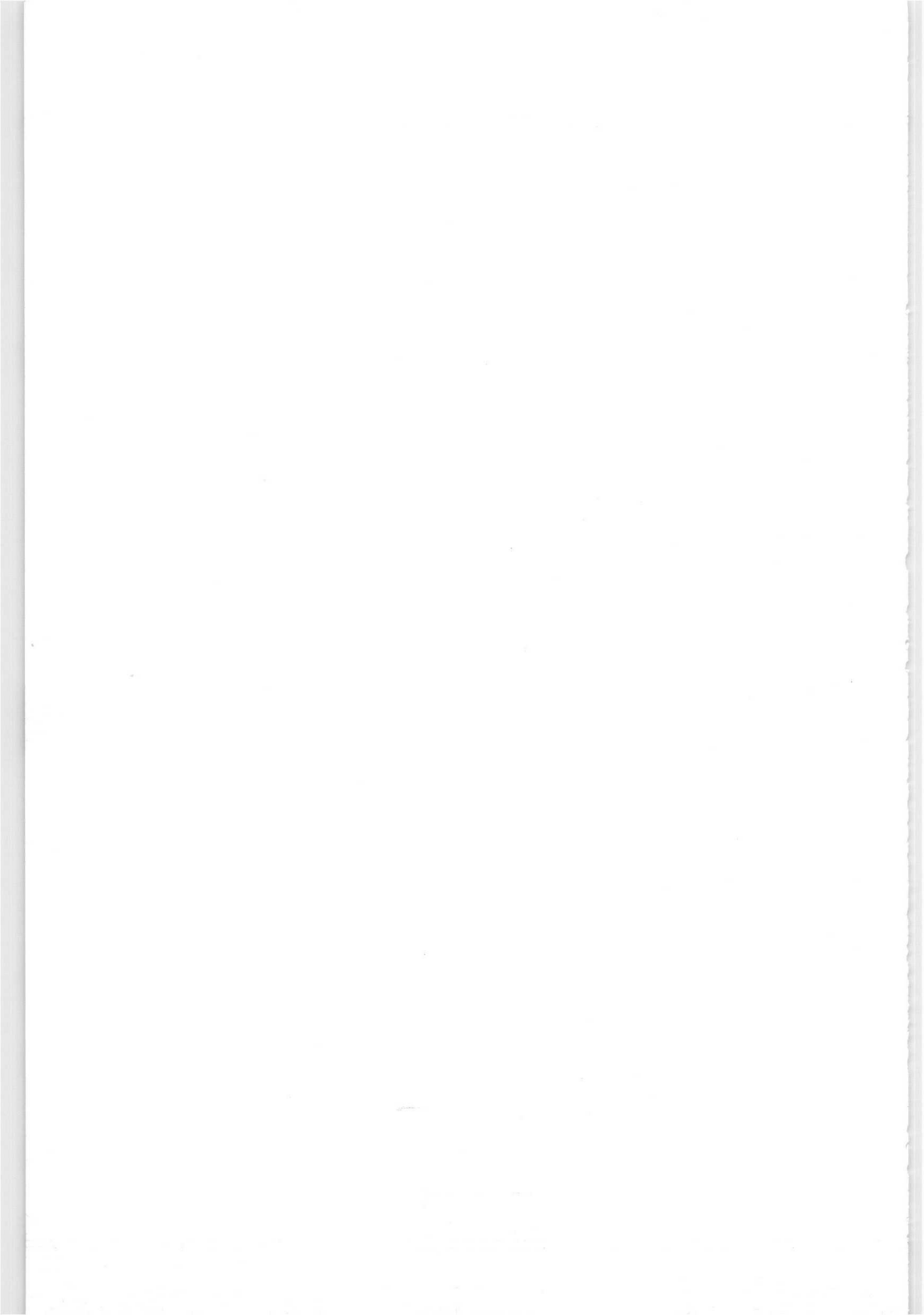
Output power at $d_{tot} = 10\%$

P_O

> 10 mW

Test circuit for measuring the transducer gain and the output power





INTEGRATED 1 WATT AUDIO AMPLIFIER

A complete a. f. amplifier in monolithic integrated form incorporating special measures to prevent cross-over distortion throughout an exceptionally wide usable range of supply voltage (4.5 V to 10 V. This, in combination with its low drain current, makes the TAA300 ideally suited for use in battery operated equipment. Due to the high a. c. feedback (≈ 20 dB) the distortion and spread in gain is very low.

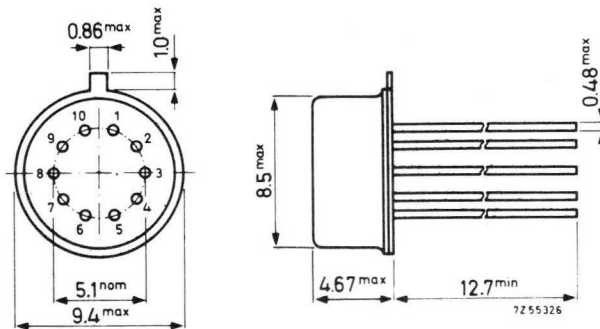
QUICK REFERENCE DATA

| | | | |
|------------------------------|-----------|------|---------------|
| Supply voltage | V_B | nom. | 9 V |
| Output power | P_O | typ. | 1 W |
| Input signal for $P_O = 1$ W | V_i | typ. | 8.5 mV |
| Input impedance | $ Z_i $ | typ. | 15 k Ω |
| Load impedance | R_L | | 8 Ω |
| Total current (no signal) | I_{tot} | typ. | 8 mA |

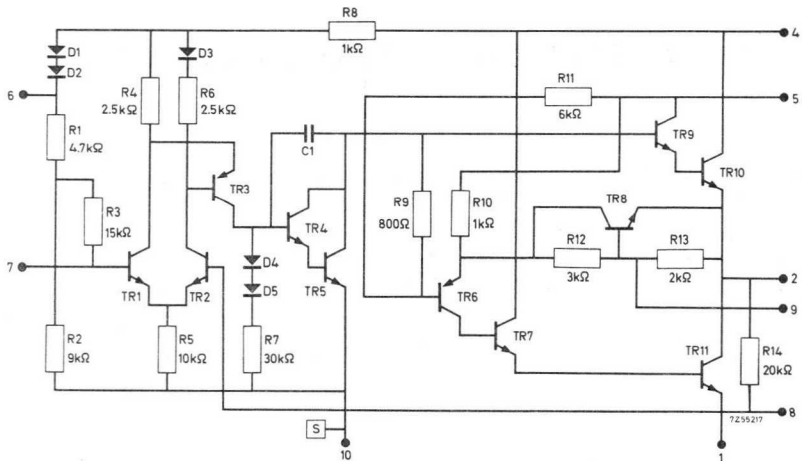
PACKAGE OUTLINE

Dimensions in mm

TO-74; reduced height



CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages (see test set-up on page 4)

| | | |
|-----------|------|--------|
| V_{4-1} | max. | 10.5 V |
| V_{7-8} | max. | 6 V |
| V_{8-7} | max. | 6 V |
| V_{2-9} | max. | 6 V |
| V_{2-1} | max. | 10.5 V |
| V_{4-2} | max. | 10.5 V |

Currents (see test set-up on page 4)

| | | |
|-----------|------|--------|
| $-I_1$ | max. | 600 mA |
| $\pm I_2$ | max. | 600 mA |
| $+I_4$ | max. | 600 mA |

Total power dissipation

P_{tot} see next page

Temperatures

Storage temperature

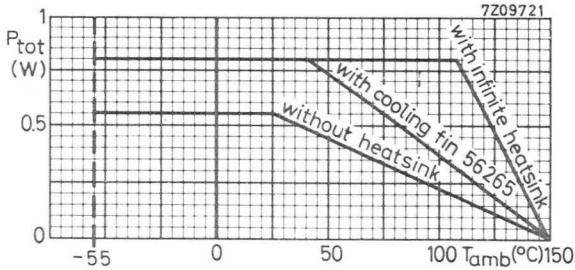
T_{stg} -55 to +150 °C

Operating ambient temperature

T_{amb} -55 to +150 °C

RATINGS (continued)

Maximum allowable total power dissipation versus ambient temperature



CHARACTERISTICS at $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_B = 9\text{ V}$

Measured in the test set-up on page 4

Output power at $d_{tot} = 10\%$

P_O typ. 1 W

Bandwidth (-3 dB)

B > 10 kHz
typ. 25 kHz

Total current (d.c.)

no signal and excluding output transistors:
with signal at $P_O = 1\text{ W}$:

I_{tot} typ. 4 mA
 I_{tot} typ. 180 mA

Total distortion at $P_O = 0.5\text{ W}$

d_{tot} typ. 0.7 %
< 3 %

Input signal at $P_O = 1\text{ W}$
 $P_O = 0.5\text{ W}$

V_i typ. 8.5 mV
 V_i < 8.5 mV

Input impedance

$|Z_i|$ > 10 k Ω
typ. 15 k Ω

Efficiency

η typ. 60 %

Signal to noise ratio related to $P_O = 1\text{ W}$

$R_S = 2\text{ k}\Omega$; $B = 30\text{ Hz to }15\text{ kHz}$

$\frac{S}{N}$ > 70 dB
typ. 75 dB

Noise output power

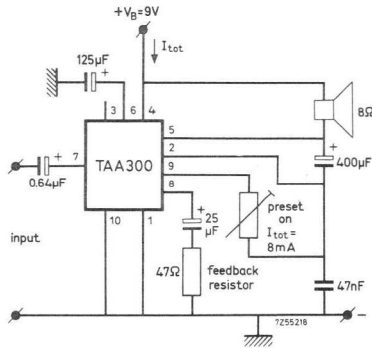
input short circuited; $B = 30\text{ Hz to }15\text{ kHz}$

P_N typ. 10 nW
< 20 nW

Preset resistor for $I_{tot} = 8\text{ mA}$

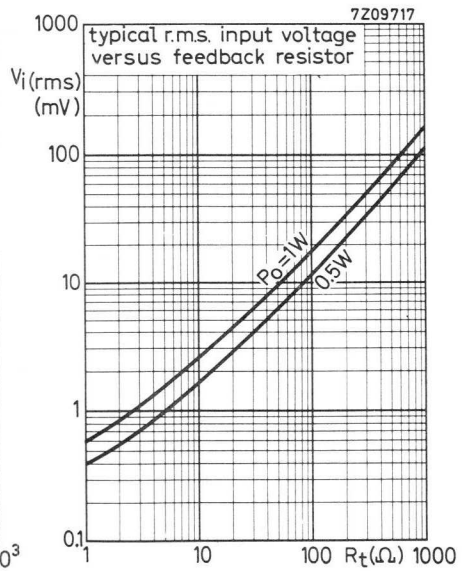
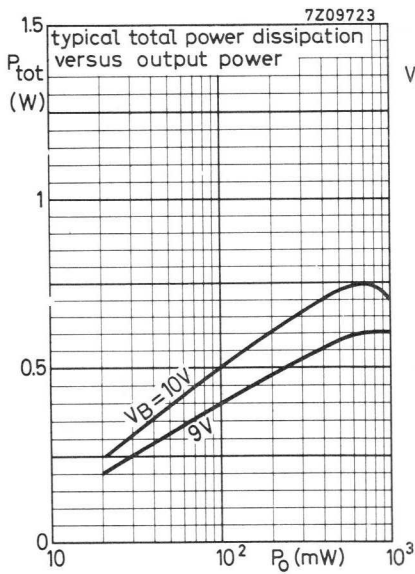
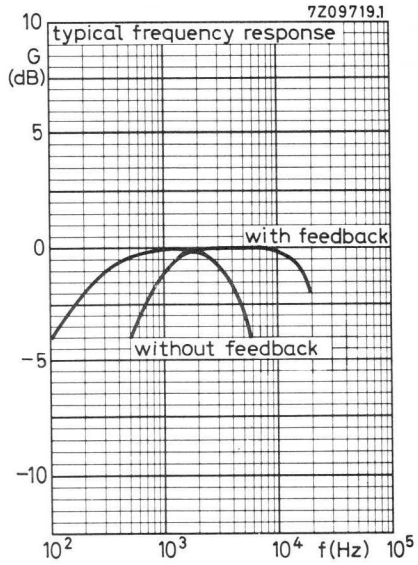
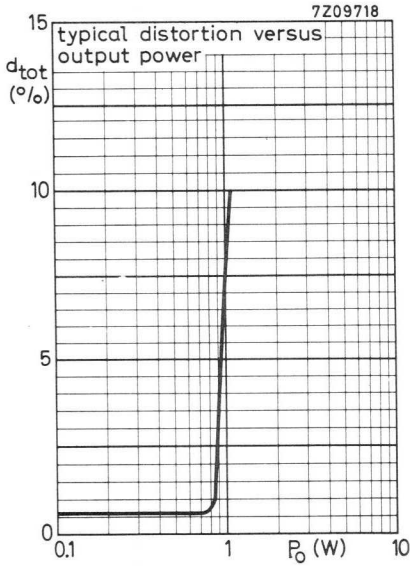
R_{pr} 4 to 25 k Ω

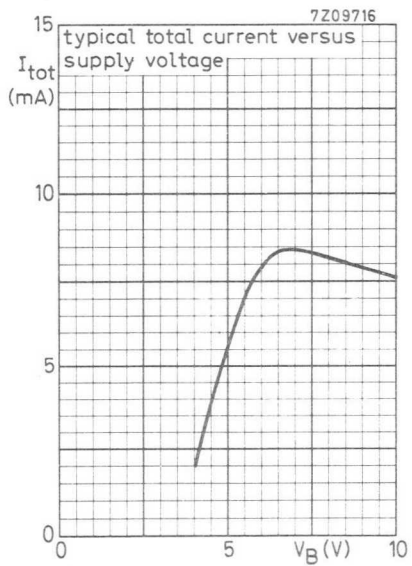
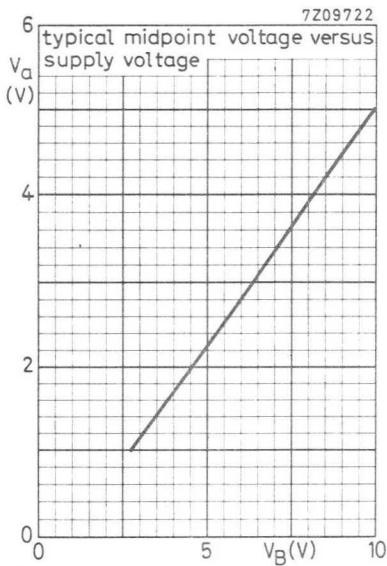
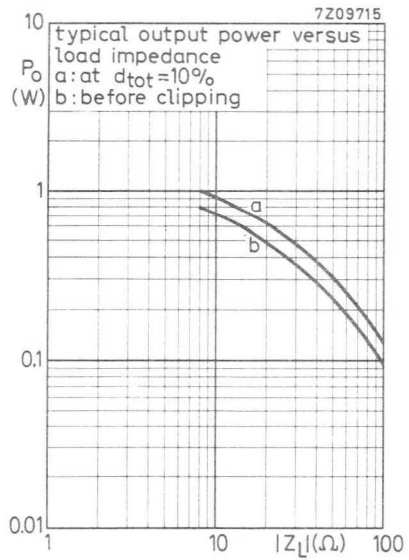
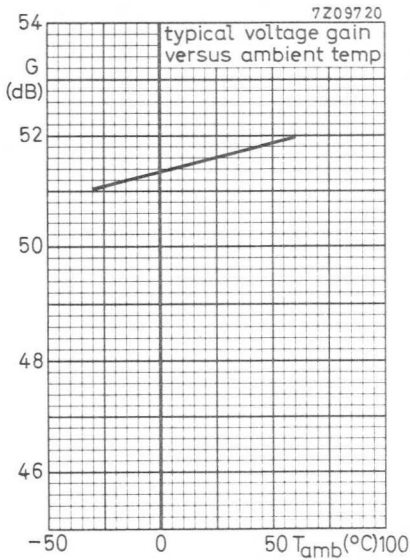
TEST SET-UP



To prevent high-frequency instability, the following precautions must be taken.

- Keep the lead inductance from the positive voltage supply to pin 4 to a minimum.
- Because of the high internal resistance of batteries (especially at end of life) a large capacitance should be connected between pin 4 and ground.
- A capacitor of at least 47 nF should be connected between pin 2 and ground to prevent instability of the lower Darlington output transistor (see also test set-up).
- Avoid coupling between output and input leads (especially those carrying signals from a high-impedance source). This coupling can be reduced by using short leads, shielded input cable or by limiting the upper frequency to 15 kHz by means of a capacitor of 560 pF between pin 7 and ground.





A.F. PREAMPLIFIER

The TAA310 is a monolithic integrated circuit designed for use as an a.f. high-gain preamplifier, with a very low noise figure (< 4 dB) and a high voltage gain of at least 90 dB. Because this gain can be achieved at a low load impedance ($1 \text{ k}\Omega$) and the input impedance is high, the TAA310 is specially suited for the recording and playback amplifier in tape recorders.

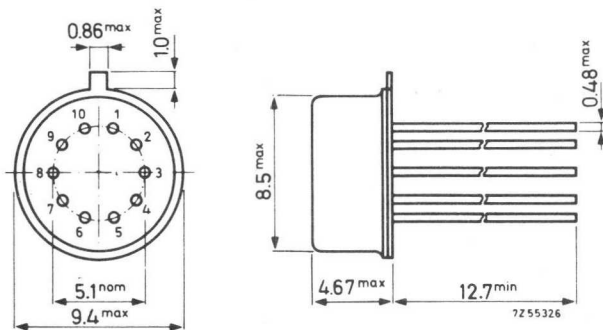
QUICK REFERENCE DATA

| | | | |
|------------------------------------|-------|------|---------------------|
| Supply voltage | V_B | nom. | +7 V |
| Voltage gain | G_V | typ. | 100 dB |
| Noise figure (B = 30 to 15.000 Hz) | F | typ. | 2.5 dB |
| Input impedance | Z_i | typ. | 20 $\text{k}\Omega$ |

PACKAGE OUTLINE

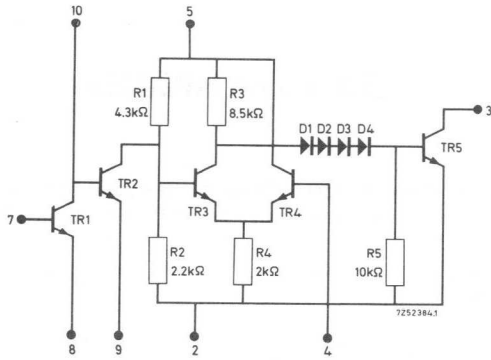
Dimensions in mm

TO-74; reduced height



Pins 1 and 6 are not connected

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

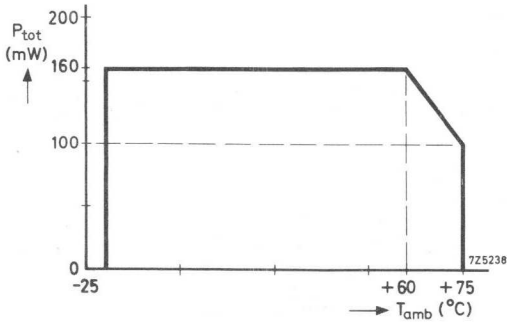
| | | |
|-------------------|------|-------|
| V ₅₋₂ | max. | 9.5 V |
| V ₃₋₂ | max. | 9.5 V |
| V ₁₀₋₈ | max. | 6 V |
| V ₈₋₇ | max. | 6 V |
| V ₉₋₁₀ | max. | 6 V |
| V ₄₋₂ | max. | 6 V |

The pins 3, 4, 5 and 10 must never have a negative potential with respect to pin 2 (substrate).

Currents

| | | |
|-----------------|------|-------|
| I ₃ | max. | 20 mA |
| I ₇ | max. | 3 mA |
| -I ₈ | max. | 10 mA |
| -I ₉ | max. | 10 mA |
| I ₁₀ | max. | 10 mA |
| I ₄ | max. | 3 mA |

Total power dissipation



Temperatures

| | | |
|-------------------------------|-----------|----------------|
| Storage temperature | T_{stg} | -20 to +125 °C |
| Operating ambient temperature | T_{amb} | -20 to +75 °C |

TAA310

CHARACTERISTICS at $T_{amb} = 25\text{ }^{\circ}\text{C}$

D.C. current gain

of first transistor

$$I_{10} = 100\text{ }\mu\text{A}; V_{10-7} = 0$$

$$h_{FE} > 40$$

Input impedance at $f = 1\text{ kHz}$

$$I_{10} = 100\text{ }\mu\text{A}; V_{10-7} = 0$$

$$z_i \text{ typ. } 20\text{ k}\Omega$$

Voltage gain

$$G_v > 93\text{ dB}$$

$$\text{typ. } 100\text{ dB}$$

Noise figure

$$R_S = 2\text{ k}\Omega; B = 30\text{ to }15000\text{ Hz}$$

$$F \text{ typ. } 2.5\text{ dB}$$

$$< 4\text{ dB}$$

Output voltage at $d_{tot} = 10\%$

$$V_{O(rms)} \text{ typ. } 2\text{ V}$$

Cut-off frequency (-3 dB)

$$f_c \geq 15\text{ kHz}$$

Saturation voltage

of output transistor at $I_3 = 7\text{ mA}$

$$V_{3-2} \text{ typ. } 0.8\text{ V}$$

$$< 1.2\text{ V}$$

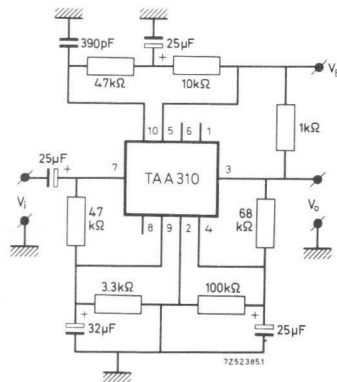
D.C. collector voltage

of output transistor at $I_9 = 200\text{ }\mu\text{A}$

$$V_{3-2} \text{ typ. } 3.8\text{ V}$$

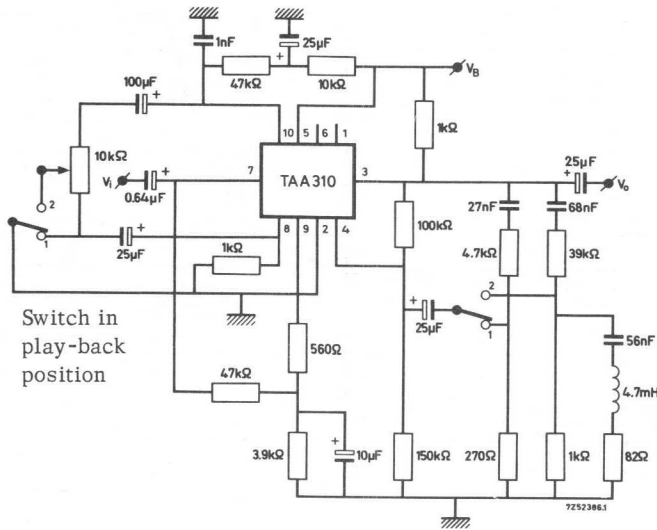
$$3.4\text{ to }4.2\text{ V}$$

Test circuit for measuring G_v , F , $V_{O(rms)}$, f_c and V_{3-2} at $V_B = 7\text{ V}$



APPLICATION INFORMATION

Practical tape-recorder preamplifier with a TAA310.



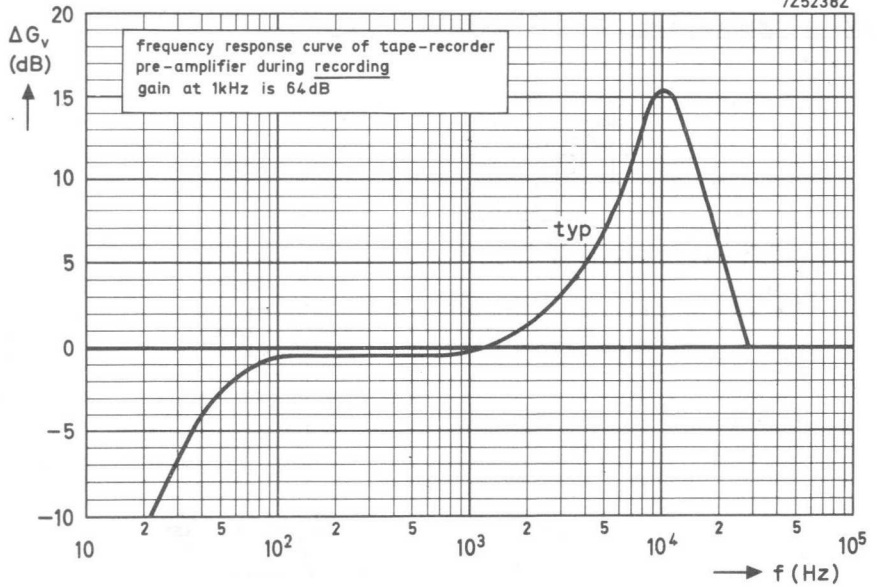
Data for use as recording amplifier (measured at $f = 1 \text{ kHz}$)

| | | |
|-----------------------------------------------------|------------------|-----------------------|
| Voltage gain | G_V | $64 \pm 2 \text{ dB}$ |
| Frequency response (see page 6) | | |
| Distortion at $V_{O(\text{rms})} = 0.5 \text{ V}$ | d_{tot} | $< 0.5 \%$ |
| Volume control range | | typ. 75 dB |
| Signal handling | | $> 20 \text{ mV}$ |
| Gain variation at V_B decreasing from 7 to 5 V | ΔG_V | typ. 3 dB |

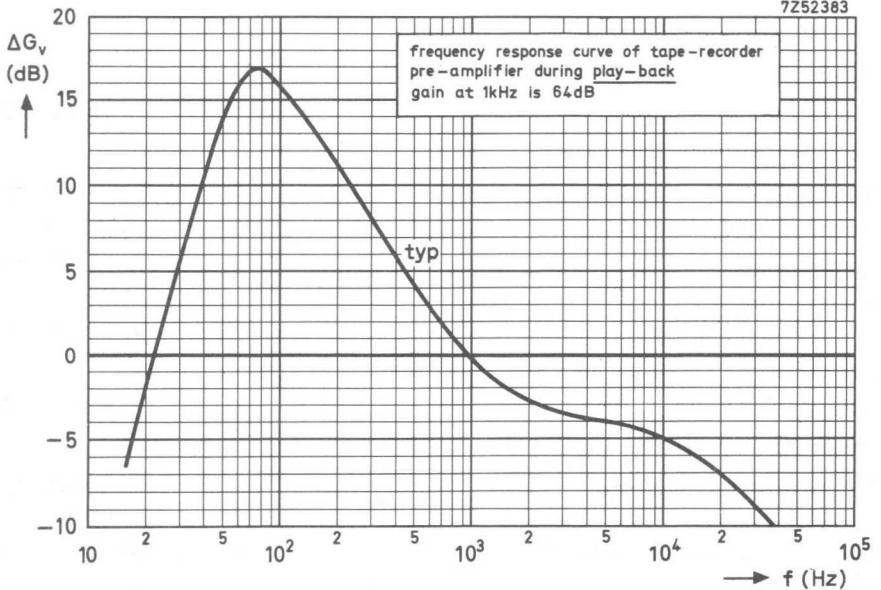
Data for use as play-back amplifier (measured at $f = 1 \text{ kHz}$)

| | | |
|-----------------------------------------------------|------------------|-----------------------|
| Voltage gain | G_V | $64 \pm 2 \text{ dB}$ |
| Frequency response (see page 6) | | |
| Distortion at $V_{O(\text{rms})} = 0.5 \text{ V}$ | d_{tot} | $< 0.5 \%$ |
| Gain variation at V_B decreasing from 7 to 5 V | ΔG_V | typ. 3 dB |

7Z52382



7Z52383



INTEGRATED MOST AMPLIFIER

The TAA320 is a silicon monolithic integrated circuit, consisting of a MOS transistor and an n-p-n transistor in a TO-18 metal envelope.

The device is primarily intended for audio amplifiers with a very high input resistance (e.g. for crystal pick-ups).

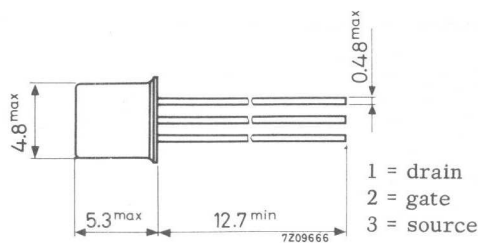
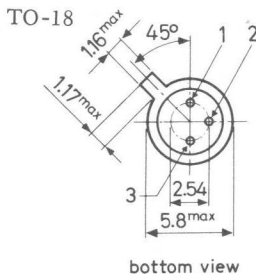
Besides this application the TAA320 is also suitable for other applications where a high input resistance is required, like impedance converters, timing circuits, microphone-amplifiers, etc.

QUICK REFERENCE DATA

| | | | |
|----------------------------------------------------------------------------------------------|------------|------|--------------------------|
| Drain-source voltage ($V_{GS} = 0$) | $-V_{DSS}$ | max. | 20 V |
| Drain current | $-I_D$ | max. | 25 mA |
| Gate-source voltage $-I_D = 10 \text{ mA}; -V_{DS} = 10 \text{ V}$ | $-V_{GS}$ | typ. | 11 V |
| Gate-source resistance $-V_{GS}$ up to 20 V; T_j up to 125 °C | r_{GS} | > | 100 $\text{G}\Omega$ |
| Transfer admittance at $f = 1 \text{ kHz}$ $-I_D = 10 \text{ mA}; -V_{DS} = 10 \text{ V}$ | $ y_{fs} $ | typ. | 75 $\text{m}\Omega^{-1}$ |

PACKAGE OUTLINE

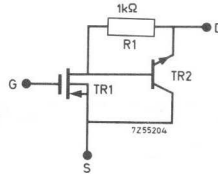
Dimensions in mm



Source connected to the case

Accessories available: 56246, 56263

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

| | | | |
|-----------------------------------------------------------|------------|------|-------|
| Drain-source voltage ($V_{GS} = 0$) | $-V_{DSS}$ | max. | 20 V |
| Gate-source voltage ($I_D = 0$) | $-V_{GSO}$ | max. | 20 V |
| Non repetitive peak gate-source voltage ($t \leq 10$ ms) | $-V_{GSM}$ | max. | 100 V |

Current

| | | | |
|---------------|--------|------|-------|
| Drain current | $-I_D$ | max. | 25 mA |
|---------------|--------|------|-------|

Power dissipation

| | | | |
|-------------------------------------------------|-----------|------|--------|
| Total power dissipation up to $T_{amb} = 25$ °C | P_{tot} | max. | 200 mW |
|-------------------------------------------------|-----------|------|--------|

Temperatures

| | | | |
|----------------------|-----------|-------------|--------|
| Storage temperature | T_{stg} | -65 to +125 | °C |
| Junction temperature | T_j | max. | 125 °C |

THERMAL RESISTANCE

| | | | |
|--------------------------------------|--------------|---|-----------|
| From junction to ambient in free air | $R_{th j-a}$ | = | 0.5 °C/mW |
|--------------------------------------|--------------|---|-----------|

CHARACTERISTICS

 $T_j = 25\text{ }^\circ\text{C}$ unless otherwise specifiedDrain current $-V_{DS} = 20\text{ V}; V_{GS} = 0$

| | | |
|------------|------|-----------------|
| $-I_{DSS}$ | typ. | 5 nA |
| | < | 1 μA |

Gate-source voltage ¹⁾ $-I_D = 10\text{ mA}; -V_{DS} = 10\text{ V}$

| | | |
|-----------|------|------|
| $-V_{GS}$ | typ. | 11 V |
| | 9 to | 14 V |

Gate-source resistance $-V_{GS}$ up to 20 V; T_j up to 125 $^\circ\text{C}$

| | | |
|----------|---|----------------------|
| r_{GS} | > | 100 $\text{G}\Omega$ |
|----------|---|----------------------|

Equivalent noise voltage

$-I_D = 10\text{ mA}; -V_{DS} = 10\text{ V}$
 $B = 50\text{ Hz to } 15\text{ kHz}$

| | | |
|-------|------|------------------|
| v_n | typ. | 25 μV |
|-------|------|------------------|

y parameters at $f = 1\text{ kHz}$ $-I_D = 10\text{ mA}; -V_{DS} = 10\text{ V}$

Transfer admittance

| | | |
|------------|-----------|--------------------------|
| $ y_{fs} $ | typ. | 75 $\text{m}\Omega^{-1}$ |
| | 40 to 120 | $\text{m}\Omega^{-1}$ |

Input capacitance

| | | |
|----------|------|------|
| C_{is} | typ. | 8 pF |
|----------|------|------|

Feedback capacitance

| | | |
|-----------|------|--------|
| $-C_{rs}$ | typ. | 1.5 pF |
|-----------|------|--------|

Output conductance

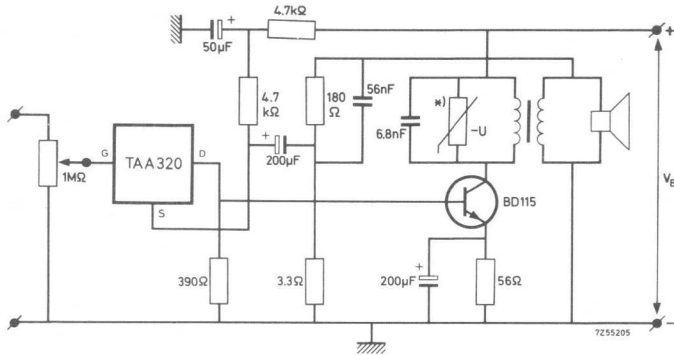
| | | |
|----------|------|----------------------------|
| g_{os} | typ. | 0.65 $\text{m}\Omega^{-1}$ |
|----------|------|----------------------------|

NOTE

To exclude the possibility of damage to the gate oxide layer by an electrostatic charge building up on the high resistance gate electrode, the leads of the device have been short circuited by a clip. The clip has been arranged so that it need not be removed until the device has been mounted in the circuit.

1) $-V_{GS}$ decreases about 6 mV/ $^\circ\text{C}$ with increasing ambient temperature at a constant $-I_D$.

APPLICATION INFORMATION 2 W audio amplifier with TAA320 and BD115



* The voltage dependent resistor (2322 552 03381) suppresses voltage transients that might otherwise exceed the safe operating limits of the BD115.

| | | | |
|-----------------------------------------------|--------|------|----------------|
| Supply voltage | V_B | = | 100 V |
| Collector current of BD115 | I_C | typ. | 50 mA |
| Drain current of TAA320 | $-I_D$ | typ. | 9.5 mA |
| Primary d.c. resistance of output transformer | | | 140 Ω |
| Primary inductance of output transformer | | | 2.7 H |
| A.C. collector load for BD115 | | | 1.8 k Ω |

Performance at $f = 1$ kHz; feedback = 16 dB

Output power at $d_{tot} = 10\%$

(on primary of the output transformer)

| | | | |
|------------------------------------|--------------|------|-----------------|
| | P_O | typ. | 2.6 W |
| Input voltage for $P_O = 50$ mW | $V_{i(rms)}$ | typ. | 13.5 mV |
| Input voltage for $P_O = 2$ W | $V_{i(rms)}$ | typ. | 86 mV |
| Total distortion at $P_O = 2$ W | d_{tot} | typ. | 3.6 % |
| Minimum frequency response (-3 dB) | | | 60 Hz to 20 kHz |
| Signal-noise ratio at $P_O = 2$ W | | typ. | 73 dB |

Mounting instruction for BD115

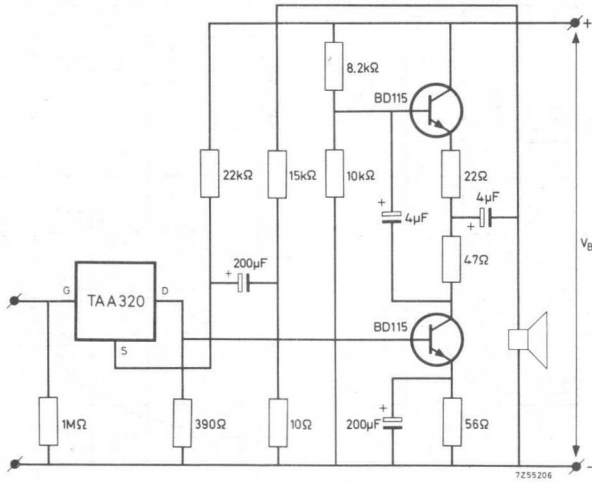
Proper continuous operation is ensured up to $T_{amb} = 50$ °C, provided the BD115 is directly mounted on a 1.5 mm blackened Al. heatsink of 30 cm² with a clamping washer of type 56218.

If the transistor is mounted on a heatsink with a mica washer, the heatsink should have an area of 50 cm².

Recommended diameter of hole in heatsink: 7.7 mm.

APPLICATION INFORMATION (continued)

4 W audio amplifier with TAA320 and 2 transistors of type BD115.



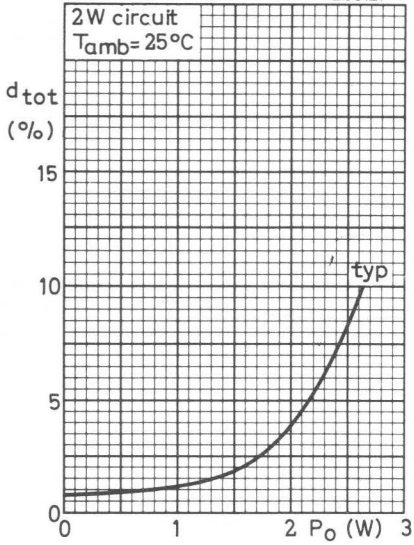
| | | | |
|------------------------------|--------|------|--------|
| Supply voltage | V_B | = | 200 V |
| Collector current of a BD115 | I_C | typ. | 52 mA |
| Drain current of TAA320 | $-I_D$ | typ. | 8.6 mA |

Performance at $f = 1$ kHz; feedback = 12 dB

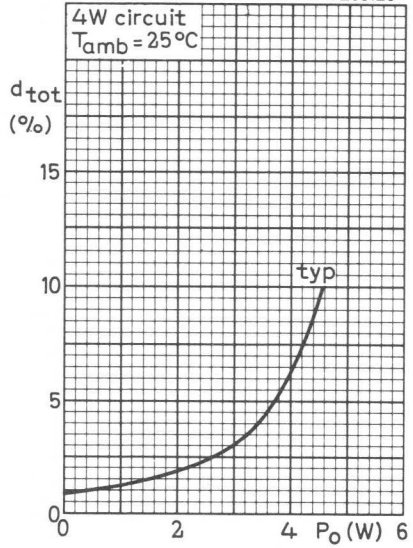
| | | | |
|------------------------------------|--------------|------|-----------------|
| Output power at $d_{tot} = 10\%$ | P_O | typ. | 4.5 W |
| Input voltage for $P_O = 50$ mW | $V_{i(rms)}$ | typ. | 7.5 mV |
| Input voltage for $P_O = 4$ W | $V_{i(rms)}$ | typ. | 67 mV |
| Total distortion at $P_O = 4$ W | d_{tot} | typ. | 6 % |
| Minimum frequency response (-3 dB) | | | 50 Hz to 20 kHz |
| Signal-noise ratio at $P_O = 4$ W | | typ. | 73 dB |

Mounting instruction for BD115 see page 4

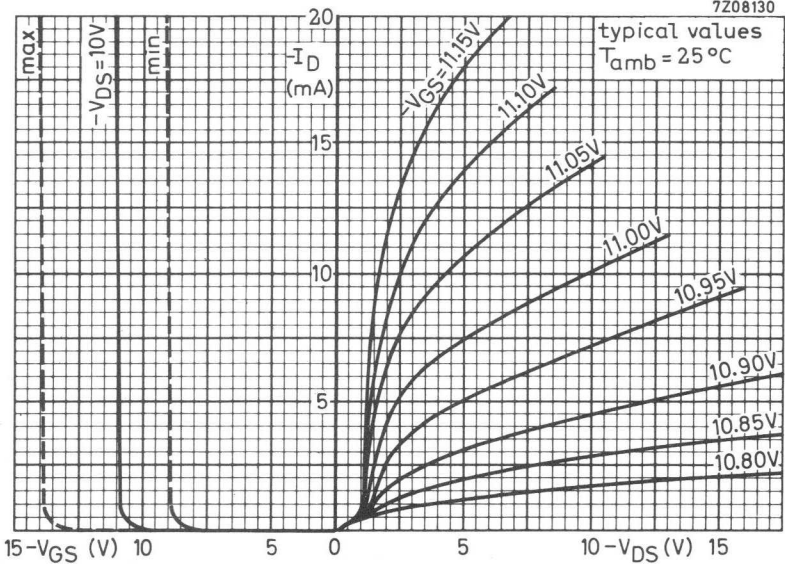
7Z08127

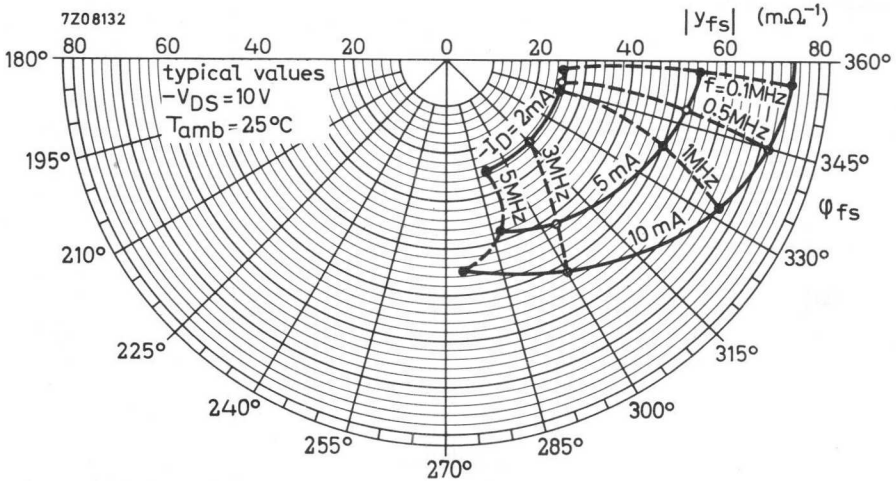
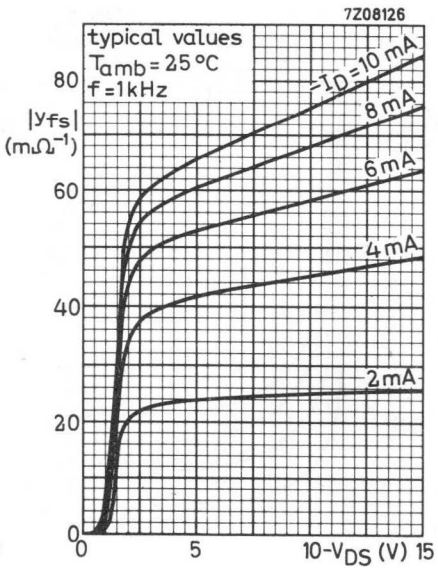
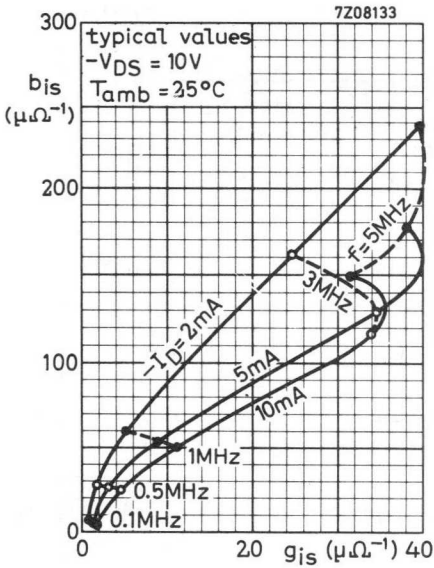


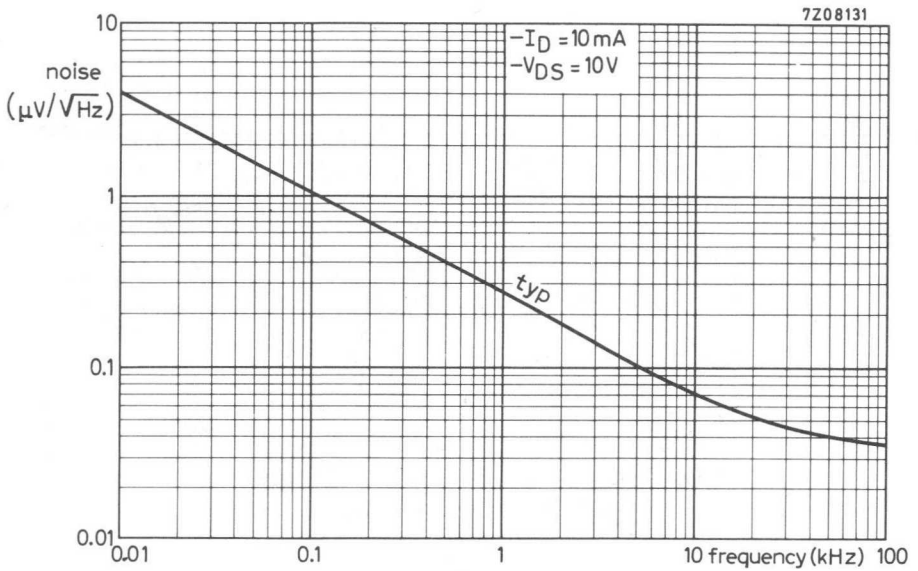
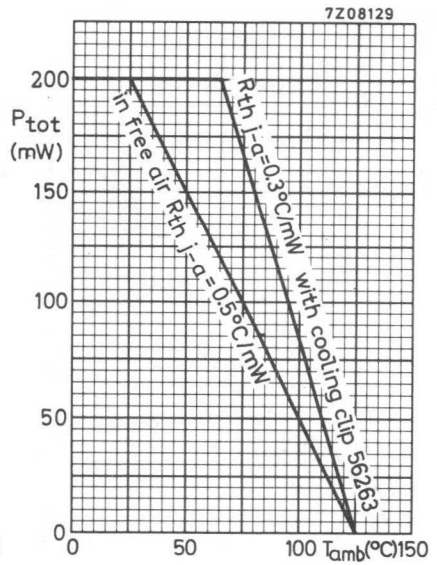
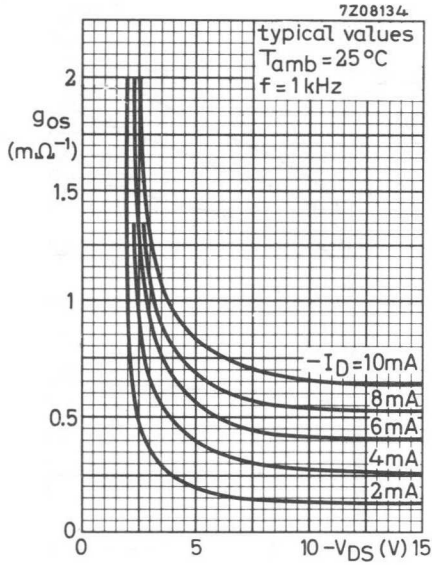
7Z08128



7Z08130







WIDEBAND DIFFERENTIAL LIMITING AMPLIFIER

A monolithic integrated i.f. amplifier for f.m. Differential amplification with current driven long-tailed pairs gives high a.m. rejection, making the amplifier suitable for use with very simple f.m. detectors. The TAA350 can be driven either symmetrically or asymmetrically.

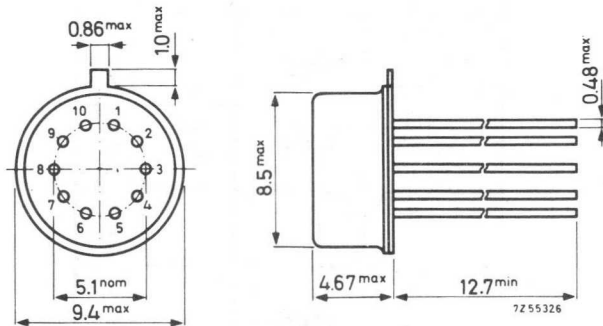
QUICK REFERENCE DATA

| | |
|----------------------------|------------------|
| Supply voltage | 6 V |
| Frequency | 5.5 MHz |
| <hr/> | |
| Total current | typ. 20 mA |
| Voltage gain | typ. 80 dB |
| Input limiting voltage | typ. 100 μ V |
| Frequency response (-3 dB) | typ. 12 MHz |
| Output impedance | typ. 75 Ω |

PACKAGE OUTLINE

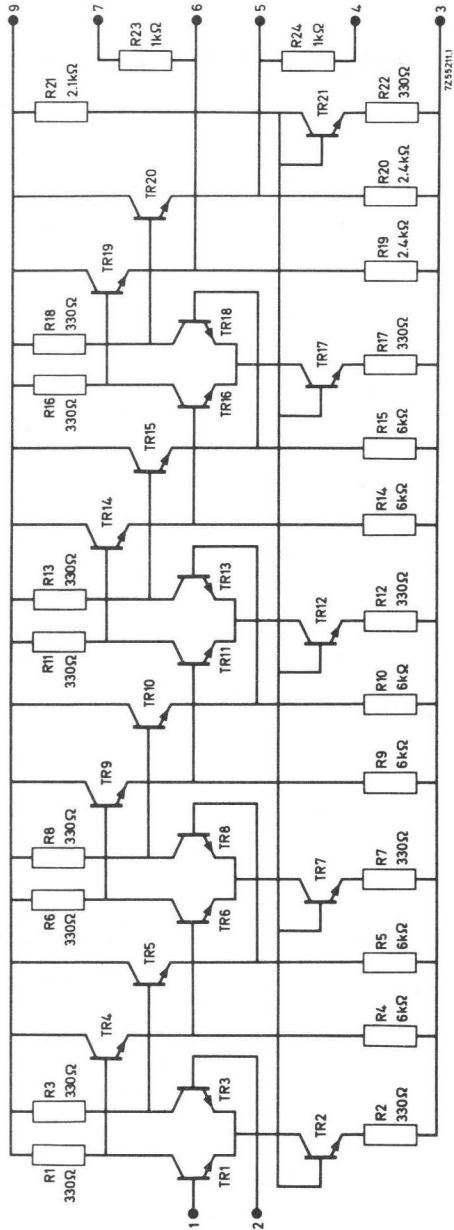
Dimensions in mm

TO-74; reduced height



TAA350

CIRCUIT DIAGRAM



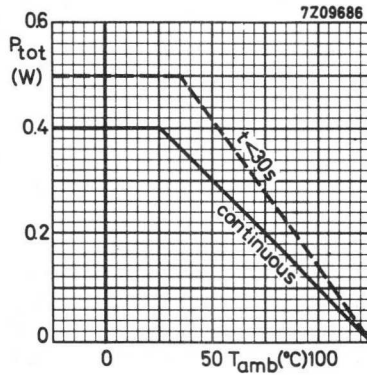
RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages with respect to pin 3

| | | | |
|-------------------------------------------------------------------|-----------|----------|---|
| Pin No.1 when $V_{2-3} = V_{1-3} \leq V_{9-3}$ | V_{1-3} | 0 to +10 | V |
| Pin No.2 when $V_{1-3} = V_{2-3} \leq V_{9-3}$ | V_{2-3} | 0 to +10 | V |
| Pin No.4 (do not apply an external voltage source) | V_{4-3} | 0 to +10 | V |
| Pin No.5 when at $ I_5 < 20 \text{ mA}$; $V_{5-3} \leq V_{9-3}$ | V_{5-3} | 0 to +10 | V |
| Pin No.6 when at $ I_6 < 20 \text{ mA}$; $V_{6-3} \leq V_{9-3}$ | V_{6-3} | 0 to +10 | V |
| Pin No.7 (do not apply an external voltage source) | V_{7-3} | 0 to +10 | V |
| Pin No.9 (with lower d.c. potential on all other terminals) | V_{9-3} | 0 to +10 | V |

Do not connect pins 8 and 10, except to earth.
 The maximum signal voltage between pins 1 and 2 is 6 V.

Total power dissipation



Temperatures

| | | | |
|-------------------------------|-----------|-------------|----|
| Storage temperature | T_{stg} | -25 to +125 | °C |
| Operating ambient temperature | T_{amb} | -25 to +125 | °C |

CHARACTERISTICS

$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

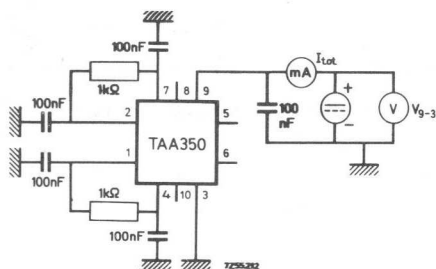
Because the TAA350 has a low ohmic output impedance and is usually driven by a bandpass or parallel tuned filter, the characteristics are described in terms of four pole hybrid k parameters.

The four-pole equations are:

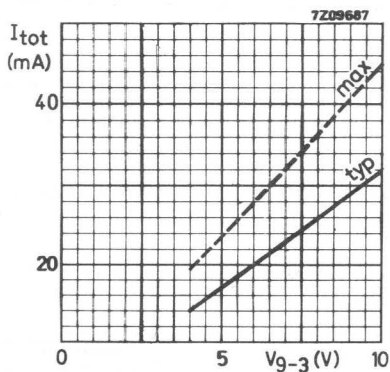
$$I_i = k_i V_i + k_r I_o$$

$$V_o = k_f V_i + k_o I_o$$

Total current (d.c.) 1)



Test circuit for measuring $I_{tot} = (V_{9-3})$



k parameters (see pages 6 to 9)

$f = 5.5\text{ MHz}$; $V_{9-3} = 6\text{ V}$

Input conductance (input pin 2)

g_i typ. $400\text{ }\mu\Omega^{-1}$

Input susceptance (input pin 2)

b_i typ. $550\text{ }\mu\Omega^{-1}$

Reverse current transfer ratio

(output pin 6, input pin 2) 2)

$|k_r|$ typ. -90 dB

Small signal voltage gain (input pin 2, output pin 6)

$|k_f|$ typ. 67 dB

Real part of output impedance (output pin 6)

$\text{Re}(k_o)$ typ. $75\text{ }\Omega$

Imaginary part of output impedance (output pin 6)

$\text{Im}(k_o)$ typ. $20\text{ }\Omega$

$f = 10.7\text{ MHz}$; $V_{9-3} = 6\text{ V}$

Reverse current transfer ratio

(output pin 6, input pin 2) 2)

$|k_r|$ typ. -80 dB

Small signal voltage gain (input pin 2, output pin 6)

$|k_f|$ typ. 65 dB

Input limiting voltage (see pp 5 and 8) 3)

$f = 5.5\text{ MHz}$; $V_{9-3} = 6\text{ V}$

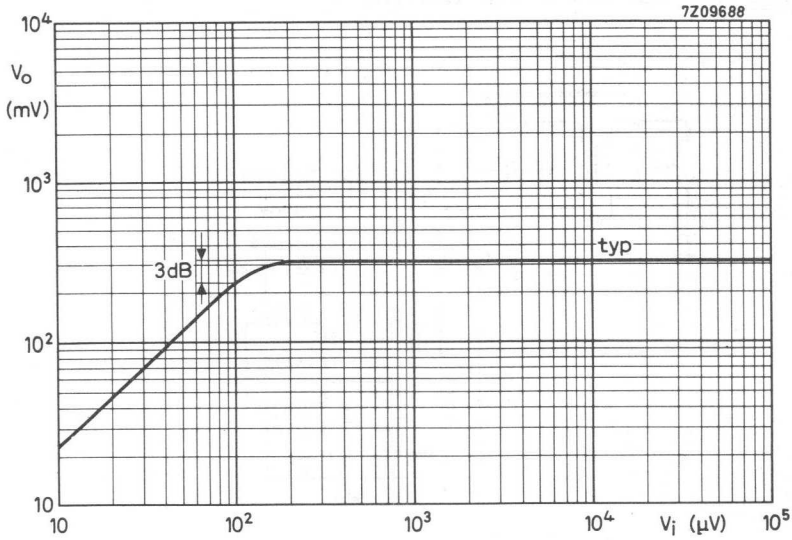
$V_{i\text{ lim}}$ typ. $100\text{ }\mu\text{V}$

1) The power dissipation is obtained from $V_{9-3} \times I_{tot}$.

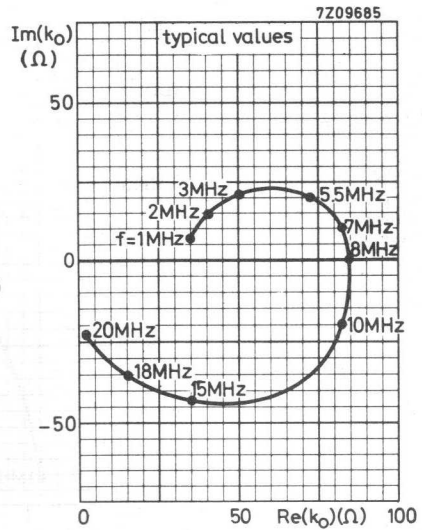
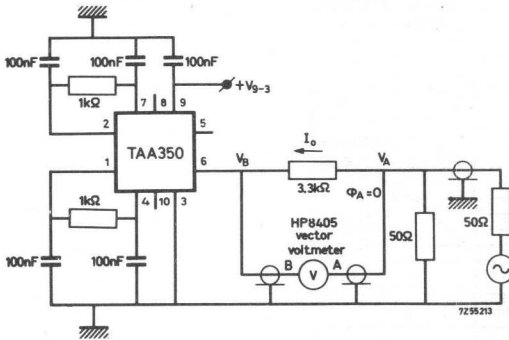
2) The output is considered open for $R_L \geq 10\text{ k}\Omega$ and $C_L \leq 10\text{ pF}$.

3) $V_{i\text{ lim}}$ is defined as the input signal voltage which reduces the output voltage 3 dB from its max. level (see also page 5).

CHARACTERISTICS (continued)

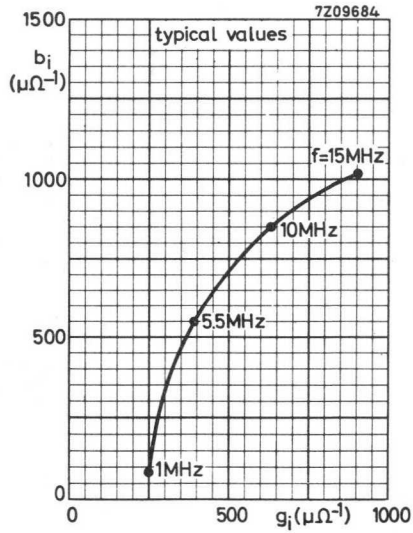
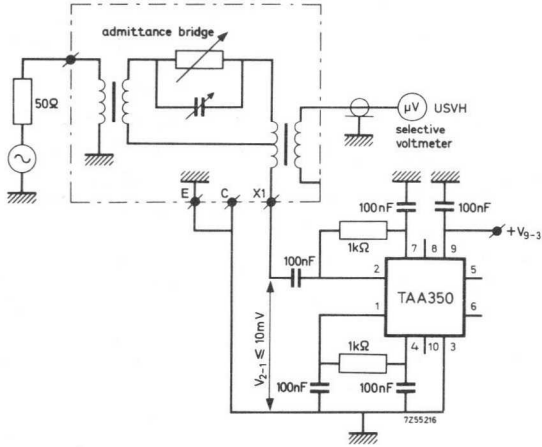


Test circuit for measuring the output characteristic



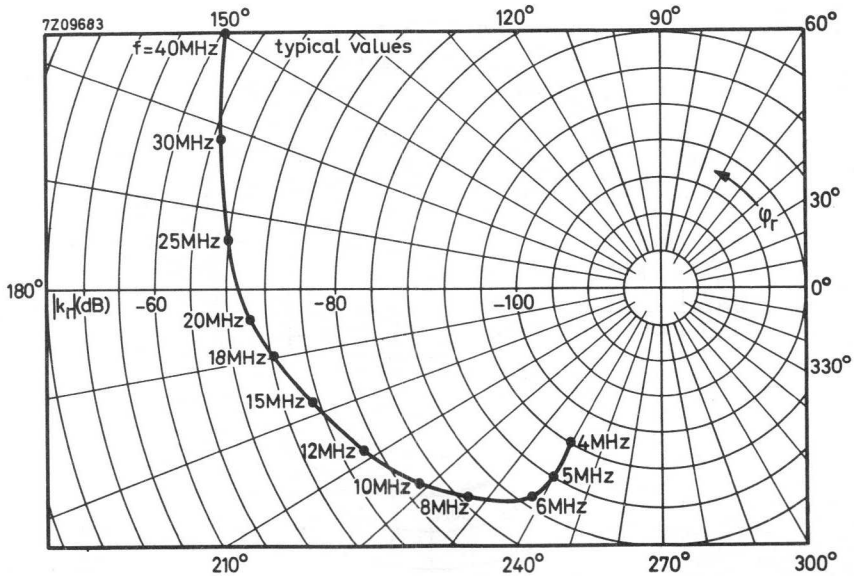
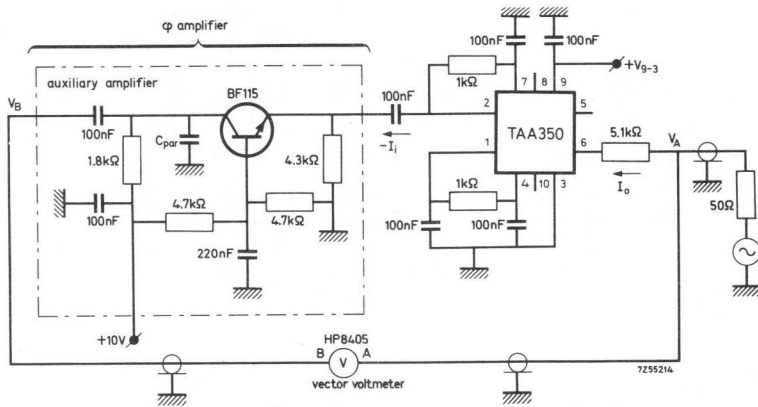
CHARACTERISTICS (continued)

Test circuit for measuring the input characteristic



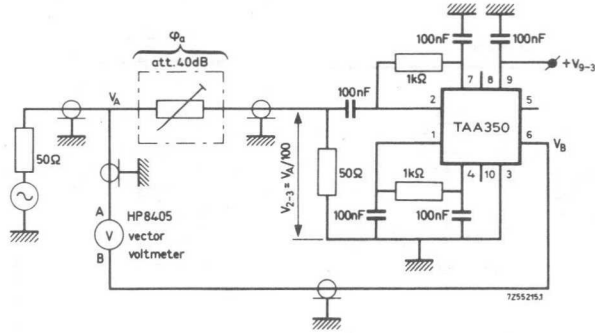
CHARACTERISTICS (continued)

Test circuit for measuring the reverse current transfer ratio



CHARACTERISTICS (continued)

Test circuit for measuring the small signal voltage gain and the input limiting voltage



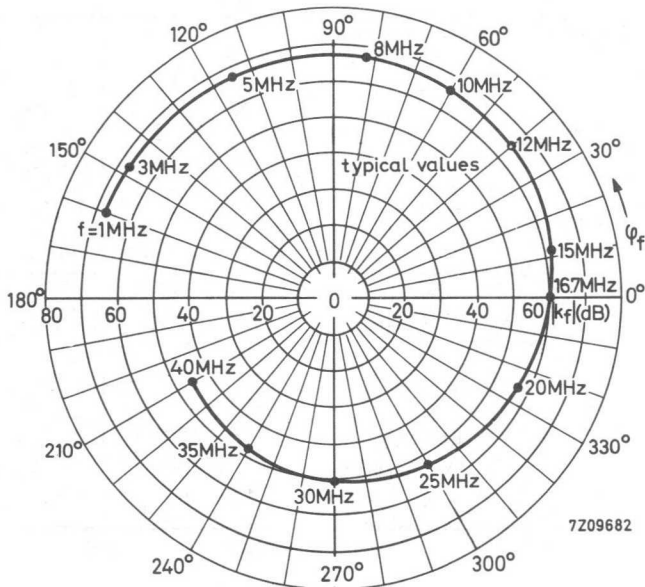
$$\overline{k_f} = |k_f| \cdot e^{j\varphi_f}, \text{ where}$$

$$|k_f| = (20 \log \frac{V_B}{V_A} + 40) \text{ dB}; \varphi_f = \varphi_{AB} - \varphi_a$$

φ_{AB} = phase angle between V_A and V_B

$$V_{i \text{ lim}} = V_{B \text{ max}} - 3 \text{ dB}$$

To find $V_{B \text{ max}}$ raise V_A until V_B remains constant



HEARING-AID AMPLIFIER

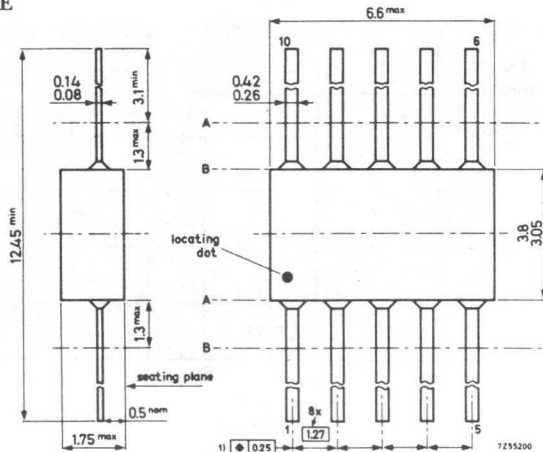
Integrated monolithic a. f. amplifier for use in hearing aids. The collector current of the class A output transistor can be determined externally, making the circuit suitable for a wide range of output powers at a low current consumption. Provision is made for the use of peak-clipping and frequency compensation circuits, and special measures have been taken to minimize the influence of temperature and supply voltage variations.

QUICK REFERENCE DATA

| | | | |
|----------------------------------------------------------------------------------|--------------|------|---------|
| Supply voltage | V_B | nom. | 1.3 V |
| Transducer gain | G_{TR} | typ. | 90 dB |
| Output power at $d_{tot} = 10\%$ | P_O | typ. | 1.5 mW |
| Saturation voltage of TR7 at $I_C = 5 \text{ mA}$; $V_{6-2} = 1.3 \text{ V}$ | V_{3-2sat} | < | 300 mV |
| Current consumption of all stages except output stage | I | typ. | 0.35 mA |
| Noise figure | F | typ. | 3 dB |

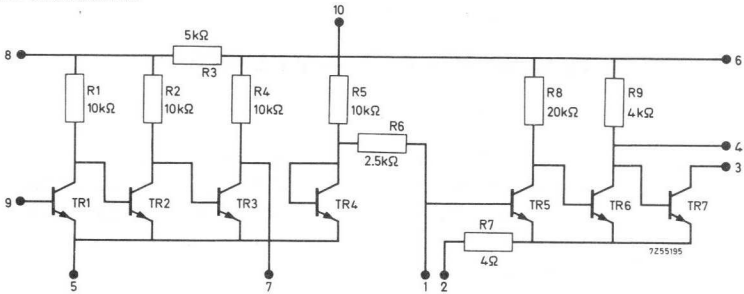
PACKAGE OUTLINE

TO-89



TAA370

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

V_{6-2} max. 5 V

V_{3-2} max. 5 V

V_{8-2} max. 5 V

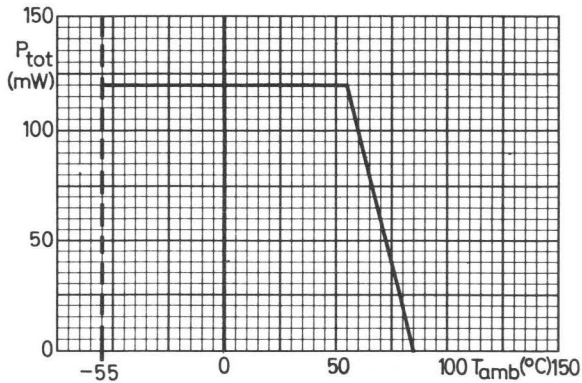
V_{5-9} max. 5 V

Currents

I_2 max. 20 mA

I_3 max. 20 mA

Maximum allowable total power dissipation versus ambient temperature



Temperatures

Storage temperature

T_{stg} -55 to +85 °C

Operating ambient temperature

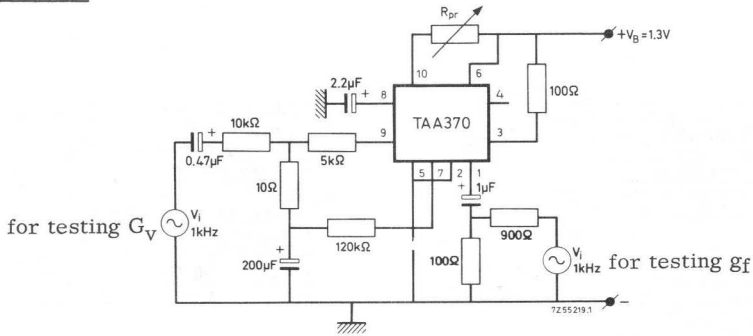
T_{amb} -55 to +85 °C

CHARACTERISTICS (see also test circuit)

$T_{amb} = 25\text{ }^{\circ}\text{C}$

| | | | |
|---------------------------------------------------------------------------------------------------------|----------------------|------------|-----------------------|
| <u>Supply voltage</u> | V_B | nom. | 1.3 V |
| <u>Voltage gain</u> of first 3 transistors (pin 9 to 7) | G_V | > | 60 dB |
| <u>Transconductance</u> of last 3 transistors (pin 1 to 3) | g_f | 200 to 280 | $\text{m}\Omega^{-1}$ |
| <u>Saturation voltage</u> of last transistor (TR7) at $I_C = 5\text{ mA}$; $V_{6-2} = 1.3\text{ V}$ | $V_{3-2\text{ sat}}$ | < | 300 mV |
| <u>Current consumption</u> of all stages except output stage | I | typ. | 0.35 mA |
| | | < | 0.5 mA |
| <u>Noise figure</u> | F | typ. | 3 dB |
| $R_S = 5\text{ k}\Omega$; $B = 400\text{ to }3200\text{ Hz}$ | | < | 6 dB |

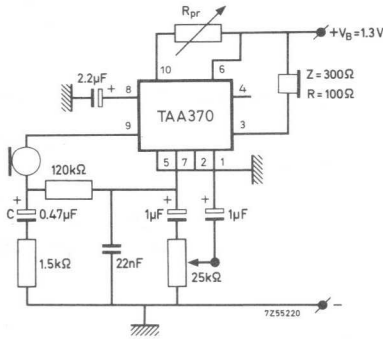
Test circuit



TAA370

APPLICATION INFORMATION

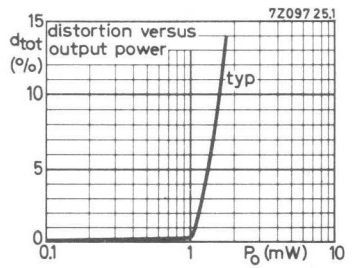
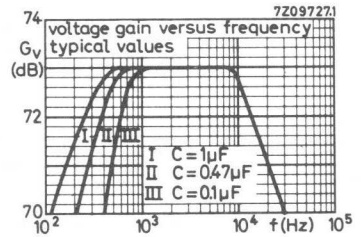
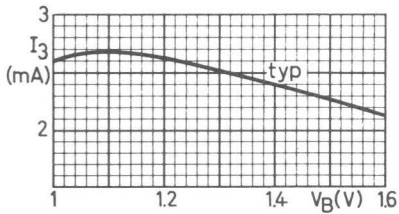
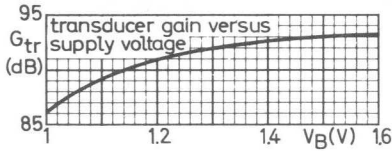
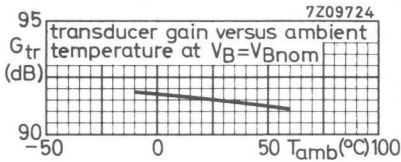
The TAA370 in a 1.5 mW amplifier



$$I_3 = 2.5 \text{ mA}$$

$$I_{tot} = 2.85 \text{ mA}$$

$$R_{pr} = 4 \text{ k}\Omega$$



LOW FREQUENCY AMPLIFIER

The TAA435 is a silicon monolithic integrated a.f. preamplifier and driver stage. Combined with a complementary output stage an output power of 4 W can be achieved.

QUICK REFERENCE DATA

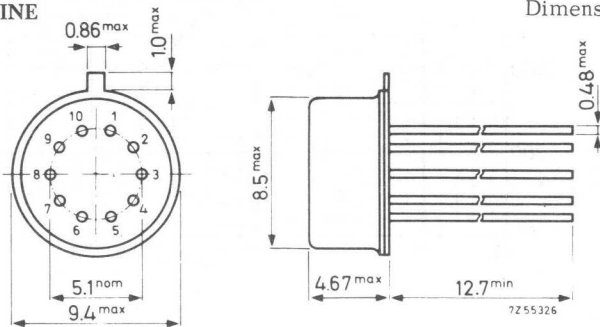
with AD161/AD162 output stage

| | | | |
|-------------------------------------|-----------|------|-------|
| Supply voltage | V_B | nom. | 14 V |
| Ambient temperature | T_{amb} | nom. | 25 °C |
| Voltage gain | G_V | typ. | 80 dB |
| Output power at $d_{tot} < 10\%$ | P_O | > | 4 W |
| Noise figure at B = 60 Hz to 10 kHz | F | typ. | 6 dB |

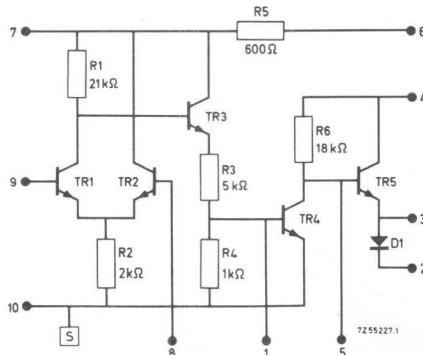
PACKAGE OUTLINE

TO-74
reduced height

Dimensions in mm



CIRCUIT DIAGRAM



TAA435

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

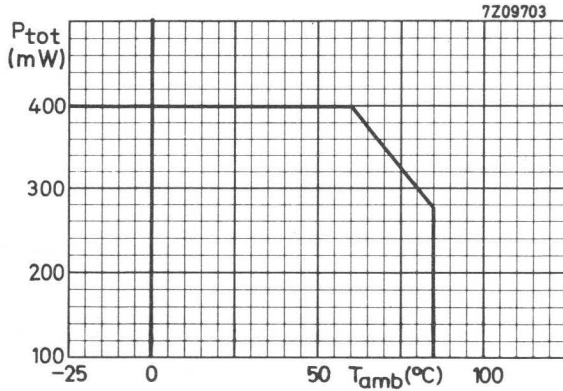
| | | |
|-------------|------|------|
| V_{6-10} | max. | 18 V |
| $-V_{9-10}$ | max. | 5 V |
| V_{4-10} | max. | 24 V |
| V_{3-10} | max. | 20 V |

Supply current

| | | |
|-------|------|-------|
| I_4 | max. | 70 mA |
|-------|------|-------|

Total power dissipation

Maximum allowable total power dissipation versus ambient temperature.



Temperatures

Operating ambient temperature

| | | |
|-----------|------------|-------------|
| T_{amb} | -25 to +85 | $^{\circ}C$ |
|-----------|------------|-------------|

Storage temperature

| | | |
|-----------|-------------|-------------|
| T_{stg} | -35 to +125 | $^{\circ}C$ |
|-----------|-------------|-------------|

CHARACTERISTICS at $V_B = 10$ to 18 V; $T_{amb} = 25$ °C

Forward voltage at $-I_2 = 30$ mA V_{3-2} typ. 0.8 V

Collector-emitter voltage at $I_4 = 50$ mA $V_{4-3} < 3.5$ V

CHARACTERISTICS at $V_B = 14$ V; $T_{amb} = 25$ °C (measured in circuit below)

Voltage gain at $f = 1$ kHz; without feedback G_V typ. 80 dB
with feedback G_V typ. 50 dB

Input impedance at $f = 1$ kHz $|Z_{9-10}| > 70$ k Ω

Noise figure at $B = 60$ Hz to 10 kHz F typ. 6 dB

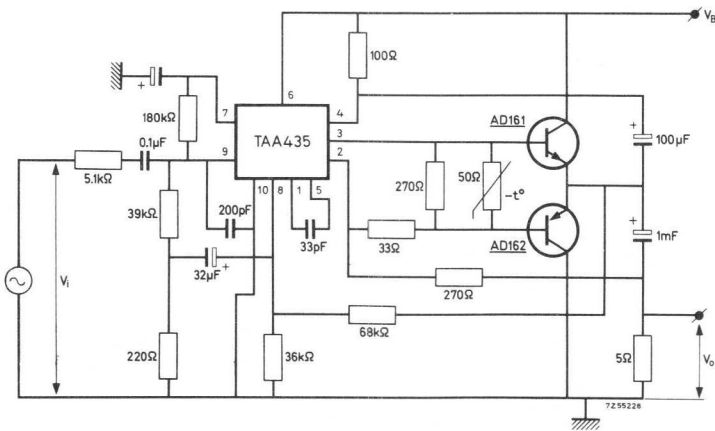
Cut-off frequency (-3 dB) $f_C > 10$ kHz

Output power at $f = 1$ kHz
 $d_{tot} = 10\%$ $P_O > 4$ W

Total distortion at $f = 1$ kHz
 $P_O = 1$ W $d_{tot} < 1$ %

Input signal for $P_O = 4$ W $V_{i(rms)}$ typ. 15 mV

Test circuit:



100
100
100
100
100

FM CHANNEL AMPLIFIER

The TAA450 is a monolithic integrated circuit containing an i.f. amplifier with limiting characteristics for use up to frequencies of 10 MHz, a ratio detector and an i.f. amplifier with connections brought out for remote volume control.

QUICK REFERENCE DATA

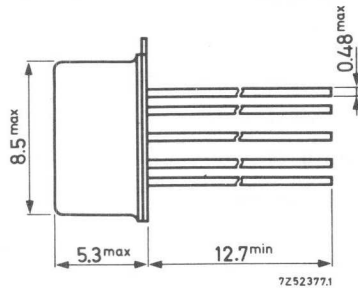
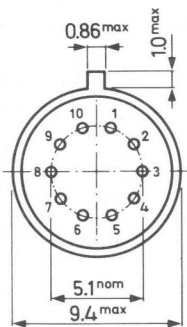
Operating characteristics of i.f. amplifier at $f = 5.5$ MHz
 Supply voltage $V_B = 7.5$ V; $T_{amb} = 25$ °C

| | | | |
|-------------------|-------|------|-------------|
| Voltage gain | G_V | typ. | 69 dB |
| Start of limiting | V_i | typ. | 300 μ V |

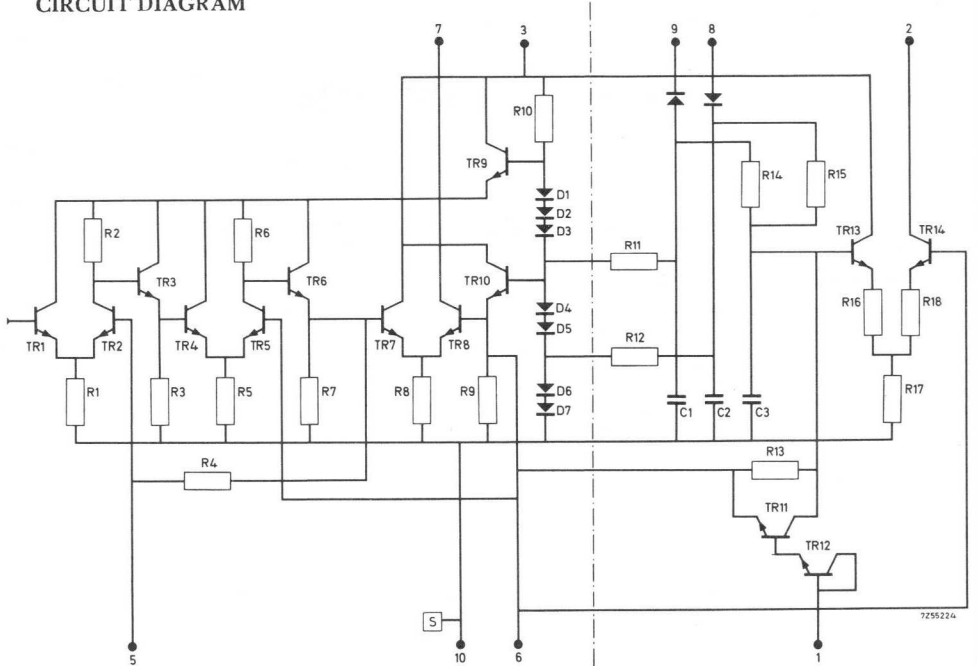
PACKAGE OUTLINE

Dimensions in mm

TO-74; reduced height



CIRCUIT DIAGRAM



RATINGS (Limiting values in accordance with the Absolute Maximum System (IEC 134))

Supply voltage (d.c.) i.f. amplifier
a.f. amplifier

$V_7 = V_3$ max. 12 V
 V_2 max. 18 V¹⁾

Total power dissipation

P_{tot} max. 380 mW

Storage temperature

T_{stg} -20 to +125 °C

Operating ambient temperature

T_{amb} -20 to +60 °C

¹⁾ During warming-up in tube receivers this value may be exceeded up to 30 V.

CHARACTERISTICS for i.f. amplifier part at $V_B = 7.5\text{ V}$; $T_{\text{amb}} = 25\text{ }^\circ\text{C}$

Voltage gain

| | | |
|-------------------------------------------------------|-------|-----------------------|
| $V_i = 100\text{ }\mu\text{V}$; $f = 1\text{ MHz}$ | G_V | typ. 71 dB |
| $V_i = 100\text{ }\mu\text{V}$; $f = 4.5\text{ MHz}$ | G_V | typ. 69 dB |
| $V_i = 100\text{ }\mu\text{V}$; $f = 5.5\text{ MHz}$ | G_V | > 66 dB typ. 69 dB |

Start of limiting at $f = 5.5\text{ MHz}$

| | |
|-------|------------------------|
| V_i | typ. 300 μV |
|-------|------------------------|

Output current (peak to peak) at $V_i = 5\text{ mV}$

| | |
|---------------------|-------------|
| $I_{7(\text{p-p})}$ | typ. 2.8 mA |
|---------------------|-------------|

Input resistance

| | |
|-------|------------------------|
| R_i | > 2.5 $\text{k}\Omega$ |
|-------|------------------------|

Input capacitance

| | |
|-------|----------------------|
| C_i | typ. 7 pF < 10 pF |
|-------|----------------------|

Output resistance

| | |
|-------|-----------------------|
| R_o | > 10 $\text{k}\Omega$ |
|-------|-----------------------|

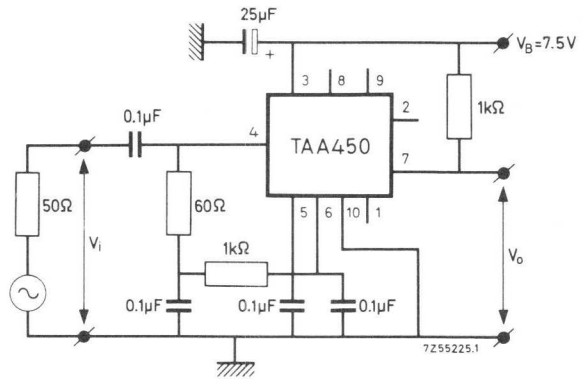
Output capacitance

| | |
|-------|---------------------|
| C_o | typ. 4 pF < 6 pF |
|-------|---------------------|

Total current

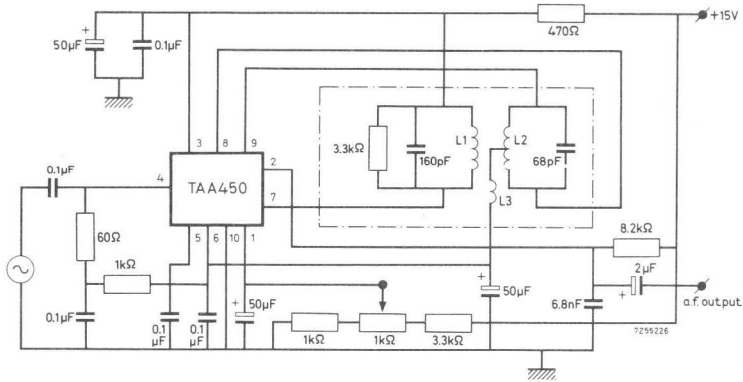
| | |
|-------|-----------------------|
| I_B | typ. 18 mA < 22 mA |
|-------|-----------------------|

Test circuit



APPLICATION INFORMATION

Circuit with the TAA450 in an i. f. -l. f. amplifier of a television receiver.



Primary: frame core AP3014/02

Secondary: no frame core

L1 = 19 turns 0.12 mm stranded Cu wire

L2 = 2 x 17 turns 0.12 mm stranded Cu wire; bifilarly wound

L3 = 14 turns 0.12 mm stranded Cu wire; bifilarly wound with L1

Top-to-top distance of frequency response curve: ≥ 250 kHz

| | | |
|------------------------|------------|--------------|
| Intermediate frequency | f_0 | = 5.5 MHz |
| Frequency deviation | Δf | ± 15 kHz |
| Modulation frequency | f_m | = 400 Hz |
| Ambient temperature | T_{amb} | = 25 °C |

| | | | |
|---------------------------------------------------------|------------------------|--------|-------------|
| Start of limiting | V_i | typ. | 300 μ V |
| I. F. output voltage at pin 7 with $V_i \geq 300 \mu$ V | V_7 | typ. | 1.2 V |
| L. F. output voltage at $V_i \geq 300 \mu$ V | $V_o(\text{rms})$ | typ. | 600 mV |
| A. M. suppression | | | |
| $f_m = 1$ kHz; $m = 0.3$; $V_i \geq 2$ mV | | \geq | 42 dB |
| Volume control range | ΔV_o | \geq | 30 dB |
| Distortion at $\Delta f \pm 15$ kHz | without volume control | d | typ. 0.015 |
| | with volume control | d | typ. 0.02 |
| $\Delta f \pm 50$ kHz | without volume control | d | typ. 0.025 |
| | with volume control | d | typ. 0.05 |
| Supply current l. f. part (pin 2) | I_{p2} | typ. | 1 mA |

OPERATIONAL AMPLIFIER

The TAA521 is a silicon monolithic integrated operational amplifier in an XA8 (TO-99) metal envelope.

It has a high gain, low offset, high input impedance, high output voltage swing and low power dissipation. The operating temperature range is 0 to +70 °C.

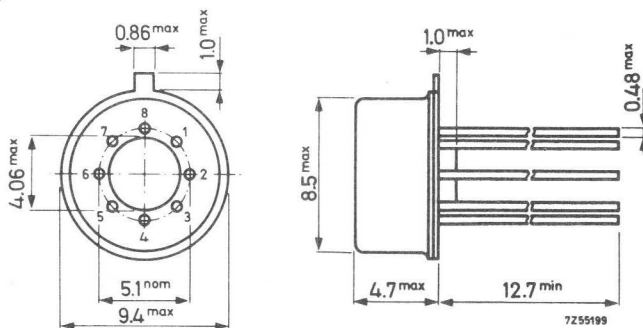
QUICK REFERENCE DATA

| | | |
|-----------------------------------------------------------|----------------------------------|--------------------------------------|
| Positive supply voltage | V_P | 15 V |
| Negative supply voltage | $-V_N$ | 15 V |
| ----- | | |
| Characteristics at $T_{amb} = 25\text{ }^\circ\text{C}$ | | |
| Voltage gain | G_V | typ. 45000 |
| Common mode rejection ratio | CMRR | typ. 90 dB |
| Input offset voltage drift; $R_S = 50\text{ }\Omega$ | $\frac{\Delta V_{io}}{\Delta T}$ | typ. 6 $\mu\text{V}/^\circ\text{C}$ |
| | $\frac{\Delta V_{io}}{\Delta T}$ | typ. 10 $\mu\text{V}/^\circ\text{C}$ |
| $R_S \leq 10\text{ k}\Omega$ | | |
| Differential input resistance | R_i | typ. 250 k Ω |
| Peak output voltage swing at $R_L \geq 10\text{ k}\Omega$ | V_{OM} | typ. $\pm 14\text{ V}$ |
| Power dissipation | P_{tot} | typ. 80 mW |

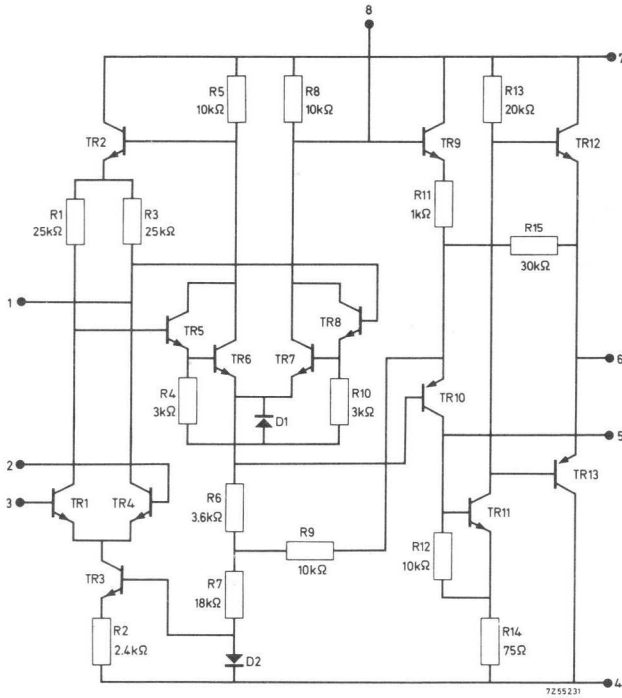
PACKAGE OUTLINE

Dimensions in mm

TO-99



CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

| | | | |
|---------------------------|-----------|------|------------|
| Positive supply voltage | V_P | max. | 18 V |
| Negative supply voltage | $-V_N$ | max. | 18 V |
| Common mode voltage | V_i | max. | ± 10 V |
| Differential mode voltage | V_{2-3} | max. | ± 5 V |

Power dissipation up to $T_{case} = 70^\circ C$ P_{tot} max. 250 mW

Output short circuit duration ($T_{amb} = 25^\circ C$) t max. 5 s

Temperatures

| | | |
|-------------------------------|-----------|-------------------------|
| Operating ambient temperature | T_{amb} | 0 to $+70^\circ C$ |
| Storage temperature | T_{stg} | -65 to $+150^\circ C$ |

CHARACTERISTICS at $V_P = 15\text{ V}$; $-V_N = 15\text{ V}$; $T_{\text{amb}} = 25^\circ\text{C}$ unless otherwise specified

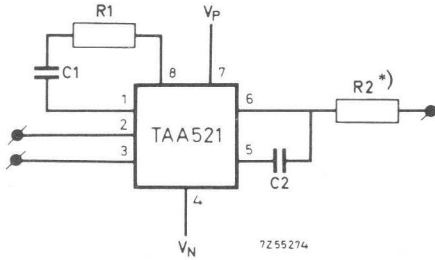
| | | | |
|------------------------------------------------------------------------------------------------------|------------------|------|----------------------------|
| <u>Voltage gain</u> ; $R_L \geq 2\text{ k}\Omega$; $V_O = \pm 10\text{ V}$ | G_V | > | 15000 |
| | | typ. | 45000 |
| <u>Input offset voltage</u> ; $R_S \leq 10\text{ k}\Omega$ $V_P = -V_N = 9\text{ to }15\text{ V}$ | V_{io} | typ. | 2.0 mV |
| | | < | 7.5 mV |
| <u>Input bias current</u> | I_i | typ. | 0.3 μA |
| | | < | 1.5 μA |
| <u>Input offset current</u> | I_{io} | typ. | 0.1 μA |
| | | < | 0.5 μA |
| <u>Common mode rejection ratio</u> ; $R_S \leq 10\text{ k}\Omega$ | CMRR | > | 65 dB |
| | | typ. | 90 dB |
| <u>Input voltage range</u> | V_i | > | $\pm 8.0\text{ V}$ |
| | | typ. | $\pm 10\text{ V}$ |
| <u>Differential input resistance</u> | R_i | > | 50 $\text{k}\Omega$ |
| | | typ. | 250 $\text{k}\Omega$ |
| <u>Output resistance</u> | R_o | typ. | 150 Ω |
| <u>Supply voltage rejection ratio</u> ; $R_S \leq 10\text{ k}\Omega$ | SVRR | typ. | 25 $\mu\text{V}/\text{V}$ |
| | | < | 200 $\mu\text{V}/\text{V}$ |
| <u>Peak output voltage swing</u> at $R_L \geq 10\text{ k}\Omega$ | V_{OM} | > | $\pm 12\text{ V}$ |
| | | typ. | $\pm 14\text{ V}$ |
| $R_L \geq 2\text{ k}\Omega$ | V_{OM} | > | $\pm 10\text{ V}$ |
| | | typ. | $\pm 13\text{ V}$ |
| <u>Power dissipation</u> at $V_O = 0$ | P_{tot} | typ. | 80 mW |
| | | < | 200 mW |

TAA521

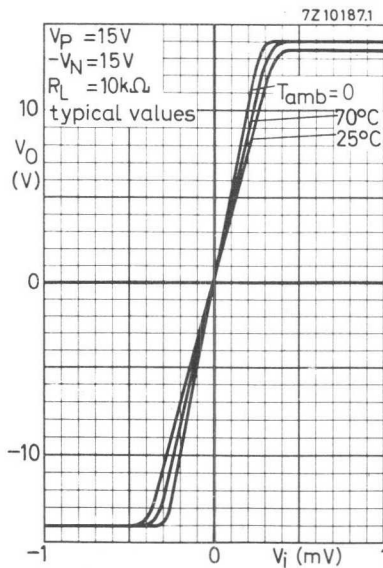
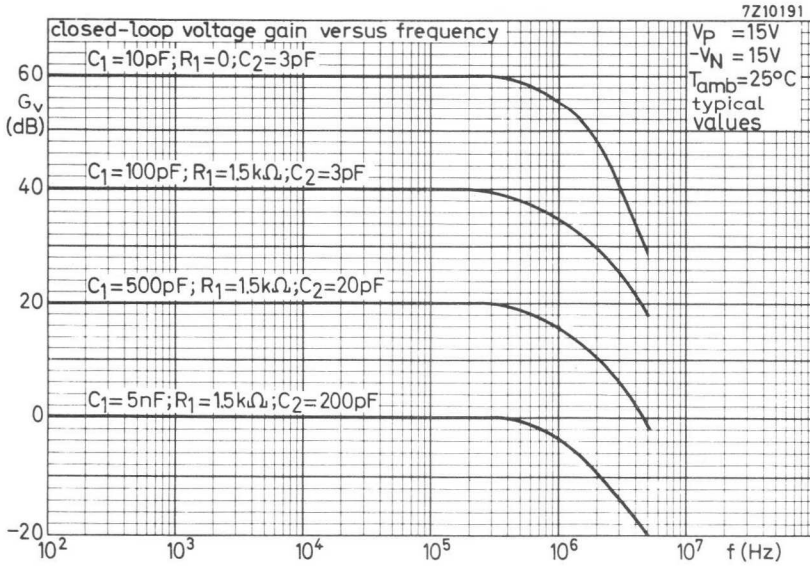
CHARACTERISTICS at $V_P = 15\text{ V}$; $-V_N = 15\text{ V}$; $T_{\text{amb}} = 0\text{ to }+70\text{ }^\circ\text{C}$ unless otherwise specified

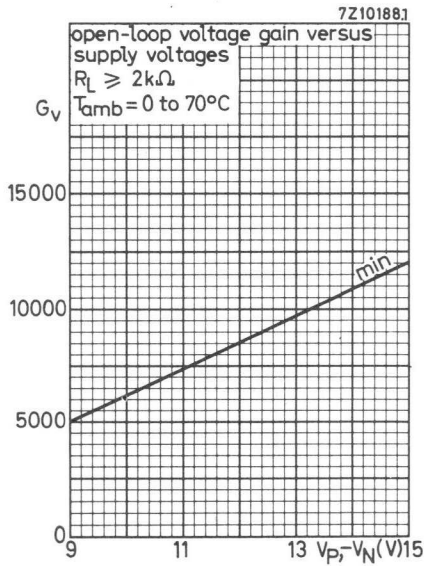
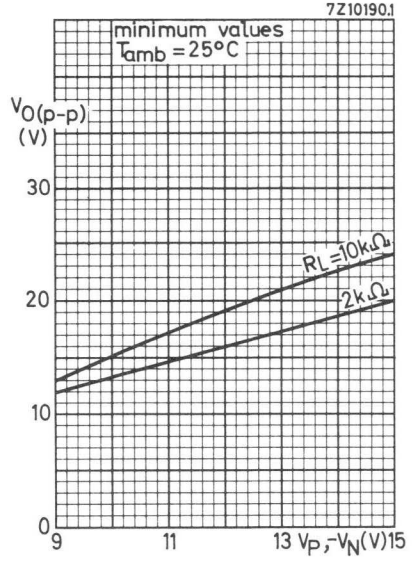
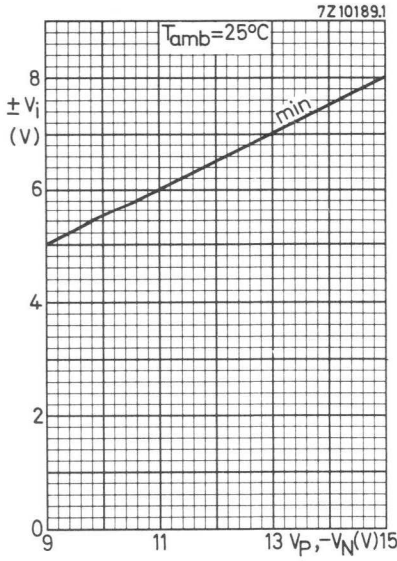
| | | | |
|--------------------------------------------------------------------------------------------------------|----------------------------------|------|---------------------------------|
| <u>Voltage gain</u> ; $R_L \geq 2\text{ k}\Omega$; $V_O = \pm 10\text{ V}$ | G_V | > | 12000 |
| <u>Input offset voltage</u> ; $R_S \leq 10\text{ k}\Omega$; $V_P = -V_N = 9\text{ to }15\text{ V}$ | V_{i0} | < | 10 mV |
| <u>Input offset voltage drift</u> ; $R_S = 50\ \Omega$ | $\frac{\Delta V_{i0}}{\Delta T}$ | typ. | 6 $\mu\text{V}/^\circ\text{C}$ |
| $R_S \leq 10\text{ k}\Omega$ | $\frac{\Delta V_{i0}}{\Delta T}$ | typ. | 10 $\mu\text{V}/^\circ\text{C}$ |
| <u>Input bias current</u> | I_i | < | 2 μA |
| <u>Input offset current</u> | I_{i0} | < | 0.75 μA |

Frequency compensation circuit :



*) For operation with a capacitive load use $R2 = 50\ \Omega$.





OPERATIONAL AMPLIFIER

The TAA522 is a silicon monolithic integrated operational amplifier in an XA8 (TO-99) metal envelope. It has a high gain, low offset, high input impedance, high output voltage swing and low power dissipation. The operating temperature range is -55 to $+125$ °C.

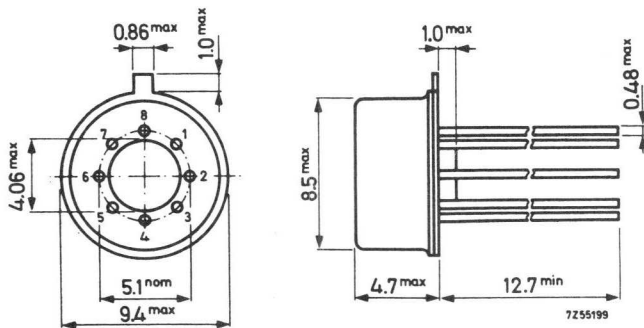
QUICK REFERENCE DATA

| | | |
|----------------------------------------------------|----------------------------------|-------------------------|
| Positive supply voltage | V_P | 15 V |
| Negative supply voltage | $-V_N$ | 15 V |
| ----- | | |
| Characteristics at $T_{amb} = -55$ to $+125$ °C | | |
| Voltage gain | G_V | typ. 45000 |
| Common mode rejection ratio | CMRR | typ. 90 dB |
| Input offset voltage drift; $R_S = 50 \Omega$ | $\frac{\Delta V_{iO}}{\Delta T}$ | typ. 3 $\mu V/^\circ C$ |
| $R_S \leq 10 k\Omega$ | $\frac{\Delta V_{iO}}{\Delta T}$ | typ. 6 $\mu V/^\circ C$ |
| Differential input resistance | R_i | typ. 100 k Ω |
| Peak output voltage swing at $R_L \geq 10 k\Omega$ | V_{OM} | typ. ± 14 V |

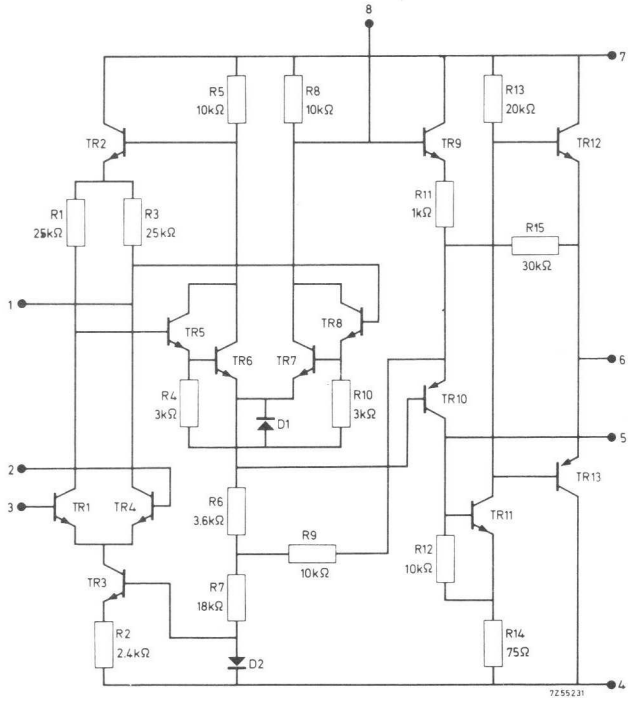
PACKAGE OUTLINE

Dimensions in mm

TO-99



CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

| | | | |
|------------------------------------------------------------------------------|-----------|------|------------|
| Positive supply voltage | V_P | max. | 18 V |
| Negative supply voltage | $-V_N$ | max. | 18 V |
| Common mode voltage | V_i | max. | ± 10 V |
| Differential mode voltage | V_{2-3} | max. | ± 5 V |
| Power dissipation up to $T_{case} = 125\text{ }^\circ\text{C}$ ¹⁾ | P_{tot} | max. | 300 mW |
| Output short circuit duration ($T_{amb} = 25\text{ }^\circ\text{C}$) | t | max. | 5 s |

Temperatures

| | | | |
|-------------------------------|-----------|-------------|------------------|
| Operating ambient temperature | T_{amb} | -55 to +125 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | -65 to +150 | $^\circ\text{C}$ |

CHARACTERISTICS at $V_P = -V_N = 9$ to 15 V; $T_{amb} = 25\text{ }^\circ\text{C}$ unless otherwise specified

| | | | |
|-----------------------------------------------------------------------------------------|------------------------|------|----------------------|
| <u>Input offset voltage</u> ; $R_S \leq 10\text{ k}\Omega$ | V_{io} | typ. | 1.0 mV |
| | | < | 5.0 mV |
| <u>Input bias current</u> | I_i | typ. | 0.2 μA |
| | | < | 0.5 μA |
| <u>Input offset current</u> | I_{io} | typ. | 50 nA |
| | | < | 200 nA |
| <u>Differential input resistance</u> | R_i | > | 150 $\text{k}\Omega$ |
| | | typ. | 400 $\text{k}\Omega$ |
| <u>Output resistance</u> | R_o | typ. | 150 Ω |
| <u>Power dissipation at $V_O = 0$; $V_P = -V_N = 15\text{ V}$</u> | P_{tot} | typ. | 80 mW |
| | | < | 165 mW |
| <u>Transient reponse</u> (see also test circuit on page 4) | | | |
| Rise time | t_r | typ. | 0.3 μs |
| | | < | 1.5 μs |
| Overshoot | $\frac{\Delta V}{V_O}$ | typ. | 10 % |
| | | < | 30 % |

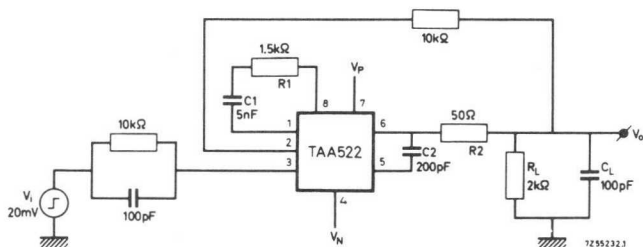
¹⁾ Rating applies to case temperatures up to 125 $^\circ\text{C}$; derate linearly at 5.5 mW/ $^\circ\text{C}$ for ambient temperatures above 95 $^\circ\text{C}$.

TAA522

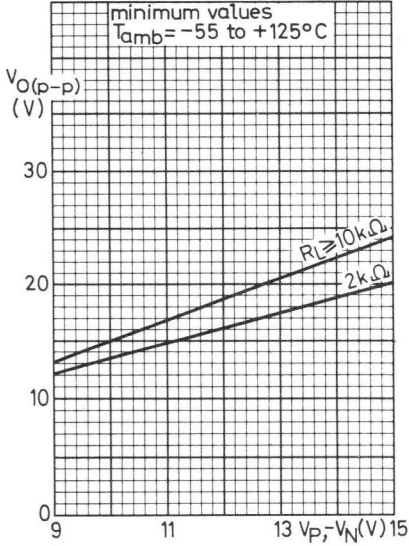
CHARACTERISTICS at $V_P = -V_N = 9$ to 15 V; $T_{amb} = -55$ to $+125$ °C unless otherwise specified

| | | |
|------------------------------------------------------------------------------------------|----------------------------------|----------------------------------------|
| <u>Voltage gain</u> at $V_P = -V_N = 15$ V $R_L \geq 2$ k Ω ; $V_O = \pm 10$ V | G_v | 25000 to 70000 typ. 45000 |
| <u>Input offset voltage</u> ; $R_S \leq 10$ k Ω | V_{iO} | < 6 mV |
| <u>Input offset voltage drift</u> ; $R_S = 50$ Ω $R_S \leq 10$ k Ω | $\frac{\Delta V_{iO}}{\Delta T}$ | typ. 3 μ V/°C typ. 6 μ V/°C |
| <u>Input voltage range</u> at $V_P = -V_N = 15$ V | V_i | > ± 8 V typ. ± 10 V |
| <u>Peak output voltage swing</u> at $V_P = -V_N = 15$ V $R_L \geq 10$ k Ω | V_{OM} | > ± 12 V typ. ± 14 V |
| $R_L \geq 2$ k Ω | V_{OM} | > ± 10 V typ. ± 13 V |
| <u>Common mode rejection ratio</u> ; $R_S \leq 10$ k Ω | CMRR | > 70 dB typ. 90 dB |
| <u>Supply voltage rejection ratio</u> ; $R_S \leq 10$ k Ω | SVRR | typ. 25 μ V/V < 150 μ V/V |
| <u>Input bias current</u> at $T_{amb} = -55$ °C | I_i | typ. 0.5 μ A < 1.5 μ A |
| <u>Input offset current</u> at $T_{amb} = -55$ °C | I_{iO} | typ. 0.1 μ A < 0.5 μ A |
| at $T_{amb} = +125$ °C | I_{iO} | typ. 20 nA < 200 nA |
| <u>Differential input resistance</u> | R_i | > 40 k Ω typ. 100 k Ω |

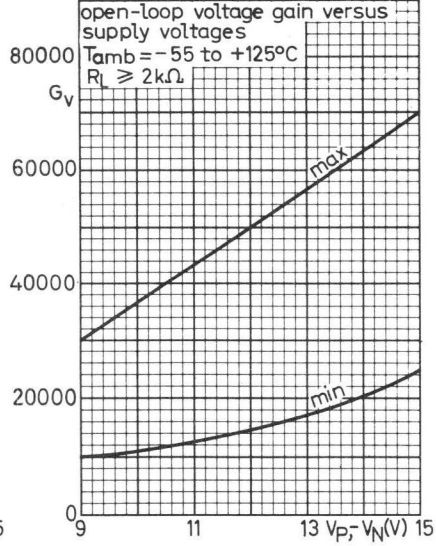
Test circuit for transient response:



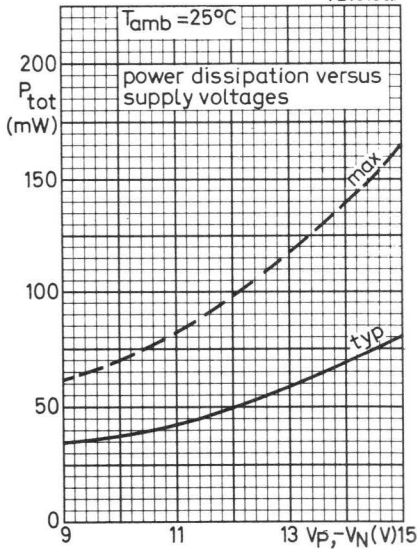
7Z10198.1



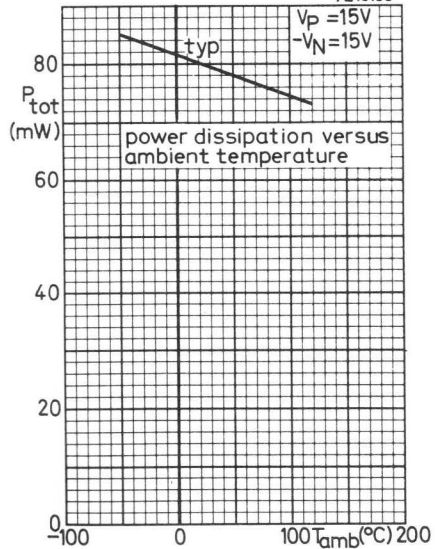
7Z10192



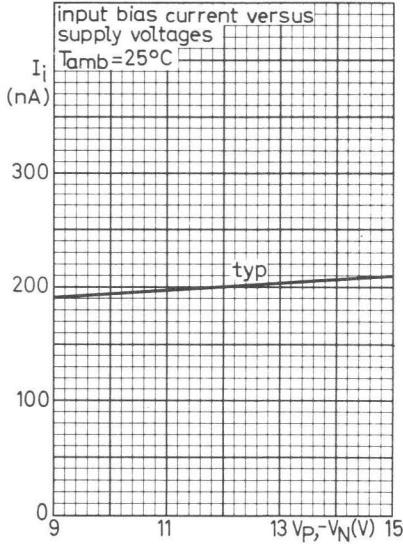
7Z10196.1



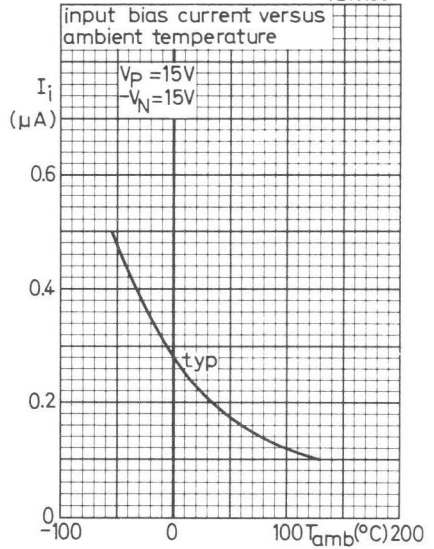
7Z10199



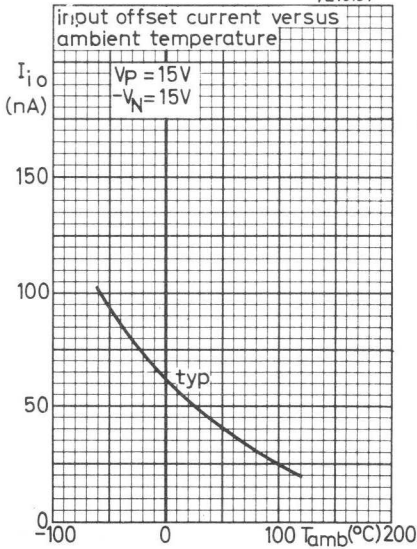
7Z10194



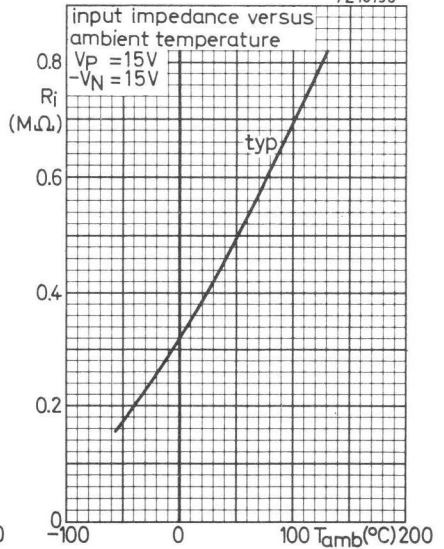
7Z10195

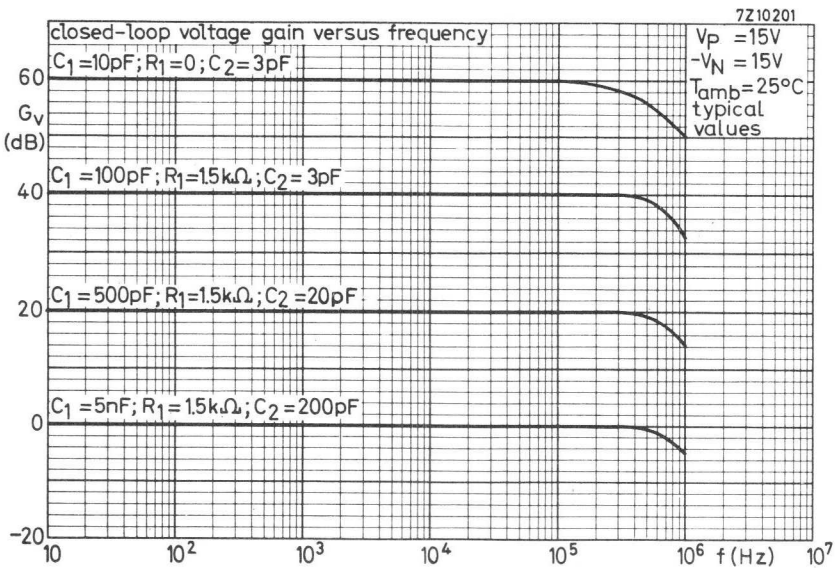
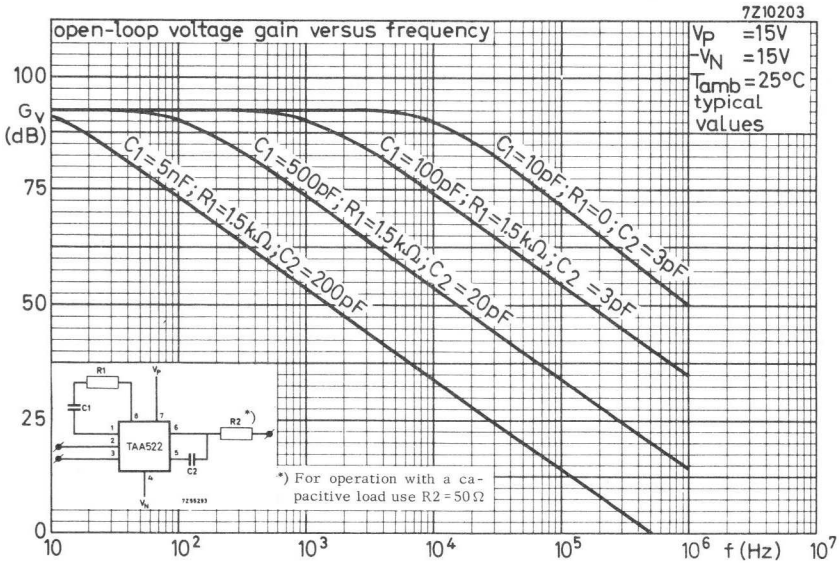


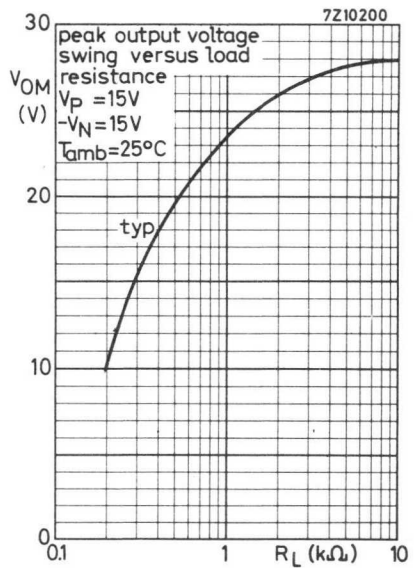
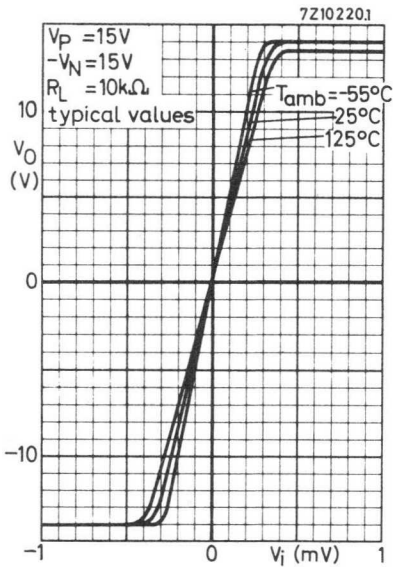
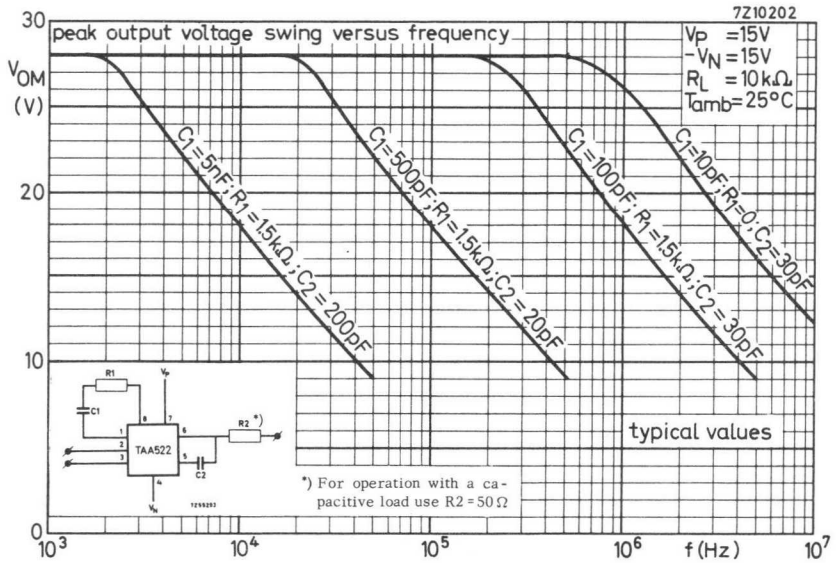
7Z10197



7Z10193







VOLTAGE STABILIZER

The TAA550 is an integrated monolithic voltage stabilizer, especially designed to provide the supply voltage for variable capacitance diodes in television tuners independent of supply voltage and temperature variations.

The TAA550 is supplied in 3 voltage groups, identified by a coloured dot on the envelope:

| | | |
|-------------------------------|------------|------------|
| Stabilized voltage V_{12} : | 31 to 32 V | red dot |
| | 32 to 34 V | yellow dot |
| | 34 to 35 V | green dot |

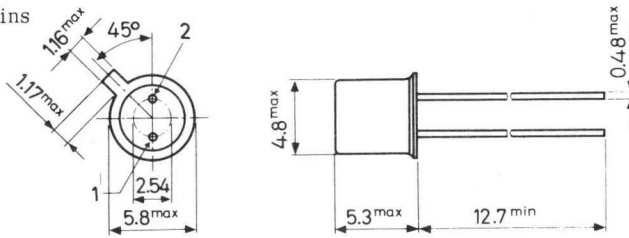
QUICK REFERENCE DATA

| | | |
|----------------------------------|----------|------------------|
| Supply current | I_1 | typ. 5 mA |
| Stabilized voltage | V_{12} | 31 to 35 V |
| Differential internal resistance | r_{12} | typ. 10 Ω |

PACKAGE OUTLINE

Dimensions in mm

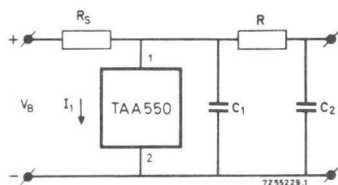
TO-18; 2 pins



pin 1 connected to the case

TAA550

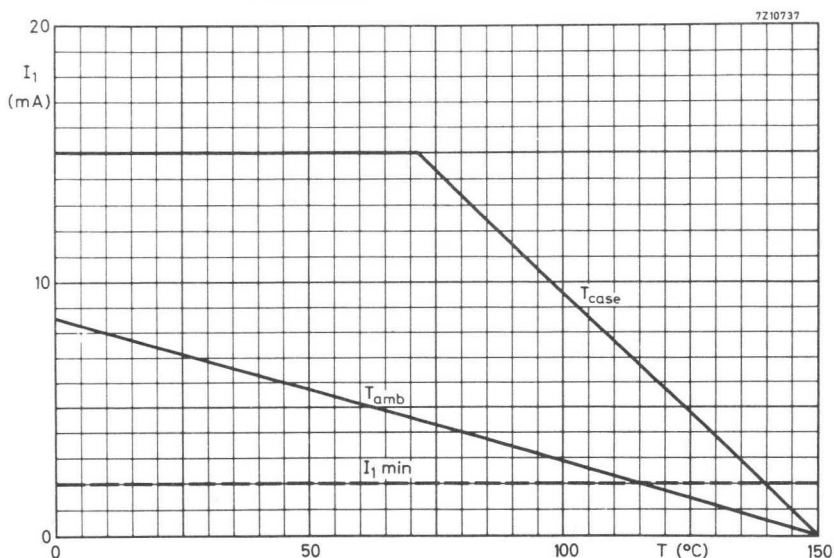
RECOMMENDED CIRCUIT



$V_B \gg V_{12}$
 I_1 typ. 5 mA
 $R \geq 22 \Omega$
 $C_1 = 300$ to 4700 pF

C_2 : to be connected if decoupling for low frequency noise is necessary.
 In practice values up to $10 \mu\text{F}$ are used.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)
Maximum allowable supply current versus temperature



Temperatures

Storage temperature
 Operating ambient temperature

T_{stg} -20 to +150 °C
 T_{amb} -20 to +150 °C

CHARACTERISTICS

Recommended supply current

I_1 > 2 mA
 typ. 5 mA

Stabilized voltage

V_{12} 31 to 35 V

Differential internal resistance at $f = 1 \text{ kHz}$

$I_1 = 5 \text{ mA}$

r_{12} typ. 10 Ω
 < 25 Ω

Temperature coefficient at $T_{\text{amb}} = 10$ to $50 \text{ }^\circ\text{C}$

$\frac{\Delta V_{12}}{\Delta T_{\text{amb}}}$ typ. -0.13 mV/°C
 -3.1 to +1.55 mV/°C

LEVEL DETECTOR

The TAA560 is a silicon monolithic integrated level detector in a (TO-72) metal envelope. A Darlington input circuit forms a Schmitt-trigger that operates at a low current level. Due to the three-stage current amplifier an output current of maximum 50 mA can be delivered.

It is primarily intended for battery fed timing circuits, such as in camera shutter control.

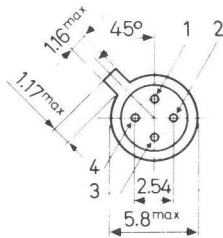
QUICK REFERENCE DATA

| | | |
|---------------------------------------|------------------|--------------|
| Total supply voltage | V ₃₋₄ | 2.5 V |
| Ambient temperature | T _{amb} | 25 °C |
| ----- | | |
| Threshold voltage (switching off TR8) | V ₂₋₄ | 1.4 to 1.6 V |
| <u>OFF-state of TR8</u> | | |
| Output current | I ₁ | ≤ 0.1 μA |
| <u>ON-state of TR8</u> | | |
| Output current | I ₁ | max. 50 mA |
| Operating ambient temperature | T _{amb} | 0 to +60 °C |

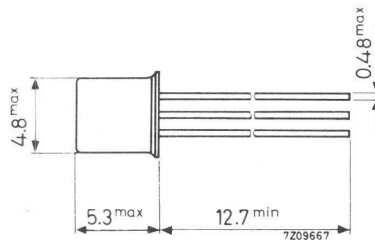
PACKAGE OUTLINE

Dimensions in mm

(TO-72)

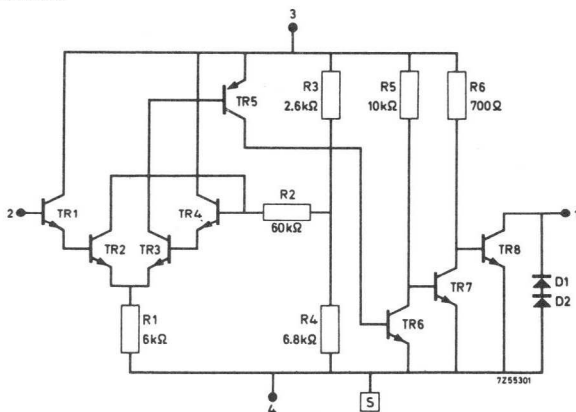


bottom view



TAA560

CIRCUIT DIAGRAM



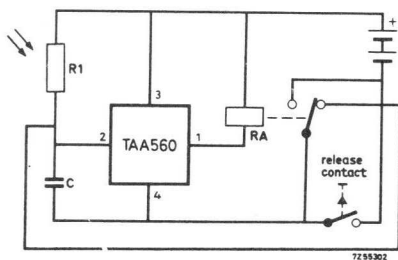
RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|-------------------------------|-----------|------|----------------|
| Total supply voltage | V_{3-4} | max. | 4.5 V |
| Input voltage | V_{2-4} | max. | 4.5 V |
| Output voltage | V_{1-4} | max. | 12.5 V |
| Output current | I_1 | max. | 50 mA |
| Total power dissipation | P_{tot} | max. | 120 mW |
| Storage temperature | T_{stg} | | -55 to +100 °C |
| Operating ambient temperature | T_{amb} | | 0 to + 60 °C |

CHARACTERISTICS

Recommended circuit for camera shutter time control:



Notes:

- For shutter time range of 2 ms to 2 s; $C \approx 100\text{nF}$; $R_1 \leq 20 \text{ M}\Omega$
- Solenoid inductance $L_S \leq 40 \text{ mH}$ and resistance $R_S = 91 \Omega$; $V_{3-4} = 2.5 \text{ V}$

CHARACTERISTICS (continued) at $T_{amb} = 25^{\circ}\text{C}$; $R_1 \leq 20\text{ M}\Omega$; $R_L = 91\ \Omega$

Threshold voltage

Switching TR8 to OFF-state

at $V_{3-4} = 2.5\text{ V}$

| | | |
|--------------|------------|-----------------|
| $V_{2-4(H)}$ | 1.4 to 1.6 | V ¹⁾ |
| $V_{2-4(H)}$ | typ. 1.5 | V |

at $V_{3-4} = 4.5\text{ V}$

| | | |
|--------------|----------|---|
| $V_{2-4(H)}$ | typ. 2.9 | V |
|--------------|----------|---|

Switching TR8 to ON-state

at $V_{3-4} = 2.5\text{ V}$

| | | |
|--------------|----------|---|
| $V_{2-4(L)}$ | typ. 1.2 | V |
|--------------|----------|---|

at $V_{3-4} = 4.5\text{ V}$

| | | |
|--------------|----------|---|
| $V_{2-4(L)}$ | typ. 1.4 | V |
|--------------|----------|---|

ON-state of TR8 (switch S closed)

Output voltage at $V_{3-4} = 2.5\text{ V}$

| | | | |
|-----------|--------|-----|----|
| V_{1-4} | \leq | 300 | mV |
|-----------|--------|-----|----|

Output current at $V_{3-4} = 2.5\text{ V}$

| | | | |
|-------|--------|------|----|
| I_1 | \leq | 26.5 | mA |
|-------|--------|------|----|

Current drain at $V_{3-4} = 2.5\text{ V}$

| | | | |
|-------|------|-----|----|
| I_3 | typ. | 3.5 | mA |
|-------|------|-----|----|

OFF-state of TR8 (switch S open)

Output current at $V_{3-4} = 2.5\text{ V}$

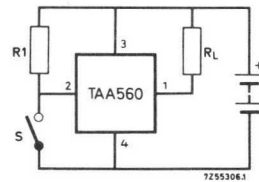
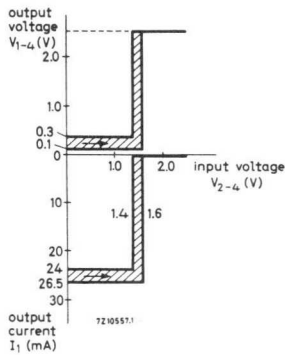
| | | | |
|-------|--------|-----|---------------|
| I_1 | \leq | 0.1 | μA |
|-------|--------|-----|---------------|

Current drain

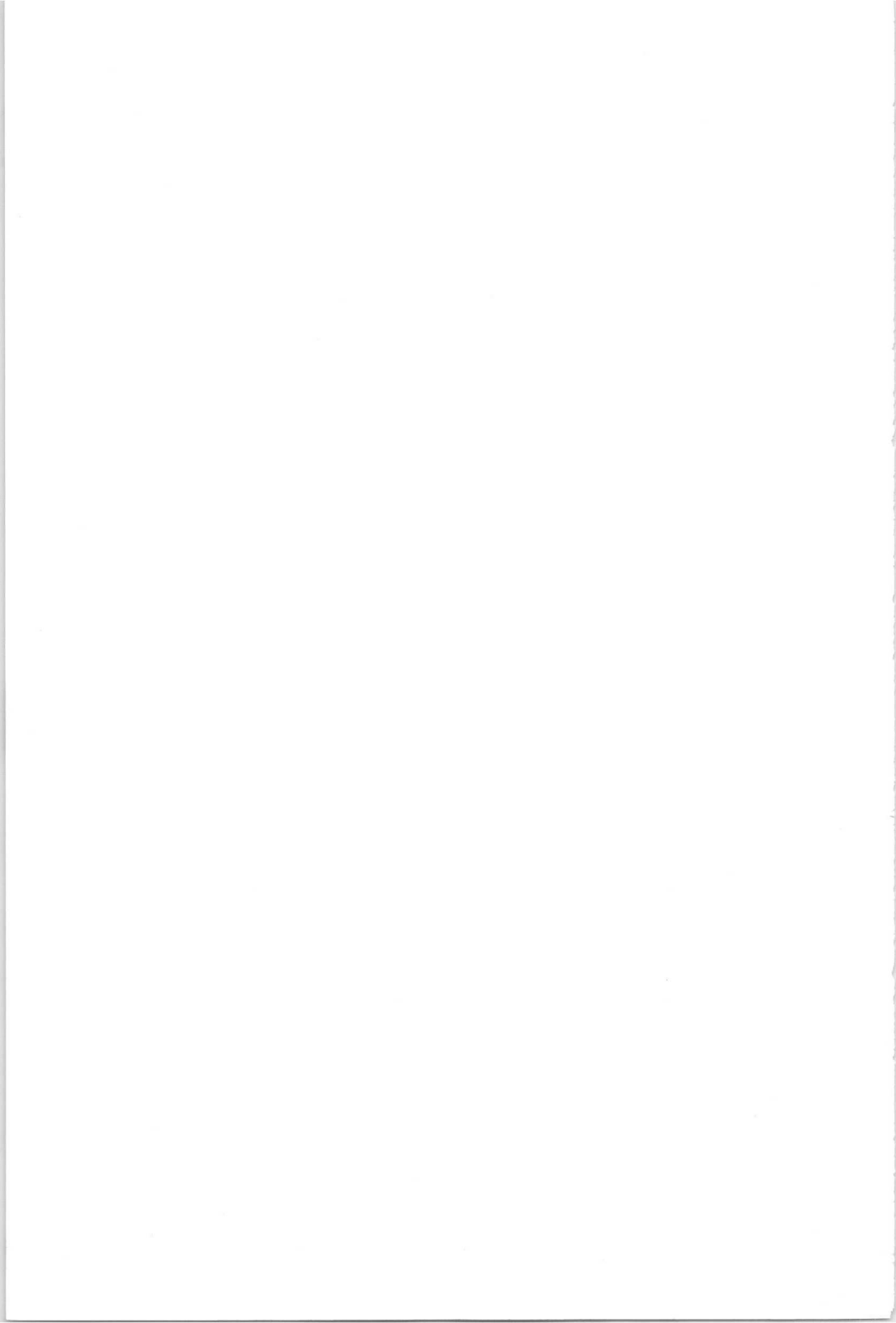
| | | | |
|-------|------|-----|----|
| I_3 | typ. | 4.1 | mA |
|-------|------|-----|----|

Transfer characteristic:

Test circuit:



1) See transfer characteristic.



LIMITER-AMPLIFIER

The TAA570 is a four-stage limiter-amplifier in a TO-74 metal envelope, with f.m. detector and remote control stage.

Excellent a.m. suppression is obtained by the use of a differential amplifier equipped with long-tailed pairs. The f.m. detector is a symmetrical phase detector. The remote control stage has a control range of about 80 dB. on the a.f. output signal.

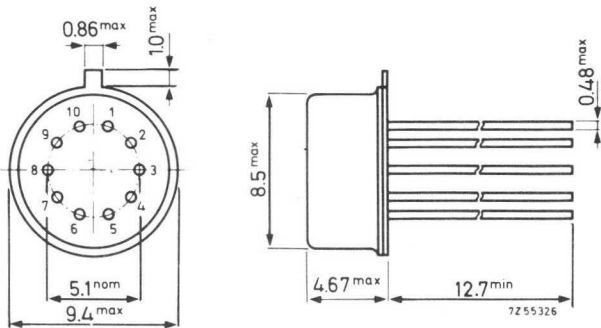
QUICK REFERENCE DATA

| | | | |
|-------------------------------------------------------------|-------------------|------|-------------------|
| Supply voltage | V_P | typ. | 12 V |
| Frequency | f_0 | | 5.5 MHz |
| <hr/> | | | |
| Total current drain | I_{tot} | typ. | 19 mA |
| Input limiting voltage | $V_i \text{ lim}$ | typ. | 100 μV |
| A.M. rejection at $V_i = 10 \text{ mV}$ | | typ. | 47 dB |
| Output at 50 kHz frequency deviation | $V_{o(rms)}$ | typ. | 1.8 V |
| Distortion at a frequency deviation of 50 kHz and full gain | d | typ. | 2.5 % |

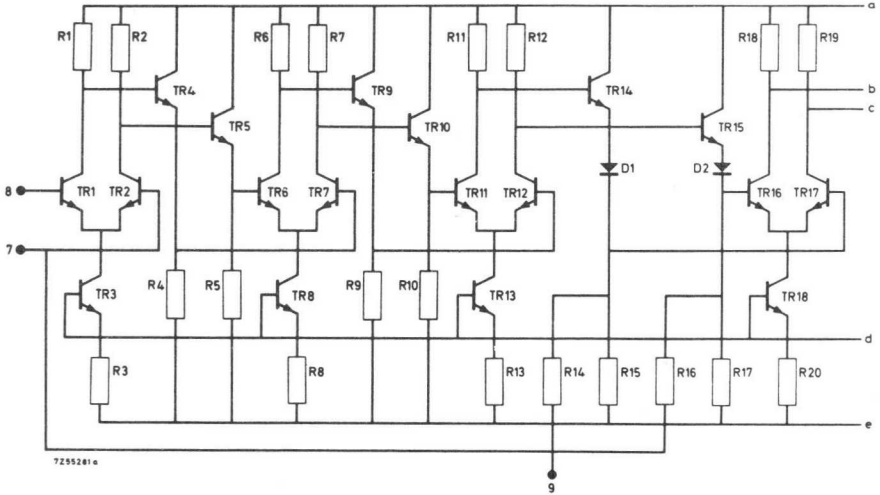
MECHANICAL DATA

Dimensions in mm

TO-74



CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

Pin No.1 voltage (do not apply an external voltage source)

Pin No.2 voltage (do not apply an external voltage source)

Pin.No.3 voltage

V₃₋₁₀ 0 to +18 V

Pin No.4 voltage; $I_4 < 1$ mA

V₄₋₁₀ 0 to +6 V

Pin No.5 voltage

V₅₋₁₀ 0 to +18 V

Pin No.6 voltage (do not apply an external voltage source)

Pin No.7 voltage; $I_7 < 1$ mA

V₇₋₁₀ 0 to +6 V

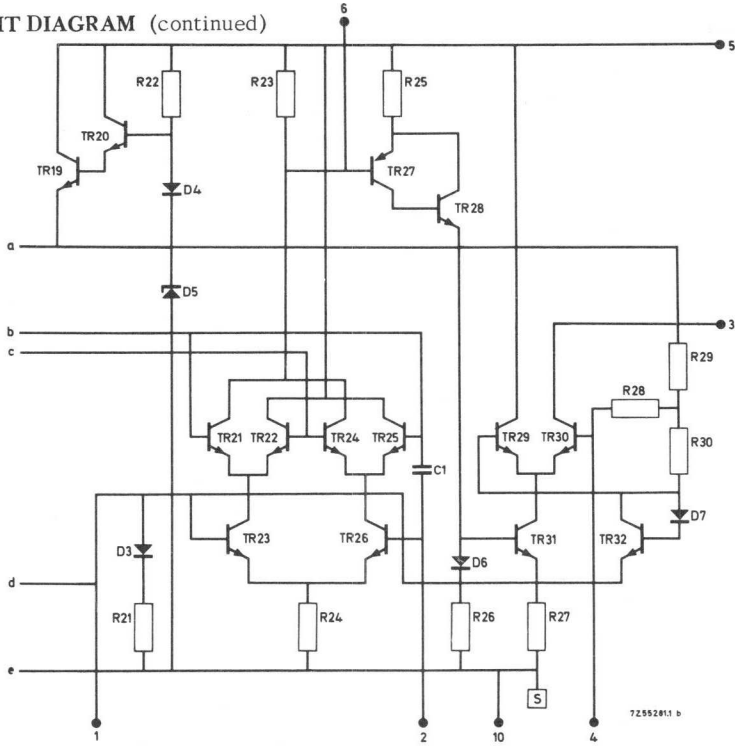
Pin No.8 voltage; $I_8 < 1$ mA

V₈₋₁₀ 0 to +6 V

Pin No.9 voltage

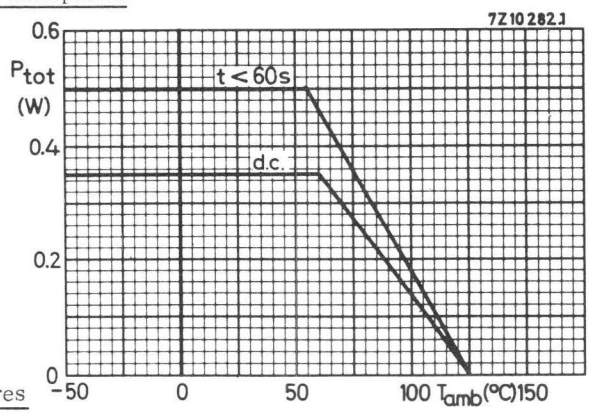
V₉₋₁₀ 0 to +6 V

CIRCUIT DIAGRAM (continued)



RATINGS (continued)

Total power dissipation



Temperatures

Storage temperature T_{stg} -25 to +125 °C

Operating ambient temperature T_{amb} -25 to +125 °C

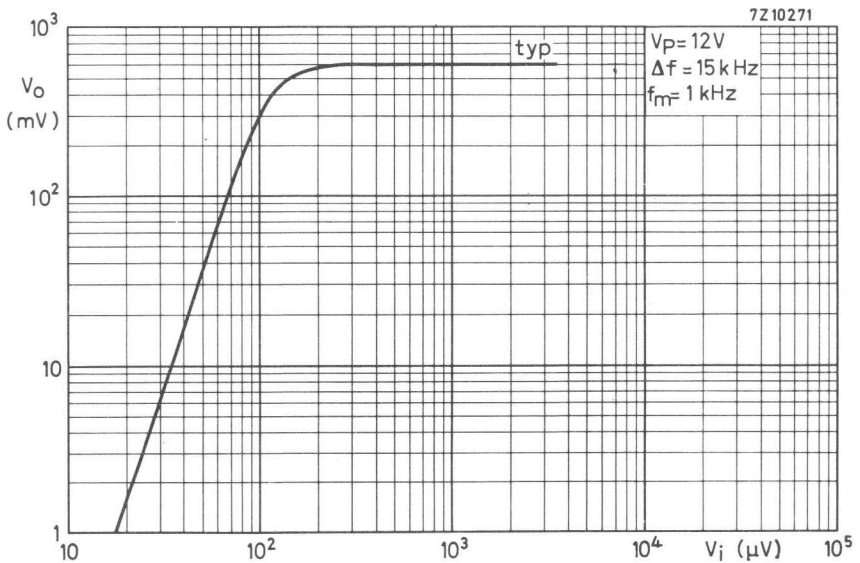
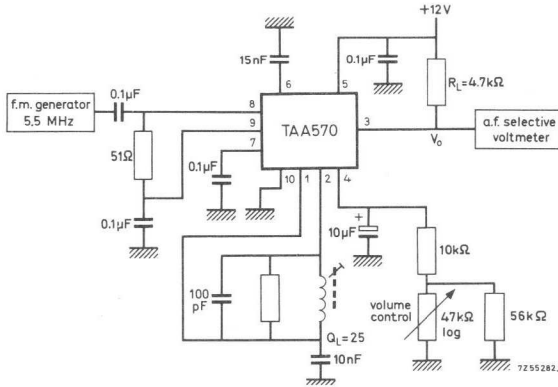
CHARACTERISTICS

Input limiting voltage

$$f_o = 5.5 \text{ MHz}; \Delta f = \pm 15 \text{ kHz}; f_m = 1 \text{ kHz}$$

$$V_{i \text{ lim}} \text{ typ. } 100 \text{ } \mu\text{V}$$

Test circuit for measuring $V_o = f(V_i)$



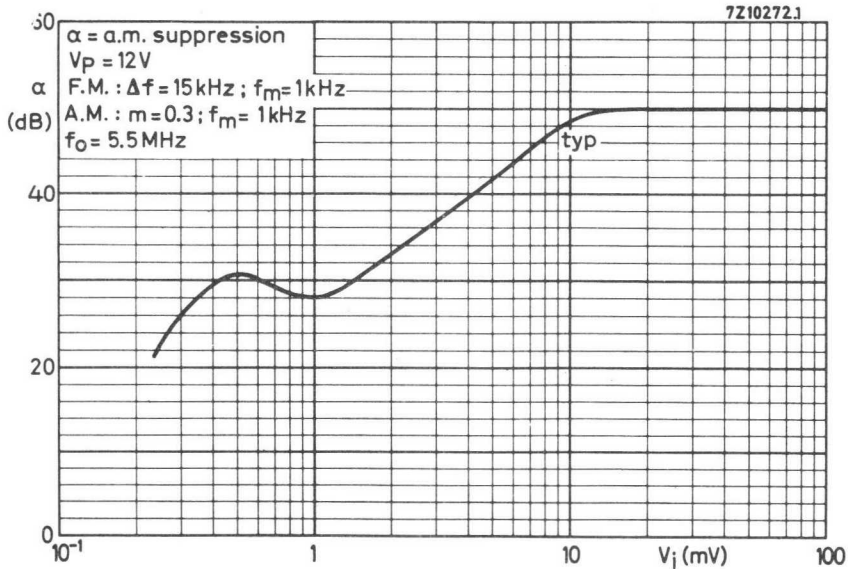
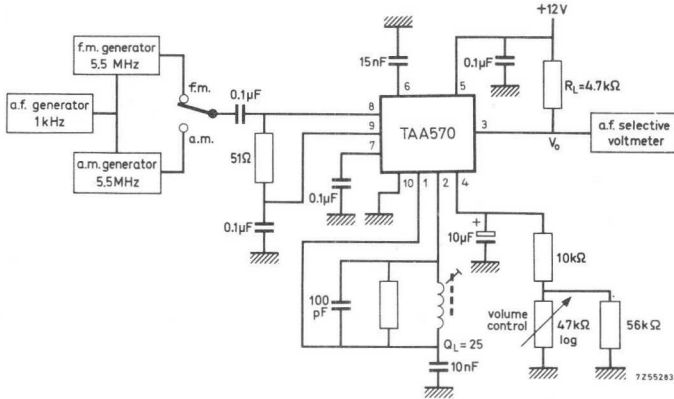
CHARACTERISTICS (continued)

A.M. suppression

F.M. : $f_o = 5.5 \text{ MHz}$; $\Delta F = \pm 15 \text{ kHz}$; $f_m = 1 \text{ kHz}$

A.M. : $f_o = 5.5 \text{ MHz}$; $m = 0.3$; $f_m = 1 \text{ kHz}$

Test circuit for measuring α (AM-suppression) = $f(V_i)$



CHARACTERISTICS (continued)

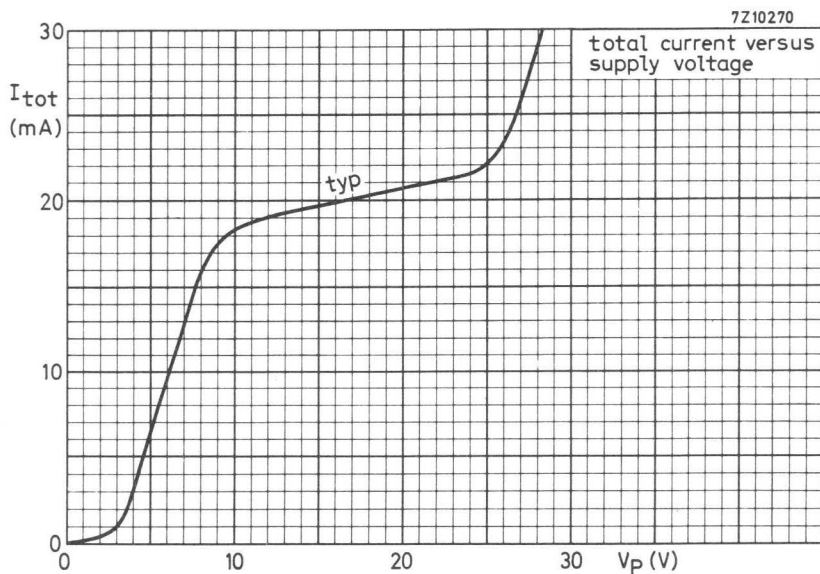
Distortion at full gain and $\Delta f = \pm 15$ kHz
 $\Delta f = \pm 50$ kHz

d typ. 1 %
d typ. 2.5 %

measuring conditions: $f_o = 5.5$ MHz
 $f_m = 1$ KHz

The distortion measurements are made with the test circuit on page 4.

Total current



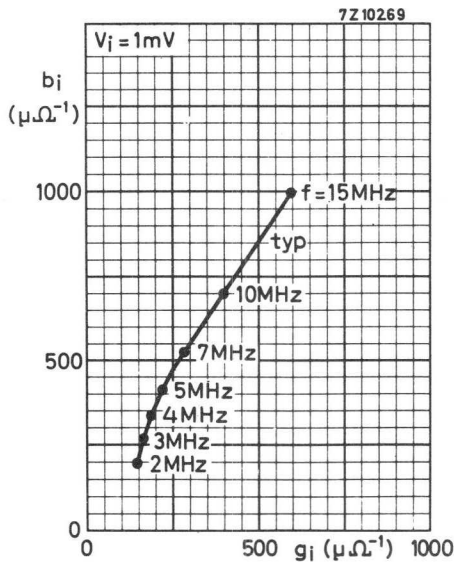
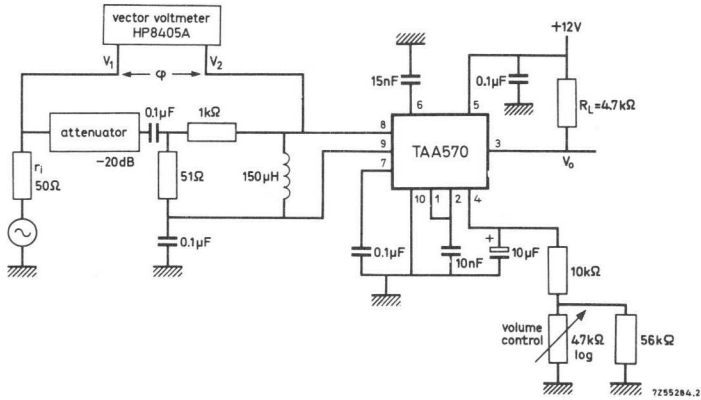
CHARACTERISTICS (continued)

y parameters.

Input admittance at $f_0 = 5.5 \text{ MHz}$

$$y_i \text{ typ. } (230 + j450) \mu\Omega^{-1}$$

Test circuit for measuring $y_i = f(f)$



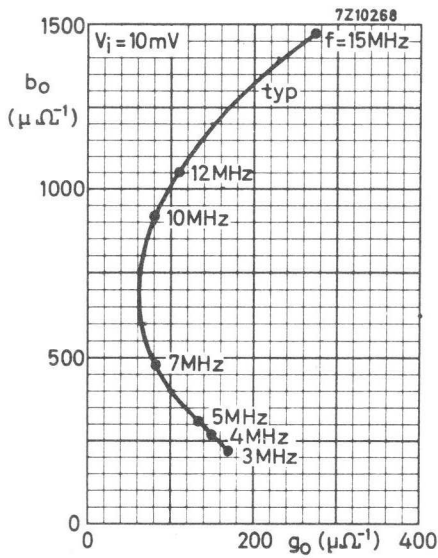
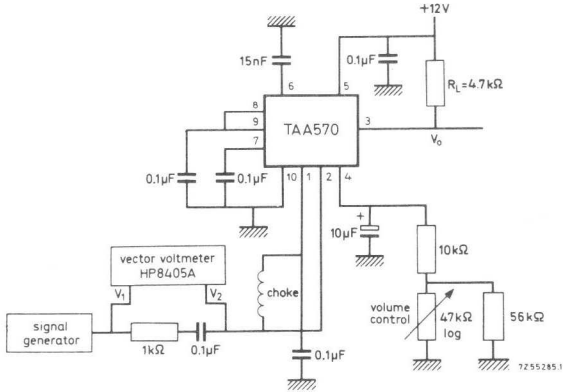
TAA570

CHARACTERISTICS (continued)

Output admittance at $f_0 = 5.5 \text{ MHz}$

$$y_o \text{ typ. } (120 + j330) \mu\Omega^{-1}$$

Test circuit for measuring $y_o = f(f)$

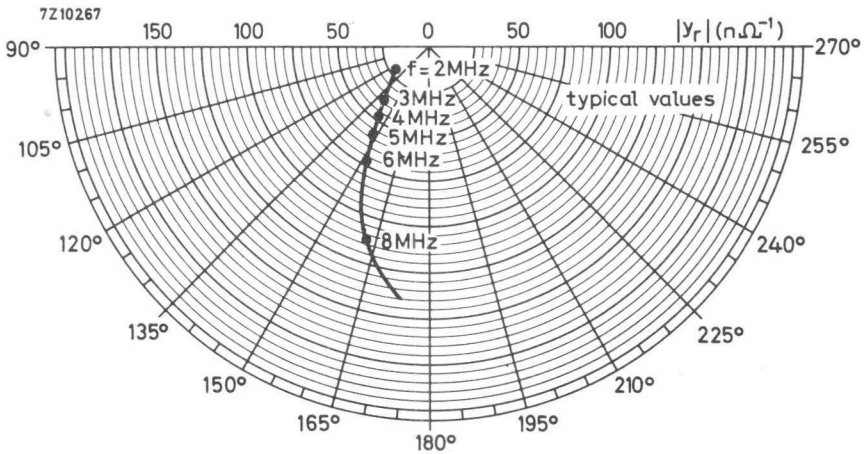
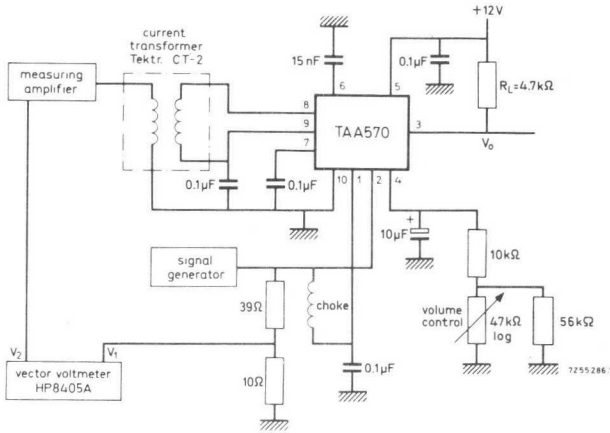


CHARACTERISTICS (continued)

Feedback admittance at $f_0 = 5.5 \text{ MHz}$

$$y_r \text{ typ. } |65| e^{j150^\circ} \text{ n}\Omega^{-1}$$

Test circuit for measuring $y_r = f(f)$



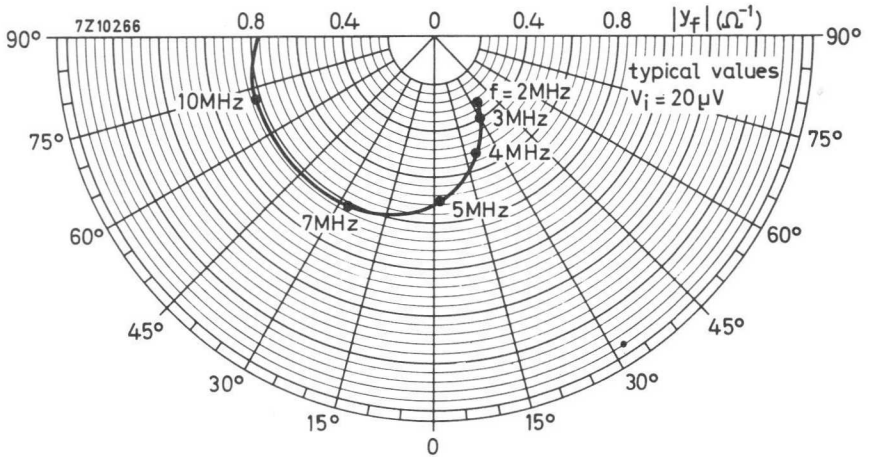
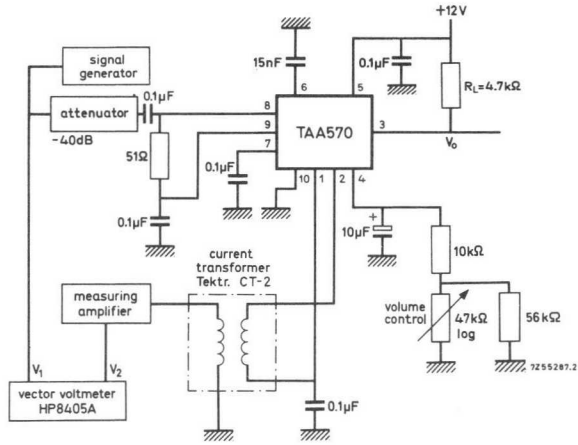
TAA570

CHARACTERISTICS (continued)

Transfer admittance at $f_0 = 5.5 \text{ MHz}$

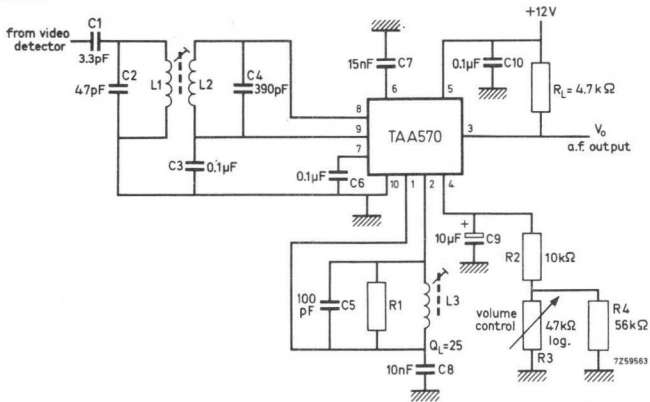
$$y_f \text{ typ. } |0.76| e^{-j6^\circ} \Omega^{-1}$$

Test circuit for measuring $y_f = f(f)$



APPLICATION INFORMATION

Practical circuit



The input bandpass filter is connected to the video detector via a small capacitor of 3.3 pF. The input bandpass filter ($kQ = 1$) has the following characteristics:

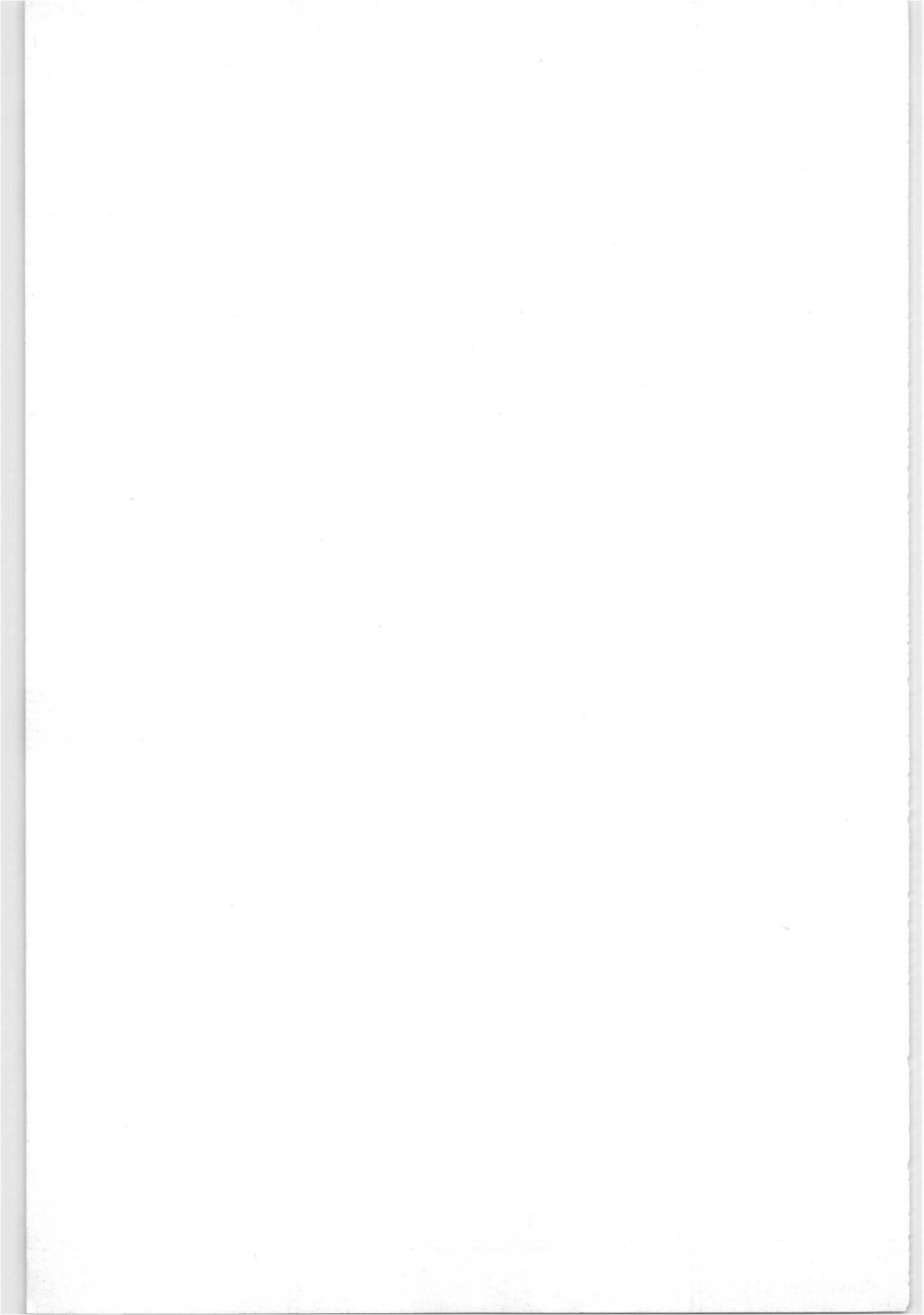
$$L1 = 18 \mu\text{H}; G_{L1} = 56 \mu\Omega^{-1}; Q_{L1} = 42; C = 47 \text{ pF}$$

$$L2 = 2.2 \mu\text{H}; G_{L2} = 490 \mu\Omega^{-1}; Q_{L2} = 23; C = 390 \text{ pF}$$

The transfer voltage is $\frac{V_1}{V_2} = 0.54$

The detector coil $L3 = 8.3 \mu\text{H}$; $C = 100 \text{ pF}$, has a loaded Q of 25.

A typical output voltage at this Q and full gain is 550 mV for $\Delta f = 15 \text{ kHz}$ with output signal distortion of 1 %.



LEVEL DETECTOR

The TAA580 is a plastic encapsulated silicon monolithic level detector. The circuit consists of a Schmitt-trigger, a three stage current amplifier and two further transistors to give flexibility in coupling to other circuits. The trigger voltage is adjustable within a limited range. The output stage can deliver 70 mA. The TAA580 is designed primarily for timing functions as in camera shutter control. Two TAA580 can be combined for a delayed action shutter.

QUICK REFERENCE DATA

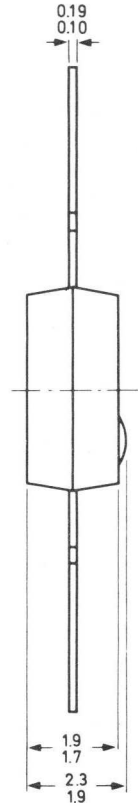
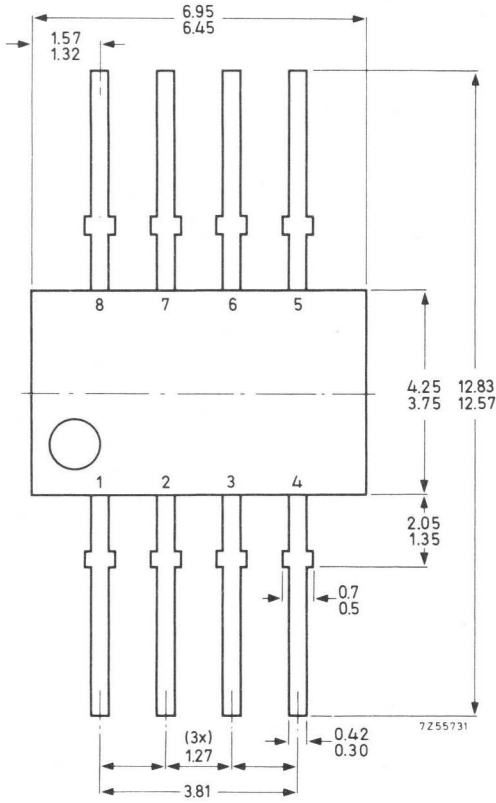
| | | | |
|---------------------------------------------------------|-----------|--------|-------------|
| Total supply voltage | V_{8-5} | nom. | 2 V |
| Threshold voltage (adjustable) | V_{2-5} | 1.4 to | 1.9 V |
| <hr style="border-top: 1px dashed black;"/> | | | |
| <u>On-state of TR9:</u> | | | |
| Output current | I_4 | max. | 70 mA |
| Output voltage at $I_4 = 28$ mA | V_{4-5} | < | 200 mV |
| <u>OFF-state of TR9:</u> | | | |
| Output current at $V_{8-5} = 4.5$ V; $V_{2-5} = 3.15$ V | I_4 | \leq | 200 μ A |

PACKAGE OUTLINE see page 2

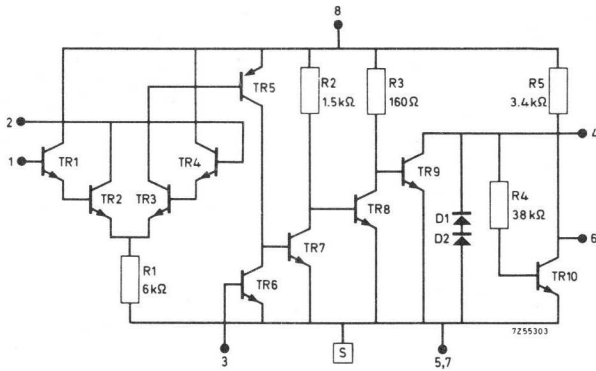
PACKAGE OUTLINE

Dimensions in mm

Pin 5 and 7 are internally connected



CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|-------------------------------|-----------|------|----------------|
| Total supply voltage | V_{8-5} | max. | 4.5 V |
| Output voltage | V_{4-5} | max. | 12.5 V |
| Output current | I_4 | max. | 70 mA |
| Total power dissipation | P_{tot} | max. | 180 mW |
| Storage temperature | T_{stg} | | -55 to +100 °C |
| Operating ambient temperature | T_{amb} | | -20 to +60 °C |

CHARACTERISTICS at $T_{amb} = -20$ to $+60$ °C; $R_1 \leq 70$ M Ω ; $R_L = 64$ Ω

Threshold voltage range at pin 6

$V_{8-5} = 2$ V; $V_{3-5} = 0$
 $V_{8-5} = 4.5$ V; $V_{3-5} = 0$

$V_{2-5} = 1.4$ to 1.9 V
 $V_{2-5} = 3.6$ to 4.2 V

Output voltage at pin 6

$V_{8-5} = 4.5$ V; $V_{2-5} = 3.15$ V ¹⁾

$V_{6-5} \leq 300$ mV ²⁾

Output voltage at pin 4

$V_{8-5} = 2$ V; $V_{2-5} = 1.9$ V ¹⁾

$V_{4-5} \leq 200$ mV ³⁾

Output current

$V_{8-5} = 2$ V
 $V_{8-5} = 4.5$ V; $V_{2-5} = 3.15$ V ¹⁾

$I_4 \leq 30.5$ mA ²⁾
 $I_4 \leq 200$ μ A ³⁾

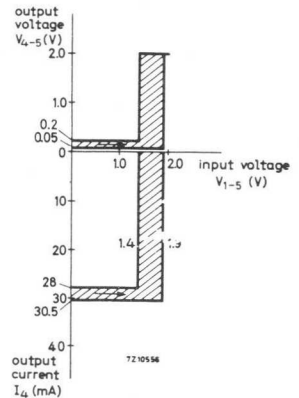
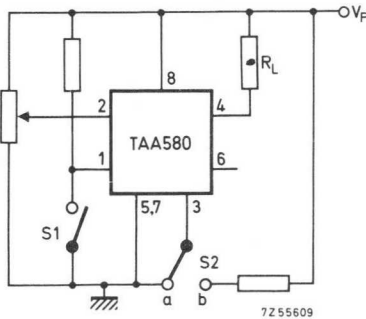
Current drain

$V_{8-5} = 4.5$ V

I_8 typ. 35 mA

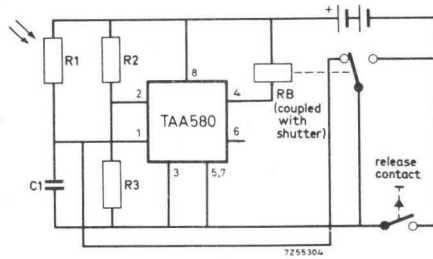
Test circuit:

Transfer characteristic:

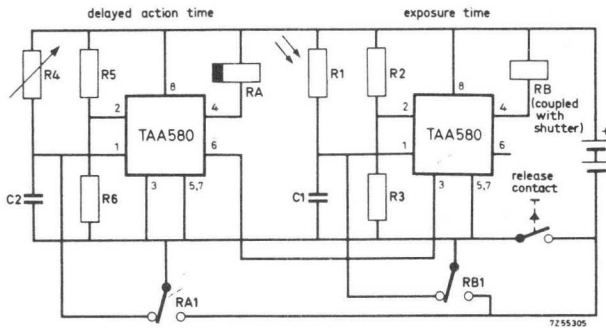


- 1) Unloaded voltage at potentiometer tap.
- 2) Switch S1 closed; switch S2 in position b.
- 3) Switch S1 closed; switch S2 in position a.

CHARACTERISTICS (continued)



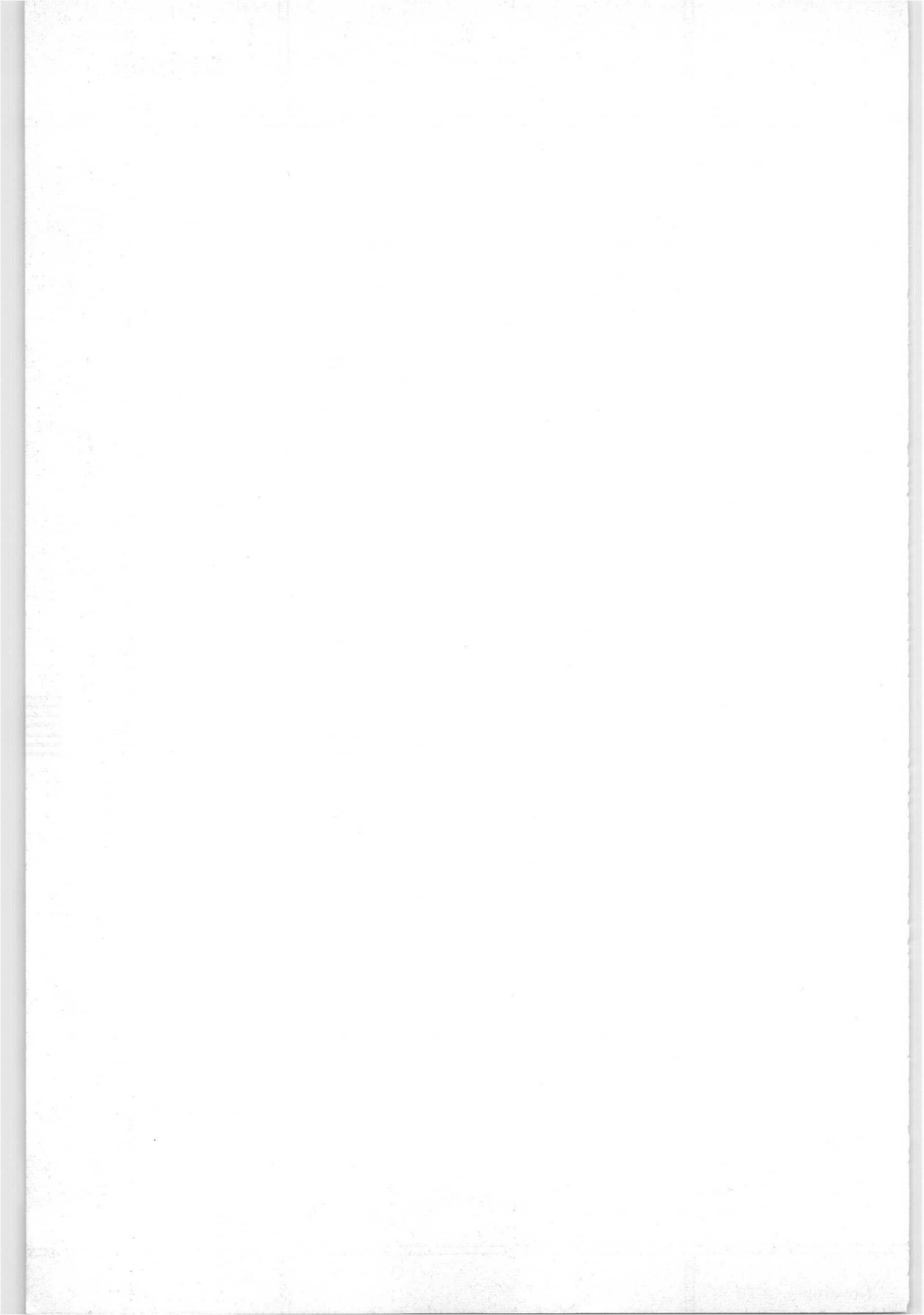
Camera shutter time control



Delayed action shutter

Notes:

- a. For shutter time range of 1 ms to 20 s; $C_1 \approx 270 \text{ nF}$; $R_1 \leq 70 \text{ M}\Omega$.
 - b. Solenoid inductance $L_S \leq 180 \text{ mH}$
- R_S values: 64 Ω to 114 Ω } DATA for RB and RA



SYNCHRONOUS DEMODULATOR FOR COLOUR DIFFERENCE DRIVE

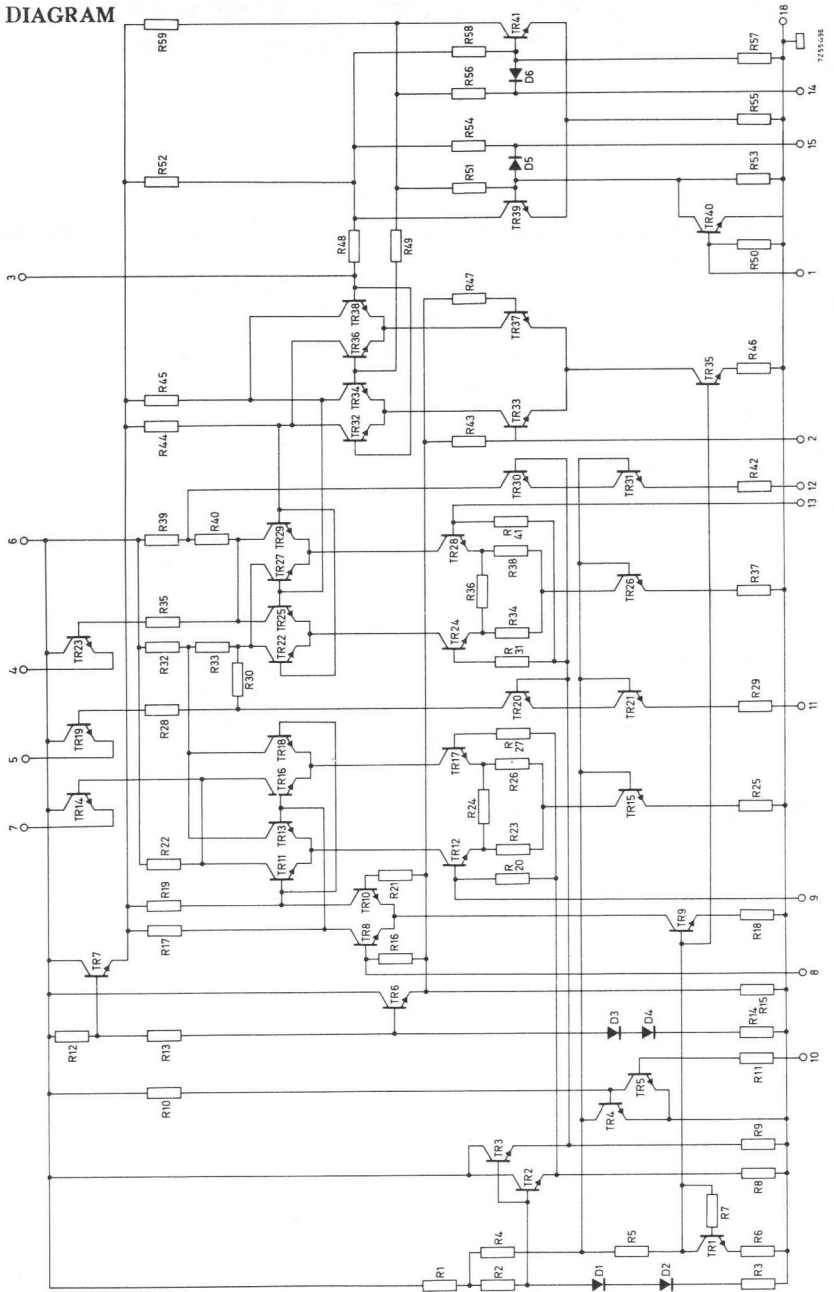
The TAA630 is a synchronous demodulator for direct drive of colour difference output stages with clamping circuits in television sets. The circuit consists of 2 amplifying synchronous demodulators for the B-Y and R-Y signals, a matrix, a PAL switch, a bistable multivibrator and colour killer switch.

QUICK REFERENCE DATA

| | | | |
|----------------------------------------------|---------------|--------|--------------|
| Supply voltage | V_{6-16} | nom. | 12 V |
| Ambient temperature | T_{amb} | | 25 °C |
| ----- | | | |
| Gain of R-Y demodulator | $G_{V(R-Y)}$ | typ. | 7 |
| Gain of B-Y demodulator | $G_{V(B-Y)}$ | typ. | 12.5 |
| Input impedance of R-Y and B-Y channel | $ Z_{9-16} $ | typ. | 1 k Ω |
| | $ Z_{13-16} $ | typ. | 1 k Ω |
| Output impedance of R-Y, B-Y and G-Y channel | $ Z_{4-16} $ | \leq | 100 Ω |
| | $ Z_{5-16} $ | \leq | 100 Ω |
| | $ Z_{7-16} $ | \leq | 100 Ω |

PACKAGE OUTLINE: 16 lead plastic dual in-line (type A) See General Section

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

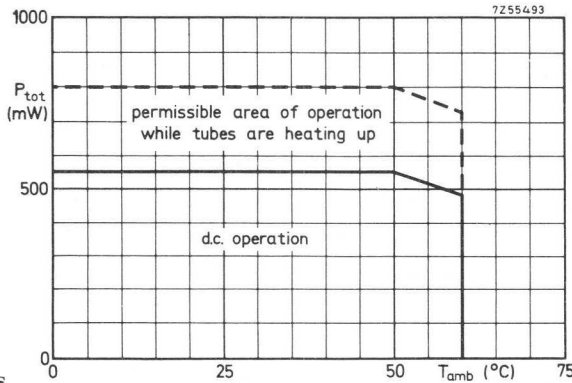
| | | |
|----------------|------------|-------------------------|
| Supply voltage | V_{6-16} | max. 13.2 V |
| | V_{6-16} | max. 16 V ¹⁾ |

Currents

| | | |
|-------------------|-------|-----------|
| Pin No. 4 current | I_4 | max. 5 mA |
| Pin No. 5 current | I_5 | max. 5 mA |
| Pin No. 7 current | I_7 | max. 5 mA |

Power dissipation

| | | |
|-------------------------|-----------|---------------------------|
| Total power dissipation | P_{tot} | max. 550 mW |
| | P_{tot} | max. 800 mW ¹⁾ |



Temperatures

| | | |
|-------------------------------|-----------|---------------|
| Storage temperature | T_{stg} | -20 to +80 °C |
| Operating ambient temperature | T_{amb} | -20 to +60 °C |

¹⁾ Permissible while tubes are heating up.

CHARACTERISTICS at $V_{6-16} = 12\text{ V}$; $V_{10-16} = 0.9\text{ V}$; $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$

Gain of colour difference signals

| | | | |
|----------------------------------------------------|---------------------------------|------|-----------------|
| $V_{i(p-p)} = 50\text{ mV}$; $f = 4.4\text{ MHz}$ | $G_{v(R-Y)}$ | typ. | 7 ¹⁾ |
| $G-Y = 0.51\text{ (R-Y)} - 0.19\text{ (B-Y)}$ | $\frac{G_{v(B-Y)}}{G_{v(R-Y)}}$ | typ. | 1.78 |

Input impedance of R-Y and B-Y channels

| | | | |
|----------------------------------------------------------------------|-------------|--------|---------------|
| $V_{i(\text{rms})} = 20\text{ mV}$ (sine wave); $f = 4.4\text{ MHz}$ | | | |
| at input F_{R-Y} ; input resistance | R_{13-16} | typ. | 1000 Ω |
| input capacitance | C_{13-16} | \leq | 10 pF |
| at input F_{B-Y} ; input resistance | R_{9-16} | typ. | 1000 Ω |
| input capacitance | C_{9-16} | \leq | 10 pF |

Input impedance of reference inputs

| | | | |
|-----------------------------------------------------------------------|--------------|------|--------------|
| $V_{i(\text{rms})} = 400\text{ mV}$ (sine wave); $f = 4.4\text{ MHz}$ | | | |
| at reference R-Y input | $ Z_{2-16} $ | typ. | 900 Ω |
| at reference B-Y input | $ Z_{8-16} $ | typ. | 900 Ω |

Colour difference output voltages

| | | | |
|----------------------------------|-----------------|--------|----------------------|
| (peak to peak values) output R-Y | $V_{4-16(p-p)}$ | \leq | $3.2\text{ V}^2)^3)$ |
| output B-Y | $V_{7-16(p-p)}$ | \leq | $4.0\text{ V}^2)^3)$ |
| output G-Y | $V_{5-10(p-p)}$ | \leq | $1.8\text{ V}^2)^3)$ |

Output impedances of R-Y, B-Y and G-Y channels

| | | | |
|---------------|--------------|--------|--------------|
| at output R-Y | $ Z_{4-16} $ | \leq | 100 Ω |
| at output B-Y | $ Z_{7-16} $ | \leq | 100 Ω |
| at output G-Y | $ Z_{5-16} $ | \leq | 100 Ω |

¹⁾ Ratio of peak to peak values of input and output voltage measured in test circuit on page 6.

$$G_{v(R-Y)} = \frac{V_{4-16}}{V_{13-16}}; G_{v(B-Y)} = \frac{V_{7-16}}{V_{9-16}}$$

²⁾ Linearity of gain ≥ 0.7

³⁾ Measured in the test circuit on page 6.

CHARACTERISTICS (continued)Colour difference d.c. output voltages

| | | |
|---------------|-------------------|-------------------------------------------------------------------|
| at output B-Y | V ₇₋₁₆ | typ. 7.4 V ¹⁾ |
| at output R-Y | | adjustable to the same level as V ₇₋₁₆ ¹⁾²⁾ |
| at output G-Y | | adjustable to the same level as V ₇₋₁₆ ¹⁾²⁾ |

Output voltage: 7.8 kHz (square wave; peak to peak value)

| | | |
|-------------------------------------------------------------------------------------------|------------------------|----------|
| $R_{load} \geq 10 \text{ k}\Omega$; V ₁₄₋₁₆ = V ₁₅₋₁₆ = 2.5 to 5 V | V _{3-10(p-p)} | typ. 3 V |
|-------------------------------------------------------------------------------------------|------------------------|----------|

Input voltagesReference voltages (peak to peak value)

| | | |
|------------------|------------------------|------------------------|
| at reference R-Y | V _{2-16(p-p)} | typ. 1 V ³⁾ |
| at reference B-Y | V _{8-16(p-p)} | typ. 1 V ³⁾ |

Horizontal deflection pulses (peak value)

| | | |
|---------------|----------------------|------------|
| at pin No. 14 | -V _{14-16M} | 2.5 to 5 V |
| at pin No. 15 | -V _{15-16M} | 2.5 to 5 V |

Identification signal (peak to peak value)

| | |
|------------------------|----------|
| V _{1-16(p-p)} | typ. 4 V |
|------------------------|----------|

Colour killer voltage

| | | |
|--------------|--------------------|----------------------|
| colour "on" | V ₁₀₋₁₆ | $\geq 0.9 \text{ V}$ |
| colour "off" | V ₁₀₋₁₆ | $\leq 0.3 \text{ V}$ |

¹⁾ Measured in the test circuit on page 6.

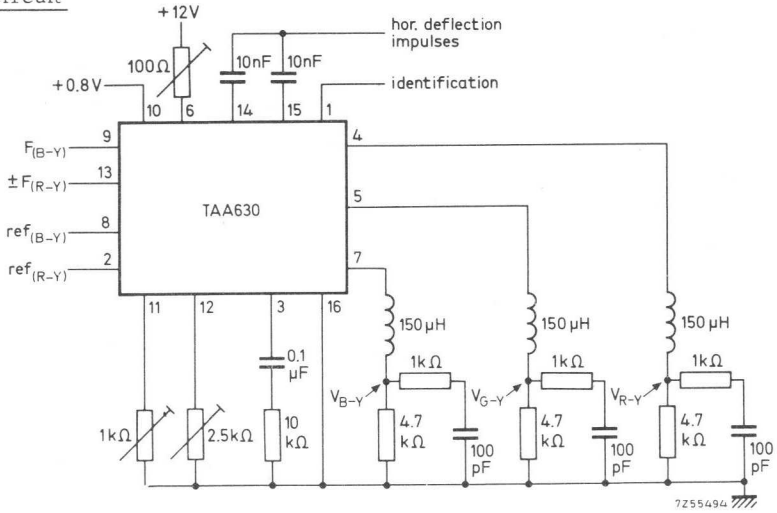
²⁾ To be adjusted with a variable voltage ($V \leq 1.2 \text{ V}$) or with resistors connected between pin 11 and pin 16 for G-Y and between pin 12 and pin 16 for R-Y.

³⁾ Permissible range 0.5 to 5 V.

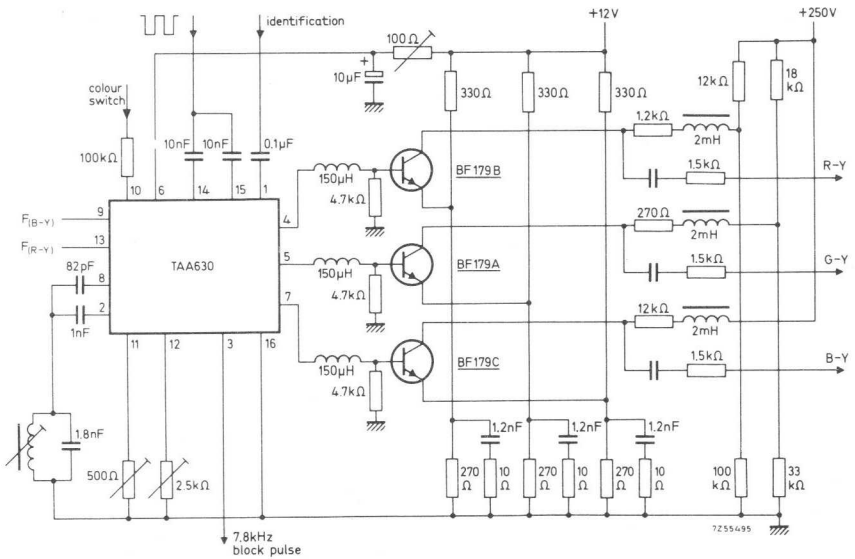
TAA630

CHARACTERISTICS (continued)

Test circuit



APPLICATION INFORMATION



LIMITER AMPLIFIER

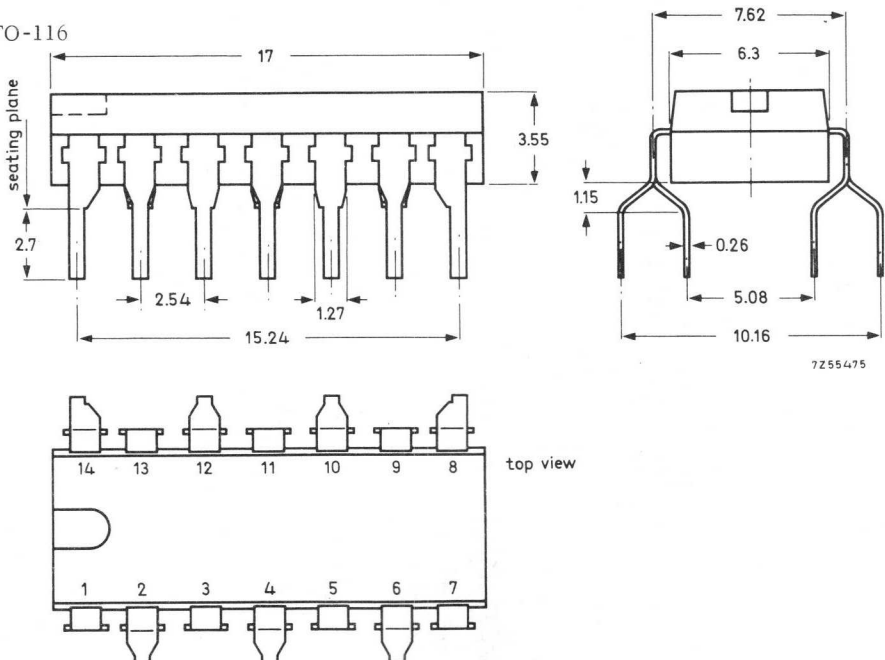
The TAA640 is a monolithic integrated four-stage limiter amplifier with f.m. detector and a.f. pre-amplifier. The envelope is TO-116. A differential amplifier with long-tailed pairs ensures excellent limiting action. The f.m. detector is a modified slope detector. Volume of the a.f. output can be remotely controlled over a range of 60 dB.

QUICK REFERENCE DATA

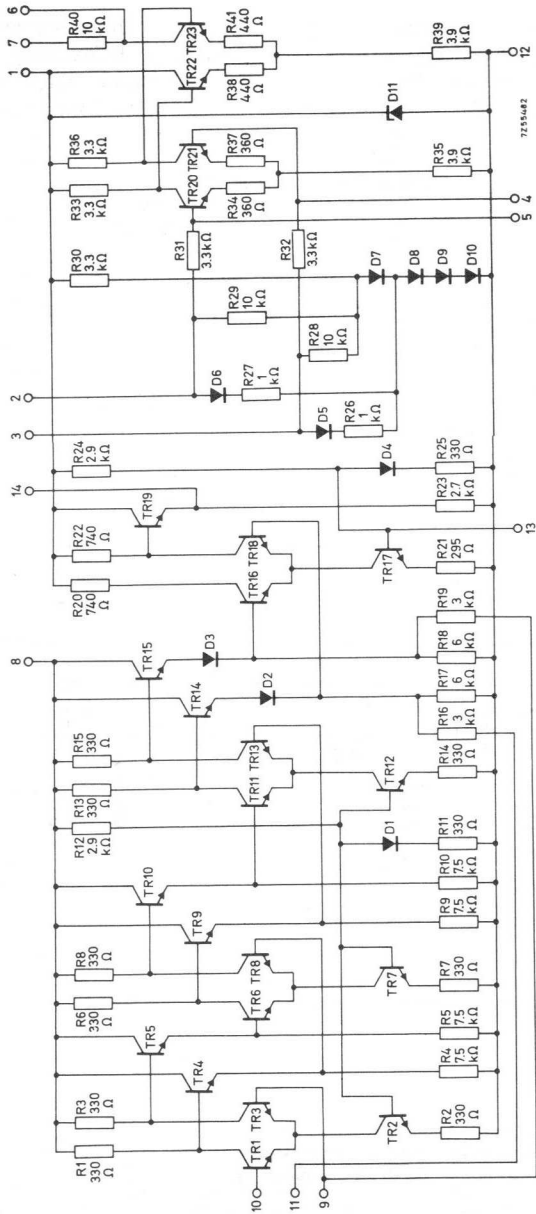
| | | | |
|------------------------------------------------------------|--------------|--------|-------------|
| Supply voltage | V_{7-12} | typ. | 22 V |
| Total current drain | I_{tot} | typ. | 26.7 mA |
| Input limiting voltage | $V_{i\ lim}$ | typ. | 100 μV |
| A.M. rejection at $V_i = 5\ mV$; $\Delta f = \pm 15\ kHz$ | | typ. | 44 dB |
| A.F. output voltage at $\Delta f = \pm 50\ kHz$ | $V_{o(rms)}$ | typ. | 1.6 V |
| Total distortion at $\Delta f = \pm 50\ kHz$ | d_{tot} | \leq | 5 % |
| Total distortion at $\Delta f = \pm 15\ kHz$ | d_{tot} | typ. | 1.6 % |

PACKAGE OUTLINE

TO-116



CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|-------------------------------|------------|------|---------------|-----------------|
| Supply voltages | V_{7-12} | max. | 32 V | ¹⁾ |
| | V_{8-12} | max. | 9 V | ¹⁾ |
| Currents | I_{tot} | max. | 40 mA | ¹⁾²⁾ |
| | I_1 | max. | 28 mA | ¹⁾ |
| Total power dissipation | P_{tot} | max. | 350 mW | |
| Operating ambient temperature | T_{amb} | | -20 to +60 °C | |
| Storage temperature | T_{stg} | | -20 to +80 °C | |

CHARACTERISTICS at $I_{tot} = 26.7$ mA; $T_{amb} = 25$ °C; $f = 5.5$ MHz; $f_{mod} = 1$ kHz measured in the test circuit on page 3.

| | | | |
|--------------------------------------------------------------------------------------------|--------------|--------|-------------|
| <u>Voltages</u> | V_{1-12} | typ. | 7.4 V |
| | | \leq | 8.5 V |
| | V_{7-12} | typ. | 22 V |
| <u>Current</u> | I_7 | typ. | 0.7 mA |
| <u>I. F. voltage gain</u> | G_v | \geq | 70 dB |
| | | typ. | 76 dB |
| <u>Input limiting voltage (-3 dB)</u> | | typ. | 100 μ V |
| <u>I. F. output voltage at $V_i = 5$ mV</u> | $V_{o(p-p)}$ | typ. | 1.7 V |
| <u>A. F. output voltage at $V_i = 5$ mV; $\Delta f = \pm 50$ kHz</u> | V_o | typ. | 1.6 V |
| <u>Total distortion</u> | | | |
| $V_i = 5$ mV; $\Delta f = \pm 50$ kHz | d_{tot} | \leq | 5 % |
| $V_i = 5$ mV; $\Delta f = \pm 15$ kHz | d_{tot} | typ. | 1.6 % |
| <u>Remote volume control range (a. f.)</u> | ΔV_o | \geq | 60 dB |
| <u>AM rejection at $V_i = 5$ mV</u> | | | |
| $\Delta f = \pm 15$ kHz, $m = 0.3$ | | typ. | 44 dB |

¹⁾ Permissible while tubes are heating up.

²⁾ $I_{tot} = I_1 + I_7 + I_8$

TAA640

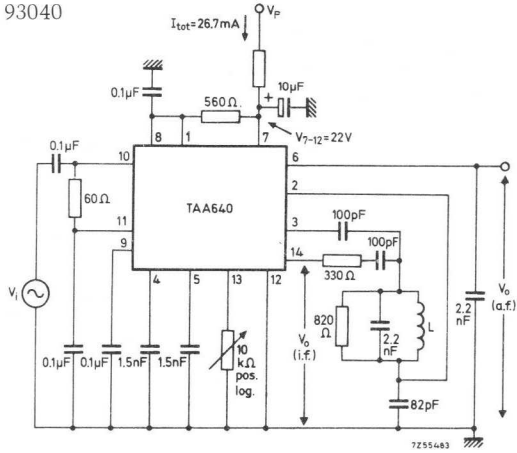
APPLICATION INFORMATION

Detector coil L: 6.5 turns 0.5 mm Cu wire.

Coil former: AP3016/02 (used without Ferroxcube frame)

Can: AP3015/02

Screw core: 3122 104 93040



TELEVISION SIGNAL PROCESSING CIRCUIT

The TAA700 is a silicon monolithic integrated signal processing circuit for television receivers. It combines following functions:

- video pre-amplifier with emitter follower output.
- gated a.g.c. detector supplying the a.g.c. voltages for the vision i.f. amplifier and tuner (delayed)
- noise inverter for gating the a.g.c. and sync separator circuits
- sync separator
- automatic horizontal synchronisation
- vertical sync.pulse separator
- blanking facility for the video amplifier

The circuit is designed for receivers equipped with tubes or transistors in the deflection and video output stages, and with n-p-n transistors in the tuner and i.f. amplifier.

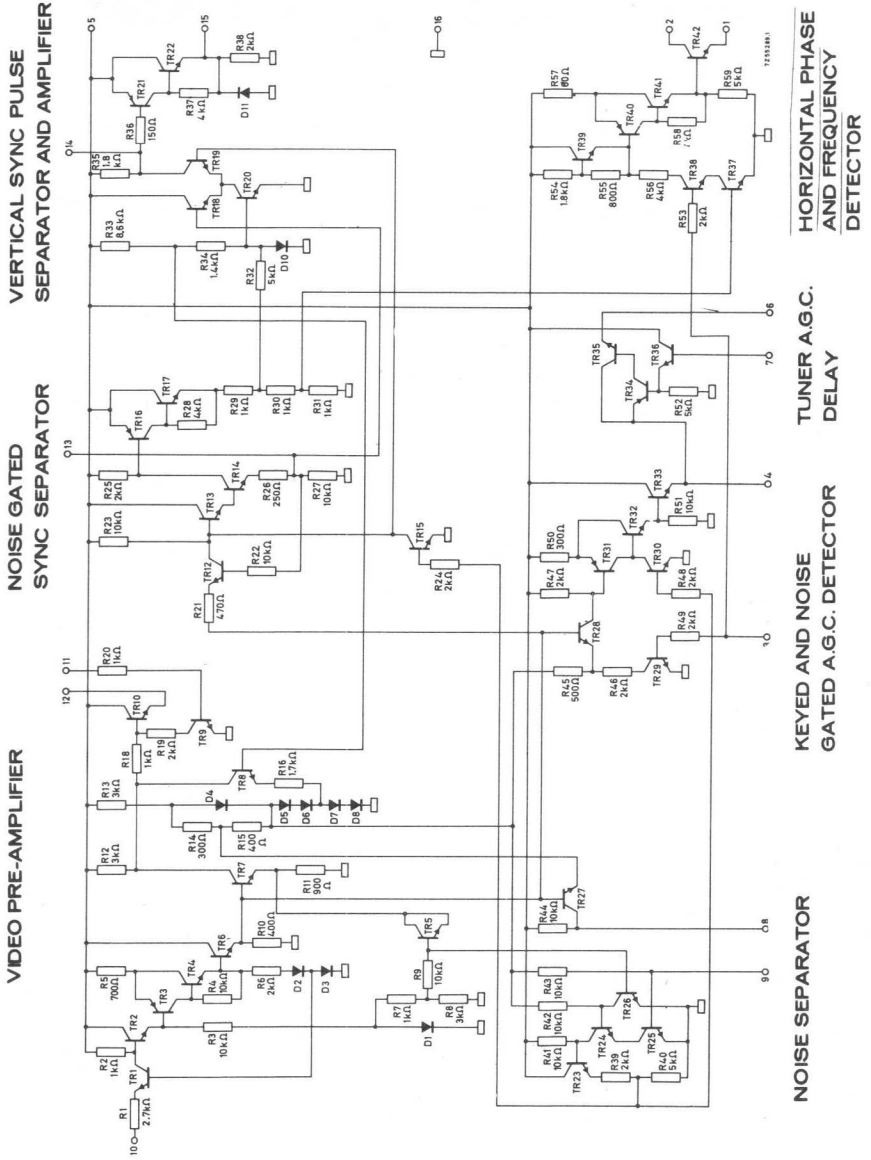
Only signals with negative modulation can be handled by the circuit.

QUICK REFERENCE DATA

| | | | |
|-------------------------------------------------------------------------|-------------------|------|----------|
| Supply voltage | V_P | typ. | 12 V |
| Ambient temperature | T_{amb} | | 25 °C |
| <hr/> | | | |
| Video input voltage (peak to peak value) | V_{10-16} (p-p) | typ. | 2 V |
| Voltage gain of the video amplifier | G_V | typ. | 9.5 dB |
| A.G.C. voltage for i.f. part ($R_1 = 2 \text{ k}\Omega$) | V_{4-16} | typ. | 0 to 8 V |
| A.G.C. voltage for tuner ($R_1 = 1 \text{ k}\Omega$) | V_{6-16} | typ. | 0 to 7 V |
| Output voltage horizontal phase detector | $\pm V_{2-1}$ | typ. | 3 V |
| Vertical sync.output voltage (positive going pulse; peak to peak value) | V_{15-16} (p-p) | > | 10 V |

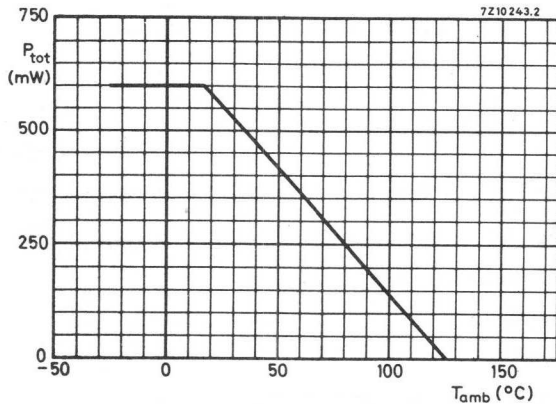
MECHANICAL DATA (See page 7)

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

| | | | |
|--------------------------|-----------|------|--------------------|
| <u>Supply voltage</u> | V_p | max. | 16 V ¹⁾ |
| <u>Power dissipation</u> | P_{tot} | max. | 600 mW |



Temperatures

| | | |
|-------------------------------|-----------|----------------|
| Storage temperature | T_{stg} | -25 to +125 °C |
| Operating ambient temperature | T_{amb} | -25 to +125 °C |

1) Permissible while tubes are heating up.

CHARACTERISTICS

| | | |
|---------------------------------------------------------------------------------------------|---------------------------------------|------------------------------|
| Supply voltage range | V_P | 10 to 14 V |
| Measured in circuit on page 6 at $T_{amb} = 25\text{ }^\circ\text{C}$; $V_P = 12\text{ V}$ | | |
| <u>Video amplifier</u> | | |
| Input resistance (detector load) | R_{10-16} | typ. 2.7 k Ω |
| Input capacitance | C_{10-16} | < 1 pF |
| Bandwith (3dB) | B | > 5 MHz |
| Voltage gain | G_V | typ. 9.5 dB |
| Video input voltage (peak to peak value) | $V_{10-16(p-p)}$ | typ. 2 V 1) |
| Video output voltage (peak to peak value) | $V_{12-16(p-p)}$ | typ. 6 V 2) |
| <u>Tolerances on video output voltage:</u> | | |
| I.C. processing spreads | $\pm\Delta V_{12-16}$ | < 550 mV |
| Temperature drift | $-\Delta V_{12-16}$ | < 20 mV/ $^\circ\text{C}$ 3) |
| Spreads over a.g.c. expansion (entire range) | $\pm\Delta V_{12-16}$ | < 270 mV 4) |
| Black level at the output | v_{12-16} | typ. 5 V 5) |
| <u>Tolerances on the black level at the output:</u> | | |
| I.C. processing spreads | $\pm\Delta v_{12-16}$ | < 300 mV |
| Temperature drift | Δv_{12-16} | < 7 mV/ $^\circ\text{C}$ 3) |
| Spreads over a.g.c. expansion (entire range) | $\pm\Delta v_{12-16}$ | < 250 mV 4)6) |
| Variation black level at the output due to supply voltage variations | $\frac{\Delta v_{12-16}}{\Delta V_P}$ | typ. 0.7 |
| Available video output current (peak value) | I_{12M} | typ. 14 mA 7) |

- 1) Negative going video signal (no pre-bias needed for the detector)
- 2) Video signal with negative going sync pulse.
- 3) Because the integrated circuit reaches 95% of its final working temperature in 100 seconds, the temperature variations to be considered are those caused by the slower rise in cabinet temperature and by changes in room temperature.
- 4) Variation about a nominal condition, the i.f. being fully controlled and the tuner uncontrolled. The video signal increases and the black level decreases with increasing antenna signal.
- 5) Only valid if the video signal is in accordance with the CCIR standard.
- 6) To this must be added $0.7\Delta V_P$, if operation of the a.g.c. causes a change in V_P .
- 7) The total load on pin 12 must be such that under nominal conditions $I_{12M} \leq 14\text{ mA}$.

CHARACTERISTICS (continued)

Video blanking

| | | |
|------------------------------------|------------------|-------------------|
| Input voltage (peak to peak value) | $V_{11-16(p-p)}$ | 1 to 5 V |
| Input resistance | R_{11-16} | typ. 1 k Ω |

A.G.C. circuit

| | | |
|------------------------------------------------------------------|-----------------|-------------------|
| Control voltage i.f. amplifier | V_{4-16} | 0 to 8 V 1) |
| Control voltage tuner | V_{6-16} | 0 to 7 V 1) |
| Signal expansion for full control of i.f. amplifier and tuner | | < 15 % 1) |
| Keying input pulse (peak to peak value) | $V_{3-16(p-p)}$ | 1 to 5 V 2) |
| Input resistance | R_{3-16} | typ. 1 k Ω |

Synchronisation circuit

| | | |
|----------------------------------------------------------------------|------------------|-------------------|
| Sync. separator | | see note 3 |
| Control voltage line oscillator | $\pm V_{2-1}$ | typ. 3 V 4) |
| Output voltage vertical sync.pulse separator (peak to peak value) | $V_{15-16(p-p)}$ | > 10 V |
| Output impedance | R_{15-16} | typ. 2 k Ω |

1) These figures are obtained with a load impedance of 2 k Ω for the i.f. control point (R4-16) and 1 k Ω for the tuner control point (R6-16). With these impedances the signal expansion for i.f. control and tuner control will be about the same. An increase of these impedances will reduce the signal expansion. Lower values will reduce the available control voltage and increase the dissipation of the integrated circuit. Therefore, the minimum values must be restricted to 1.5 k Ω for the i.f. control point and 750 Ω for the tuner control point.

2) The TAA700 may be operated unkeyed but then point 3 must be connected to the positive supply line via a resistor of suitable value (e.g. 10 k Ω). However, the following consequences should be borne in mind:

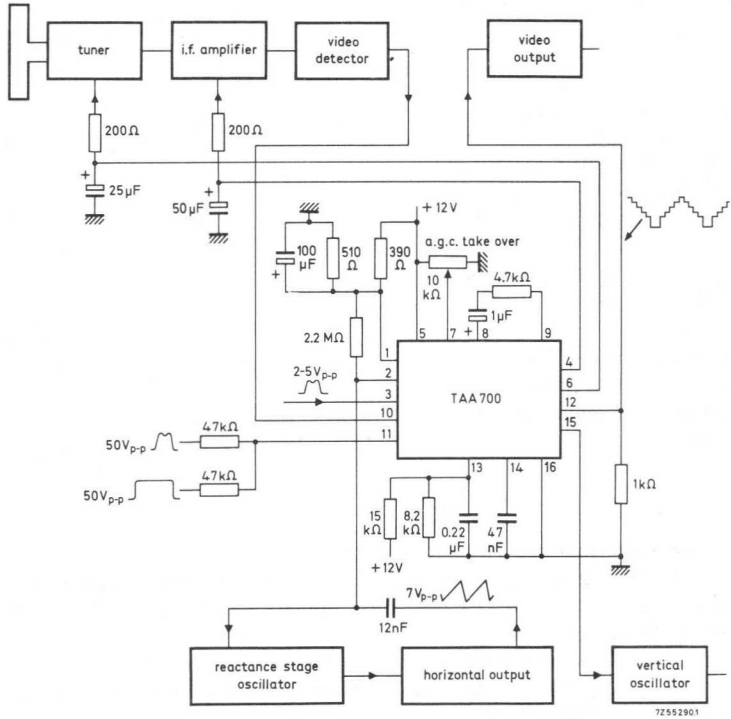
- The decoupling capacitors at the i.f. and tuner control points must be larger to prevent ripple voltages due to the vertical sync pulses. In consequence the a.g.c. will not follow fast signal fluctuations (airplane flutter).
- Since the horizontal phase detector is designed to be keyed, unkeyed operation will result in the phase detector not operating as a frequency detector when the horizontal oscillator is out of sync. This considerably decreases the catching range.

3) The sync pulse is sliced about 30% below top sync level.

4) Required reference voltage $V_{2(p-p)}$ (sawtooth or differentiated line fly-black pulse) = 7 V. For an oscillator-reactance stage with a control sensitivity of 400 Hz/V this gives a holding range of about ± 1000 Hz.

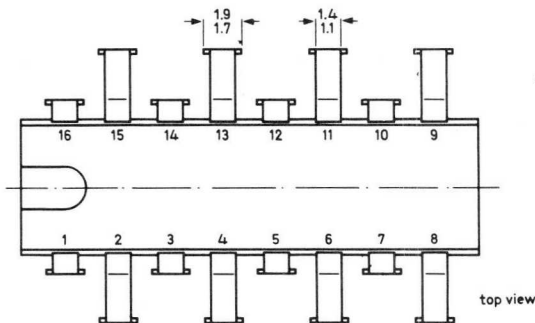
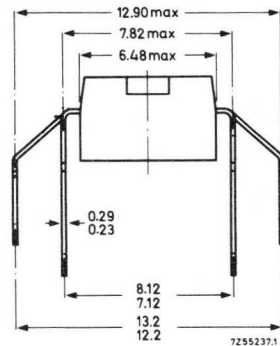
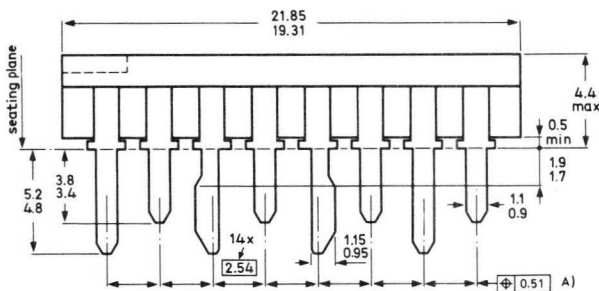
Because the phase detector is keyed a catching range of ± 700 Hz is obtained without affecting the noise immunity.

APPLICATION INFORMATION



MECHANICAL DATA

Dimensions in mm



- A) Centre-lines of all leads are within ± 0.254 mm of the nominal positions shown; in the worst case, the spacing between any two leads may deviate from nominal by ± 0.51 mm.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

260 °C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

INTEGRATED A.M. RADIO RECEIVER CIRCUIT

The TAA840 is a monolithic integrated circuit for use in a.m. radio; it incorporates an r.f. amplifier, mixer-oscillator, i.f. amplifier, a.g.c., detector, audio pre-amplifier and driver.

An audio output stage suiting the requirements of the receiver must be added separately.

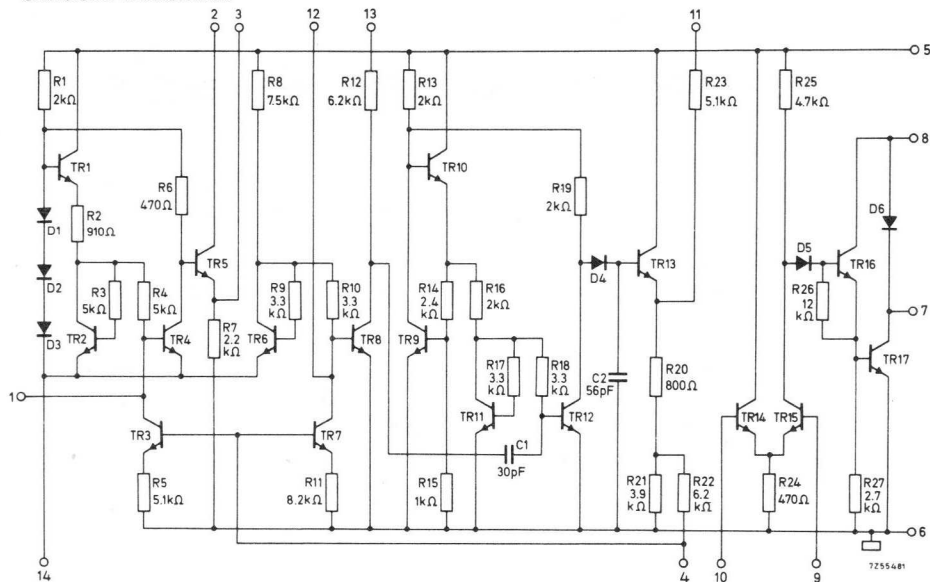
The detection capacitor and resistor of the series detector are integrated. The i.f. amplifier incorporates provision for the use of a tuning indicator. Since the circuit is adapted to operate in conjunction with i.f. filters having low input and output impedance, pre-aligned i.f. block-filters can be used.

QUICK REFERENCE DATA

| | | |
|----------------------------------------------------------------------------------------|-----------|-----------------|
| Ambient temperature | T_{amb} | 25 °C |
| Supply voltage | V_P | typ. 6 V |
| ----- | | |
| A.F. output power at $d_{tot} = 10\%$ (with AC187/AC188) | P_o | typ. 900 mW |
| Total quiescent current (except output stages) | I_{tot} | typ. 17 mA |
| R.F. input voltage (at pin 1) for a signal to noise ratio of 26 dB | V_i | typ. 20 μ V |
| A.G.C. range (change in r.f. input voltage for 10 dB expansion in audio range) | | typ. 64 dB |
| R.F. signal handling (at pin 1) | | typ. 20 mW |
| R.F. input voltage (at pin 1) for full output (start of clipping at $P_o = 650$ mW) | | typ. 3 μ V |
| Harmonic distortion of h.f. part (over most of a.g.c. range) | d_{tot} | typ. 1.2 % |
| $m = -30\%$ | | |
| $m = 80\%$ | d_{tot} | typ. 2.6 % |

PACKAGE OUTLINE : 14 lead dual in-line (See General Section)

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum system (IEC 134)

Voltages (tolerated minimum: 0 V)

| | | | |
|--------------------|------------|------|------|
| Pin No. 2 voltage | V_{2-6} | max. | 12 V |
| Pin No. 3 voltage | V_{3-6} | max. | 6 V |
| Pin No. 4 voltage | V_{4-6} | max. | 1 V |
| Pin No. 5 voltage | V_{5-6} | max. | 12 V |
| Pin No. 7 voltage | V_{7-6} | max. | 12 V |
| Pin No. 8 voltage | V_{8-6} | max. | 12 V |
| Pin No. 11 voltage | V_{11-6} | max. | 12 V |
| Pin No. 13 voltage | V_{13-6} | max. | 12 V |

Currents (tolerated minimum: 0 mA)

| | | | |
|--------------------|----------|------|------------|
| Pin No. 1 current | I_1 | max. | 80 μ A |
| Pin No. 9 current | I_9 | max. | 80 μ A |
| Pin No. 10 current | I_{10} | max. | 80 μ A |
| Pin No. 12 current | I_{12} | max. | 80 μ A |

Dissipation

| | | |
|-----------|------|--------|
| P_{tot} | max. | 260 mW |
|-----------|------|--------|

Temperatures

| | | |
|-------------------------------|-----------|--------------------------|
| Storage temperature | T_{stg} | -55 to +125 $^{\circ}$ C |
| Operating ambient temperature | T_{amb} | -20 to +55 $^{\circ}$ C |

CHARACTERISTICS at $T_{amb} = 25^{\circ}\text{C}$; $V_P = 6\text{ V}$ ¹⁾Measured in the circuit on page 5

| | | | |
|-----------------------------------------------------------------------------------|-------------------------------------|-----------|------------------------------|
| Breakdown voltage of driver stage | $V_{(BR)CEO}$ | > | 12 V |
| Saturation voltage of driver stage | $V_{CE\text{ sat}}$ | < | 0.6 V |
| Pin No.5 voltage at $V_P = 6\text{ V}$ (via a series resistor of 68 Ω) | V_{5-6} | typ. | 5.5 V |
| Current drain | $I_2 + I_5 + I_{13}$ $I_7 + I_8$ | typ. | 8 mA 8.4 mA ²⁾ |
| Quiescent current of a.f. output stage with AC187/AC188 | I_Q | typ. | 5 mA |
| Total chip dissipation | P_{tot} | typ. < | 65 mW 125 mW |
| Supply voltage for 20 mV (r.m.s value) oscillator operation at $f = 1\text{ MHz}$ | | > | 3 V |

A.C. characteristics

| | | | |
|----------------------------------------------------------------------------------|-------|------|----------------------------------------------|
| A.F. output power at $d_{tot} = 10\%$ (with AC187/AC188) $f = 1000\text{ Hz}$ | P_O | typ. | 900 mW |
| A.F. output power (onset of clipping) $f = 1000\text{ Hz}$ | P_O | typ. | 650 mW |
| R.F. input voltage (at pin 1) for signal to noise ratio of 26 dB | V_i | typ. | 20 μV ³⁾ ⁴⁾ |
| A.G.C. range (change in r.f. input voltage for 10 dB expansion in audio range) | | typ. | 64 dB ³⁾ ⁴⁾ |

1) Circuit designed for use in receivers with 6 V or 9 V battery.

Voltage at pin 5 to be adjusted 5.5 V regardless of battery voltage; a.f. driver (pin No.8) can be fed direct from either 6 V or 9 V.

2) $I_7 + I_8$ depend on the load resistances at pins 7 and 8.

3) Measured at 1 MHz with the antenna circuit connected (source resistance of about 1 k Ω for pin 1)

4) 30% modulation, $f_m = 1000\text{ Hz}$.

CHARACTERISTICS (continued)

Signal handling:

| | |
|-----------------------------------------------------------------------------------------|---------------------------------------|
| R.F. input voltage (at pin 1) to obtain 10% distortion at 80% modulation, $f_m = 1$ kHz | typ. 20 mV ¹⁾ |
| R.F. input voltage (at pin 1) for 10 mV (a.f.) across volume control | typ. 2.7 μ V ¹⁾²⁾ |
| A.F. voltage across volume control for 100 μ V (r.f.) input voltage (at pin 1) | typ. 30 mV ¹⁾²⁾ |
| Input conductance of r.f. amplifier (at pin 1) | typ. 0.5 $m\Omega^{-1}$ ¹⁾ |
| Input conductance of i.f. amplifier at $f = 500$ kHz (at pin 12) | typ. 0.5 $m\Omega^{-1}$ |
| Signal to noise ratio for 1 mV (r.f.) input voltage (at pin 1) | typ. 46 dB ^{1) 2)} |
| A.F. voltage (at pin 9) for 50 mW output power | < 4.5 mV |
| A.F. voltage (at pin 9) for output power at onset of clipping | typ. 10 mV |
| Loss of overall receiver sensitivity at cell voltage of 0.9 V and 50 mW output power | typ. 4 dB ¹⁾²⁾ |
| Oscillator frequency shift over range of supply voltage at $f_{osc} = 2$ MHz | < 1.3 kHz/V |

→ Note

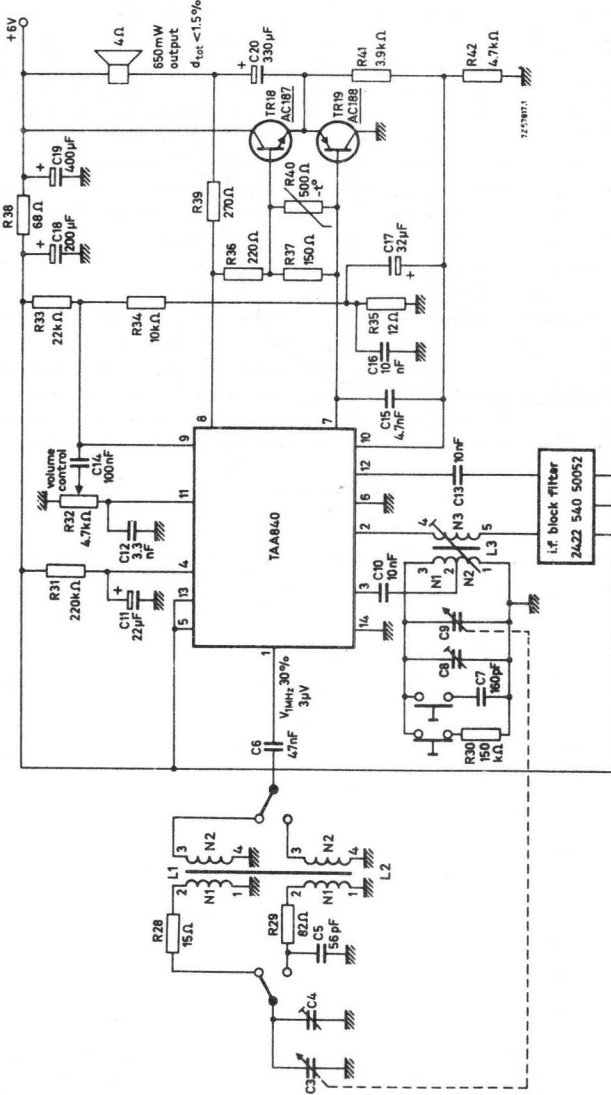
Tuning indicator inserted in pin 13

¹⁾ Measured at 1 MHz with the antenna circuit connected (source resistance of about 1 $k\Omega$ for pin 1)

²⁾ 30% modulation, $f_m = 1000$ Hz

APPLICATION INFORMATION

Circuit of a medium wave-long wave radio receiver, with TAA840 (given for m.w.)



Ferrite rod aerial coils

Medium wave: N1 : N2 = 65 : 3.5

L1 = 450 μH; Q0 = 100 at 1 MHz

Long wave: N1 : N2 = 200 : 10

L2 = 3.5 mH; Q0 = 75 at 200 kHz

Oscillator coils:

N1 : N2 = 135 : 2 (N1 + N2) : N3 = 137 : 12

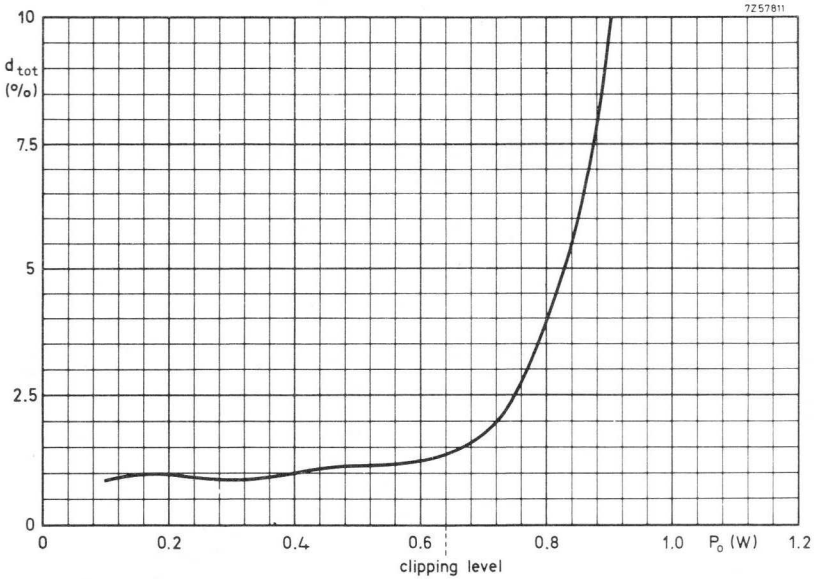
L3 = 300 μH; Q0 = 95 at 1 MHz

C3 = 0 to 195 pF C9 = 0 to 80 pF

C4 = trimmer C8 = trimmer

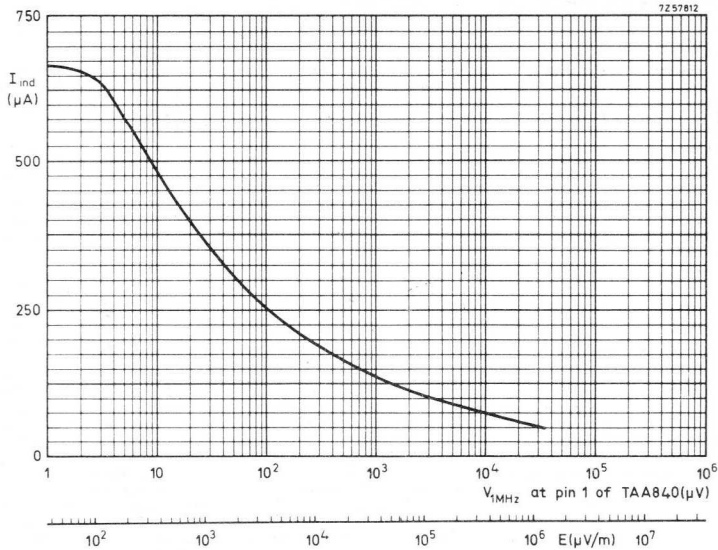
2222 807 10039

APPLICATION INFORMATION (continued)

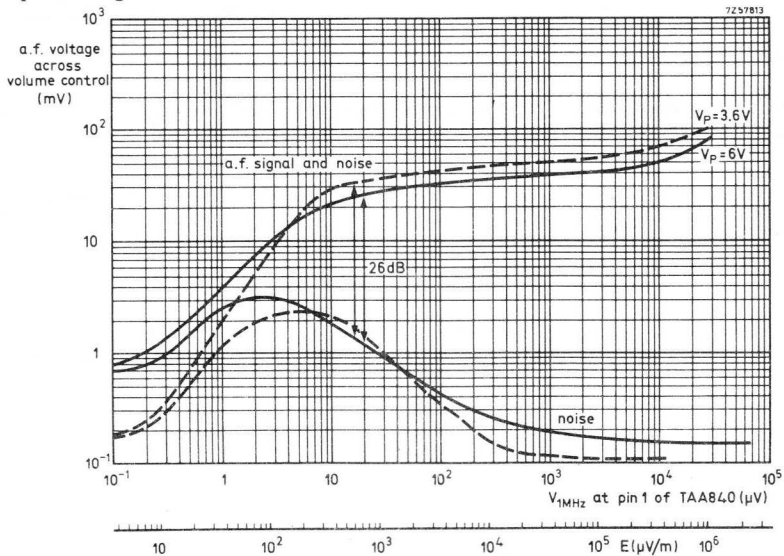


Total harmonic distortion of the audio part versus a.f. output power at 1 kHz

APPLICATION INFORMATION (continued)



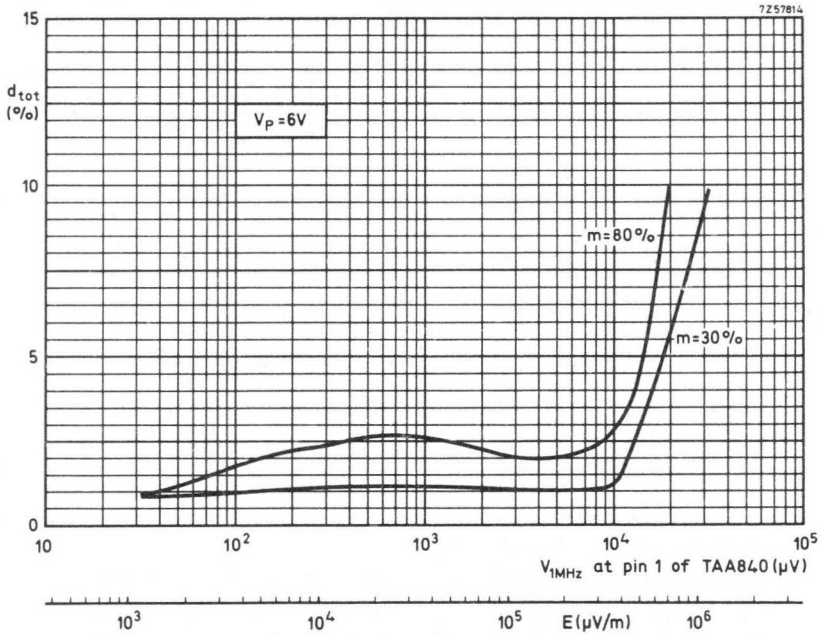
Current flowing through lead (pin 13) in which tuning indicator may be inserted versus r.f. input voltage and field strength. ¹⁾



A.F. signal and noise voltage across volume control and a.f. noise voltage across volume control versus r.f. input voltage and field strength. ¹⁾

¹⁾ Field strength scale valuable for ferrite aerial of 200 mm length and 10 mm diameter;
R.F. input signal 30% modulated with 1 kHz sine wave.

APPLICATION INFORMATION (continued)



Total harmonic distortion of the h.f. part measured across volume control versus r.f input voltage and field strength.

Input signal 30% and 80% modulated with 1 kHz sinewave.

Field strength scale valuable for ferrite aerial of 200 mm length and 10 mm diameter.

TRIPLE AMPLIFIER FOR ACTIVE FILTERS

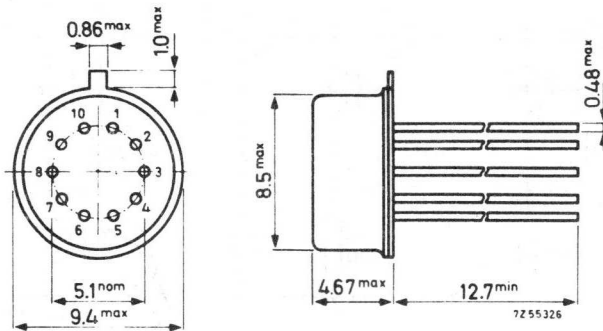
The TAA960 consists of three identical general-purpose amplifiers integrated in a single silicon chip. The amplifiers can be used **separately** or can be cascaded to give a voltage gain of 117 dB. One of the amplifiers has an additional emitter-follower stage. The TAA960 is very suitable for use in an active RC band-pass filter with Q up to 60.

QUICK REFERENCE DATA

| | | | | |
|----------------------------------------|------------|------|-----|----------------|
| Supply voltage | V_{3-10} | nom. | 6 | V |
| Supply current | I_3 | typ. | 2 | mA |
| Transfer admittance (each amplifier) | $ y_{fs} $ | typ. | 9.5 | $m\Omega^{-1}$ |
| Voltage gain (each amplifier) | G_V | typ. | 39 | dB |
| Input resistance (on pins 1, 7 and 8) | R_i | > | 25 | $k\Omega$ |
| Output resistance (on pins 2, 5 and 6) | R_o | typ. | 9 | $k\Omega$ |
| (on pin 4) | R_o | typ. | 500 | Ω |
| Q factor (in typical RC filter) | Q | typ. | 45 | |

PACKAGE OUTLINE TO-74; reduced height

Dimensions in mm



TAA960

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages with respect to pin 10

| | | | | |
|------------------------------|----------------------|------|----|---|
| Supply voltage ¹⁾ | V_3 | max. | 10 | V |
| Input voltage | V_8, V_7, V_1 | max. | 4 | V |
| Output voltage | V_6, V_5, V_4, V_2 | max. | 10 | V |

Currents

| | | | | |
|---------------|-----------------|------|----|---------------|
| Input current | I_8, I_7, I_1 | max. | 50 | μA |
|---------------|-----------------|------|----|---------------|

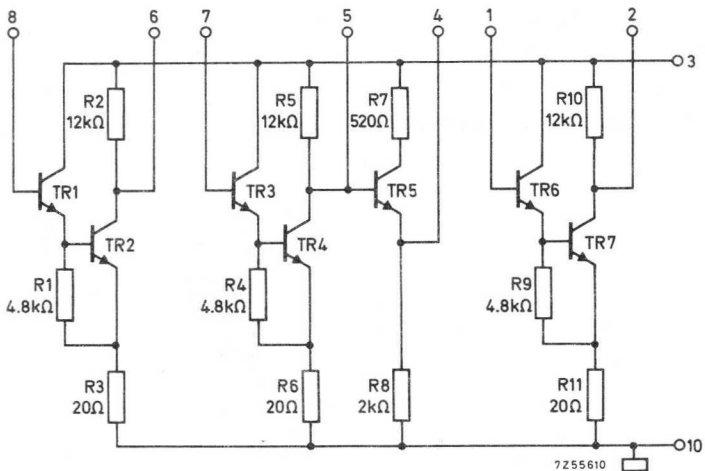
Total power dissipation

| | | | |
|------------------|------|-----|----|
| P_{tot} | max. | 250 | mW |
|------------------|------|-----|----|

Temperatures

| | | | |
|-------------------------------|------------------|-------------|--------------------|
| Storage temperature | T_{stg} | -65 to +125 | $^{\circ}\text{C}$ |
| Operating ambient temperature | T_{amb} | -55 to +65 | $^{\circ}\text{C}$ |

CIRCUIT DIAGRAM



¹⁾ With lower d. c. potential on all other terminals.

CHARACTERISTICS at $V_3 = 6\text{ V}$; $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ unless otherwise specified.

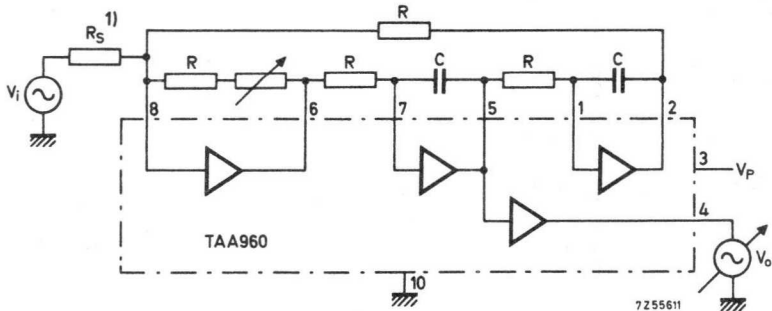
| | | | | |
|------------------------------------------------------------|-------|------|------------|------------|
| <u>Supply current</u> ¹⁾ | I_3 | | 1.5 to 2.5 | mA |
| | | typ. | 2.0 | mA |
| <u>Supply current</u> ¹⁾ at $V_3 = 10\text{ V}$ | I_3 | | 1.5 to 3.8 | mA |
| | | typ. | 2.6 | mA |
| <u>Voltage gain</u> (each amplifier) | G_V | | 60 to 150 | |
| | | typ. | 90 | |
| <u>Input resistance</u> (each amplifier) | R_i | > | 25 | k Ω |
| <u>Output resistance</u> on terminals 2, 5 and 6 | R_o | > | 8 | k Ω |
| | | typ. | 9 | k Ω |
| on terminals 4 | R_o | | 135 to 750 | Ω |



¹⁾ Terminal 8 connected to terminal 6
 " 7 " " " 5
 " 1 " " " 2

APPLICATION INFORMATION

Active RC filter for frequencies up to 150 kHz



$R = 10 \text{ k}\Omega$

| | | | | |
|--------------------------------------------------------------|-----------|------|---------------------|------------------|
| <u>Frequency</u> | f | typ. | $\frac{1}{2\pi RC}$ | |
| <u>Supply voltage</u> | V_P | typ. | 6 | V |
| <u>Filter performance</u> at $T_{amb} = 25^\circ\text{C}$ | Q | | 40 to 55 | |
| | | typ. | 45 | |
| at $T_{amb} = -30 \text{ to } +65^\circ\text{C}$ | Q | | 35 to 55 | |
| <u>Input voltage</u> | V_i | typ. | 400 | mV |
| <u>Output voltage</u> | V_o | typ. | 400 | mV |
| <u>Distortion</u> at $V_o = 350 \text{ mV}$ | d_{tot} | typ. | 2 | % |
| <u>S/N ratio</u> at $V_o = 400 \text{ mV}$ | S/N | > | 50 | dB |
| <u>Input resistor</u> ¹⁾ | R_S | typ. | 470 | $\text{k}\Omega$ |

¹⁾ Value of input resistor to be determined for $\frac{V_o}{V_i} = 0.90 \text{ to } 1.1$.

MICROPHONE AMPLIFIER

The TAA970 is a monolithic integrated microphone amplifier for use in telephone systems. It is compatible with both piezo-electric and dynamic microphones of suitable impedance and sensitivity.

Special features are:

- almost constant voltage gain and d.c. voltage drop with supply current variations of 10 to 100 mA
- output voltage before limiting: 1 V (r.m.s. value)
- operation is independent of supply voltage polarity
- gain can be set to either of two values
- only one external capacitor required
- output impedance determined by internal feed back

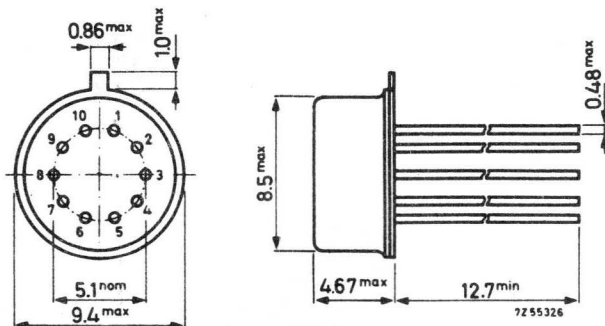
QUICK REFERENCE DATA

| | | |
|---------------------------|---------------|-------------------|
| Supply current | $\pm I_2$ | 10 to 100 mA |
| Supply voltage drop | $\pm V_{2-4}$ | typ. 4.8 V |
| Voltage gain | | |
| pin 9 not connected | G_V | typ. 130 |
| pin 9 connected to pin 10 | G_V | typ. 180 |
| Output impedance | | |
| pin 9 not connected | R_O | typ. 80 Ω |
| pin 9 connected to pin 10 | R_O | typ. 115 Ω |

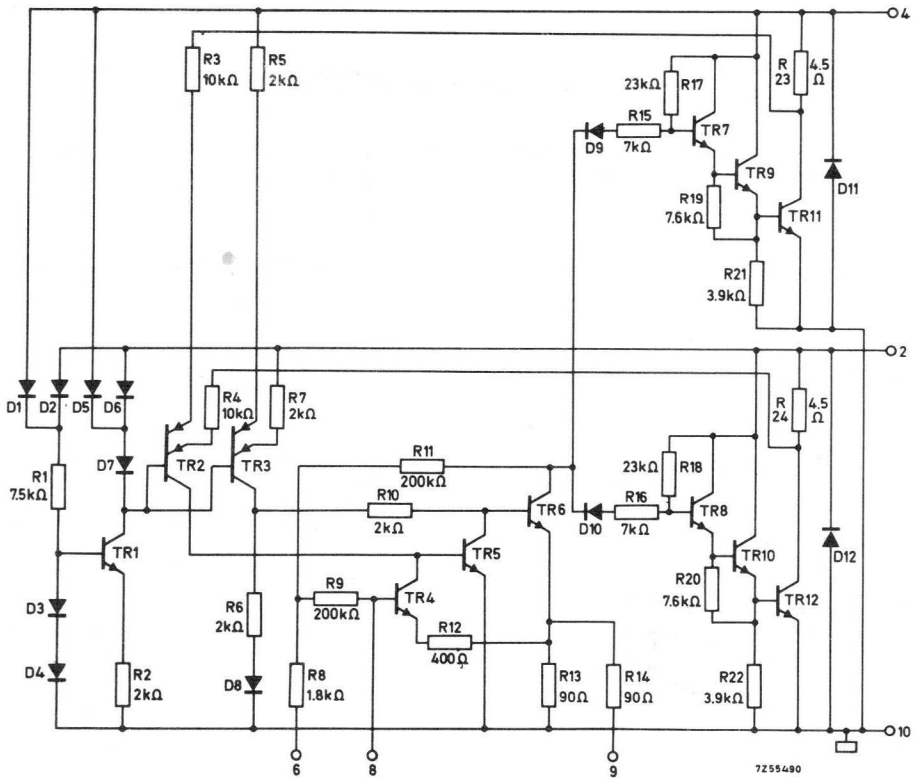
PACKAGE OUTLINE

TO-74 (reduced height)

Dimensions in mm



CIRCUIT DIAGRAM



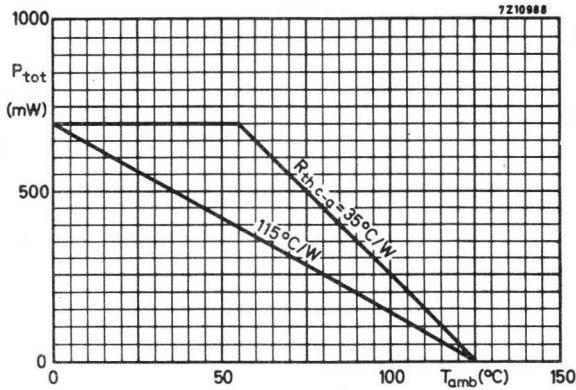
RATINGS Limiting values in accordance to the Absolute Maximum System (IEC 134).

Currents

| | | | |
|-----------------------------------------------|----------|--------------|---------|
| Supply current (d.c.) | I_2 | -100 to +100 | mA |
| A.C. component of supply current (peak value) | I_{2m} | max. 100 | mA |
| Pin No.6 current | I_6 | max. 100 | μ A |
| Pin No.8 current | I_8 | max. 100 | μ A |

Power dissipation

| | | | |
|-------------------------|-----------|----------|----|
| Total power dissipation | P_{tot} | max. 700 | mW |
|-------------------------|-----------|----------|----|



Temperatures

| | | | |
|-------------------------------|-----------|-------------|----|
| Storage temperature | T_{stg} | -55 to +125 | °C |
| Operating ambient temperature | T_{amb} | -35 to +75 | °C |

THERMAL RESISTANCE

| | | | | |
|-----------------------|---------------|---|----|------|
| From junction to case | $R_{th\ j-c}$ | = | 65 | °C/W |
|-----------------------|---------------|---|----|------|

TAA970

CHARACTERISTICS at $R_L = 200\Omega$; $f = 2\text{ kHz}$; $T_{amb} = 25\text{ }^\circ\text{C}$ unless otherwise specified. (see test circuit below).

Supply voltage drop at $R_{th\ j-a} = 100\text{ }^\circ\text{C/W}$

| | | | |
|---------------------------|---------------|------|-------|
| $\pm I_2 = 10\text{ mA}$ | $\pm V_{2-4}$ | < | 5.4 V |
| $\pm I_2 = 50\text{ mA}$ | $\pm V_{2-4}$ | typ. | 4.5 V |
| $\pm I_2 = 100\text{ mA}$ | $\pm V_{2-4}$ | < | 5.8 V |
| | $\pm V_{2-4}$ | < | 6.3 V |

Voltage gain

| | | | |
|---------------------------|--------------------------|-------|------------|
| pin 9 not connected | $\pm I_2 = 10\text{ mA}$ | G_V | 105 to 155 |
| | $\pm I_2 = 50\text{ mA}$ | G_V | typ. 130 |
| pin 9 connected to pin 10 | $\pm I_2 = 10\text{ mA}$ | G_V | 105 to 155 |
| | $\pm I_2 = 50\text{ mA}$ | G_V | 135 to 200 |
| | | | typ. 180 |
| | | | 150 to 200 |

Change of voltage gain

| | | | |
|------------------------------------------|--------------|---|------|
| due to change of supply voltage polarity | ΔG_V | < | 10 % |
|------------------------------------------|--------------|---|------|

Gain reduction at $f = 300\text{ Hz}$
(with respect to $f = 2\text{ kHz}$)

| | | |
|--------------|------|------|
| ΔG_V | typ. | 1 dB |
| | < | 3 dB |

Output impedance at $\pm I_2 = 50\text{ mA}$

| | | | |
|---------------------------|-------|------|--------------|
| pin 9 not connected | R_O | typ. | 80 Ω |
| pin 9 connected to pin 10 | R_O | typ. | 115 Ω |

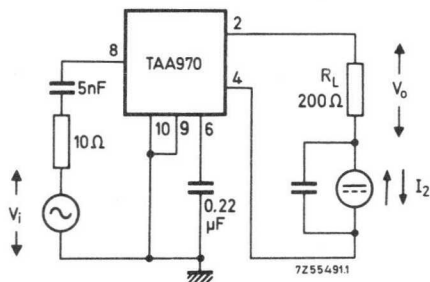
Noise output voltage at $B = 0.3\text{ kHz to }4\text{ kHz}$

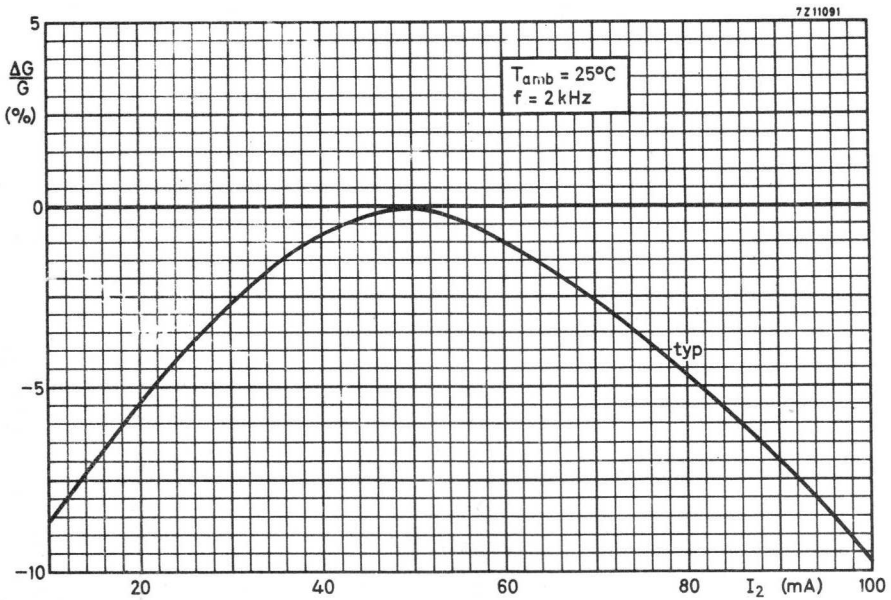
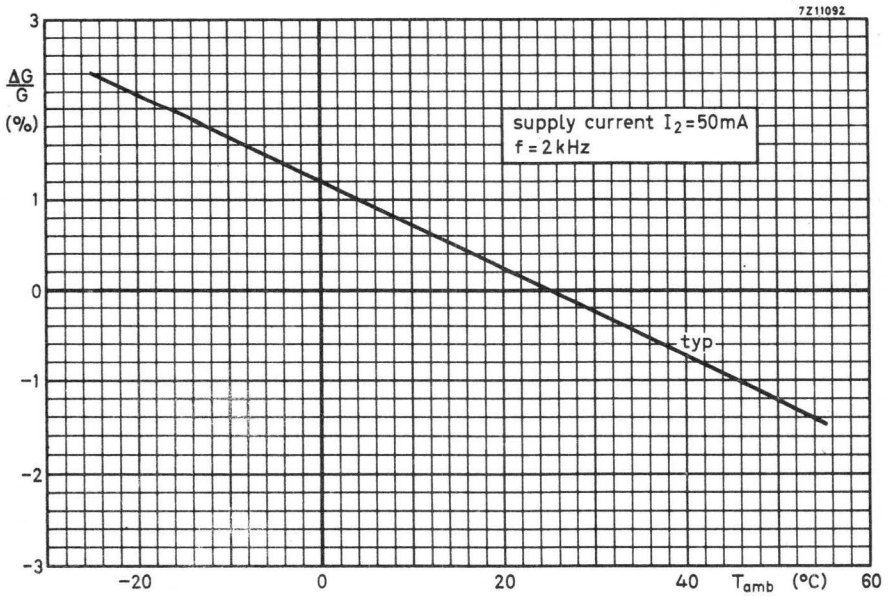
| | | | |
|---------------------------|---------------------|---|--------|
| pin 9 not connected | $V_{n(\text{rms})}$ | < | 1 mV |
| pin 9 connected to pin 10 | $V_{n(\text{rms})}$ | < | 1.3 mV |

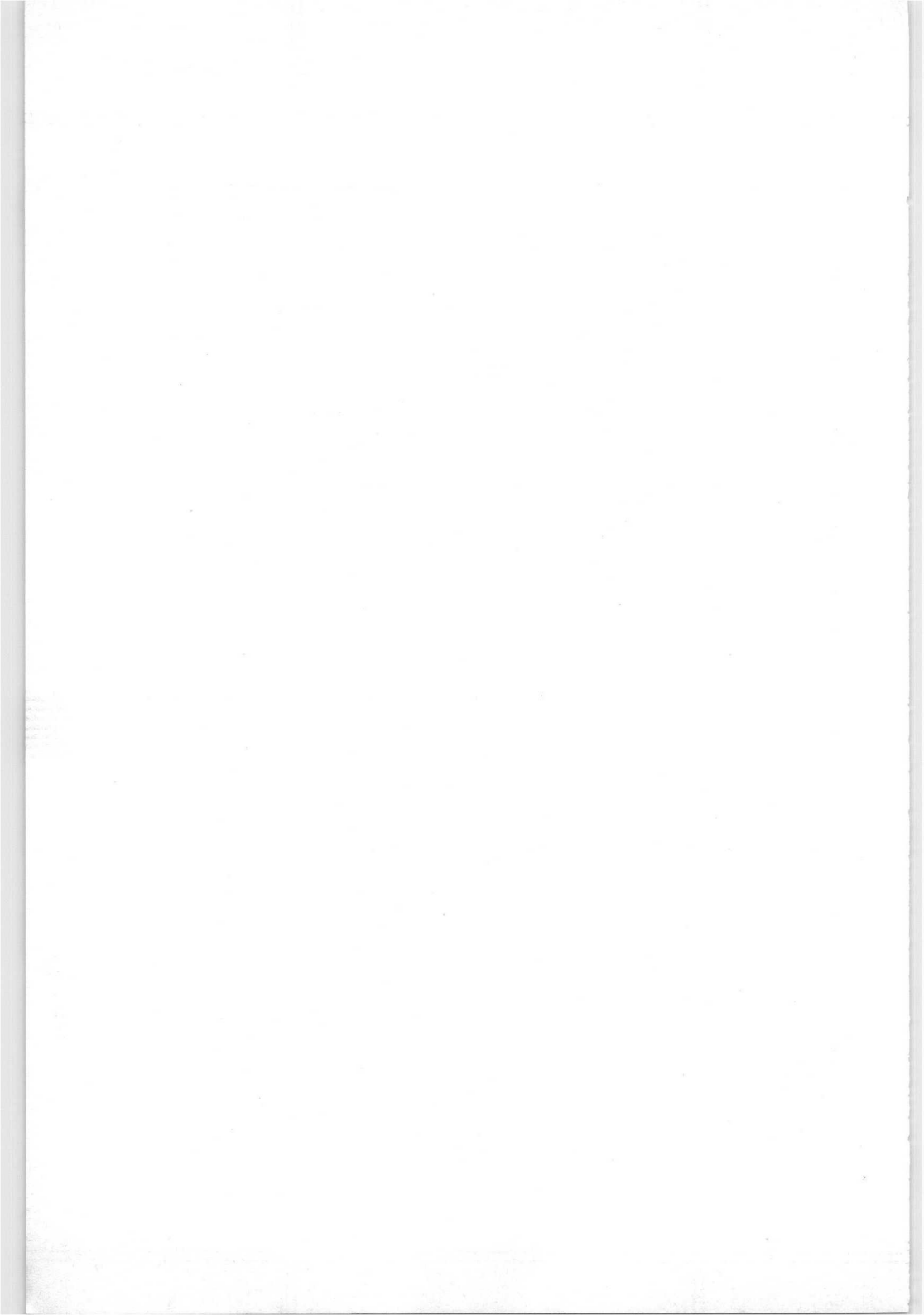
Output voltage

| | | | |
|----------------------------------------|-------|------|-------|
| $I_2 = 50\text{ mA}$; $d_{tot} = 5\%$ | V_O | > | 0.7 V |
| | | typ. | 1.0 V |

Test circuit:







RING (DE)MODULATOR FOR TELEPHONY AND INDUSTRIAL EQUIPMENT

The TAB101 is a monolithic integrated circuit comprising a 4-transistor modulator and demodulator circuit. The circuit being made on a single crystal ensures a great similarity in characteristics of the transistors and optimal tracking of their parameters with temperature variations. Consequently, the TAB101 gives a better balancing and therefore less carrier leakage than a conventional circuit. The use of transistors instead of diodes provides a better isolation between input and output circuits.

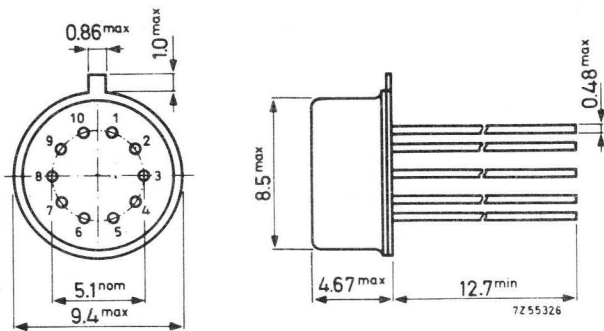
QUICK REFERENCE DATA

| | | |
|-----------------------------------------------------------------------------------------------------------------------------------|-----------------------|--------------------|
| Collector cut-off current $V_{CB} = 5 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$ | I_{CBO} | $< 100 \text{ nA}$ |
| Base-emitter voltage differences between transistors 1, 2, 3, 4 $V_{CB} = 5 \text{ V}; -I_E = 150 \text{ } \mu\text{A}$ | $ V_{BE1} - V_{BE2} $ | $< 5 \text{ mV}$ |
| | $ V_{BE3} - V_{BE4} $ | $< 5 \text{ mV}$ |
| Common-base current gain differences between transistors 1, 2, 3, 4 $V_{CB} = 5 \text{ V}; -I_E = 150 \text{ } \mu\text{A}$ | $ h_{FB1} - h_{FB2} $ | < 0.008 |
| | $ h_{FB3} - h_{FB4} $ | < 0.008 |

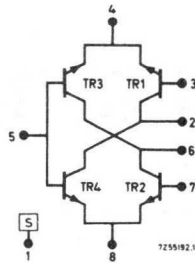
PACKAGE OUTLINE

Dimensions in mm

TO-74 (reduced height)



CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages (each transistor)

| | | | |
|---------------------------------------|-----------|------|------|
| Collector-base voltage (open emitter) | V_{CBO} | max. | 10 V |
| Emitter-base voltage (open collector) | V_{EBO} | max. | 5 V |
| Collector-substrate voltage | V_{CS} | max. | 12 V |

Currents (each transistor)

| | | | |
|-------------------|-------|------|-------|
| Collector current | I_C | max. | 10 mA |
|-------------------|-------|------|-------|

Power dissipation (4 transistors)

| | | | |
|---------------------------------------------------------------------|-----------|------|--------|
| Total power dissipation up to $T_{amb} = 100\text{ }^\circ\text{C}$ | P_{tot} | max. | 100 mW |
|---------------------------------------------------------------------|-----------|------|--------|

Temperatures

| | | | |
|-------------------------------|-----------|-------------|------------------|
| Storage temperature | T_{stg} | -35 to +125 | $^\circ\text{C}$ |
| Operating ambient temperature | T_{amb} | -25 to +100 | $^\circ\text{C}$ |

CHARACTERISTICS (each transistor)

$T_{amb} = 25\text{ }^{\circ}\text{C}$

Collector cut-off current

$I_E = 0; V_{CB} = 5\text{ V}$

I_{CBO}

typ. 5 nA
< 100 nA

Collector-substrate leakage current

$V_{CS} = 9.5\text{ V}$

I_{CS}

typ. 5 nA
< 100 nA

Emitter cut-off current

$I_C = 0; V_{EB} = 1\text{ V}$

I_{EBO}

typ. 5 nA
< 100 nA

Break down voltages

$I_E = 0; I_C = 10\text{ }\mu\text{A}$

$V_{(BR)CBO}$

> 10 V

$I_B = 0; I_C = 10\text{ }\mu\text{A}$

$V_{(BR)CEO}$

> 9 V

$-I_S = 10\text{ }\mu\text{A}$

$V_{(BR)CS}$

> 12 V

$I_C = 0; I_E = 200\text{ }\mu\text{A}$

$V_{(BR)EBO}$

> 5 V

D.C. current gain

$I_C = 150\text{ }\mu\text{A}; V_{CE} = 5\text{ V}$

h_{FE}

> 20
typ. 75

Spot noise figure at $f = 1\text{ kHz}$

$-I_E = 150\text{ }\mu\text{A}; V_{CB} = 5\text{ V}$

$R_S = 1\text{ k}\Omega; \text{Bandwidth: } 200\text{ Hz}$

typ. 6 dB

Base-emitter voltage difference

between transistors TR1 and TR2 at

$-I_{E1} = -I_{E2} = 150\text{ }\mu\text{A}; V_{CB1} = V_{CB2} = 5\text{ V}$

$|V_{BE1} - V_{BE2}|$

typ. 2 mV
< 5 mV

between transistors TR3 and TR4 at

$-I_{E3} = -I_{E4} = 150\text{ }\mu\text{A}; V_{CB3} = V_{CB4} = 5\text{ V}$

$|V_{BE3} - V_{BE4}|$

typ. 2 mV
< 5 mV

Current amplification factor difference

between transistors TR1 and TR2 at

$-I_{E1} = -I_{E2} = 150\text{ }\mu\text{A}; V_{CB1} = V_{CB2} = 5\text{ V}$

$|h_{FB1} - h_{FB2}|$

typ. 0.002
< 0.008

between transistors TR3 and TR4 at

$-I_{E3} = -I_{E4} = 150\text{ }\mu\text{A}; V_{CB3} = V_{CB4} = 5\text{ V}$

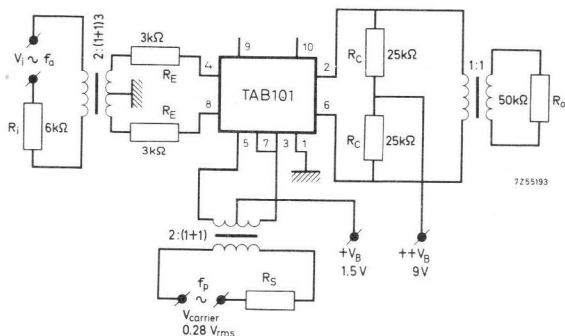
$|h_{FB3} - h_{FB4}|$

typ. 0.002
< 0.008

TAB101

APPLICATION INFORMATION

Telephony carriers ring modulator



Performance at $T_{amb} = 25\text{ }^{\circ}\text{C}$

Conversion gain at $f_a = 1\text{ kHz}$,

$V_i = 0.4\text{ V}$; $f_p = 34\text{ kHz}$

Carrier leakage power in R_o at $f_p = 34\text{ kHz}$

G_c typ. -0.75 dB

P_{oc} typ. 3 nW

INTEGRATED A.M.-RADIO RECEIVER CIRCUIT

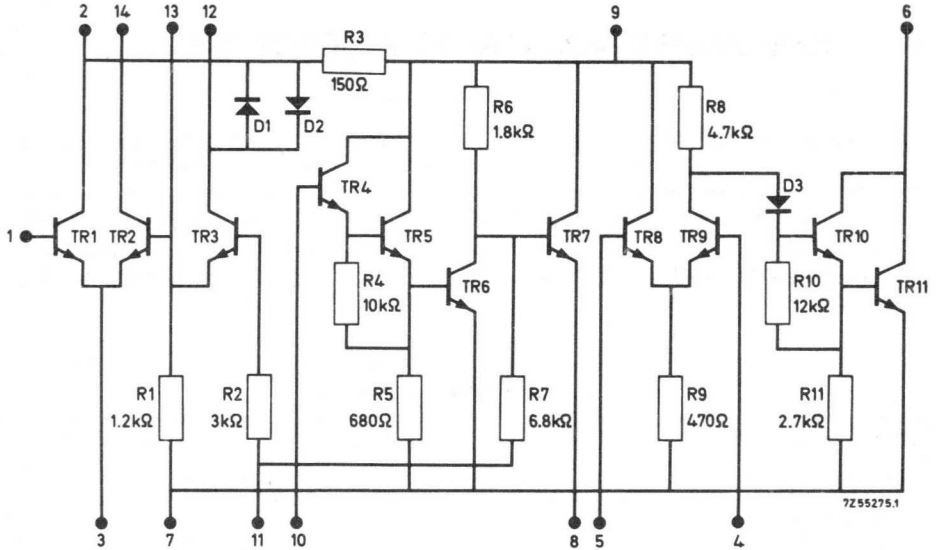
The TAD100 is a monolithic integrated circuit, primarily intended for a.m.-radio receivers. The circuit incorporates the mixer, oscillator, i.f. amplifier, a.g.c., detector, audio pre-amplifier and driver stages. The audio output transistors are not included. This enables the use of different power output stages to suit individual receiver requirements. The frequency response of the circuit is such that the front half of the circuit may be used as part of an i.f. amplifier at 10.7 MHz for f.m. receivers.

QUICK REFERENCE DATA

| | | | | |
|-----------------------------------------------------------------------------------|-----------|------|-----|------------|
| Ambient temperature | T_{amb} | | 25 | °C |
| Supply voltages | V_p | nom. | 6.0 | 9.0 V |
| Output power at $d_{tot} = 10\%$ (with AC187/AC188) | | typ. | 0.7 | 1.5 W |
| Total quiescent current (except output stages) | | typ. | 15 | 23 mA |
| R.F. input signal level (at pin 1) for a signal to noise ratio of 26 dB | | typ. | 30 | 25 μ V |
| A.G.C. range (change in R.F. input voltage for 10 dB expansion in audio range) | | typ. | 62 | 62 dB |
| R.F. signal handling (at pin 1) | | typ. | 30 | 30 mV |
| Harmonic distortion of h.f. part (over most of a.g.c. range) | | < | 2.5 | 2.5 % |

PACKAGE OUTLINE; 14 lead dual in-line (See General Section)

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

| | | | |
|---------------------------------------|-----------|------|------|
| Pin No. 6 voltage | V_{6-7} | max. | 12 V |
| Pin No. 2 voltage | V_{2-7} | max. | 9 V |
| Pin No. 9 voltage (via 150 Ω) | V_{9-7} | max. | 9 V |

Currents

| | | | |
|--------------------------------|-----------|------|-------|
| Pin No. 6 current (peak value) | I_{6M} | max. | 30 mA |
| Pin No. 6 average current | I_{6AV} | max. | 20 mA |

Power dissipation

| | | | |
|-------------------------|-----------|------|--------|
| Total power dissipation | P_{tot} | max. | 150 mW |
|-------------------------|-----------|------|--------|

Temperatures

| | | | |
|-------------------------------|-----------|------------|--------------------|
| Storage temperature | T_{stg} | -25 to +85 | $^{\circ}\text{C}$ |
| Operating ambient temperature | T_{amb} | -10 to +55 | $^{\circ}\text{C}$ |

CHARACTERISTICS at $T_{amb} = 25^{\circ}\text{C}$

A.F. driver saturation voltage

 $I_C = 30 \text{ mA}$
 $I_C = 1.0 \text{ mA}$
 $\left\{ \begin{array}{l} \text{typ. } 0.82 \text{ V} \\ < 1.0 \text{ V} \\ > 0.70 \text{ V} \end{array} \right.$
Measured in the circuit on page 5:

 Output power at $d_{tot} = 10\%$
 (with AC187/AC188)

 $V_p = 9 \quad 6 \text{ V}$

 typ. 1.5 0.7 W

 Total receiver current drain
 (excepting the output matched pair
 AC187/AC188)

 17 to 26 $11 \text{ to } 15 \text{ mA}$

 typ. 20 13 mA

 R.F. input voltage (at pin 1)
 for a signal to noise ratio of 26 dB

 typ. 25 $30 \mu\text{V}^1)$

 A.G.C. range (change in r.f. input voltage
 for 10 dB expansion in audio range)

 typ. 62 $62 \text{ dB}^1)$

 Harmonic distortion of h.f. part
 (over most of a.g.c. range)

 $< 2.5 \quad 2.5 \%^1)$

Signal handling:

 R.F. input voltage (at pin 1) to obtain 10% distortion
 at 80% modulation; $f_m = 400 \text{ Hz}$; R.F. = 1 MHz

 typ. 30 30 mV

 R.F. input voltage (at pin 1)
 for 10 mV a.f. at detector load

 typ. 3.3 $5 \mu\text{V}^1)$
 $< 6.0 \quad 10 \mu\text{V}^1)$

 A.F. voltage at detector load
 for 100 μV r.f. at pin 1

 $> 30 \quad 30 \text{ mV}^1)$

 typ. 50 $50 \text{ mV}^1)$

 Signal to noise ratio for r.f. input
 voltage of 1 mV (at pin 1)

 typ. 40 $41 \text{ dB}^1)$

 A.F. voltage (at pin 4)
 for 50 mW output power

 $< 5.0 \quad 5.0 \text{ mV}$

 Loss of overall receiver sensitivity for 50 mW
 output power at cell voltage of 0.9 V

 typ. 7 $11 \text{ dB}^1)$

 Oscillator voltage at pin 13 (r.m.s. value)
 at a battery voltage of 3.6 V to 9 V

 $> 95 \quad 95 \text{ mV}$

Oscillator-frequency shift at 2 MHz over a.g.c. range

 $< 350 \quad 350 \text{ Hz}$

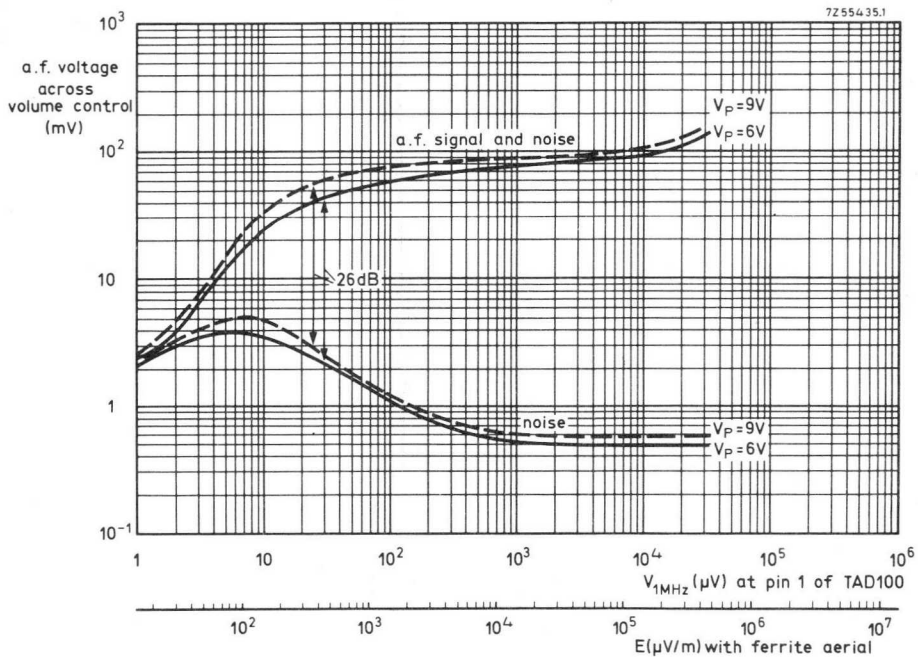
 Oscillator-frequency shift at 2 MHz
 over range of supply voltage

 typ. 300 300 Hz

Typical overall fidelity (flat within 3 dB)

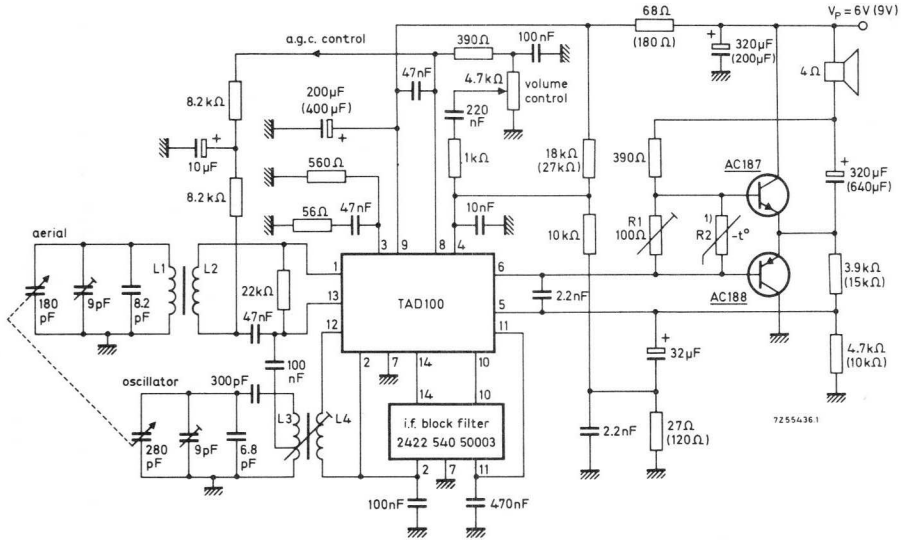
 $120 \text{ to } 2000 \text{ Hz}$
¹⁾ R.F. = 1 MHz; 30% modulation; $f_m = 400 \text{ Hz}$

CHARACTERISTICS (continued)



APPLICATION INFORMATION

Medium-wave receiver using the TAD100



Medium wave aerial coil:

$L1 = 310 \mu\text{H}$; $Q_{\text{loaded}} = 100$ at 1 MHz; FXC rod for 2 MHz

$$\frac{VL1}{VL2} \approx 11$$

Medium wave oscillator coil:

$L3 = 165 \mu\text{H}$; $Q_0 = 100$ at 1.4 MHz; tapping ratio $L3 \approx \frac{1}{46}$

$$\frac{VL3}{VL4} \approx 9$$

Quiescent current (adjusted by R1): 5 mA

Modification for 9 V supply voltage:

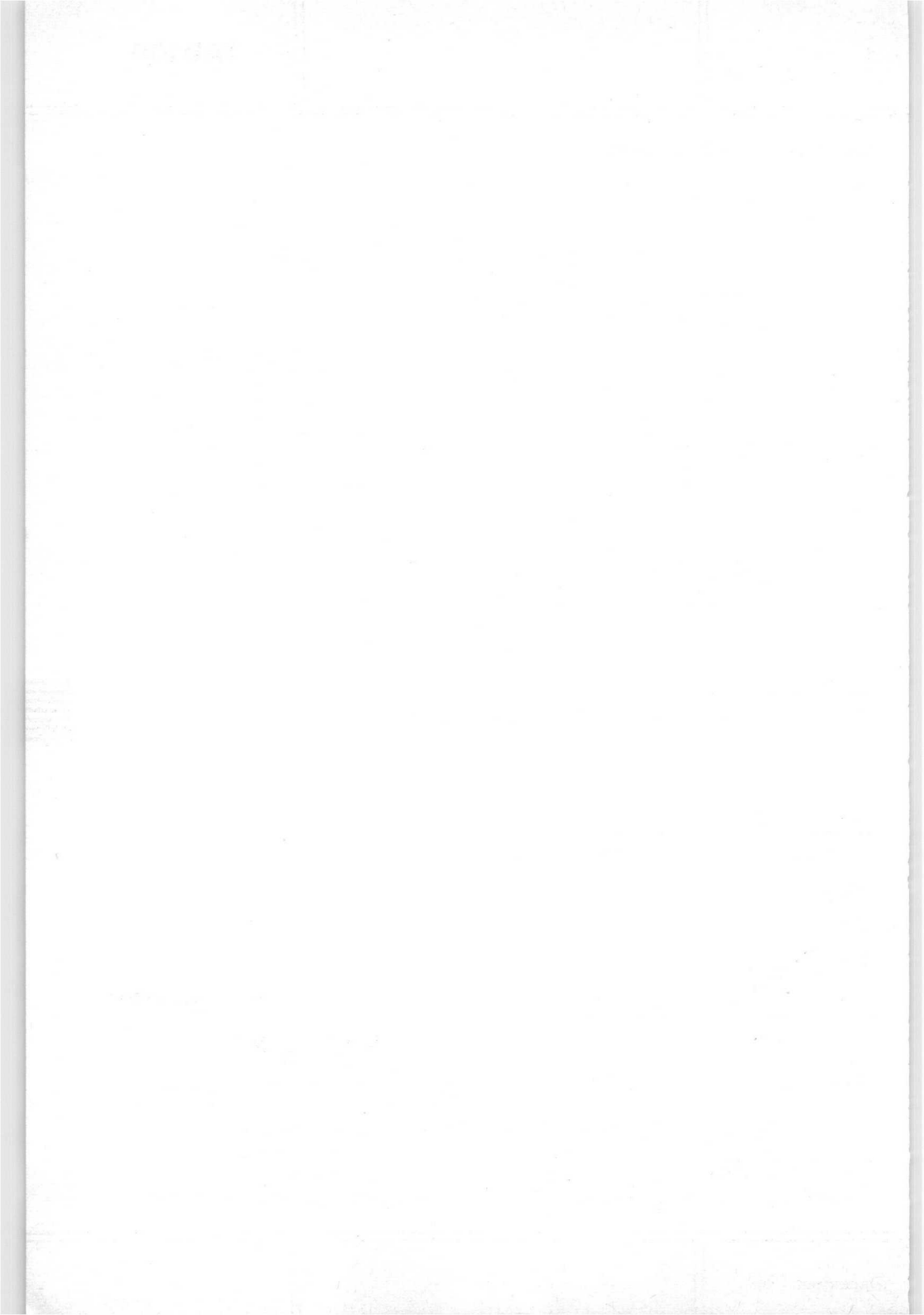
Values in brackets refer only to a 9 V supply, the others apply to 6 V and 9 V supplies.

AC187 and AC188 with cooling clip 56227 on 1.5 mm blackened Al. heatsinks of 9 cm^2 .

APPLICATION INFORMATION bulletins available on request

¹⁾ For 6 V supply: 130 Ω; disk type NTC resistor (2322 610 90004)

For 9 V supply: 50 Ω; disk type NTC resistor on metal strip (2322 610 90016)



OPERATIONAL AMPLIFIER

The TBA221 is a silicon monolithic integrated operational amplifier for use at temperatures from 0 to 70 °C. Special features are:

- no frequency compensation required
- continuous short circuit protection
- offset voltage adjustable to zero
- large input voltage range
- low power consumption
- no latch up

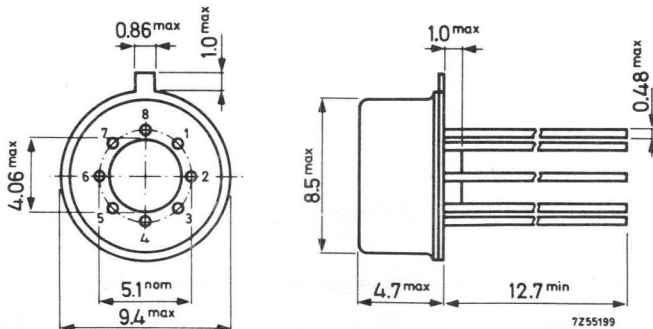
The TBA221 is equivalent to 741C.

QUICK REFERENCE DATA

| | | | |
|-----------------------------------------------------------------------|-----------|--------------|------------|
| Positive supply voltage | V_P | 15 | V |
| Negative supply voltage | $-V_N$ | 15 | V |
| ----- | | | |
| Characteristics at $T_{amb} = 25\text{ }^\circ\text{C}$ | | | |
| Voltage gain at $R_L \geq 2\text{ k}\Omega$; $V_O = \pm 10\text{ V}$ | G_V | typ. 100.000 | |
| Common mode rejection ratio | CMRR | typ. 90 | dB |
| Differential input resistance | R_i | typ. 1 | M Ω |
| Peak output voltage swing at $R_L = 10\text{ k}\Omega$ | V_{OM} | > ± 12 | V |
| Input voltage range | V_i | > ± 12 | V |
| Power dissipation | P_{tot} | typ. 50 | mW |

PACKAGE OUTLINE TO-99

Dimensions in mm



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

| | | | | |
|-----------------------------------------|-----------|------|----------|---|
| Positive supply voltage | V_P | max. | 18 | V |
| Negative supply voltage | $-V_N$ | max. | 18 | V |
| Common mode input voltage ¹⁾ | V_i | max. | ± 15 | V |
| Differential input voltage | V_{2-3} | max. | ± 30 | V |

Power dissipation

P_{tot} max. 500 mW

Output short circuit duration ²⁾

indefinite

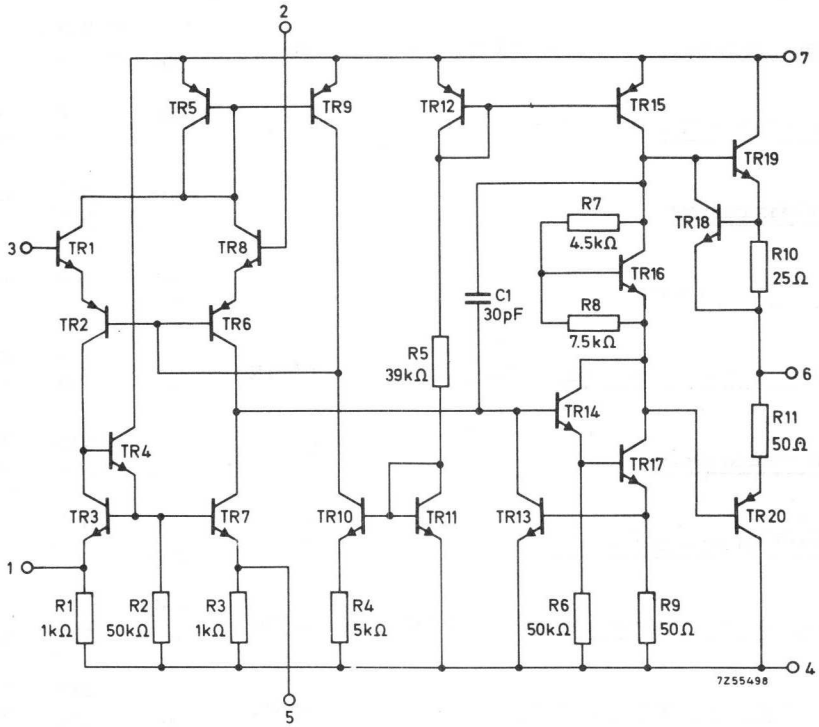
Temperatures

| | | | |
|-------------------------------|-----------|---------------|-------------|
| Operating ambient temperature | T_{amb} | 0 to + 70 | $^{\circ}C$ |
| Storage temperature | T_{stg} | - 65 to + 150 | $^{\circ}C$ |

1) For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

2) Continuous short circuit is allowed to ground or either supply.

CIRCUIT DIAGRAM

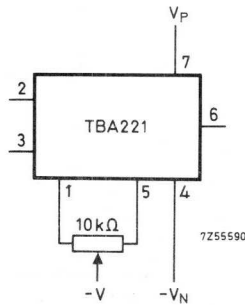


CHARACTERISTICS at $V_P = 15\text{ V}$; $-V_N = 15\text{ V}$; $T_{\text{amb}} = 25^\circ\text{C}$ unless otherwise specified

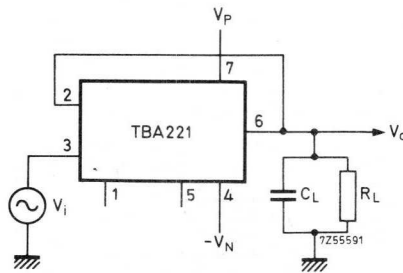
| | | | | |
|-----------------------------------------------------------------------------|------------------|------|----------|------------------|
| <u>Voltage gain</u> ; $R_L \geq 2\text{ k}\Omega$; $V_O = \pm 10\text{ V}$ | G_V | > | 20.000 | |
| | | typ. | 100.000 | |
| <u>Input offset voltage</u> ; $R_S \leq 10\text{ k}\Omega$ | V_{io} | typ. | 2.0 | mV |
| | | < | 6.0 | mV |
| <u>Input bias current</u> | I_i | typ. | 0.2 | μA |
| | | < | 0.5 | μA |
| <u>Input offset current</u> | I_{io} | typ. | 30 | nA |
| | | < | 0.2 | μA |
| <u>Common mode rejection ratio</u> ; $R_S \leq 10\text{ k}\Omega$ | CMRR | > | 70 | dB |
| | | typ. | 90 | dB |
| <u>Input voltage range</u> | V_i | > | ± 12 | V |
| | | typ. | ± 13 | V |
| <u>Differential input resistance</u> | R_i | > | 0.3 | $\text{M}\Omega$ |
| | | typ. | 1 | $\text{M}\Omega$ |
| <u>Supply voltage rejection ratio</u> ; $R_S \leq 10\text{ k}\Omega$ | SVRR | typ. | 30 | $\mu\text{V/V}$ |
| | | < | 150 | $\mu\text{V/V}$ |
| <u>Peak output voltage swing</u> at $R_L \geq 10\text{ k}\Omega$ | V_{OM} | > | ± 12 | V |
| | | typ. | ± 14 | V |
| | | > | ± 10 | V |
| $R_L \geq 2\text{ k}\Omega$ | V_{OM} | typ. | ± 13 | V |
| <u>Power dissipation</u> at $V_O = 0$ | P_{tot} | typ. | 50 | mW |
| | | < | 85 | mW |
| <u>Transient response</u> (unity gain) | | | | |
| $V_i = 20\text{ mV}$; $R_L = 2\text{ k}\Omega$; $C_L = 100\text{ pF}$ | | | | |
| Rise time | | typ. | 0.3 | μs |
| Overshoot | | typ. | 5.0 | % |
| <u>Slew rate</u> (unity gain) | | | | |
| $R_L \geq 2\text{ k}\Omega$ | | typ. | 0.5 | V/ μs |

CHARACTERISTICS at $V_P = 15\text{ V}$; $-V_N = 15\text{ V}$; $T_{\text{amb}} = 0\text{ to }70^\circ\text{ C}$ unless otherwise specified

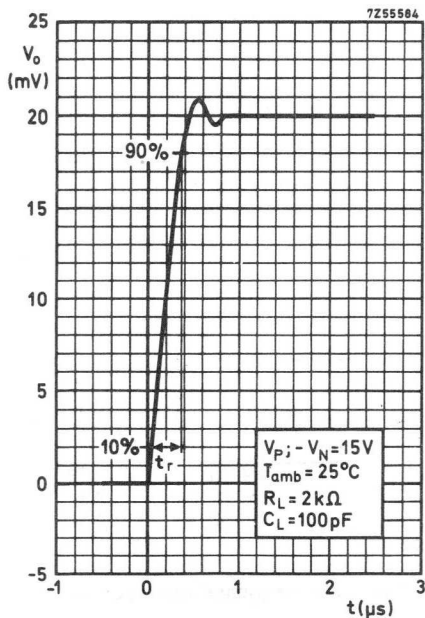
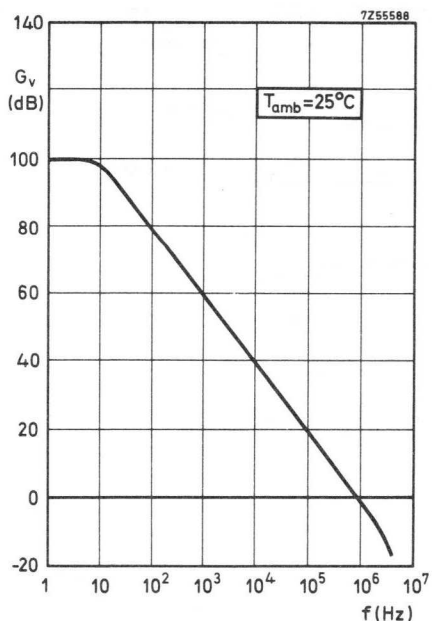
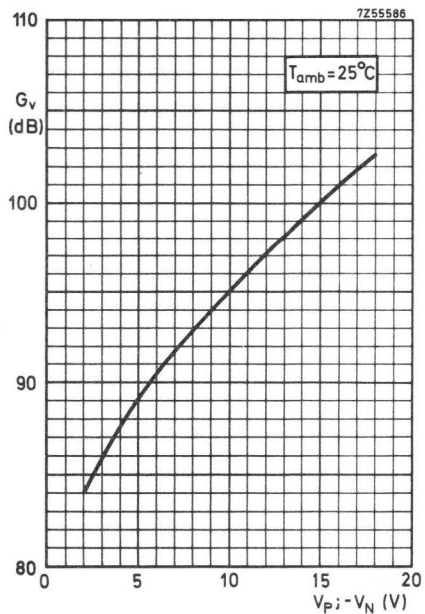
| | | | |
|-----------------------------------------------------------------------------|----------|-----|-------------------|
| <u>Voltage gain</u> ; $R_L \geq 2\text{ k}\Omega$; $V_O = \pm 10\text{ V}$ | G_V | $>$ | 15.000 |
| <u>Input offset voltage</u> ; $R_S \leq 10\text{ k}\Omega$ | V_{iO} | $<$ | 7.5 mV |
| <u>Input bias current</u> | I_i | $<$ | 0.8 μA |
| <u>Input offset current</u> | I_{iO} | $<$ | 0.3 μA |
| <u>Peak output voltage swing</u> ; $R_L \geq 2\text{ k}\Omega$ | V_{OM} | $>$ | $\pm 10\text{ V}$ |



Offset voltage zeroing circuit



Transient response test circuit



OPERATIONAL AMPLIFIER

The TBA222 is a silicon monolithic integrated operational amplifier for use at temperatures from -55 to +125 °C. Special features are:

- no frequency compensation required
- continuous short-circuit protection
- offset voltage adjustable to zero
- large input voltage range
- low power consumption
- no latch-up

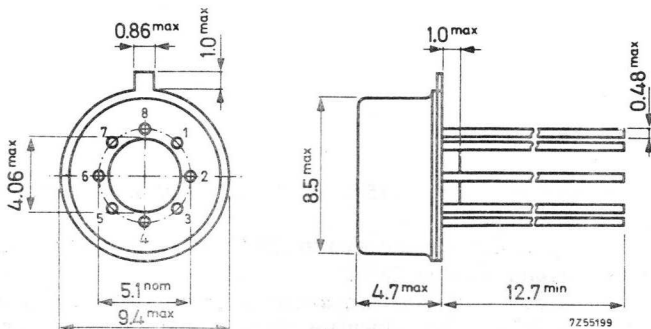
The TBA222 is equivalent to 741.

QUICK REFERENCE DATA

| | | | |
|-----------------------------------------------------------------------|-----------|--------------|------------|
| Positive supply voltage | V_P | 15 | V |
| Negative supply voltage | $-V_N$ | 15 | V |
| ----- | | | |
| Characteristics at $T_{amb} = 25\text{ }^\circ\text{C}$ | | | |
| Voltage gain at $R_L \geq 2\text{ k}\Omega$; $V_O = \pm 10\text{ V}$ | G_V | typ. 200 000 | |
| Common mode rejection ratio | CMRR | typ. 90 | dB |
| Differential input resistance | R_i | typ. 1 | M Ω |
| Peak output voltage swing at $R_L = 10\text{ k}\Omega$ | V_{OM} | > ± 12 | V |
| Input voltage range | V_i | > ± 12 | V |
| Power dissipation | P_{tot} | typ. 50 | mW |

PACKAGE OUTLINE TO-99

Dimensions in mm



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

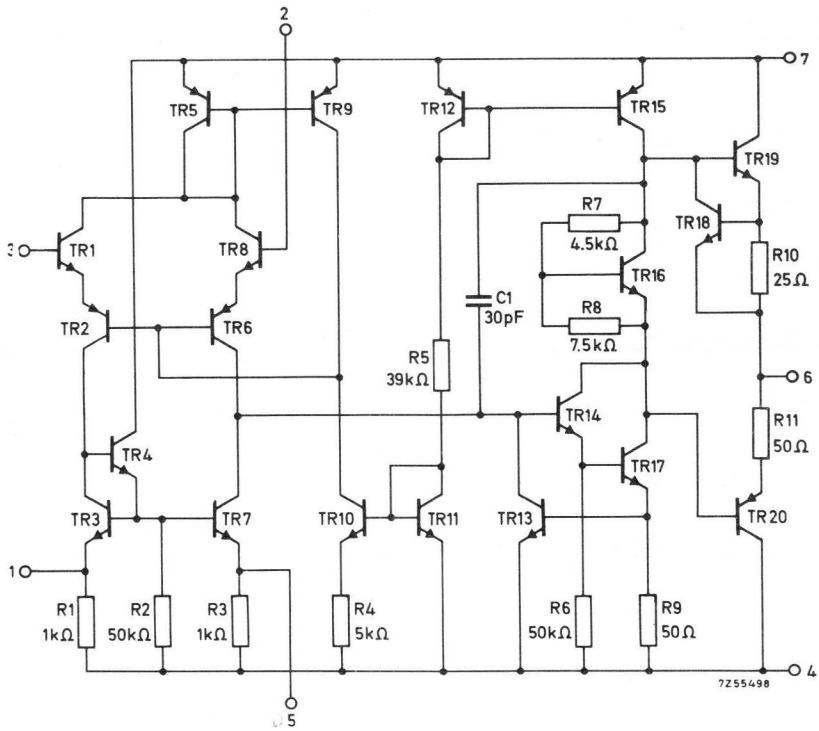
| | | | | |
|----------------------------------------------------|-----------|------|------------|----|
| Positive supply voltage | V_P | max. | 22 | V |
| Negative supply voltage | $-V_N$ | max. | 22 | V |
| Common mode input voltage ¹⁾ | V_i | max. | ±15 | V |
| Differential input voltage | V_{2-3} | max. | ±30 | V |
| <u>Power dissipation</u> ²⁾ | P_{tot} | max. | 500 | mW |
| <u>Output short circuit duration</u> ³⁾ | | | indefinite | |

Temperatures

| | | | |
|-------------------------------|-----------|-------------|----|
| Operating ambient temperature | T_{amb} | -55 to +125 | °C |
| Storage temperature | T_{stg} | -65 to +150 | °C |

- ¹⁾ For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.
- ²⁾ Rating applies for **case temperatures up to 125 °C**; derate linearly at 6.5 mW/°C for ambient temperatures above 75 °C.
- ³⁾ Continuous short circuit is allowed for case temperatures up to 125 °C and ambient temperatures up to 70 °C. Short circuit is allowed to ground or either supply.

CIRCUIT DIAGRAM

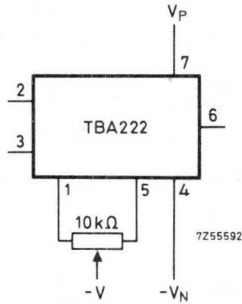


CHARACTERISTICS at $V_P = 15\text{ V}$; $-V_N = 15\text{ V}$; $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ unless otherwise specified

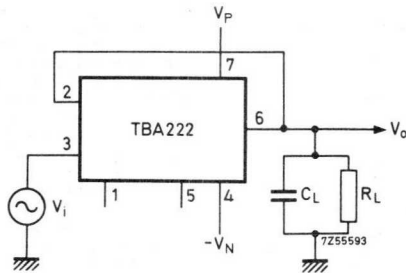
| | | | |
|----------------------------------------------------------------------------------------------------------------------|------------------|-----------|---------------------------------------------------------|
| <u>Voltage gain</u> ; $R_L \geq 2\text{ k}\Omega$; $V_O = \pm 10\text{ V}$ | G_V | > typ. | 50 000 200 000 |
| <u>Input offset voltage</u> ; $R_S \leq 10\text{ k}\Omega$ | V_{io} | typ. < | 1.0 mV 5.0 mV |
| <u>Input bias current</u> | I_i | typ. < | 0.2 μA 0.5 μA |
| <u>Input offset current</u> | I_{io} | typ. < | 30 nA 0.2 μA |
| <u>Common mode rejection ratio</u> ; $R_S \leq 10\text{ k}\Omega$ | CMRR | > typ. | 70 dB 90 dB |
| <u>Input voltage range</u> | V_i | > typ. | $\pm 12\text{ V}$ $\pm 13\text{ V}$ |
| <u>Differential input resistance</u> | R_i | > typ. | 0.3 $\text{M}\Omega$ 1.0 $\text{M}\Omega$ |
| <u>Supply voltage rejection ratio</u> ; $R_S \leq 10\text{ k}\Omega$ | SVRR | typ. < | 30 $\mu\text{V}/\text{V}$ 150 $\mu\text{V}/\text{V}$ |
| <u>Peak output voltage swing</u> at $R_L \geq 10\text{ k}\Omega$ | V_{OM} | > typ. | $\pm 12\text{ V}$ $\pm 14\text{ V}$ |
| $R_L \geq 2\text{ k}\Omega$ | V_{OM} | > typ. | $\pm 10\text{ V}$ $\pm 13\text{ V}$ |
| <u>Power dissipation</u> at $V_O = 0$ | P_{tot} | typ. < | 50 mW 85 mW |
| <u>Transient response</u> (unity gain) $V_i = 20\text{ mV}$; $R_L = 2\text{ k}\Omega$; $C_L \leq 100\text{ pF}$ | | | |
| Rise time | | typ. | 0.3 μs |
| Overshoot | | typ. | 5.0 % |
| <u>Slew rate</u> (unity gain) $R_L \geq 2\text{ k}\Omega$ | | typ. | 0.5 $\text{V}/\mu\text{s}$ |

CHARACTERISTICS at $V_P = 15\text{ V}$; $-V_N = 15\text{ V}$; $T_{\text{amb}} = -55\text{ to }+125\text{ }^\circ\text{C}$ unless otherwise specified.

| | | | |
|-----------------------------------------------------------------------------|----------|---|-------------------|
| <u>Voltage gain</u> ; $R_L \geq 2\text{ k}\Omega$; $V_O = \pm 10\text{ V}$ | G_V | > | 25.000 |
| <u>Input offset voltage</u> ; $R_S \leq 10\text{ k}\Omega$ | V_{iO} | < | 6 mV |
| <u>Input bias current</u> | I_i | < | 1.5 μA |
| <u>Input offset current</u> | I_{iO} | < | 0.5 μA |
| <u>Peak output voltage swing</u> $R_L \geq 2\text{ k}\Omega$ | V_{OM} | > | $\pm 10\text{ V}$ |

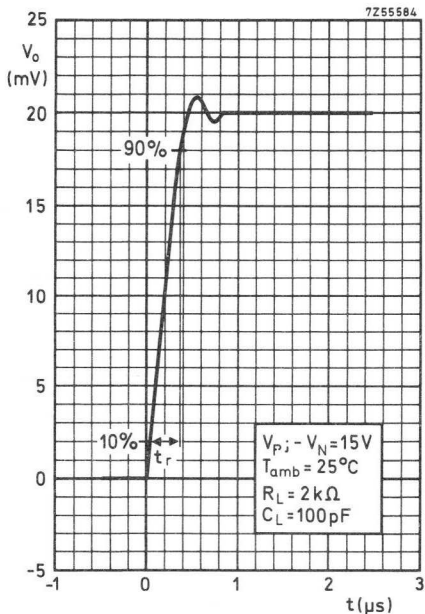
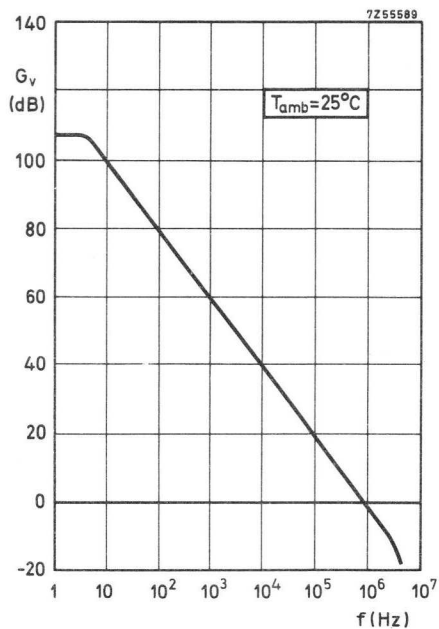
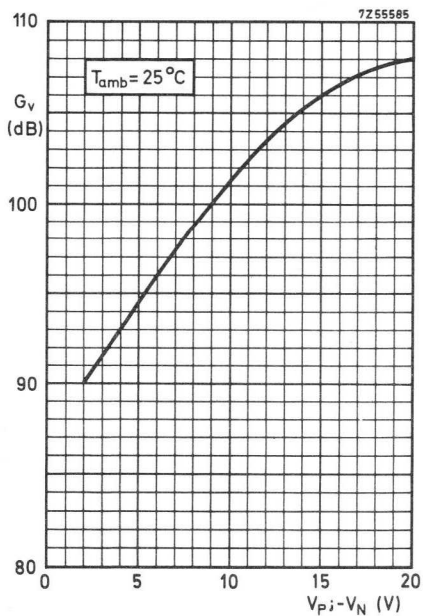
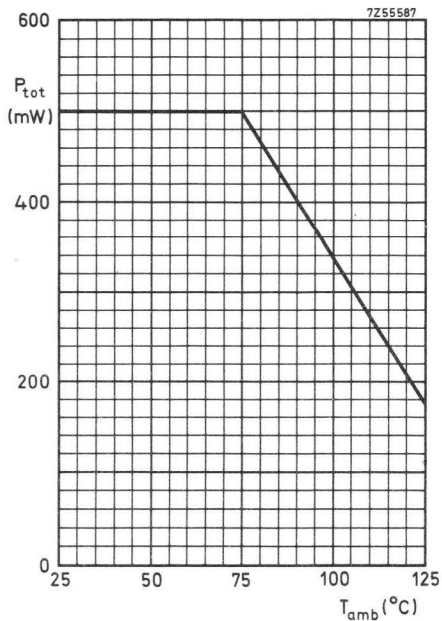


Offset voltage zeroing circuit



Transient response test circuit

TBA222



AUTOMATIC LINE SYNCHRONISATION CIRCUIT

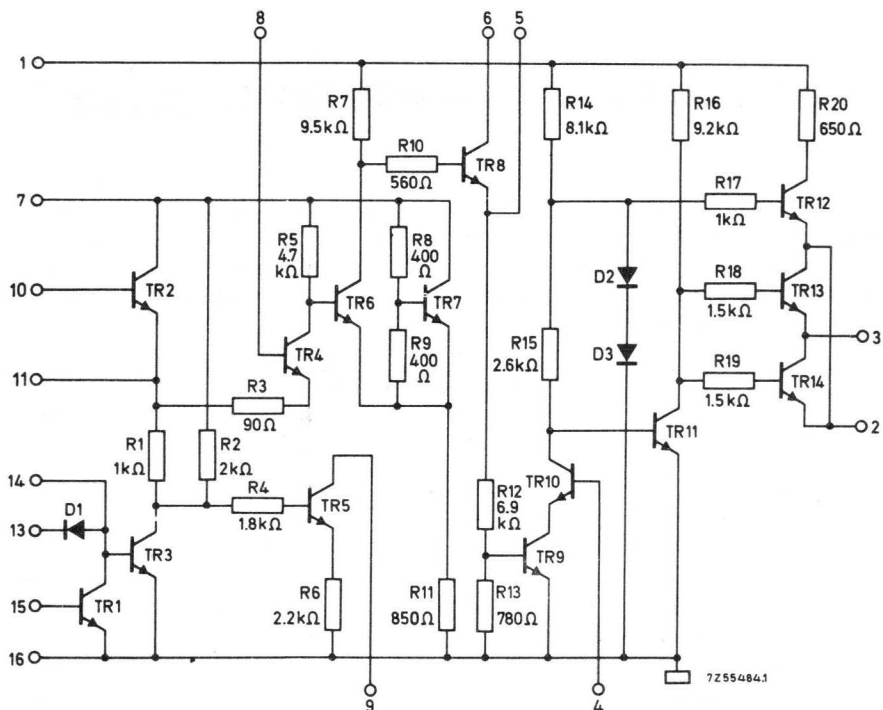
The TBA240 is a monolithic integrated noise detector and inverter, sync separator, catching circuit, and line discriminator. It can be used in a wide variety of b-w and colour television receivers and is designed for best operation with negative-modulated video signals but is also compatible with positive modulation. The required supply voltages are +5.5 V and +12 V.

QUICK REFERENCE DATA

| | | |
|---------------------------------------------------------------------------------------|------------------------|-------------|
| Supply voltages | V ₇₋₁₆ | typ. 5.5 V |
| | V ₁₋₁₆ | typ. 12 V |
| Ambient temperature | T _{amb} | typ. 25 °C |
| ----- | | |
| Total average power dissipation | P _{tot} | typ. 100 mW |
| <u>Required input signals</u> | | |
| Typical composite peak white to peak sync voltage | V ₁₀₋₁₆ | 0.5 to 3 V |
| Negative noise pulse current (peak value) | I _{13M} | > 100 μA |
| Positive noise pulse current (peak value) | I _{15M} | > 10 μA |
| <u>Delivered output signals</u> | | |
| Discriminator output voltage (peak to peak value) | V _{3-16(p-p)} | < 4 V |
| Positive going sinc pulse voltage (peak to peak value) | V _{5-16(p-p)} | typ. 7.5 V |
| Negative going noise pulse voltage (peak to peak value) | V _{9-16(p-p)} | typ. 2 V |
| Typical composite video , with inverted noise pulses, peak white to peak sync voltage | V ₁₁₋₁₆ | 0.5 to 3 V |

PACKAGE OUTLINE : 16 lead quadruple in-line (See page 8)

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

| | |
|-----------------------------------------------------------------------------------------------------|---------------------------------------|
| Pin No.1 voltage ($V_{1-16} > V_{7-16}$) | V_{1-16} max. 13 V ¹⁾ |
| Pin No.2 voltage | see test circuit on page 5 |
| Pin No.3 voltage | do not apply external voltage |
| Pin No.4 voltage (via $R_2 \geq 1 \text{ k}\Omega$) | V_{4-16} -5 to +1.5 V ²⁾ |
| Pin No.6 voltage (connect pin 6 to pin 1, via $R_3 \leq 2 \text{ k}\Omega$); $V_{6-16} > V_{7-16}$ | V_{6-16} max. 13 V ¹⁾²⁾ |

¹⁾ Tolerated minimum voltage: 0 V

²⁾ See test circuit on page 5.

RATINGS (continued)

| | | | |
|--------------------------------------------------------------------------------|-------------------------------|----------|-------------------|
| Pin No. 7 voltage | V_{7-16} | max. | 7 V ¹⁾ |
| Pin No. 8 voltage (connect pin 8 to pin 7, via $R_4 > 50 \text{ k}\Omega$) | V_{8-16} | max. | 7 V ¹⁾ |
| Pin No. 9 voltage (connect pin 9 to pin 7, via $R_5 < 10 \text{ k}\Omega$) | V_{9-16} | max. | 7 V ¹⁾ |
| Pin No. 10 voltage (via $R_6 > 2 \text{ k}\Omega$) $V_{10-16} < V_{7-16}$ | V_{10-16} | max. | 7 V ¹⁾ |
| Pin No. 11 voltage | do not apply external voltage | | |
| Pin No. 12 voltage | do not connect | | |
| Pin No. 13 voltage (via $R_7 > 1 \text{ k}\Omega$) | V_{13-16} | -1 to +5 | V |
| Pin No. 15 voltage | $-V_{15-16}$ | max. | 5 V |

Currents

| | | | |
|--------------------|--------------|------------|--------------------|
| Pin No. 5 current | I_5 | -5 to +0.5 | mA |
| Pin No. 11 current | $\pm I_{11}$ | max. | 250 μA |
| Pin No. 13 current | $-I_{13}$ | max. | 1 mA ²⁾ |
| Pin No. 14 current | $\pm I_{14}$ | max. | 1 mA |
| Pin No. 15 current | I_{15} | max. | 1 mA |

| | | | |
|--------------------------------|------------------|------|----------------------|
| <u>Total power dissipation</u> | P_{tot} | max. | 260 mW ³⁾ |
|--------------------------------|------------------|------|----------------------|

Temperatures

| | | | |
|-------------------------------|------------------|-------------|--------------------|
| Operating ambient temperature | T_{amb} | 0 to +60 | $^{\circ}\text{C}$ |
| Storage temperature | T_{stg} | -25 to +125 | $^{\circ}\text{C}$ |

¹⁾ Tolerated minimum voltage: 0 V

²⁾ Tolerated minimum current: 0 mA

³⁾ Derated from $T_{\text{amb}} \geq 60 \text{ }^{\circ}\text{C}$ with 4 mW/ $^{\circ}\text{C}$.

CHARACTERISTICS at $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{7-16} = 5.5\text{ V}$; $V_{1-16} = 12\text{ V}$

Total average power dissipation P_{tot} typ. 100 mW

Required input signals

Typical composite peak white to peak sync voltage V_{10-16} 0.5 to 3 V

Negative noise pulse current (peak value) I_{13M} $\geq 100\text{ }\mu\text{A}$

Positive noise pulse current (peak value) I_{15M} $\geq 10\text{ }\mu\text{A}$

Delivered output signals

Discriminator output voltage (peak to peak value) $V_{3-16(p-p)}$ $\leq 4\text{ V}$

Positive going sync pulse voltage (peak to peak voltage) $V_{5-16(p-p)}$ typ. 7.5 V

Negative going noise pulse voltage (peak to peak value) $V_{9-16(p-p)}$ typ. 2 V

Typical composite video, with inverted noise pulses, peak white to peak sync voltage (to be utilized if external frame sync is applied) V_{11-16} 0.5 to 3 V

Frequency response for signal voltages:

V_{2-16} , V_{5-16} and V_{9-16} with respect to V_{10-16} $t_{pdr} + t_r \leq 600\text{ ns}$

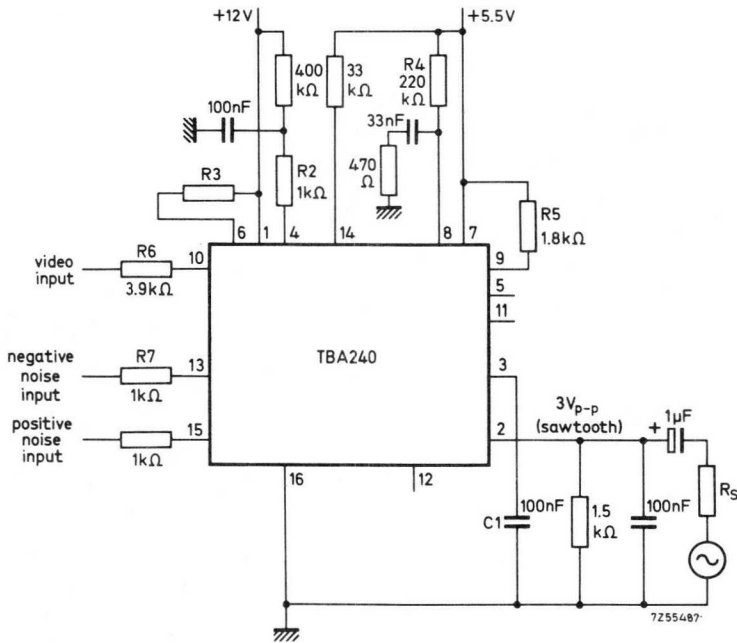
$t_{pdf} + t_f \leq 600\text{ ns}$

Symmetry fault in discriminator

Pin No. 2 and No. 3 voltage difference (for symmetrical saw tooth of 3 V_{p-p}) $V_{2-16} - V_{3-16} \leq 0.2\text{ V}$

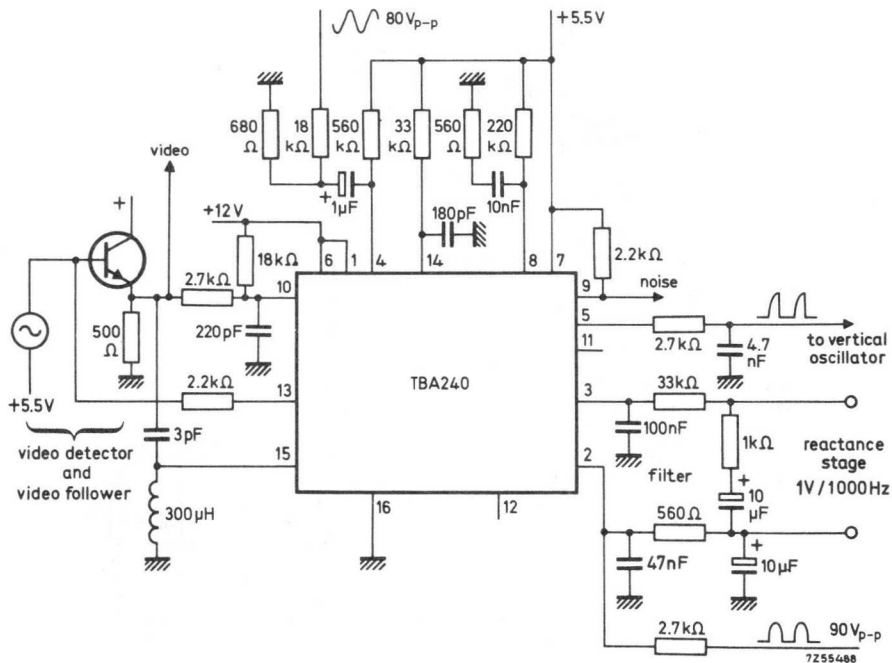
CHARACTERISTICS (continued)

Test circuit:



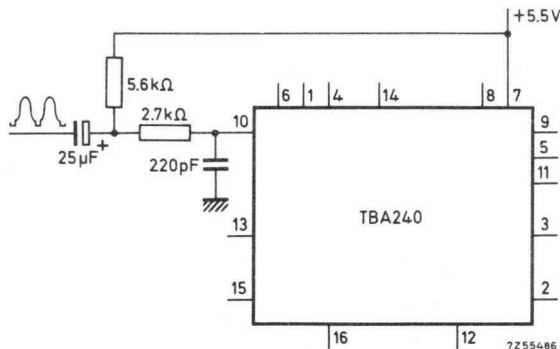
APPLICATION INFORMATION

Example of a circuit for negative modulated signals



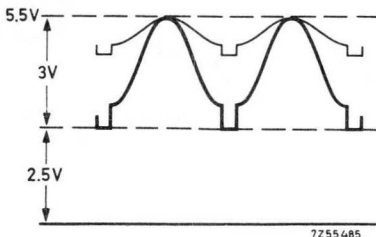
Notes:

1. The video signal is d. c. coupled to the clipping circuit and the sync pulse is sliced about 30% below top sync.
2. For positive modulation a. c. coupling is preferred (see figure below); slicing then varies between 10% and 30% below top sync, depending on picture content.



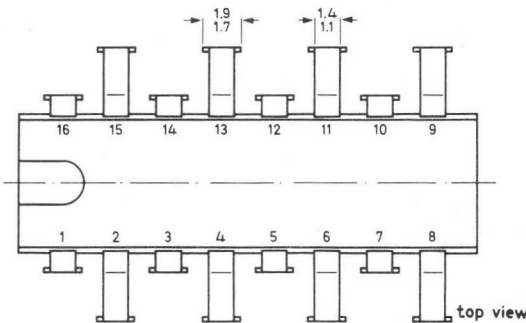
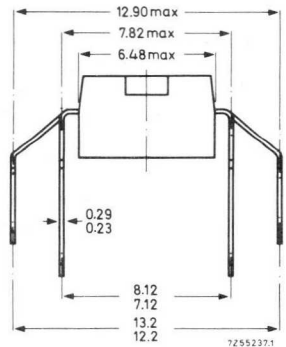
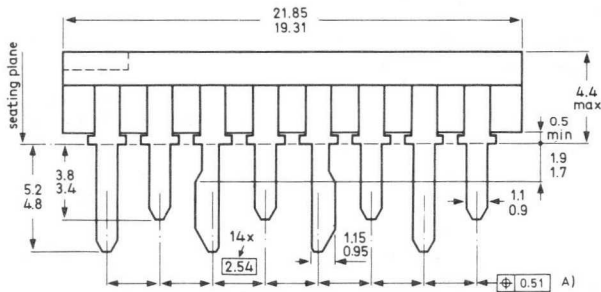
APPLICATION INFORMATION (continued)

3. In the top circuit on page 6, pin 13 gives amplitude selective and pin 15 frequency selective noise inversion. The amplitude selective inversion starts when impulses pass zero in the negative direction; the frequency selective inversion, when the peak voltage across the coil exceeds 0.7 V.
4. The keying voltage on pin 4 (top circuit on page 6) is derived from the voltage across the capacitor in series with the line deflection coils; alternatively, it can be derived from a positive flyback voltage across the coils (less components), but in that case the vertical pulse may exercise a stronger influence on the line flywheel.
5. In the out-of-sync conditions the phase discriminator operates as a frequency detector; to keep the catching range from being shifted, the d.c. load at pin 3 should not be allowed to exceed about $6 \mu\text{A}$. Good results are obtained with a reactance stage sensitivity of 1 kHz/V ($\pm 700 \text{ Hz}$ catching range).
6. An integral stabilization circuit (TR12) establishes the level of the comparison sawtooth at pin 2. To avoid overloading the stabilization circuit, the direct current from pin 2 to earth must not exceed 1 mA.
7. The clipper input (pin 10) calls for a video signal with negative-going sync pulses. The figure below shows the optimum levels. The clipped slice is proportional to the difference between the top sync level and +5.5 V (i.e. to 3 V in figure below).



16 LEAD QUADRUPLE IN-LINE

Dimensions in mm



A) Centre-lines of all leads are within ± 0.254 mm of the nominal positions shown; in the worst case, the spacing between any two leads may deviate from nominal by ± 0.51 mm.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

260 °C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

VOLTAGE REGULATOR

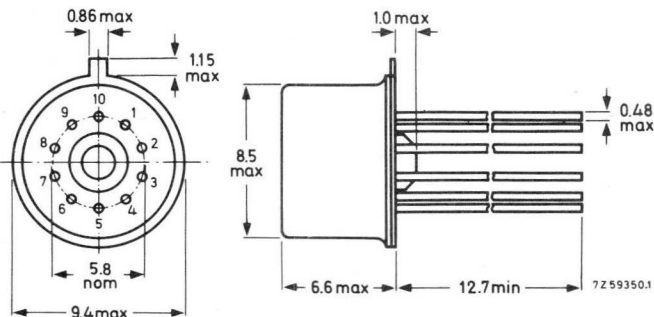
The TBA281 is a monolithic voltage regulator. It comprises a temperature compensated reference amplifier, an error amplifier, a power series pass transistor and current limit circuitry. External series pass transistors may be added if the load current exceeds the maximum limit. The circuit can be used with adjustable current limiting and remote shut down. It features low stand-by current drain, low temperature drift and high ripple rejection. The TBA281 can be used with positive or negative supply voltages as a series, shunt, switching or floating regulator in the ambient temperature range 0 to +70°C. The TBA281 is equivalent to the 723C.

QUICK REFERENCE DATA

| | | | |
|---------------------------------------------------|------|-----------|---------|
| Line regulation $V_i = 12V$ to $40V$ | typ. | 0.1 | % V_o |
| Load regulation $I_L = 1$ mA to 50 mA | typ. | 0.03 | % V_o |
| Stand-by current drain $V_i = 30V$, $I_o = 0$ | typ. | 2.3 | mA |
| Input voltage range | | 9.5 to 40 | V |
| Output voltage range | | 2.0 to 37 | V |
| Input-output voltage difference | | 3.0 to 38 | V |

PACKAGE OUTLINE

Dimensions in mm



For details of pin numbering see page 3.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

| | | | | |
|---------------------------------|-----------|------|----|---|
| Input voltage | V_7 | max. | 40 | V |
| Supply voltage | V_8 | max. | 40 | V |
| Input-output voltage difference | V_{7-6} | max. | 40 | V |

Currents

| | | | | |
|-----------------------------------------|--------|------|-----|----|
| Output current | $-I_6$ | max. | 150 | mA |
| Current from reference amplifier output | $-I_4$ | max. | 15 | mA |

Power dissipation ¹⁾

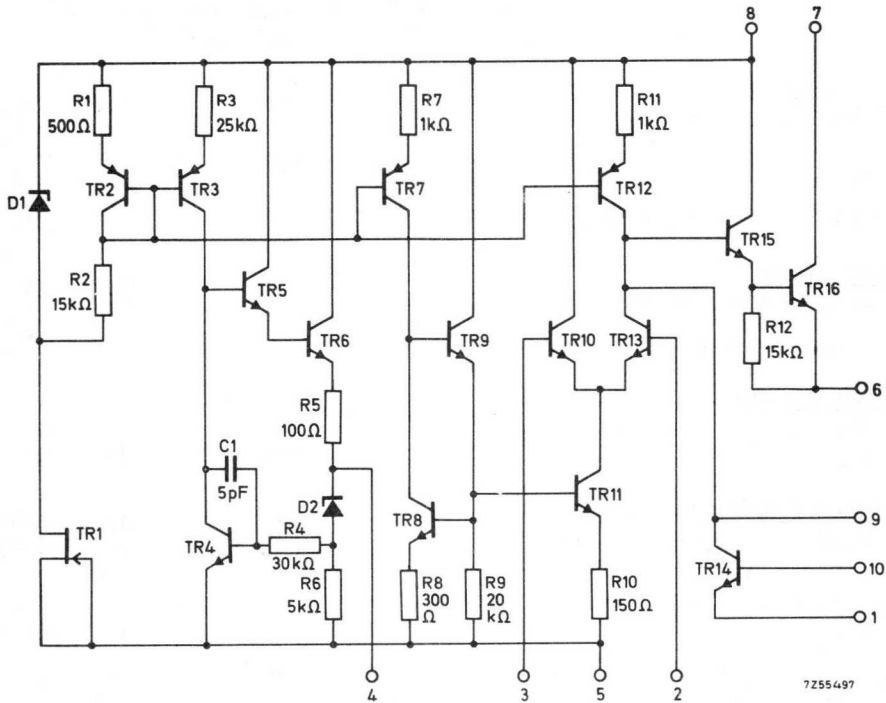
| | | | |
|-----------|------|-----|----|
| P_{tot} | max. | 800 | mW |
|-----------|------|-----|----|

Temperatures

| | | | | |
|-------------------------------|-----------|--------|------|----|
| Operating ambient temperature | T_{amb} | 0 to | +70 | °C |
| Storage temperature | T_{stg} | -65 to | +150 | °C |

¹⁾ For operation above ambient temperature of 25 °C derate linearly at 6.8 mW/°C.

CIRCUIT DIAGRAM



7255497

PINNING

- | | |
|---------------------------------------|--------------------------------------|
| 1. Current sense | 6. Output voltage (V_O) |
| 2. Inverting input | 7. Collector voltage (V_C) |
| 3. Non-inverting input | 8. Positive supply voltage (V_P) |
| 4. Reference voltage (V_{ref}) | 9. Frequency compensation |
| 5. Negative supply voltage ($-V_N$) | 10. Current limit |

CHARACTERISTICS at $T_{amb} = 25^{\circ}C$; $V_i = V_P = V_C = 12V$; $-V_N = 0V$; $V_O = 5V$; $I_L = 5\text{ mA}$,
 $R_{SC} = 0$; $C_1 = 100\text{ pF}$; $C_{ref} = 0$ unless otherwise specified;
 (for testcircuit see figs. 1, 2 and 3 on page 5)

| | | | |
|----------------------------------------------------------------------------------|-------------|------------|----------------|
| <u>Line regulation</u> | | | |
| at $V_i = 12$ to $V_i = 15V$ | typ. | 0.01 | % V_O |
| | < | 0.1 | % V_O |
| at $V_i = 12$ to $V_i = 40V$ | typ. | 0.1 | % V_O |
| | < | 0.5 | % V_O |
| at $V_i = 12$ to $V_i = 15V$; $T_{amb} = 0$ to $+70^{\circ}C$ | < | 0.3 | % V_O |
| <u>Load regulation</u> | | | |
| at $I_L = 1$ to $I_L = 50\text{ mA}$ | typ. | 0.03 | % V_O |
| | < | 0.2 | % V_O |
| at $I_L = 1\text{ mA}$ to $I_L = 50\text{ mA}$; $T_{amb} = 0$ to $+70^{\circ}C$ | < | 0.6 | % V_O |
| <u>Ripple rejection</u> at $f = 50\text{ Hz}$ to 10 kHz | | | |
| $C_{ref} = 0$ | typ. | 74 | dB |
| $C_{ref} = 5\mu\text{F}$ | typ. | 86 | dB |
| <u>Average temperature coefficient</u> | | | |
| of output voltage at $T_{amb} = 0$ to $+70^{\circ}C$ | typ. | 0.003 | %/ $^{\circ}C$ |
| | < | 0.015 | %/ $^{\circ}C$ |
| <u>Short circuit current limit</u> | | | |
| $R_{SC} = 10\Omega$; $V_O = 0$ | typ. | 65 | mA |
| <u>Reference voltage</u> | | | |
| | V_4 typ. | 7.15 | V |
| | | 6.8 to 7.5 | V |
| <u>Output noise voltage</u> at $B = 100\text{ Hz}$ to 10 kHz | | | |
| $C_{ref} = 0$ | V_n typ. | 20 | μV |
| $C_{ref} = 5\mu\text{F}$ | V_n typ. | 2.5 | μV |
| <u>Long term stability</u> | | | |
| over 1000 hours | | 0.1 | % |
| <u>Stand-by current drain</u> | | | |
| $I_L = 0$; $V_i = 30V$ | I_P typ. | 2.3 | mA |
| | < | 4.0 | mA |
| <u>Input voltage range</u> | V_i | 9.5 to 40 | V |
| <u>Output voltage range</u> | V_O | 2.0 to 37 | V |
| <u>Input-output voltage difference</u> | $V_i - V_O$ | 3.0 to 38 | V |

CHARACTERISTICS (continued)

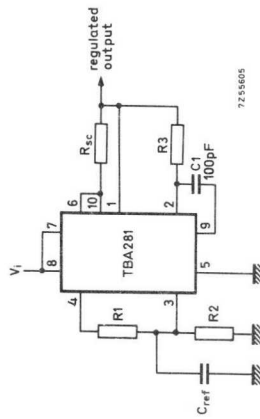


Fig. 1 1)2)

Basic low voltage regulator

($V_o = 2$ to $7V$)

Typical performance

Regulated output voltage = $5V$

Line regulation ($\Delta V_i = 3V$) = $0.5mV$

Load regulation ($\Delta I_L = 50mA$) = $1.5mV$

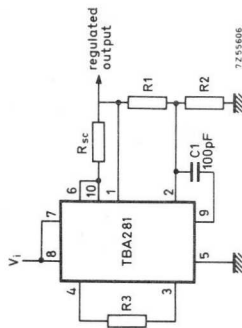


Fig. 2 1)2)

Basic high voltage regulator

($V_o = 7$ to $37V$)

Typical performance

Regulated output voltage = $15V$

Line regulation ($\Delta V_i = 3V$) = $1.5mV$

Load regulation ($\Delta I_L = 50mA$) = $4.5mV$

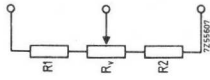


Fig. 3 2)
Output voltage adjust

- 1) $R_3 = \frac{R_1 \cdot R_2}{R_1 + R_2}$ for minimum temperature drift. R_3 may be eliminated for minimum component count.
- 2) For adjustable output voltage replace R_1/R_2 in fig. 1 and 2 with divider circuit shown in fig. 3.

Formulae for intermediate output voltages

Outputs from +2 V to +7 V (fig. 1)

$$V_o = V_{\text{ref}} \times \frac{R_2}{R_1 + R_2}$$

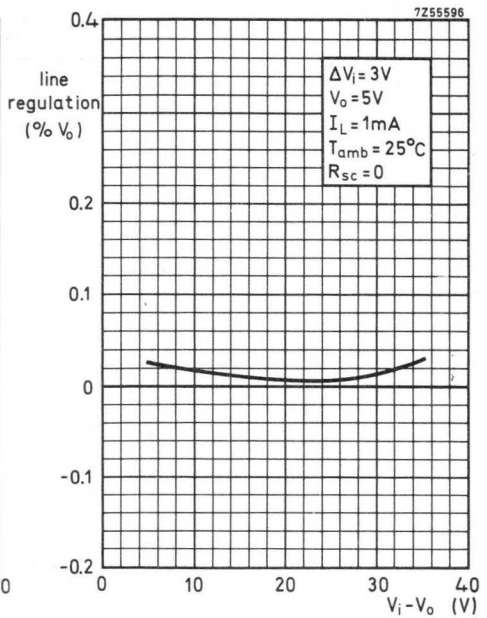
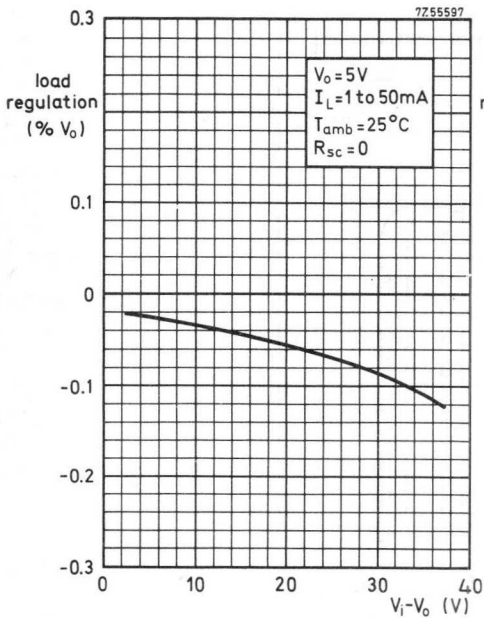
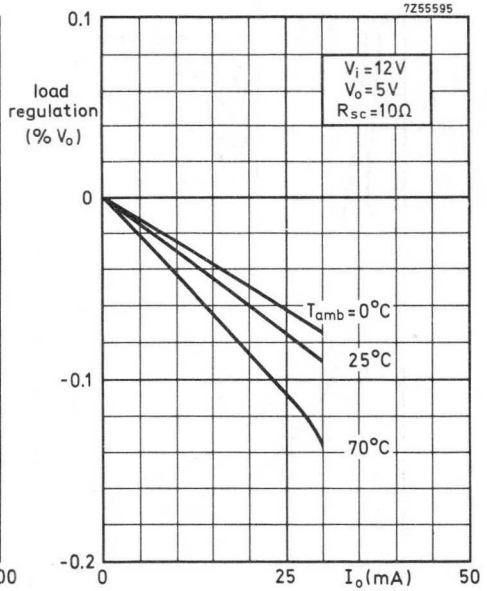
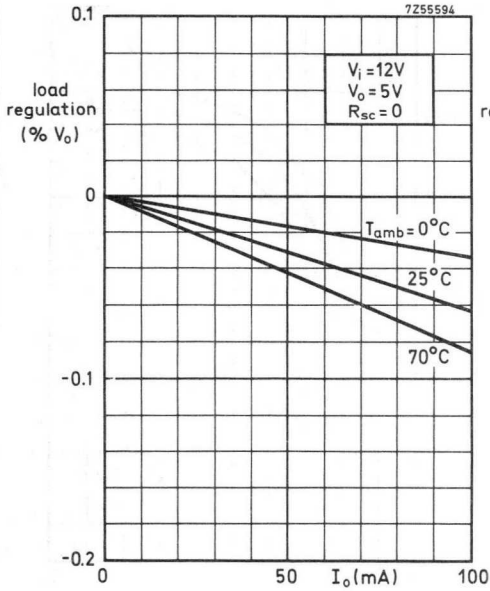
Outputs from +7 V to +37 V (fig. 2)

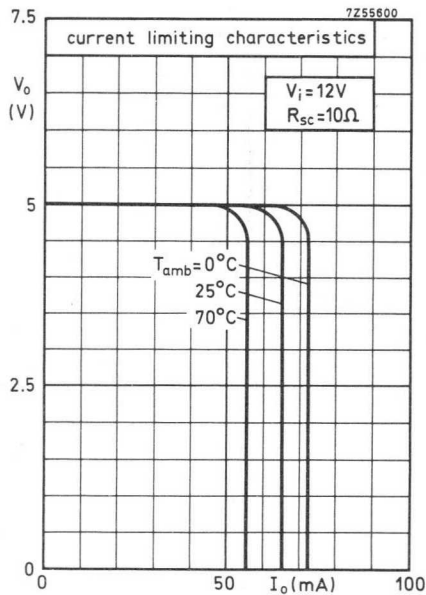
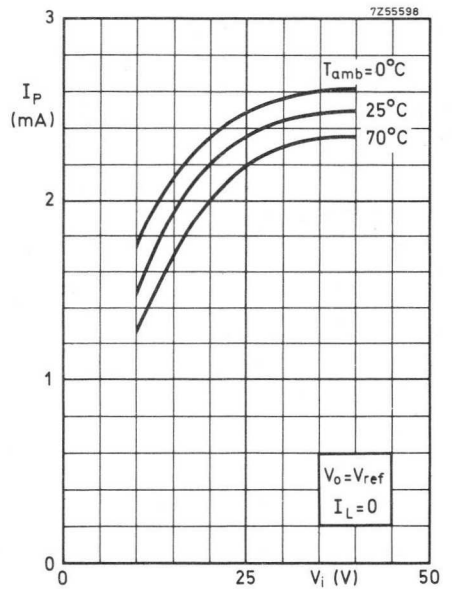
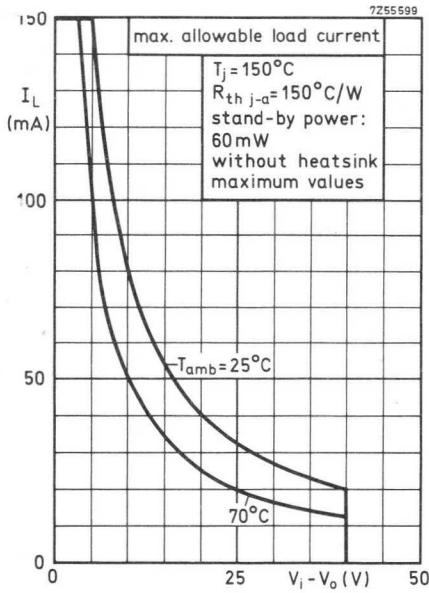
$$V_o = V_{\text{ref}} \times \frac{R_1 + R_2}{R_2}$$

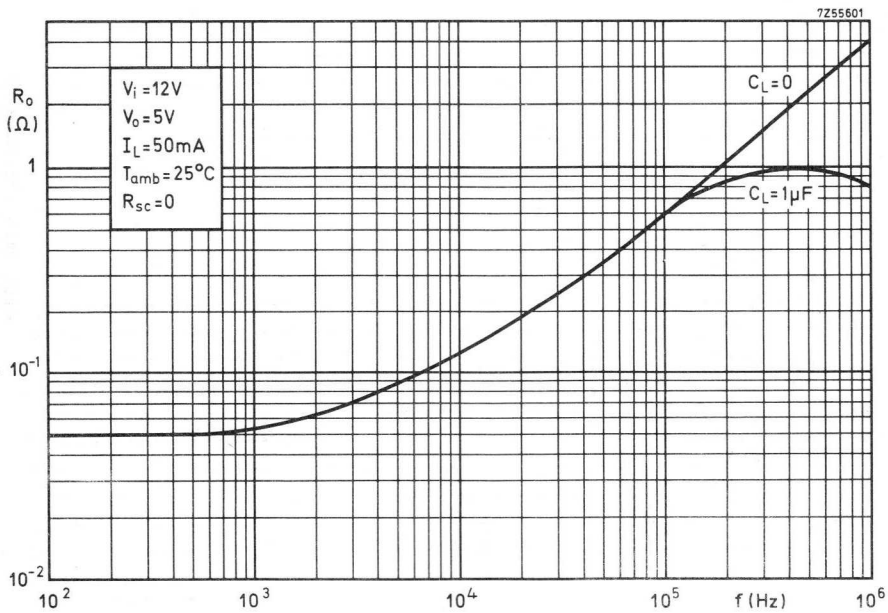
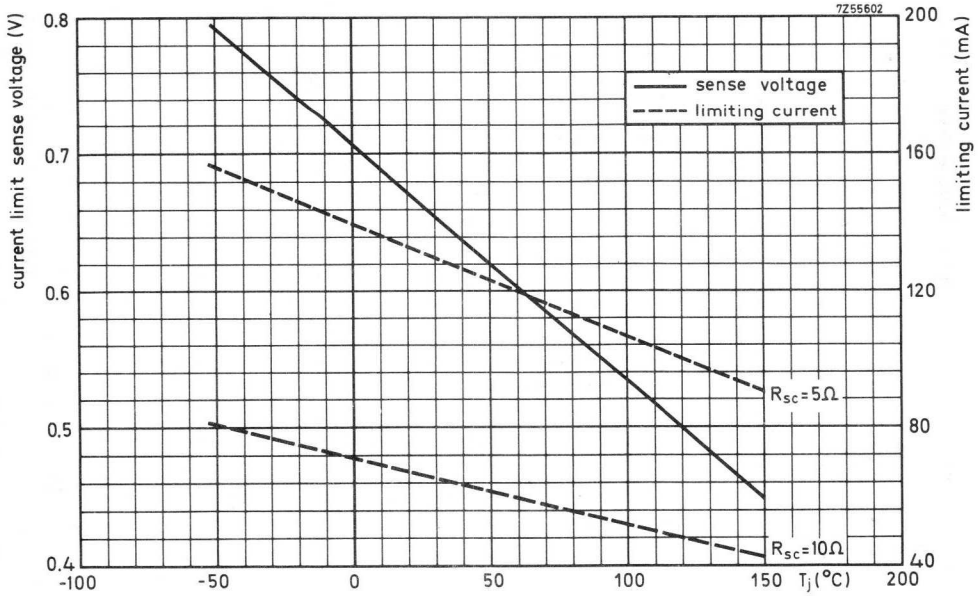
Resistor values (kΩ) for standard output voltages.

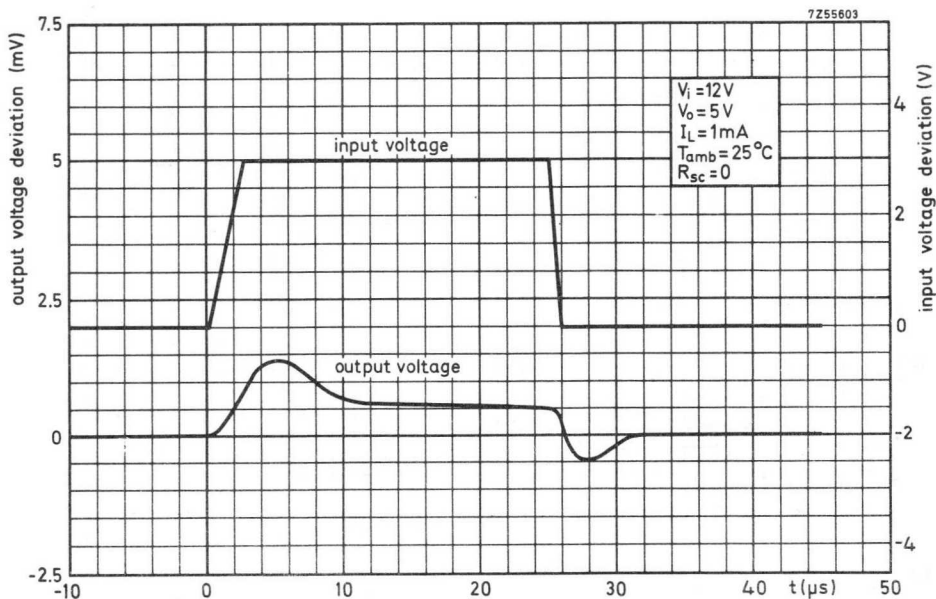
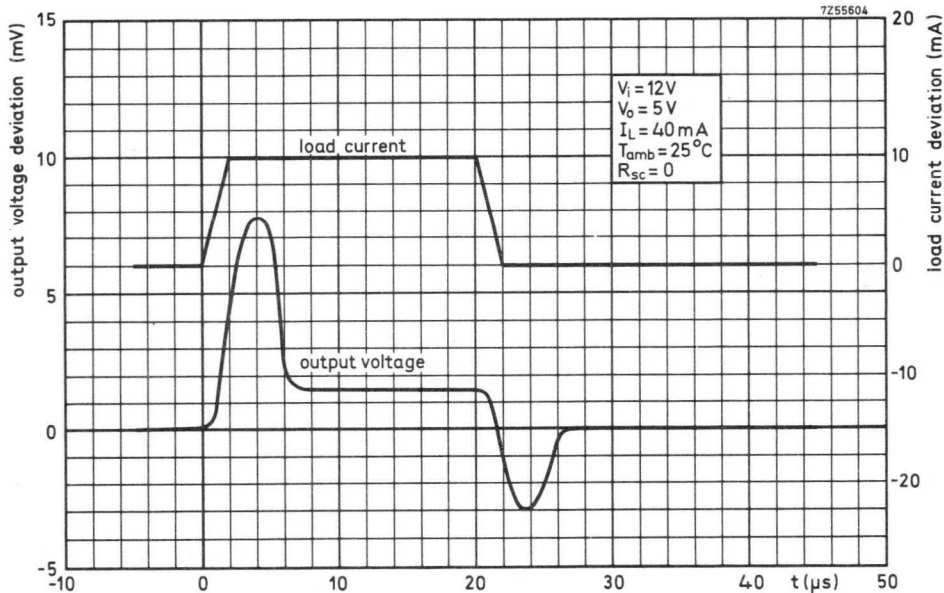
| positive output voltage (V) | figure | fixed output ± 5% | | adjustable output ¹⁾ ± 10% (see fig. 3) | | |
|-----------------------------|--------|-------------------|----------------|----------------------------------------------------|----------------|----------------|
| | | R ₁ | R ₂ | R ₁ | R _v | R ₂ |
| + 3.0 | 1 | 4.12 | 3.01 | 1.8 | 0.5 | 1.2 |
| + 3.6 | 1 | 3.57 | 3.65 | 1.5 | 0.5 | 1.5 |
| + 5.0 | 1 | 2.15 | 4.99 | 0.75 | 0.5 | 2.2 |
| + 6.0 | 1 | 1.15 | 6.04 | 0.5 | 0.5 | 2.7 |
| + 9.0 | 2 | 1.87 | 7.15 | 0.75 | 1.0 | 2.7 |
| + 12 | 2 | 4.87 | 7.15 | 2.0 | 1.0 | 3.0 |
| + 15 | 2 | 7.87 | 7.15 | 3.3 | 1.0 | 3.0 |
| + 28 | 2 | 21.0 | 7.15 | 5.6 | 1.0 | 2.0 |

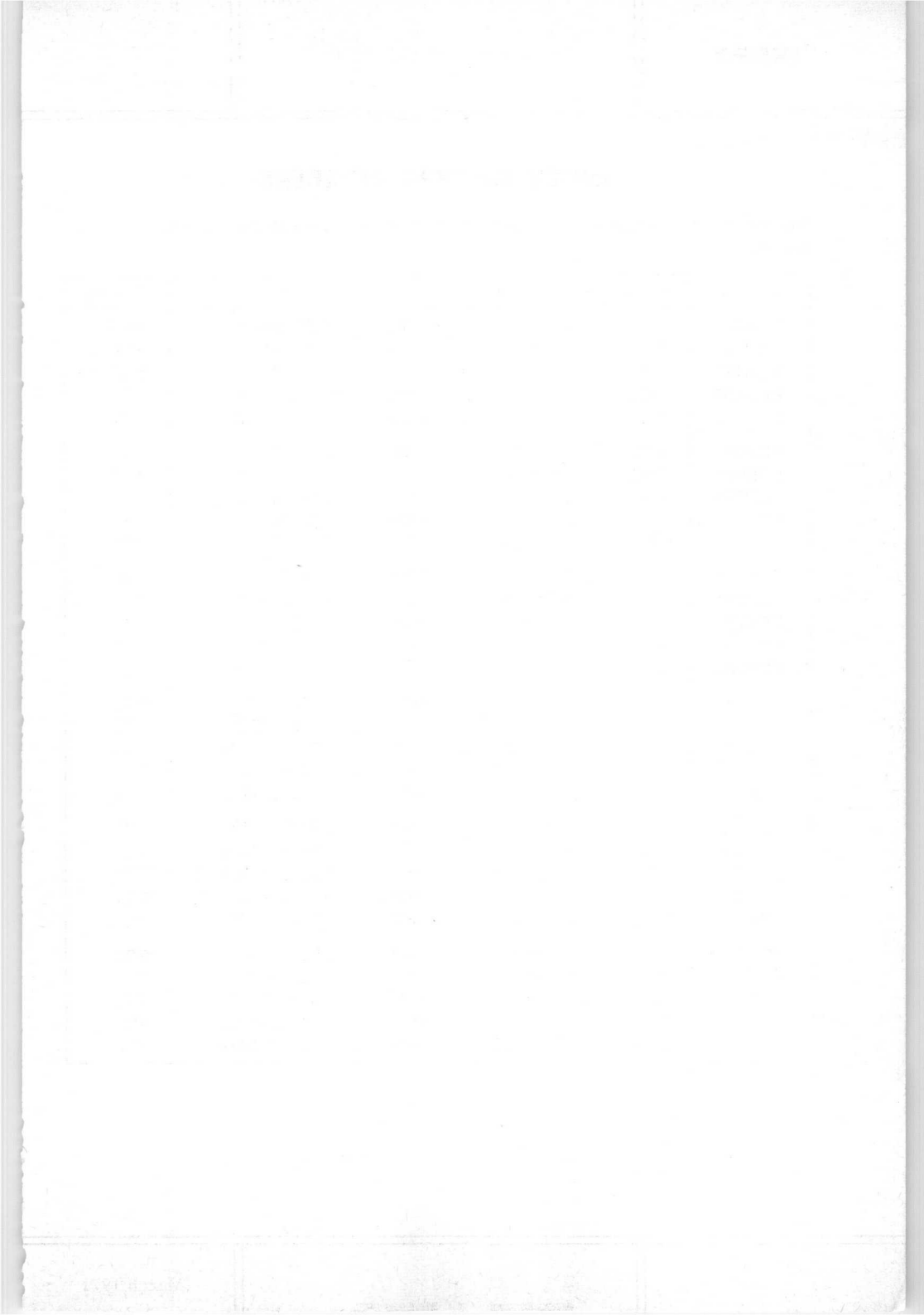
¹⁾ For adjustable output voltage replace R₁/R₂ in fig. 1 and 2 with divider circuit shown in fig. 3 (on page 5).











INDEX OF TYPE NUMBERS

The inclusion of a type number in this publication does not necessarily imply its availability.

| Type No. | Section | Type No. | Section | Type No. | Section |
|----------|---------|----------|---------|----------------|---------|
| FCH101 | DTL | FCY101 | DTL | FDR126Z1 | MOS |
| FCH111 | DTL | FDH106 | MOS | FDR131Z | MOS |
| FCH121 | DTL | FDH116 | MOS | FDR131Z1 | MOS |
| FCH131 | DTL | FDH126 | MOS | FJH101/7430 | TTL |
| FCH141 | DTL | FDH136 | MOS | FJH111/7420 | TTL |
| FCH151 | DTL | FDH146 | MOS | FJH121/7410 | TTL |
| FCH161 | DTL | FDH156 | MOS | FJH131/7400 | TTL |
| FCH171 | DTL | FDJ106 | MOS | FJH141/7440 | TTL |
| FCH181 | DTL | FDN106 | MOS | FJH151/7450 | TTL |
| FCH191 | DTL | FDN116 | MOS | FJH161/7451 | TTL |
| FCH201 | DTL | FDN126 | MOS | FJH171/7453 | TTL |
| FCH211 | DTL | FDN136 | MOS | FJH181/7454 | TTL |
| FCH221 | DTL | FDN146 | MOS | FJH191/7480 | TTL |
| FCH231 | DTL | FDN146A | MOS | FJH201/7482 | TTL |
| FCH281 | DTL | FDN156 | MOS | FJH211/7483 | TTL |
| FCH291 | DTL | FDN156A | MOS | FJH221/7402 | TTL |
| FCH301 | DTL | FDN166A | MOS | FJH231/7401 | TTL |
| FCH311 | DTL | FDN186 | MOS | FJH241/7404 | TTL |
| FCH321 | DTL | FDN196A | MOS | FJH251/7405 | TTL |
| FCJ101 | DTL | FDN206 | MOS | FJH261/7442 | TTL |
| FCJ111 | DTL | FDN206A | MOS | FJH291/7403 | TTL |
| FCJ121 | DTL | FDN506 | MOS | FJH301/7426 | TTL |
| FCJ131 | DTL | FDN516A | MOS | FJH311/7401-S1 | TTL |
| FCJ141 | DTL | FDN526A | MOS | FJH321/7403-S1 | TTL |
| FCJ191 | DTL | FDQ106 | MOS | FJJ101/7470 | TTL |
| FCJ201 | DTL | FDR106Z | MOS | FJJ111/7472 | TTL |
| FCJ211 | DTL | FDR106Z1 | MOS | FJJ121/7473 | TTL |
| FCJ221 | DTL | FDR116Z | MOS | FJJ131/7474 | TTL |
| FCK111 | DTL | FDR116Z1 | MOS | FJJ141/7490 | TTL |
| FCL101 | DTL | FDR126Z | MOS | FJJ151/7491A | TTL |

DTL = FC family
MOS = FD family
TTL = FJ family

| Type No. | Section | Type No. | Section | Type No. | Section |
|--------------|---------|----------|---------|----------|---------|
| FJJ181/7475 | TTL | TAA370 | L | TAB101 | L |
| FJJ191/7476 | TTL | TAA435 | L | TAD100 | L |
| FJJ211/7493 | TTL | TAA450 | L | TBA221 | L |
| FJJ251/7492 | TTL | TAA521 | L | TBA222 | L |
| FJJ261/74107 | TTL | TAA522 | L | TBA240 | L |
| FJK101/74121 | TTL | TAA550 | L | TBA281 | L |
| FJL101/7441A | TTL | TAA560 | L | | |
| FJY101/7460 | TTL | TAA570 | L | | |
| OM200 | L | TAA580 | L | | |
| TAA263 | L | TAA630 | L | | |
| TAA293 | L | TAA640 | L | | |
| TAA300 | L | TAA700 | L | | |
| TAA310 | L | TAA840 | L | | |
| TAA320 | L | TAA960 | L | | |
| TAA350 | L | TAA970 | L | | |

TTL = FJ family

L = Linear integrated circuits



General

DTL

FC family

TTL

FJ family

MOS

FD family

Linear integrated circuits

